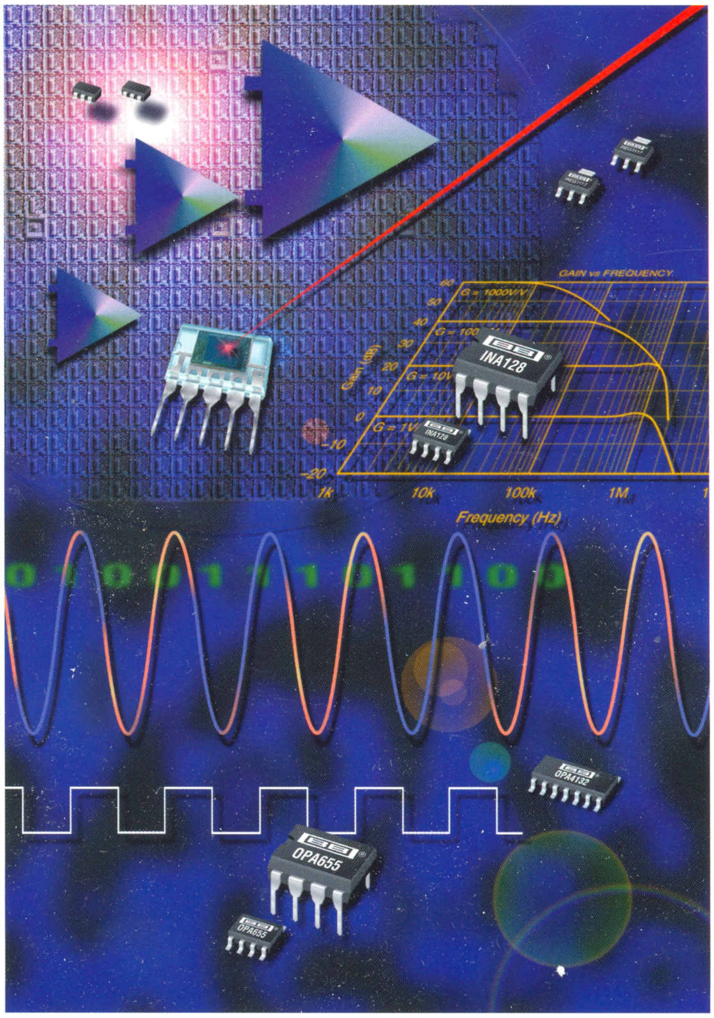
1996/1997

Linear Products



BURR - BROWN®

Product Index

NOTE: (*) This product can be found in the 1996 Burr-Brown IC Data Book—Mixed Signal Products.

Product Index

NOTE: (*) This product can be found in the 1996 Burr-Brown IC Data Book—Mixed Signal Products.

For information on any of these products or to receive the *Burr-Brown Mixed Signal Products IC Data Book*, call our automated literature request line at 1-520-741-3884, or contact your local sales representative.

How to Use This Book

If you know the **MODEL NUMBER,**	Use the Model Index on the **INSIDE FRONT COVER.**
If you know the **PRODUCT TYPE,**	Use the **TABBED TABLE OF CONTENTS,** or use the **SELECTION GUIDE TABLES** at the front of each tabbed section.
If you want **NEW MODELS,**	Use the Model Index on the **INSIDE FRONT COVER** or the **SELECTION GUIDE TABLES** at the front of each tabbed section. All new models contained in this edition are shown in **boldface.** Also, contact your local Burr-Brown representative for information on new models released since publication of this data book.
If you want a **PRICE,**	Contact your local Burr-Brown office or sales representative. See the sales office listing at the back of the book.
If you want **TAPE & REEL,**	See **TAPE & REEL INFORMATION,** Appendix B, or contact your local Burr-Brown representative.

Burr-Brown Integrated Circuits Data Book

Linear Products

1996

BURR-BROWN®

LI-480

Printed in USA

Burr-Brown Corporation
International Airport Industrial Park

Mailing Address:
PO Box 11400
Tucson, AZ 85734

Street Address:
6730 S. Tucson Blvd.
Tucson, AZ 85706

Tel: (520) 746-1111 • FAX: (520) 889-1510 • Cable: BBRCORP

For immediate Product Information or Technical Assistance, call
1-800-548-6132
in the USA.

World Wide Web Address
http://www.burr-brown.com/

Burr-Brown FAXLine (USA/Canada Only)
1-800-548-6133

Worldwide FAX Number
1-520-889-1510

Table of Contents

1 Burr-Brown Corporation

About Burr-Brown

Corporate Profile

Burr-Brown Corporation designs, manufactures, and markets a broad line of high-performance, standard analog and mixed signal integrated circuits used in the processing of electronic signals. Our products are used in a wide range of markets and applications, including industrial and process control, test and measurement, medical and scientific instrumentation, medical imaging, digital audio and video, telecommunications, personal computers, and multimedia.

Our product strategy is to design proprietary circuits that yield maximum functional value in our customers' applications. Many of the products, although produced in standard configurations, are strategically designed, specified, and tested to position them for targeted applications such as audio signal processing or sensor-specific signal conditioning.

Burr-Brown's products include: operational amplifiers, instrumentation amplifiers, programmable gain amplifiers, isolation amplifiers, DC/DC converters, voltage references and regulators, voltage-to-frequency converters, optoelectronic amplifiers, analog-to-digital converters, digital-to-analog converters, and "application specific" standard products. Our products are manufactured using a variety of wafer fabrication processes that include bipolar, complementary bipolar, BiCMOS and CMOS with lithography requirements down to the 0.6 micron level.

We sell our products worldwide through our direct sales force, independent sales representatives, and third-party distributors. Burr-Brown has six direct sales offices in the United States and international sales subsidiaries in France, Germany, Italy, Japan, the Netherlands, Switzerland, and the United Kingdom. Through direct sales and distributors, our products reach over 25,000 OEM customers worldwide. Sales are divided evenly throughout the world, with approximately one-third from the United States market, one-third from Europe, and the remainder from Japan and the South East Asian region.

Burr-Brown employs over 1,900 people worldwide with manufacturing and technical facilities in Tucson, Arizona; Atsugi, Japan; and Livingston, Scotland. Located in Tucson, Arizona, corporate headquarters also includes an integrated circuit wafer fab, assembly and test operations. Burr-Brown was incorporated in Arizona in 1956; stock is traded on NASDAQ under the symbol, BBRC.

Burr-Brown Receives ISO9001 Certification in U.S. and Europe

In September 1993, Burr-Brown Corporation received ISO9001 certification in the United States and Europe, simultaneously. In the United States, registration is recognized through the TUV Product Service Quality Registrar by the Registration Accreditation Board (RAB). Certification is accepted through the Electronics Industries Quality Registrar by the Dutch Registration Board (RCV) in Europe.

ISO9001 is the international standard for assessing the quality systems of companies that design, manufacture, and test products. Adopted by 91 member countries, it's the international quality standard for manufacturing, trade, and communications industries. Certification indicates that a formal quality system exists for all processes and that these processes are audited on a timely basis.

BURR-BROWN ISO9001 CERTIFIED

Applications Library

Applications Bulletins and Design Software

APPLICATIONS LIBRARY

The following applications information is available from Burr-Brown at no charge.

Call 1-800-548-6132 to order.

APPLICATIONS BULLETINS

Or, Call Customer Service at 1-800-548-6132 (USA Only)

Applications Library

Applications Bulletins and Design Software

DESIGN SOFTWARE

1

BURR-BROWN CORPORATION

Sales and Service

ABOUT THIS BOOK

To keep with the easy-to-use format we established last year, the *Burr-Brown Integrated Circuits Data Books* for 1996/97 will be similar to the 1995 books. Both the Linear Products and Mixed Signal Products books are available free from your local salesperson or representative—see **Sales Office Listings** at back of book—or by calling our literature request line at **1-800-548-6132** (US or Canada). Order both, or just the one that fits your needs.

How to Use This Book

Burr-Brown product numbers are listed in the Selection Trees and Tables at the beginning of each tabbed section. With these tools you can quickly compare specs among different products and choose the best part for your design. Products appearing in **boldface** type are new products introduced by Burr-Brown since publication of the 1995 data books.

Data sheets are arranged alphanumerically by product type, so if you know the name of the part you can find it quickly. Or, use the Product Index on the **inside front cover**, or page numbers as listed in the Selection Guide trees and tables.

CUSTOMER SERVICE

Burr-Brown is committed to providing the best customer service in the industry—whether it be a need for additional technical literature, technical assistance, to place an order, or to return products. For immediate assistance with any problem or inquiry, contact your local Burr-Brown salesperson or representative. See **Sales Office Listings** at back of book.

Direct factory assistance is available by calling the following number: **1-800-548-6132** (US or Canada; 7:00am to 5:00pm MST).

Technical Literature or Applications Assistance

In addition to individual data sheets, Burr-Brown also provides its customers with applications bulletins, promotional samples, comprehensive brochures featuring many product types, and applications assistance by calling **1-800-548-6132** (US or Canada).

Internet

Burr-Brown information is now available on the Internet via the World Wide Web. Customers with Internet access can visit our home page at **http://www.burr-brown.com/** to obtain on-line data sheets and corporate information any time of the day, any day of the year.

FAX*Line*

Burr-Brown's **FAX*Line*** is available for customers to request product literature. Call **1-800-548-6133** (USA/Canada Only) to receive a Document Catalog, complete with **FAX*Line*** literature order numbers. Up to three pieces of literature may be requested per call.

Prices and Quotations

Price quotations made by Burr-Brown or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement. Please call your local sales representative or distributor (see list at the back of this book).

Placing Orders

You can place orders via telephone, FAX, or mail with any authorized Burr-Brown field sales office, sales representative, or authorized distributors. See **Sales Office Listings** at back of book for the office nearest you.

Sales and Service

Returns and Warranty Service

When returning products for any reason, contact Burr-Brown prior to shipping for authorization and shipping instructions. For complete instructions, contact your local salesperson or representative. Customers outside the USA should call the nearest sales office for details and information—see **International Sales Office Listing** at back of book.

To return product, please call for your Return Material Authorization (RMA) number. Ship units prepaid and supply the original purchase order number and date, along with an explanation for the return. Upon receipt of the returned devices, Burr-Brown will verify and inform you of the warranty status, cost to repair or replace, credits, and status of replacements where applicable.

2 Operational Amplifiers

The following selection guides include new products which combine exceptional performance with monolithic IC reliability and economy. Many of these products feature new package options for a maximum in design flexibility. The newest in package design, the SOT23-5, gives designers the same great Burr-Brown quality and precision in a size that economizes valuable board space.

The following highlights some of our newest developments:

OPA130 Series—Low-power FET-input op amps that combine precision dc performance with low quiescent current (530µA per amplifier). Available in single, dual, and quad configurations.

OPA131 Series—A family of single, dual and quad op amps that offer excellent overall performance for general purpose applications. Design features include 4MHz bandwidth and 10V/µs slew rate, yet quiescent current is only 1.5mA per amplifier.

OPA132 Series—High speed, precision, FET-input op amps that feature 8MHz GBW, and excellent dc performance at low cost. They are available in single, dual, and quad versions for maximum design flexibility.

OPA234 Series—A new line of single supply general purpose op amps that combine low offset voltage, high common-mode rejection, and wide supply range to provide excellent accuracy and versatility.

OPA650, OPA2650, OPA4560—A family of single, dual, and quad wideband voltage feedback amplifiers featuring low power, unity gain stable bandwidth up to 560MHz, fast 12-bit settling, and low differential gain/phase errors—ideal for medical equipment and telecommunications applications. OPA650 is available in SOT23-5 package.

OPA651—A low-power, wideband voltage feedback op amp that is decompensated for stability in gains of 2 or greater. It features 940MHz GBW and low 50mW power dissipation, and is available in 8-pin DIP, SO-8, and SOT23-5 packages.

OPA655—A new SpeedPLUS op amp that combines a wideband unity gain stable voltage feedback op amp with a FET-input stage to offer an ultra high dynamic range amplifier for ADC buffering and transimpedance applications. Available in 8-pin plastic DIP, or SO-8 surface mount packages.

OPA658—An ultra-wideband (900MHz), low power current feedback op amp featuring high slew rate, and low differential gain/phase error. Its ±5V power supply requirement makes it an excellent choice for portable applications. It is available in 8-pin DIP, 8-lead SOIC, and SOT23-5 packages.

Spice macromodels are available for many of our products. By using a simulation program with integrated circuit emphasis (SPICE), designers can simulate amplifier behavior to show circuit function and performance over a wide range of conditions and signals.

Power operational amplifiers and buffers are described in Section 3, instrumentation amplifiers in Section 4, and isolation amplifiers in Section 5.

Operational Amplifiers

OPERATIONAL AMPLIFIERS

PRECISION

Low Drift (V_{OS} Over Temp, max)

OPA177 (0.1µV/°C)
OPA77 (0.3µV/°C)
OPA27 (0.6µV/°C)
OPA37 (0.6µV/°C)
OPA627 (0.8µV/°C)
OPA637 (0.8µV/°C)
OPA111 (1µV/°C)
OPA602 (2µV/°C)
OPA124 (2µV/°C)
OPA1013 (2.5µV/°C, Dual)
OPA2111 (2.8µV/°C, Dual)
OPA234 (3µV/°C)
OPA2234 (3µV/°C, Dual)
OPA4234 (3µV/°C, Quad)

Low Bias Current I_B, (max)

OPA128 (75fA)
OPA129 (100fA)
OPA111 (1pA)
OPA124 (1pA)
OPA602 (1pA)
OPA2111 (4pA, Dual)
OPA404 (4pA, Quad)
OPA121 (5pA)
OPA627 (5pA)
OPA637 (5pA)
OPA2107 (5pA, Dual)
OPA606 (10pA)
OPA130 (20pA)
OPA2130 (20pA, Dual)
OPA4130 (20pA, Quad)
OPA131 (50pA)
OPA654 (50pA)
OPA671 (50pA)
OPA2131 (50pA, Dual)
OPA4131 (50pA, Quad)
OPA132 (50pA)
OPA2132 (50pA, Dual)
OPA4132 (50pA, Quad)
OPA655 (100pA)

Low Noise (Voltage Noise at 10kHz, max)

BIPOLAR INPUT

OPA27 (3.8nV/√Hz)
OPA37 (3.8nV/√Hz)
OPA77 (11nV/√Hz)

FET INPUT

OPA627 (6nV/√Hz)
OPA637 (6nV/√Hz)
OPA655 (6nV/√Hz)
OPA132 (8nV/√Hz)
OPA2132 (8nV/√Hz)
OPA4132 (8nV/√Hz)
OPA124 (8nV/√Hz)
OPA2111 (8nV/√Hz, Dual)
OPA111 (8nV/√Hz)
OPA2107 (8nV/√Hz, Dual)

Single Supply (V_S, min)

OPA237 (2.7V)
OPA2237 (2.7V, Dual)
OPA4237 (2.7V, Quad)
OPA234 (2.7V)
OPA2234 (2.7V, Dual)
OPA4234 (2.7V, Quad)
OPA1013 (4V, Dual)

GENERAL PURPOSE

OPA27 (Single)
OPA37 (Single)
OPA131 (Single)
OPA177 (Single)
OPA604 (Single)
OPA77 (Single)
OPA2131 (Dual)
OPA2604 (Dual)
OPA4131 (Quad)

HIGH SPEED

Voltage Feedback Stable for G = > 2

GBWP = > 400MHz

OPA643 (SR = 1000V/µs)
OPA621 (SR = 350V/µs)
OPA675 (SR = 350V/µs)
OPA676 (SR = 350V/µs)
OPA651 (SR = 300V/µs)

GBWP = < 400MHz

OPA654 (SR = 750V/µs)
OPA641 (SR = 650V/µs)
OPA678 (SR = 350V/µs)
OPA637 (SR = 100V/µs)

Voltage Feedback Unity Gain Stable

GBWP = > 200MHz

OPA622 (SR = 1600V/µs*)
OPA642 (SR = 380V/µs)
OPA640 (SR = 350V/µs)
OPA655 (SR = 210V/µs, FET)
OPA646 (SR = 180V/µs)
OPA620 (SR = 175V/µs)

GBWP = < 200MHz

OPA628 (SR = 310V/µs)
OPA650 (SR = 240V/µs)
OPA2650 (SR = 240V/µs, Dual)
OPA4650 (SR = 240V/µs, Quad)
OPA671 (SR = 100V/µs)

Current Feedback SR > 1000V/µs (BW at G = +2)

OPA658 (680MHz)
OPA648 (600MHz)
OPA2658 (500MHz, Dual)
OPA4658 (450MHz, Quad)
OPA644 (300MHz)
OPA623 (290MHz)
OPA603 (160MHz)

SPECIAL PURPOSE

OPA675 (TTL Switched Input)
OPA676 (ECL Switched Input)
OPA678 (Switched Input, G = +1 Stable)
VCA610 (Voltage Controlled Gain)
OPA660 (Transconductance)
OPA2662 (Transconductance, Dual)

MULTI-CHANNEL (refer to tables for details)

DUAL

OPA1013 (Precision, Low Drift, Single Supply)
OPA2107 (Precision, Low Bias Current)
OPA2111 (Precision, Low Noise)
OPA2131 (Precision, Low Bias Current)
OPA2132 (Single Supply)
OPA2234 (Single Supply)
OPA2237 (Single Supply)
OPA2604 (Precision, Low Bias Current)
OPA2650 (High Speed, VFB)
OPA2658 (High Speed, CFB)
OPA2662 (Transconductance)

QUAD

OPA404 (Precision, Low Bias Current)
OPA4131 (Precision, Low Bias Current)
OPA4234 (Single Supply)
OPA4237 (Single Supply)
OPA4650 (High Speed, VFB)
OPA4658 (High Speed, CFB)

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

PRECISION

Product	Offset Voltage Drift max (±μV/°C)	Bias Current 25°C max (pA)	Noise Voltage at 10kHz max (nV/√Hz)	Offset Voltage 25°C max (±mV)	Open Loop Gain min (dB)	Rated Voltage Output(2) min (±V)	Rated Current Output min (±mA)	Description
AD515	15	±75fA	NS	1	88	10	10	FET, Still Available
OPA27	0.6	±40nA	3.8	0.025	120	12	16.7	Bipolar
OPA37	0.6	±40nA	3.8	0.025	120	12	16.7	Bipolar
OPA77	0.3	±2nA	11	0.025	134	12	12	Bipolar
OPA103	2	±1	25*	0.25	100	10	5	FET, Still Available
OPA104	10	±75fA	35*	0.5	100	10	5	FET, Still Available
OPA111	1	±1	8	0.25	120	11	5.5	FET
OPA121	10	±5	6*	2	110	11	5.5	Low Cost
OPA124	2	±1	6*	0.25	120	11	5.5	FET
OPA128	5	±75fA	15*	0.5	110	10	5	FET, Ultra-Low, Bias Current
OPA129	10	±100fA	15*	2	94	10	6	FET, Ultra-Low, Bias Current
OPA130	**10**	**±20**	**16**	**1**	**120**	**12**	**18***	**FET, Low Power**
OPA131	10	±50	15*	1	94	12	25*	FET
OPA132	**10**	**50**	**8**	**0.5**	**120**	**12.5**	**40**	**FET, High Speed**
OPA177	0.1	1.5nA	10*	0.025	134	12	12	Bipolar
OPA234	**3**	**–20nA**	**25(1)**	**0.1**	**110**	**+14/–14.5**	**22***	**Single Supply Amp**
OPA404	3*	±4	12*	0.75	92	11.5	5	FET, Quad
OPA602	2	±1	12*	0.25	92	11.5	15	Wideband, (5MHz, min)
OPA606	5	±10	13	0.5	100	12	5	Wideband, (9MHz, min)
OPA627	0.8	±5	6	0.1	112	11.5	45*	FET
OPA637	0.8	±5	6	0.1	112	11.5	45*	FET
OPA654	40*	±50	14*	3	94*	11	200*	Wideband, (750V/μs, slew rate)
OPA655	**10**	**100**	**6***	**2**	**53**	**2.5**	**25**	**FET**
OPA671	10*	±50	12*	5.0	74	10.5	50	FET
OPA1013	2.5	30nA	NS	0.3	120	12	6.5	Low Power, Dual Single Supply Operation
OPA2111	2.8	±3	8	0.5	114	10	5	FET, Dual
OPA2107	5	±5	8*	0.5	84	11	5.5	FET, Dual
OPA2130	**10**	**±20**	**16**	**1**	**120**	**12**	**18***	**FET, Low Power, Dual**
OPA2131	10	±50	15*	1	94	12	25*	FET, Dual
OPA2132	**10**	**50**	**8**	**0.5**	**120**	**12.5**	**40**	**FET, High Speed, Dual**

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

PRECISION (CONT)

Product	Offset Voltage Drift max (±µV/°C)	Bias Current 25°C max (pA)	Noise Voltage at 10kHz max (nV/√Hz)	Offset Voltage 25°C max (±mV)	Open Loop Gain min (dB)	Rated Voltage Output(2) min (±V)	Rated Current Output min (±mA)	Description
OPA2234	**3**	**–20nA**	**25(1)**	**0.1**	**110**	**+14/–14.5**	**22***	**Single Supply Amp, Dual**
OPA4130	**10**	**±20**	**16**	**1**	**120**	**12**	**18**	**FET, Low Power, Quad**
OPA4131	10	±50	15*	1	94	12	25*	FET, Quad
OPA4132	**10**	**±50**	**8**	**0.5**	**120**	**12.5**	**40***	**FET, High Speed, Quad**
OPA4234	**3**	**–20nA**	**25(1)**	**0.1**	**110**	**+14/–14.5**	**22***	**Single Supply Amp, Quad**
3507	30*	±250	NS	10	77	10	10	FET, Still Available
3527	2	±2	25*	0.25	100	10	10	FET, Still Available
3528	5	±150fA	40*	0.25	92	10	5	FET, Still Available

NOTE: (1) Typical Noise Voltage at 1kHz (nV/√Hz). (2) For ±15V supplies.

SINGLE SUPPLY

Product	Single Supply Range min to max (V)	Quiescent Current max (mA, per amp)	Bias Current 25°C max (nA)	Small Signal Unity Gain typ (kHz)	Offset Voltage 25°C max (±µV)	Temp Range(1)	Pkg	Description
OPA234	**2.7 to 36**	**0.3**	**–20**	**350**	**100**	**XInd**	**DIP, SO-8, MSOP-8**	**Single, Bipolar**
OPA237	***2.7 to 36***	***0.35***	***±40***	***1.5MHz***	***250***	***XInd***	***SOT-23-5***	***Single, Bipolar***
OPA1013	4 to 36	0.55	–30	750	300	Com/Ind	DIP	Dual, Bipolar
OPA2234	**2.7 to 36**	**0.3**	**–20**	**350**	**100**	**XInd**	**DIP, SO-8**	**Dual, Bipolar**
OPA2237	***2.7 to 36***	***0.35***	***±40***	***1.5MHz***	***250***	***XInd***	***MSOP-8***	***Dual, Bipolar***
OPA4234	**2.7 to 36**	**0.3**	**–20**	**350**	**100**	**XInd**	**DIP, SO-14**	**Quad, Bipolar**
OPA4237	***2.7 to 36***	***0.35***	***±40***	***1.5MHz***	***250***	***XInd***	***SSOP-16***	***Quad, Bipolar***

NOTE: (1) Com = 0°C to 70°C, Ind = –25°C to 85°C, XInd = –40°C to 85°C.

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

For Immediate Assistance, Contact Your Local Salesperson

GENERAL PURPOSE

Product	Offset Voltage 25°C max (±mV)	Offset Voltage Drift max (±µV/°C)	Bias Current 25°C max (nA)	Small Signal Unity Gain min (MHz)	Power Supply Range (V)	Quiescent Current, max (mA)	Description
OPA27	0.025	0.6	40	5	±4.0 to ±22	4.7	Bipolar
OPA37	0.025	0.6	40	80(1)	±4.0 to ±22	4.7	Bipolar
OPA77	0.025	0.3	2	0.4	±3.0 to ±18	2.0	Bipolar
OPA130	**1.0**	**10**	**25pA**	**1**	**±2.5 to ±18**	**0.65**	**FET, Low Power**
OPA131	1.0	10	50pA	4*	±4.5 to ±18	1.75	FET
OPA132	**0.5**	**10**	**50pA**	**8**	**±2.5 to ±18**	**4.8**	**FET, High Speed**
OPA177	0.01	0.1	1.5	0.4	±3.0 to ±18	2.0	Bipolar
OPA604	5.0	8*	50pA	20*(2)	±4.5 to ±24	6.0	FET, Low Distortion (0.0003%)
OPA2130	**1.0**	**10**	**25pA**	**1**	**±2.5 to ±18**	**0.65**	**FET, Low Power, Dual**
OPA2131	1.0	10	50pA	4*	±4.5 to ±18	3.5	FET, Dual
OPA2132	**0.5**	**10**	**50pA**	**8**	**±2.5 to ±18**	**4.8**	**FET, High Speed, Dual**
OPA2604	5.0	8*	0.1	20*(2)	±4.5 to ±24	12	FET, Dual, Low Distortion (0.0003%)
OPA4130	**1.0**	**10**	**25pA**	**1**	**±2.5 to ±18**	**0.65**	**FET, Low Power, Quad**
OPA4131	1.0	10.00	50pA	4*	±4.5 to ±18	7.0	FET, Quad
OPA4132	**0.5**	**10**	**50pA**	**8**	**±2.5 to ±18**	**4.8**	**FET, High Speed, Quad**

NOTE: (1) Gain Bandwidth at Gain = 5V/V. (2) Gain = 100.

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

HIGH SPEED - VOLTAGE FEEDBACK

Product	Small Signal at Specified Gain typ (MHz)	Slew Rate min (V/µs)	Settling Time to ±0.1% (ns)	Rated Voltage Output min (±V)	Rated Current Output min (±mA)	Description
OPA620	300, G = 1	175	13	3	50	Low Noise 2.3nV/$\sqrt{\text{Hz}}$, Wideband
OPA621	500, G = 2	350	15	3	50	Low Noise 2.3nV/$\sqrt{\text{Hz}}$, Wideband, G = 2 minimum
OPA622	250, G = 1	1600*	17	3	70*	High Slew Rate
OPA628	160, G = 1	310*	20	3	30	Low Distortion, Low Noise 2.5nV/$\sqrt{\text{Hz}}$
OPA640	1.3GHz, G = 1	350*	18	2.25	25	Voltage Feedback, Low Noise 2.9nV/$\sqrt{\text{Hz}}$
OPA641	800, G = 2	650*	13	2.6	25	Voltage Feedback, Low Noise 2.8nV/$\sqrt{\text{Hz}}$, G = 2 minimum
OPA642	450, G = 1	380*	11.5	3.0	50	Voltage Feedback, Low Distortion, Low Noise 2.3nV/$\sqrt{\text{Hz}}$
OPA643	300, G = 5	1000*	16.5	3.0	50	Voltage Feedback, Low Distortion, G = 5 minimum, Low Noise 1.8nV/$\sqrt{\text{Hz}}$
OPA646	650, G = 1	180*	11.5	2.5	30	Voltage Feedback, Low Power
OPA650	560, G = 1	240	10.2	2.4	+75/–65	Low Power
OPA651	470, G = 2	300	11.5	2.4	45	Voltage Feedback, Low Power, G = 2 minimum
OPA654	11, G = 1	750*	150	11	200*	FET, External Compensation
OPA655	**400, G = 1**	**210**	**8**	**2.8**	**35**	**FET, Wideband, Low Distortion**
OPA671	33, G = 1	107*	150	10.5	50*	FET
OPA675	100, G = 2	240	15	2.1	30	Very Fast Settling Switched Input, G = 2 minimum
OPA676	100, G = 2	240	15	2.1	30	Very Fast Settling Switched Input, G = 2 minimum
OPA678	200, G = 1	250	22	2.5	44	Very Fast Settling Switched Input
OPA2650	360, G = 1	240	11	2.4	+75/–65	Dual
OPA4650	360, G = 1	240	10.3	2.2	+75/–65	Quad

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

HIGH SPEED - CURRENT FEEDBACK

Product	Small Signal Bandwidth for G = +2V/V typ (MHz)	Slew Rate typ (V/µs)	Settling time, to ±0.1% (ns)	Rated Voltage Output min (±V)	Rated Current Output min (±mA)	Description
OPA603	160	1000	50	10	15	
OPA623	290	2100	9	3.0	70	Flexible Operation, High Slew Rate
OPA644	300	2500	16.5	3.0	50	High Slew Rate
OPA648	600	1200	9	2.75	33	Video Amplifier, Fast Settling
OPA658	680	1700	11.5	2.5	+80/–60	Low Power
OPA2658	500	1700	12.6	2.5	+80/–60	Dual
OPA4658	450	1700	15.1	2.5	+80/–60	Quad

SPECIAL PURPOSE

Product	Offset Voltage 25°C max (±mV)	Offset Voltage Drift max (±µV/°C)	Bias Current 25°C max (µA)	Small Signal Bandwidth typ (MHz)	Rated Voltage Output min (±V)	Rated Current Output min (±mA)	Description
OPA660	+7*	50*	NS	850	3.7	10	Transconductance Amp and Buffer
OPA675	1	5	30	185, G = 10	2.1	30	Two-Channel, G = 2 minimum, TTL Controlled
OPA676	1	5	30	185, G = 10	2.1	30	Two-Channel, G = 2 minimum, ECL Controlled
OPA678	1	10	50	200, G = 1	2.5	30	Two-Channel, TTL & ECL Controlled
OPA2662	75	12*	NS	370	3.4	75	Transconductance Amp, Dual
VCA610	NS	NS	6*	30, G = 40dB	3.0*	80*	Voltage Controlled Gain

* DENOTES TYPICAL

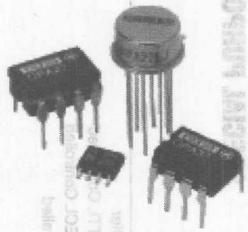
BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR - BROWN®



OPA27
OPA37

Ultra-Low Noise Precision OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: 3.8nV/√Hz max at 1kHz
- LOW OFFSET: 25µV max
- LOW DRIFT: 0.6µV/°C
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 114dB min
- HIGH POWER SUPPLY REJECTION: 100dB min
- FITS OP-07, OP-05, AD510, AD517 SOCKETS

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIER
- RADIATION HARD EQUIPMENT

DESCRIPTION

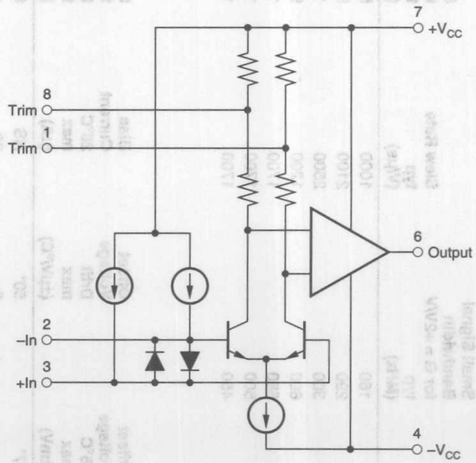
The OPA27/37 is an ultra-low noise, high precision monolithic operational amplifier.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit allows bias and offset current specifications to be met over the full –55°C to +125°C temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5.

The Burr-Brown OPA27/37 is an improved replacement for the industry-standard OP-27/OP-37.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

		OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT											
NOISE(6)											
Voltage, f_O = 10Hz			3.1	5.5		3.5	5.5		3.8	8.0	nV/√Hz
f_O = 30Hz			2.9	4.5		3.1	4.5		3.3	5.6	nV/√Hz
f_O = 1kHz			2.7	3.8		3.0	3.8		3.2	4.5	nV/√Hz
f_B = 0.1Hz to 10Hz			0.07	0.18		0.08	0.18		0.09	0.25	µVp-p
Current,(1) f_O = 10Hz			1.7	4.0		1.7	4.0		1.7		pA/√Hz
f_O = 30Hz			1.0	2.3		1.0	2.3		1.0		pA/√Hz
f_O = 1kHz			0.4	0.6		0.4	0.6		0.4	0.6	pA/√Hz
OFFSET VOLTAGE (2)											
Input Offset Voltage			±6	±25		±12	±60		±25	±100	µV
Average Drift (3)	$T_{A\,MIN}$ to $T_{A\,MAX}$		±0.2	±0.6		±0.3	±1.3		±0.4	±1.8 (6)	µV/°C
Long Term Stability (4)			0.2	1		0.3	1.5		0.4	2.0	µV/mo
Supply Rejection	$\pm V_{CC}$ = 4 to 18V	100	134		100	125		94	120		dB
	$\pm V_{CC}$ = 4 to 18V		±0.2	±10		±0.6	±10		±1	±20	µV/V
BIAS CURRENT											
Input Bias Current			±11	±40		±13	±55		±15	±80	nA
OFFSET CURRENT											
Input Offset Current			6	35		8	50		10	75	nA
IMPEDANCE											
Common-Mode			3 ǁ 2.5			2.5 ǁ 2.5			2 ǁ 2.5		GΩ ǁ pF
VOLTAGE RANGE											
Common-Mode Input Range		±11	±12.3		±11	±12.3		±11	±12.3		V
Common-Mode Rejection	V_{IN} = ±11VDC	114	128		106	125		100	122		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	120	126		120	125		117	124		dB
	$R_L \geq 1k\Omega$	118	125		118	125			124		dB
FREQUENCY RESPONSE											
Gain-Bandwidth Product (5)	OPA27	5	8		5	8		5 (6)	8		MHz
	OPA37	45	63		45	63		45 (6)	63		MHz
Slew Rate (5)	V_O = ±10V, R_L = 2kΩ										
	OPA27, G = +1	1.7	1.9		1.7	1.9		1.7 (6)	1.9		V/µs
	OPA37, G = +5	11	11.9		11	11.9		11 (6)	11.9		V/µs
Settling Time, 0.01%	OPA27, G = +1		25			25			25		µs
	OPA37, G = +5		25			25			25		µs
RATED OUTPUT											
Voltage Output	$R_L \geq 2k\Omega$	±12	±13.8		±12	±13.8		±12	±13.8		V
	$R_L \geq 600\Omega$	±10	±12.8		±10	±12.8		±10	±12.8		V
Output Resistance	DC, Open Loop		70			70			70		Ω
Short Circuit Current	R_L = 0Ω		25	60		25	60		25	60 (6)	mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±4		±22	±4		±22	±4		±22	VDC
Current, Quiescent	I_O = 0mADC		3	4.7		3	4.7		3.3	5.7	mA
TEMPERATURE RANGE											
Specification											
A, B, C (J, Z)		–55		+125	–55		+125	–55		+125	°C
E, F (J, Z)		–25		+85	–25		+85				°C
G (P, U, J, Z)								–40		+85	°C
Operating											
J, Z		–55		+125	–55		+125	–55		+125	°C
P, U								–40		+85	°C

NOTES: (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specifications on grades A and E are also guaranteed with units fully warmed up. Grades B, C, F, and G are measured with automatic test equipment after approximately 0.5 seconds from power turn-on. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Typical specification only on plastic package units. Slew rate varies on all units due to differing test methods. Minimum specification applies to open-loop test. (6) This parameter guaranteed by design.

ELECTRICAL

At $V_{CC} = \pm15VDC$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

		OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TEMPERATURE RANGE											
Specification Range											
A, B, C (J, Z)		–55		+125	–55		+125	–55		+125	°C
E, F (J, Z)		–25		+85	–25		+85				°C
G (P, U, J, Z)								–40		+85	°C
INPUT											
OFFSET VOLTAGE (1)											
Input Offset Voltage											
A, B, C			±24	±60		±45	±200		±60	±300	µV
E, F, G			±17	±50		±33	±140		±48	±220 (3)	µV
Average Drift (2)	$T_{A\,MIN}$ to $T_{A\,MAX}$		±0.2	±0.6		±0.3	±1.3		±0.4	±1.8 (3)	µV/°C
Supply Rejection											
A, B, C	$\pm V_{CC} = 4.5$ to 18V	96	130		94	127		86	122		dB
E, F, G	$\pm V_{CC} = 4.5$ to 18V	97	130		96	127		90 (3)	122		dB
BIAS CURRENT											
Input Bias Current											
A, B, C			±16	±60		±22	±95		±29	±150	nA
E, F, G			±13	±60		±16	±95		±21	±150 (3)	nA
OFFSET CURRENT											
Input Offset Current											
A, B, C			23	50		25	85		35	135	nA
E, F, G			12	50		14	85		20	135 (3)	nA
VOLTAGE RANGE											
Common-Mode Input Range											
A, B, C		±10.3	±11.5		±10.3	±11.5		±10.3	±11.5		V
E, F, G		±10.5	±11.8		±10.5	±11.8		±10.5 (3)	±11.8		V
Common-Mode Rejection	$V_{IN} = \pm11VDC$										
A, B, C		108	124		100	122		94	120		dB
E, F, G		110	126		102	124		96 (3)	122		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$										
A, B, C		116	121		114	120		110	118		dB
E, F, G		118	123		117	122		113(3)	120		dB
RATED OUTPUT											
Voltage Output	$R_L = 2k\Omega$										
A, B, C		±11.5	±13.7		±11.0	±13.5		±10.5	±13.3		V
E, F, G		±11.7	±13.8		±11.4	±13.6		±11.0 (3)	±13.4		V
Short Circuit Current	$V_O = 0VDC$		25			25			25		mA

NOTES: (1) Offset voltage specifications on grades A and E are also guaranteed with the units fully warmed up. Grades B, C, F, and G are measured with automatic test equipment after approximately 0.5s from power turn-on. (2) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (3) This parameter guaranteed by design in P-DIP, "P" package and SOIC "U" package.

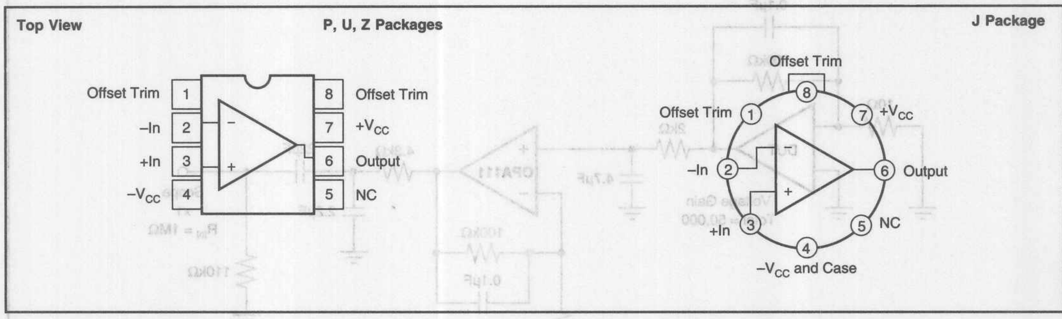
ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Internal Power Dissipation (1) 500mW
Input Voltage .... $\pm V_{CC}$
Output Short-Circuit Duration (2) .... Indefinite
Differential Input Voltage (3) .... ±0.7V
Differential Input Current (3) .... ±25mA
Storage Temperature Range:
J, Z .... –65°C to +150°C
P, U .... –55°C to +125°C
Operating Temperature Range:
A, B, C, E, F, G (J, Z) .... –55°C to +125°C
G (P, U) .... –40°C to +85°C
Lead Temperature:
J, Z, P (soldering, 10s) .... +300°C
U (soldering, 3s) .... +260°C

PACKAGE TYPE	θ_{JA}	UNITS
TO-99 (J)	150	°C/W
8-Pin Hermetic DIP (Z)	150	°C/W
8-Pin Plastic DIP (P)	100	°C/W
8-Pin SOIC (U)	160	°C/W

NOTES: (1) Maximum package power dissipation vs ambient temperature. (2) To common with $\pm V_{CC} = 15V$. (3) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

CONNECTION DIAGRAMS



ORDERING INFORMATION

MODEL (1)	PACKAGE	TEMPERATURE RANGE (°C)	OFFSET VOLTAGE MAX (µV), 25°C
OPA27AJ	TO-99	–55 to +125	±25
OPA27BJ	TO-99	–55 to +125	±60
OPA27CJ	TO-99	–55 to +125	±100
OPA27EJ	TO-99	–25 to +85	±25
OPA27FJ	TO-99	–25 to +85	±60
OPA27GJ	TO-99	–40 to +85	±100
OPA27AZ	Ceramic	–55 to +125	±25
OPA27BZ	Ceramic	–55 to +125	±60
OPA27CZ	Ceramic	–55 to +125	±100
OPA27EZ	Ceramic	–25 to +85	±25
OPA27FZ	Ceramic	–25 to +85	±60
OPA27GZ	Ceramic	–40 to +85	±100
OPA27GP	Plastic	–40 to +85	±100
OPA27GU (2)	SOIC	–40 to +85	±100

NOTE: (1) Packages and prices for OPA37 are same as for OPA27. (2) OPA27GU may be marked OPA27U. Likewise, OPA37GU may be marked OPA37U.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA27AJ	TO-99	001
OPA27BJ	TO-99	001
OPA27CJ	TO-99	001
OPA27EJ	TO-99	001
OPA27FJ	TO-99	001
OPA27GJ	TO-99	001
OPA27AZ	Ceramic	001
OPA27BZ	Ceramic	161
OPA27CZ	Ceramic	161
OPA27DZ	Ceramic	161
OPA27EZ	Ceramic	161
OPA27FZ	Ceramic	161
OPA27GZ	Ceramic	161
OPA27GP	Plastic	006
OPA27GU	SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

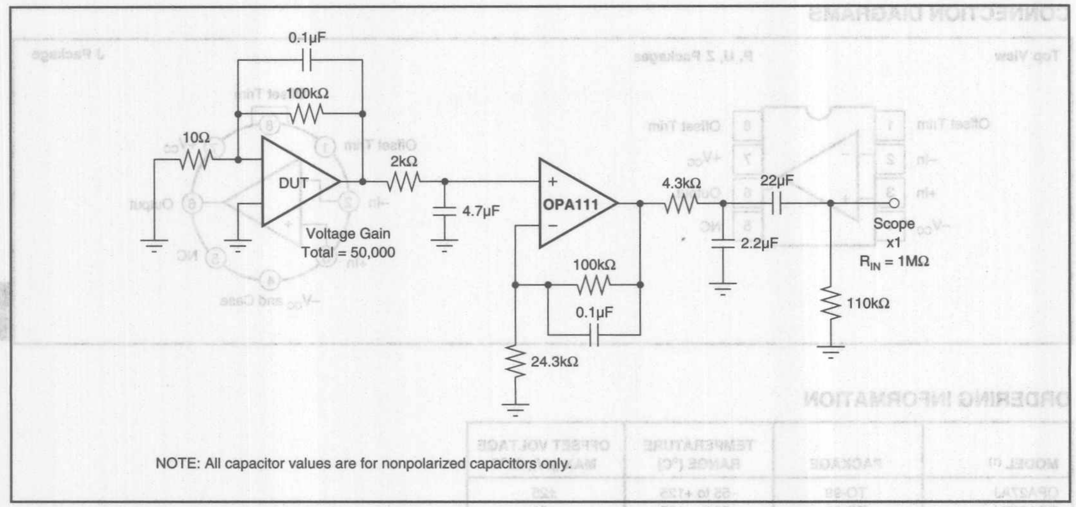


FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

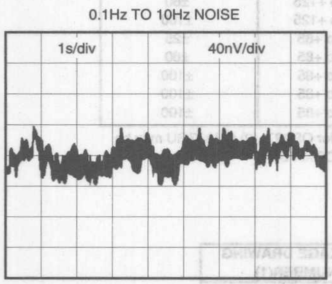
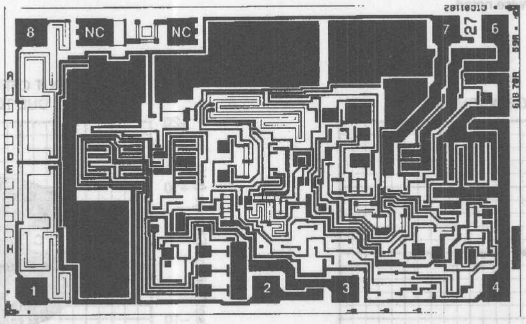
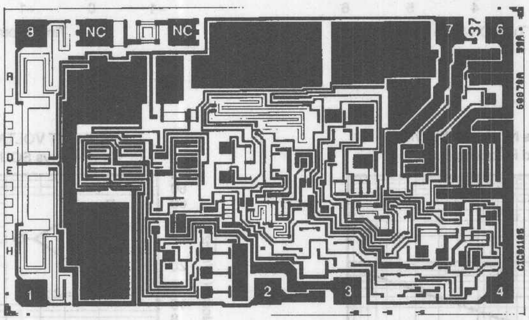


FIGURE 2. Low Frequency Noise.

DICE INFORMATION



OPA27 DIE TOPOGRAPHY



OPA37 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Trim	5	No Pad
2	–In	6	Output
3	+In	7	$+V_{CC}$
4	$-V_{CC}$	8	Offset Trim
		NC	No Connection

Substrate Bias: $-V_{CC}$

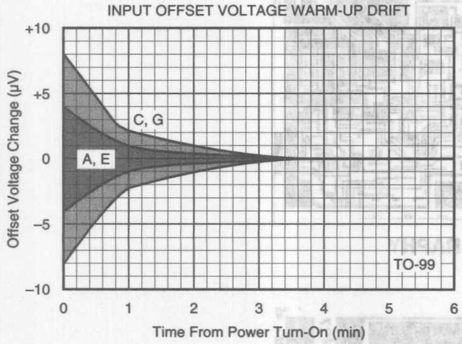
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	99 x 61 ±5	2.51 x 1.55 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
OPA27 Transistor Count		47
OPA37 Transistor Count		42
Backing		Gold

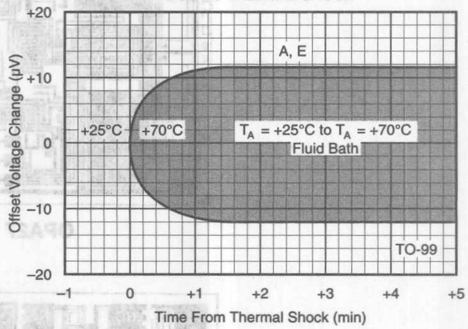
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $\pm V_{CC} = \pm 15VDC$ unless otherwise noted.

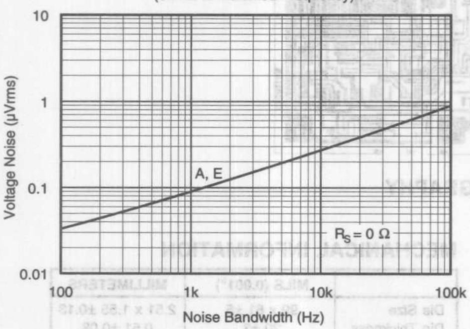
INPUT OFFSET VOLTAGE WARM-UP DRIFT



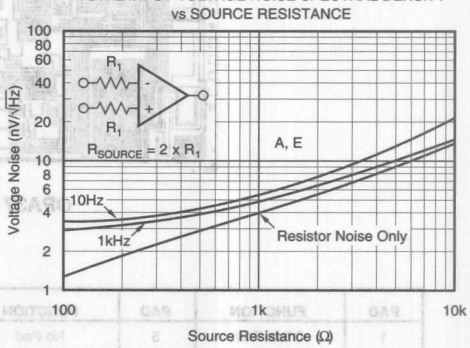
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



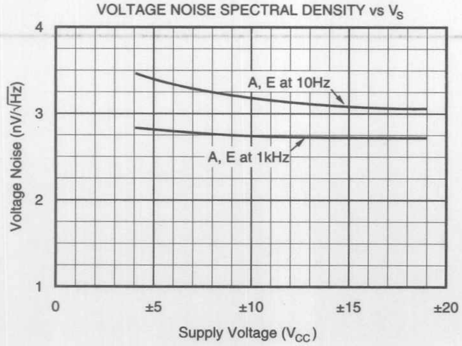
INPUT VOLTAGE NOISE vs NOISE BANDWIDTH (0.1Hz to Indicated Frequency)



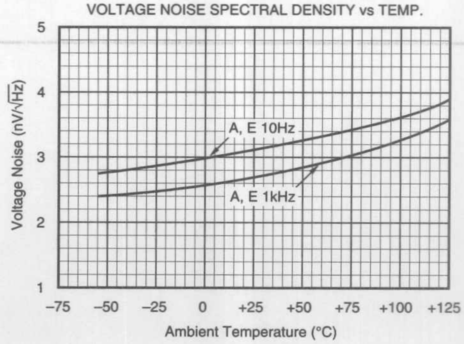
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



VOLTAGE NOISE SPECTRAL DENSITY vs V_S

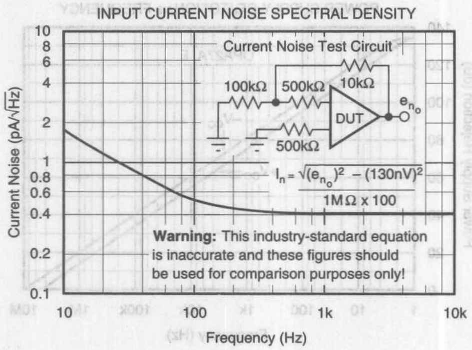


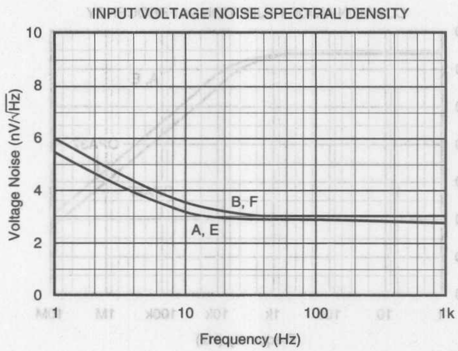
VOLTAGE NOISE SPECTRAL DENSITY vs TEMP.

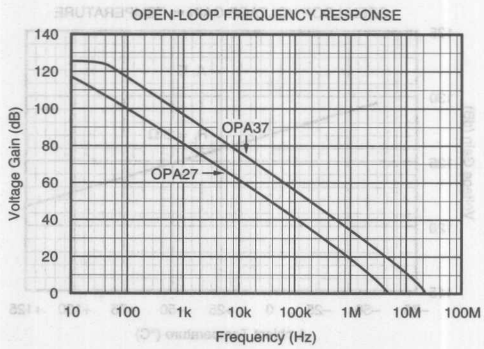


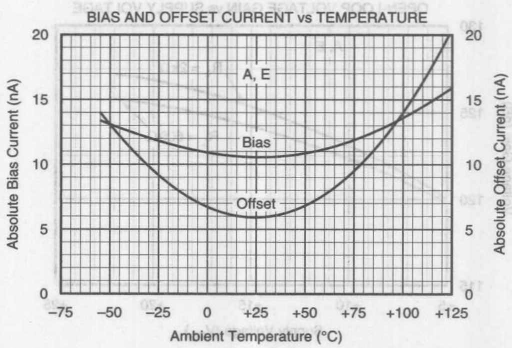
TYPICAL PERFORMANCE CURVES (CONT)

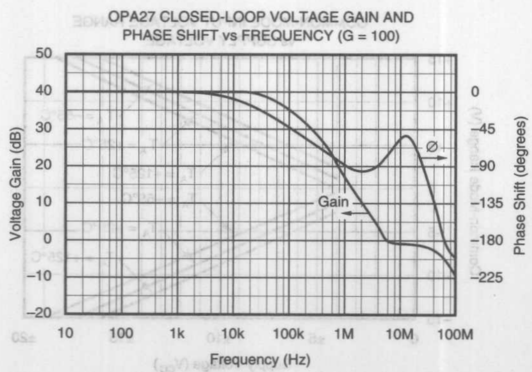
T_A = +25°C, $\pm V_{CC}$ = ±15VDC unless otherwise noted.

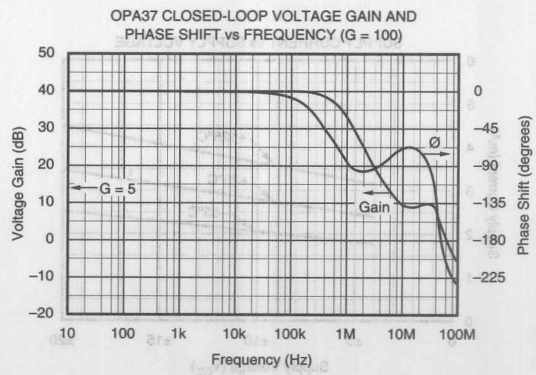






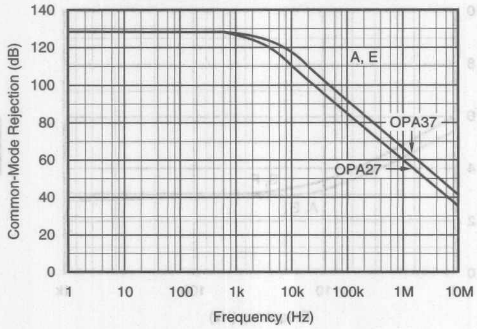




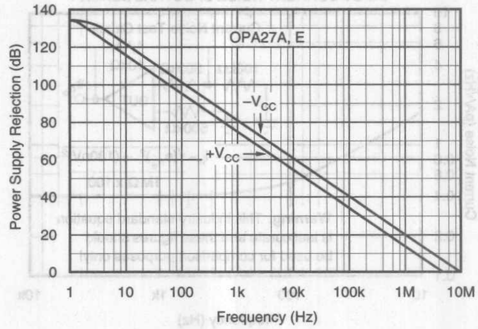


$T_A = +25°C$, $\pm V_{CC} = \pm 15VDC$ unless otherwise noted.

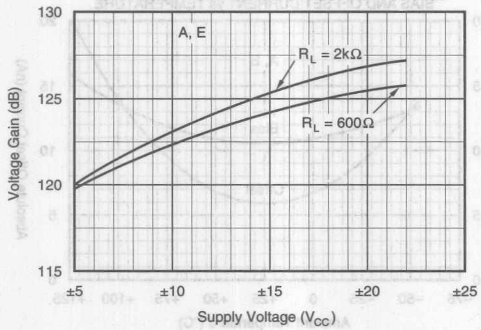
COMMON-MODE REJECTION vs FREQUENCY



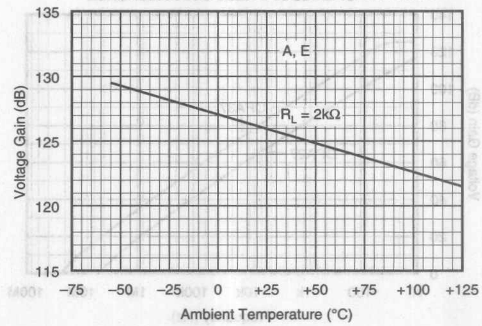
POWER SUPPLY REJECTION vs FREQUENCY



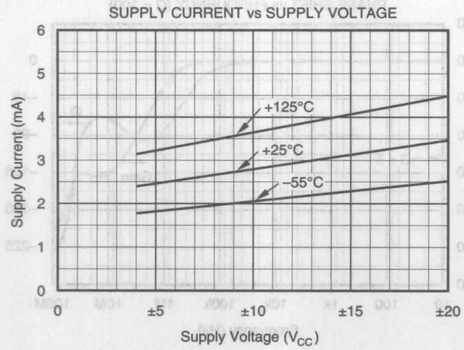
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



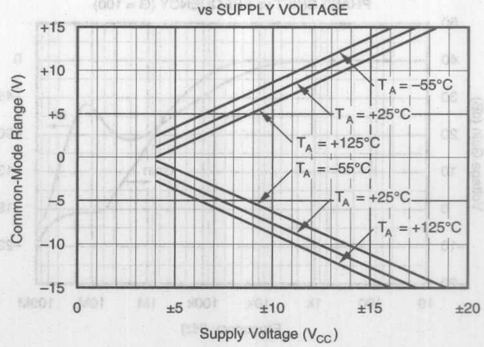
OPEN-LOOP VOLTAGE GAIN vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE



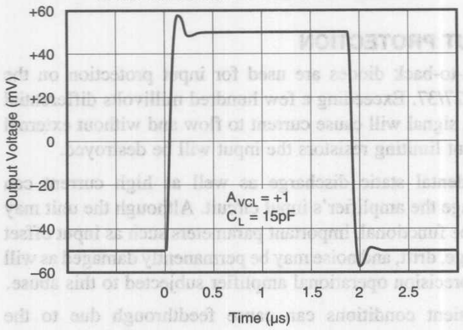
COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



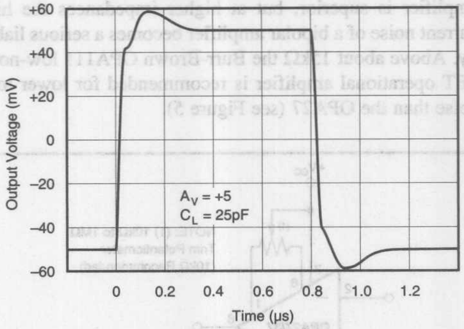
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $\pm V_{CC} = \pm 15VDC$ unless otherwise noted.

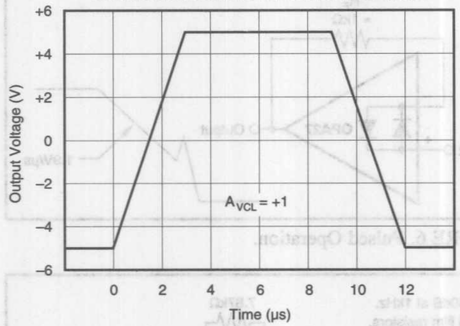
OPA27 SMALL SIGNAL TRANSIENT RESPONSE



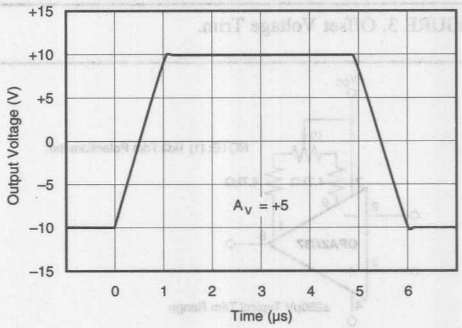
OPA37 SMALL SIGNAL TRANSIENT RESPONSE



OPA27 LARGE SIGNAL TRANSIENT RESPONSE



OPA37 LARGE SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA27/37 offset voltage is laser-trimmed and will require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a 10kΩ trim potentiometer. Other potentiometer values from 1kΩ to 1MΩ can be used but V_{OS} drift will be degraded by an additional 0.1 to 0.2µV/°C. Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately 3.3µV/°C per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very small offsets, the higher resolution circuit shown in Figure 4 is recommended.

The OPA27/37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

THERMOELECTRIC POTENTIALS

The OPA27/37 is laser-trimmed to microvolt-level input offset voltage and for very low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMFs if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference. See Figure 11.

Short, direct mounting of the OPA27/37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.

NOISE: BIPOLAR VERSUS FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the Burr-Brown OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27 (see Figure 5).

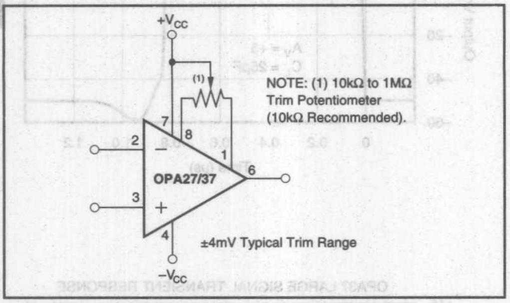


FIGURE 3. Offset Voltage Trim.

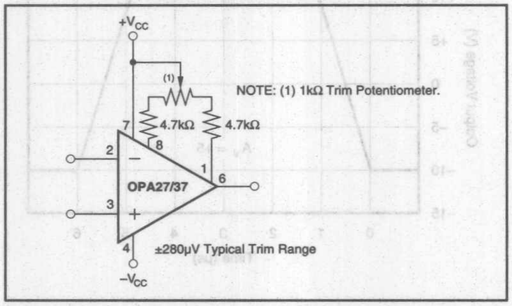


FIGURE 4. High Resolution Offset Voltage Trim.

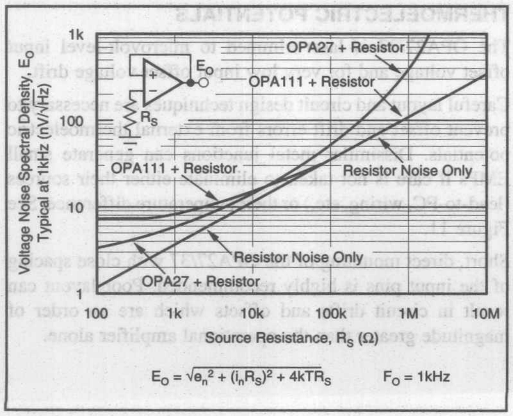


FIGURE 5. Voltage Noise Spectral Density Versus Source Resistance.

COMPENSATION

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor (R_F) which is greater than 2kΩ. This capacitor will compensate the pole generated by R_F and C_{IN} and eliminate peaking or oscillation.

INPUT PROTECTION

Back-to-back diodes are used for input protection on the OPA27/37. Exceeding a few hundred millivolts differential input signal will cause current to flow and without external current limiting resistors the input will be destroyed.

Accidental static discharge as well as high current can damage the amplifier's input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged as will any precision operational amplifier subjected to this abuse.

Transient conditions can cause feedthrough due to the amplifier's finite slew rate. When using the OP-27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended (see Figure 6).

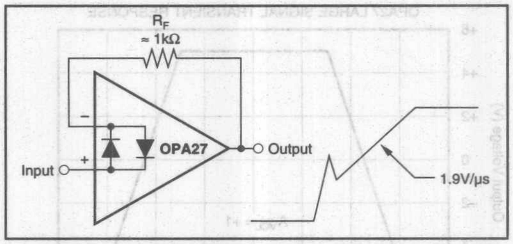


FIGURE 6. Pulsed Operation.

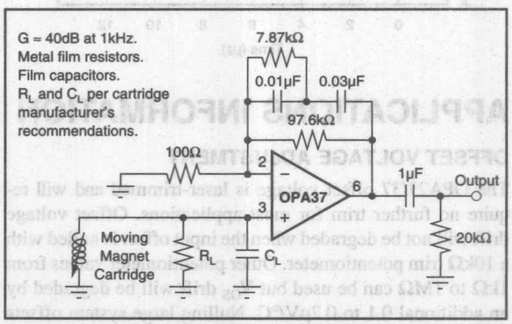


FIGURE 7. Low-Noise RIAA Preamplifier.

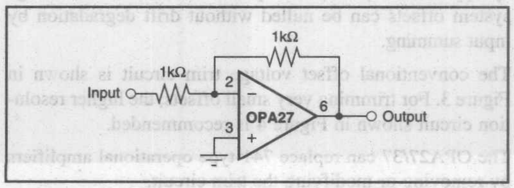


FIGURE 8. Unity-Gain Inverting Amplifier.

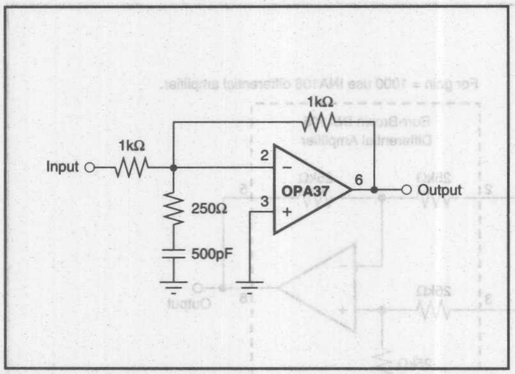


FIGURE 9. High Slew Rate Unity-Gain Inverting Amplifier.

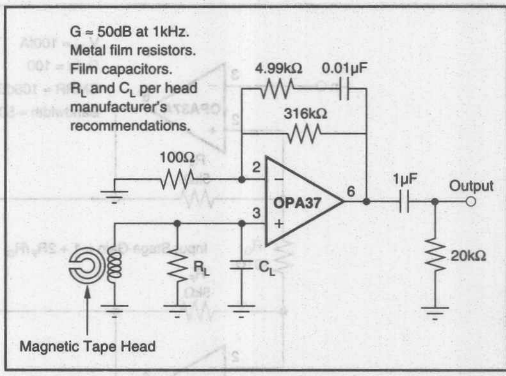


FIGURE 10. NAB Tape Head Preamplifier.

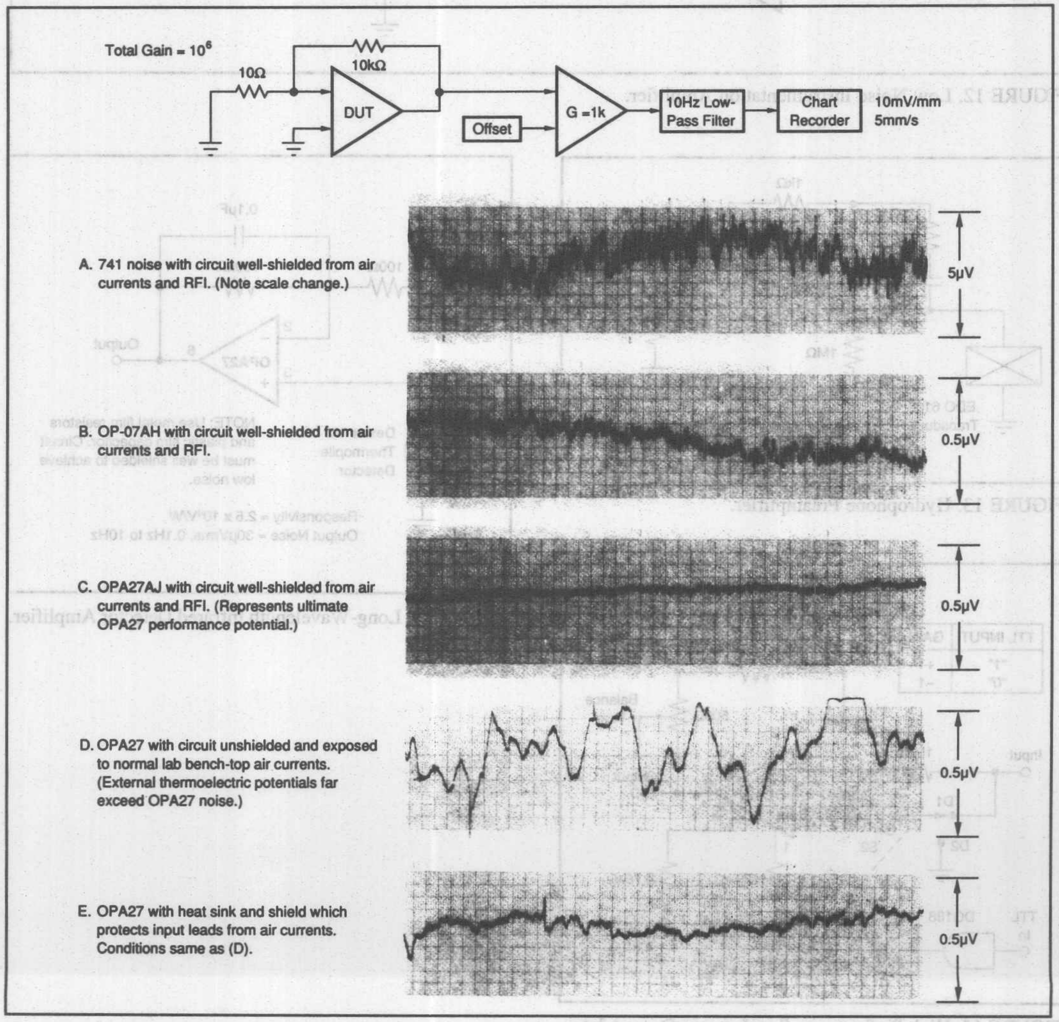


FIGURE 11. Low Frequency Noise Comparison.

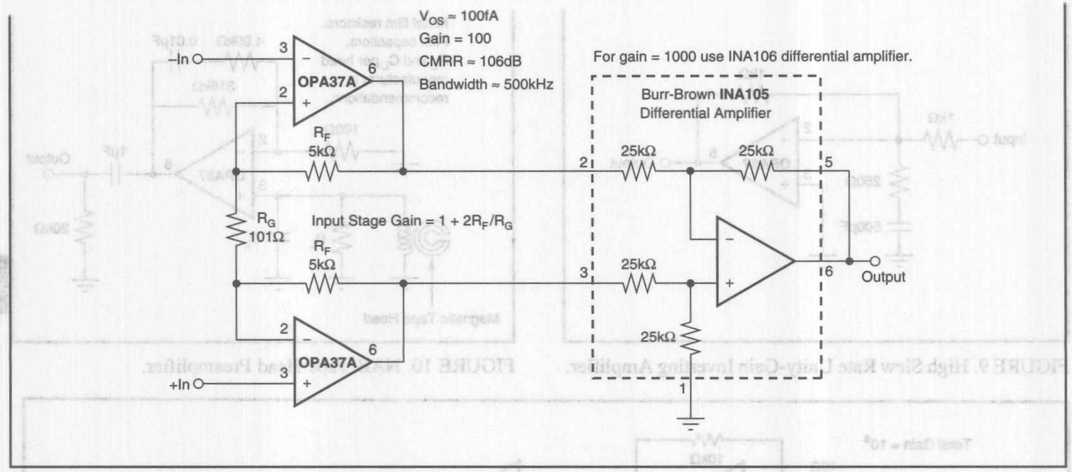


FIGURE 12. Low Noise Instrumentation Amplifier.

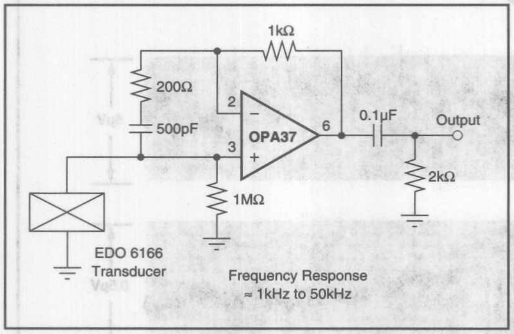


FIGURE 13. Hydrophone Preamplifier.

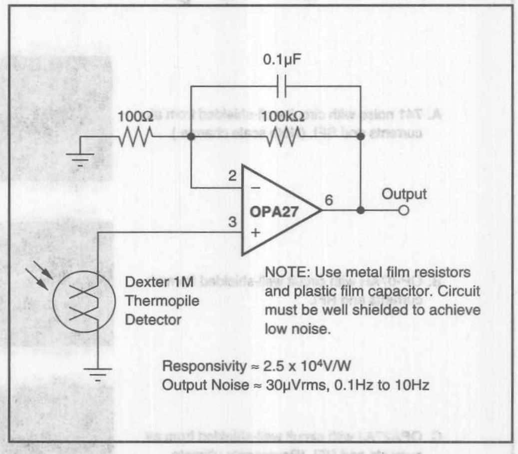


FIGURE 14. Long-Wavelength Infrared Detector Amplifier.

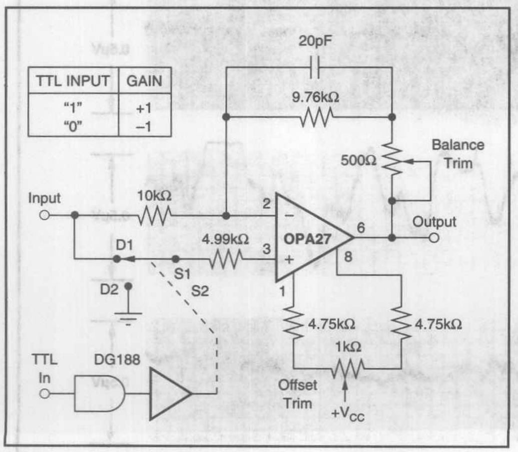


FIGURE 15. High Performance Synchronous Demodulator.

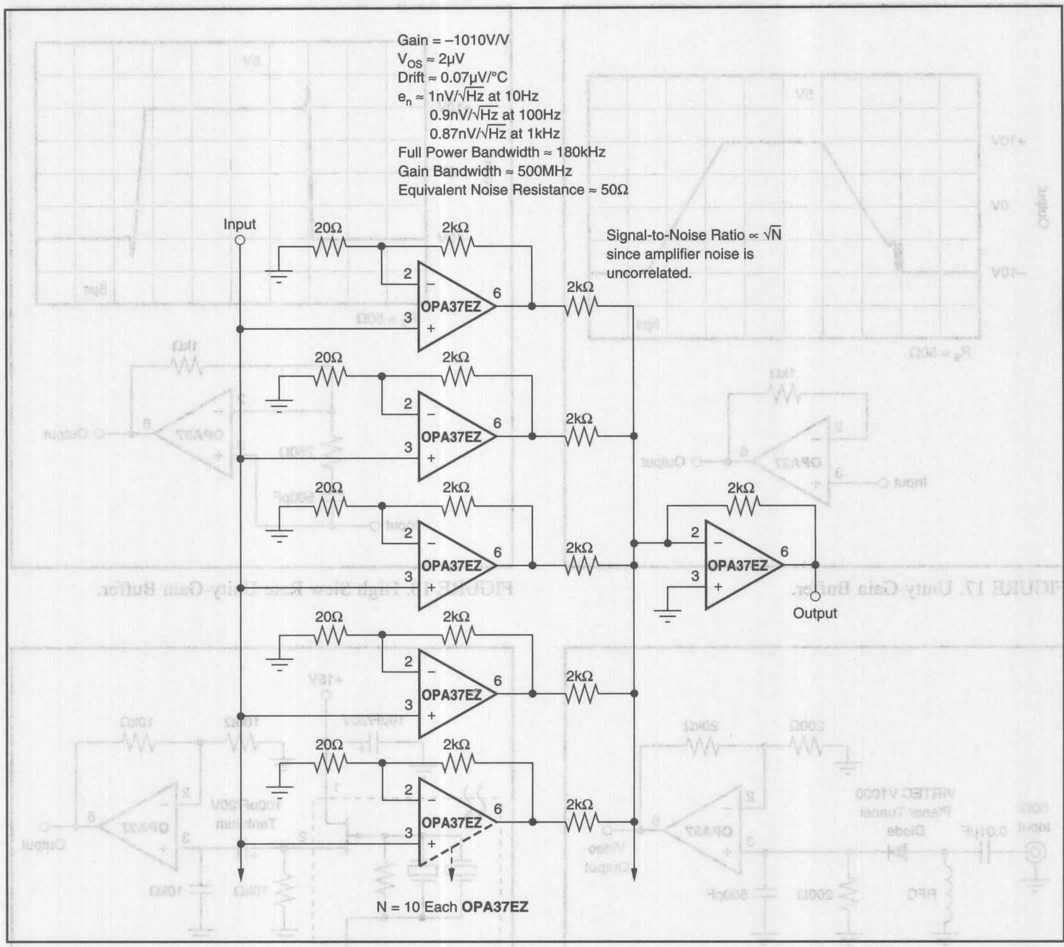


FIGURE 16. Ultra-Low Noise "N" Stage Parallel Amplifier.

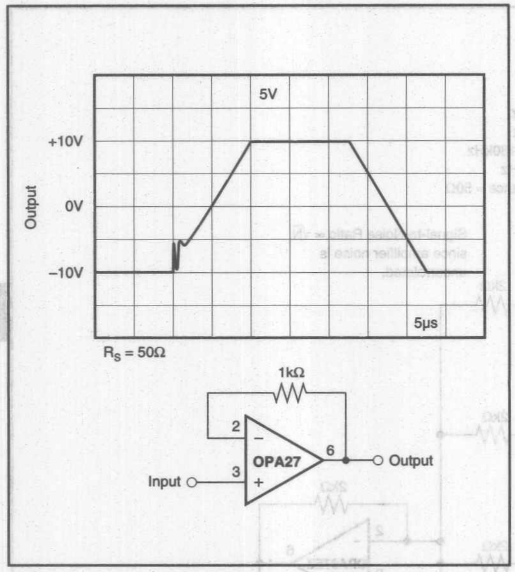


FIGURE 17. Unity-Gain Buffer.

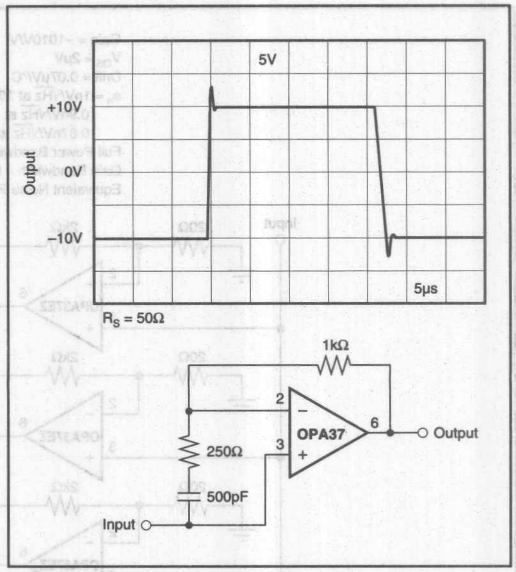


FIGURE 18. High Slew Rate Unity-Gain Buffer.

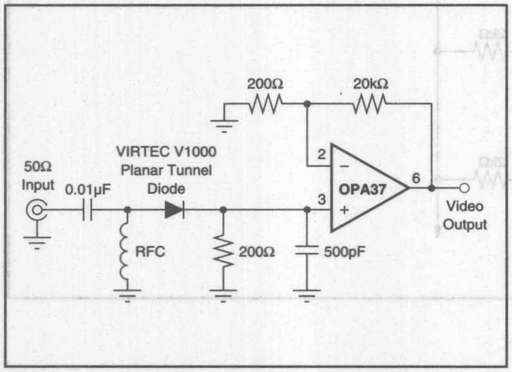


FIGURE 19. RF Detector and Video Amplifier.

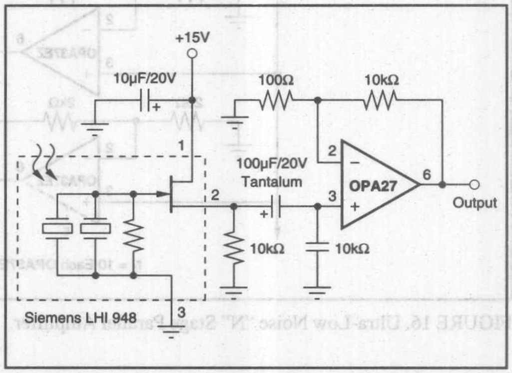


FIGURE 20. Balanced Pyroelectric Infrared Detector.

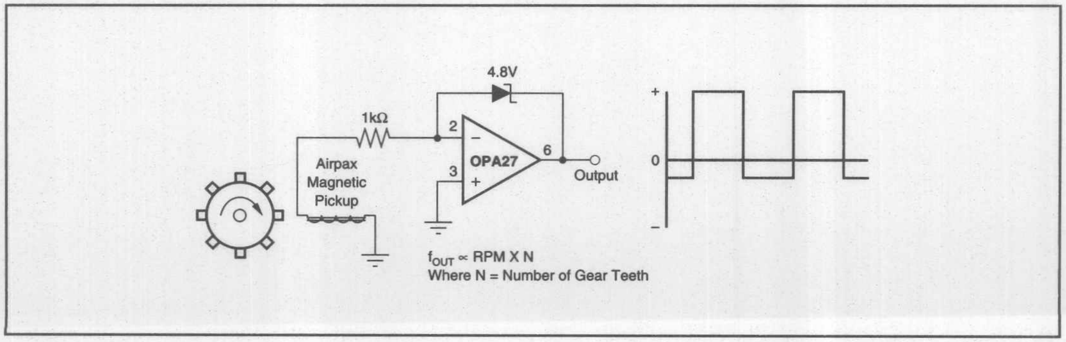
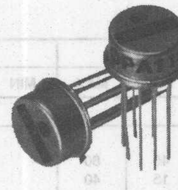


FIGURE 21. Magnetic Tachometer.

BURR - BROWN®



OPA111

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10526

Low Noise Precision *Difet*®
OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% Tested, 8nV$\sqrt{\text{Hz}}$ max (10kHz)
- LOW BIAS CURRENT: 1pA max
- LOW OFFSET: 250μV max
- LOW DRIFT: 1μV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 100dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- OPTOELECTRONICS
- MEDICAL EQUIPMENT—CAT SCANNER
- RADIATION HARD EQUIPMENT

DESCRIPTION

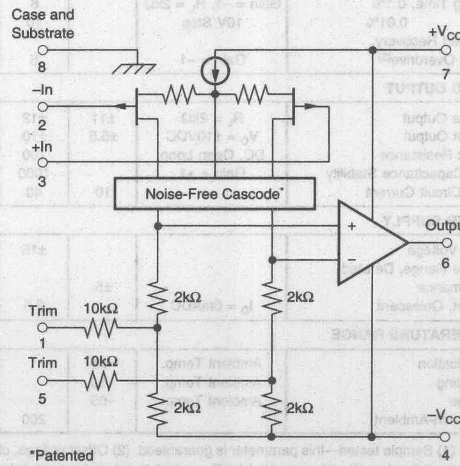
The OPA111 is a precision monolithic dielectrically isolated FET (*Difet*®) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



BIFET® National Semiconductor Corp., *Difet*® Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

		OPA111AM			OPA111BM			OPA111SM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT											
NOISE											
Voltage, f_O = 10Hz	100% Tested		40	80		30	60		40	80	nV/√Hz
f_O = 100Hz	100% Tested		15	40		11	30		15	40	nV/√Hz
f_O = 1kHz	100% Tested		8	15		7	12		8	15	nV/√Hz
f_O = 10kHz	100% Tested		6	8		6	8		6	8	nV/√Hz
f_B = 10Hz to 10kHz	100% Tested		0.7	1.2		0.6	1		0.7	1.2	µVrms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3	µVp-p
Current, f_B = 0.1Hz to 10Hz	(1)		9.5	15		7.5	12		9.5	15	fAp-p
f_O = 0.1Hz thru 20kHz	(1)		0.5	0.8		0.4	0.6		0.5	0.8	fA/√Hz
OFFSET VOLTAGE(2)											
Input Offset Voltage	V_{CM} = 0VDC		±100	±500		±50	±250		±100	±500	µV
Average Drift	T_A = T_{MIN} to T_{MAX}		±2	±5		±0.5	±1		±2	±5	µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	90	110		100	110		90	110		dB
			±3	±31		±3	±10		±3	±31	µV/V
BIAS CURRENT(2)											
Input Bias Current	V_{CM} = 0VDC		±0.8	±2		±0.5	±1		±0.8	±2	pA
OFFSET CURRENT(2)											
Input Offset Current	V_{CM} = 0VDC		±0.5	±1.5		±0.25	±0.75		±0.5	±1.5	pA
IMPEDANCE											
Differential			10^{13} ∥ 1			10^{13} ∥ 1			10^{13} ∥ 1		Ω ∥ pF
Common-Mode			10^{14} ∥ 3			10^{14} ∥ 3			10^{14} ∥ 3		Ω ∥ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		100	110		90	110		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	114	125		120	125		114	125		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			2			2			2		MHz
Full Power Response	20Vp-p, R_L = 2kΩ	16	32		16	32		16	32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2		1	2		1	2		V/µs
Settling Time, 0.1%	Gain = –1, R_L = 2kΩ		6			6			6		µs
0.01%	10V Step		10			10			10		µs
Overload Recovery, 50% Overdrive(3)	Gain = –1		5			5			5		µs
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		±11	±12		V
Current Output	V_O = ±10VDC	±5.5	±10		±5.5	±10		±5.5	±10		mA
Output Resistance	DC, Open Loop		100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		2.5	3.5		2.5	3.5		2.5	3.5	mA
TEMPERATURE RANGE											
Specification	Ambient Temp.	–25		+85	–25		+85	–55		+125	°C
Operating	Ambient Temp.	–55		+125	–55		+125	–55		+125	°C
Storage	Ambient Temp.	–65		+150	–65		+150	–65		+150	°C
θ Junction-Ambient			200			200			200		°C/W

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

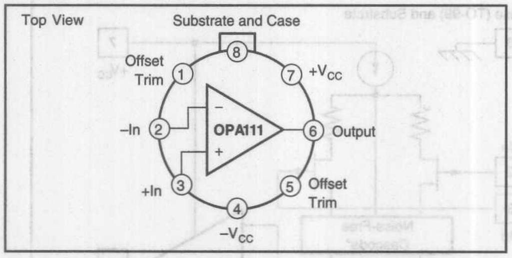
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

		OPA111AM			OPA111BM			OPA111SM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE											
Specification Range	Ambient Temp.	–25		+85	–25		+85	–55		+125	°C
INPUT											
OFFSET VOLTAGE(1)											
Input Offset Voltage	V_{CM} = 0VDC		±220	±1000		±110	±500		±300	±1500	µV
Average Drift			±2	±5		±0.5	±1		±2	±5	µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	86	100		90	100		86	100		dB
			±10	±50		±10	±32		±10	±50	µV/V
BIAS CURRENT(1)											
Input Bias Current	V_{CM} = 0VDC		±50	±250		±30	±130		±820	±4100	pA
OFFSET CURRENT(1)											
Input Offset Current	V_{CM} = 0VDC		±30	±200		±15	±100		±510	±3100	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	110	120		114	120		110	120		dB
RATED OUTPUT											
Voltage Output	$R_L = 2k\Omega$	±10.5	±11		±11	±11.5		±11	±11.5		V
Current Output	V_O = ±10VDC	±5.25	±10		±5.25	±10		±5.25	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		10	40		mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		2.5	3.5		2.5	3.5		2.5	3.5	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation(1)	750mW
Differential Input Voltage(2)	±36VDC
Input Voltage Range(2)	±18VDC
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration(3)	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{JC} = 150°C/W or θ_{JA} = 300°C/W. (2) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to $+18V > V_{IN} > -V_{CC} - 6V$. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

PACKAGE INFORMATION

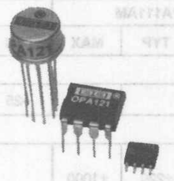
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA111AM	TO-99	001
OPA111BM	TO-99	001
OPA111SM	TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE, MAX (µV)
OPA111AM	TO-99	–25°C to +85°C	±500
OPA111BM	TO-99	–25°C to +85°C	±250
OPA111SM	TO-99	–55°C to +125°C	±500

BURR - BROWN®



OPA121

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10539

Low Cost Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 6nV/√Hz typ at 10kHz
- LOW BIAS CURRENT: 5pA max
- LOW OFFSET: 2mV max
- LOW DRIFT: 3μV/°C typ
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 86dB min

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- MEDICAL EQUIPMENT
- RADIATION HARD EQUIPMENT

DESCRIPTION

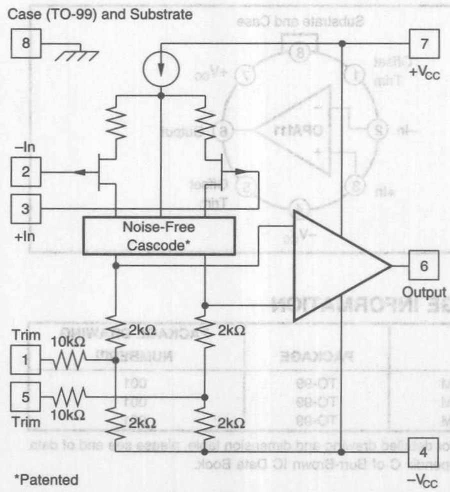
The OPA121 is a precision monolithic dielectrically-isolated FET (*Difet*®) operational amplifier. Outstanding performance characteristics are now available for low-cost applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



OPA121 Simplified Circuit

Difet®, Burr-Brown Corp.
BIFET®, National Semiconductor Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA121KM MIN	OPA121KM TYP	OPA121KM MAX	OPA121KP, KU MIN	OPA121KP, KU TYP	OPA121KP, KU MAX	UNITS
INPUT								
NOISE								
Voltage, f_O = 10Hz	(1)		40			50		nV/√Hz
f_O = 100Hz	(1)		15			18		nV/√Hz
f_O = 1kHz	(1)		8			10		nV/√Hz
f_O = 10kHz	(1)		6			7		nV/√Hz
f_B = 10Hz to 10kHz	(1)		0.7			0.8		μVrms
f_B = 0.1Hz to 10 Hz	(1)		1.6			2		μVp-p
Current, f_B = 0.1Hz to 10Hz	(1)		15			21		fA, p-p
f_O = 0.1Hz thru 20kHz	(1)		0.8			1.1		fA/√Hz
OFFSET VOLTAGE(2)								
Input Offset Voltage	V_{CM} = 0VDC		±0.5	±2		±0.5	±3	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		±3	±10	μV/°C
Supply Rejection		86	104		86	104		dB
			±6	±50		±6	±50	μV/V
BIAS CURRENT(2)								
Input Bias Current	V_{CM} = 0VDC Device Operating		±1	±5		±1	±10	pA
OFFSET CURRENT(2)								
Input Offset Current	V_{CM} = 0VDC Device Operating		±0.7	±4		±0.7	±8	pA
IMPEDANCE								
Differential			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			10^{14} ‖ 3		Ω ‖ pF
VOLTAGE RANGE								
Common-Mode Input Range		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	104		82	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	R_L ≥ 2kΩ	110	120		106	114		dB
FREQUENCY RESPONSE								
Unity Gain, Small Signal			2			2		MHz
Full Power Response	20Vp-p, R_L = 2kΩ		32			32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ		2			2		V/μs
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		6			6		μs
0.01%	10V Step		10			10		μs
Overload Recovery, 50% Overdrive(3)	Gain = −1		5			5		μs
RATED OUTPUT								
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		V
Current Output	V_O = ±10VDC	±5.5	±10		±5.5	±10		mA
Output Resistance	DC, Open Loop		100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000		pF
Short Circuit Current		10	40		10	40		mA
POWER SUPPLY								
Rated Voltage			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		2.5	4		2.5	4.5	mA
TEMPERATURE RANGE								
Specification	Ambient Temperature	0		+70	0		+70	°C
Operating	Ambient Temperature	−40		+85	−25		+85	°C
Storage	Ambient Temperature	−65		+150	−55		+125	°C
θ Junction-Ambient			200			150(4)		°C/W

NOTES: (1) Sample tested. (2) Offset voltage, offset current, and bias current are specified with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) 100°C/W for KU grade.

PARAMETER	CONDITIONS	OPA121KM MIN	OPA121KM TYP	OPA121KM MAX	OPA121KP, KU MIN	OPA121KP, KU TYP	OPA121KP, KU MAX	UNITS
TEMPERATURE RANGE								
Specification Range	Ambient Temperature	0		+70	0		+70	°C
INPUT								
OFFSET VOLTAGE(1)								
Input Offset Voltage	V_{CM} = 0VDC		±1	±3		±1	±5	mV
Average Drift			±3	±10		±3	±10	µV/°C
Supply Rejection		82	94		82	94		dB
			±20	±80		±20	±80	µV/V
BIAS CURRENT(1)								
Input Bias Current	V_{CM} = 0VDC Device Operating		±23	±115		±23	±250	pA
OFFSET CURRENT(1)								
Input Offset Current	V_{CM} = 0VDC Device Operating		±16	±100		±16	±200	pA
VOLTAGE RANGE								
Common-Mode Input Range		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	82	98		80	96		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	116		100	110		dB
RATED OUTPUT								
Voltage Output	$R_L = 2k\Omega$	±10.5	±11		±10.5	±11		V
Current Output	V_O = ±10VDC	±5.25	±10		±5.25	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		mA
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		2.5	4.5		2.5	5	mA

NOTE: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

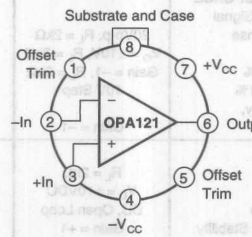
ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	
M package	–65°C to +150°C
P, U packages	–55°C to +125°C
Operating Temperature Range	
M package	–40°C to +85°C
P, U packages	–25°C to +85°C
Lead Temperature	
M, P packages (soldering, 10s)	+300°C
U package (soldering, 3s)	+260°C
Output Short-Circuit Duration(2)	Continuous
Junction Temperature	+175°C

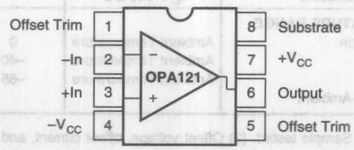
NOTES: (1) Packages must be derated based on θ_{JA} = 150°C/W (P package); θ_{JA} = 200°C/W (M package); θ_{JA} = 100°C/W (U package). (2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

CONNECTION DIAGRAMS

Top View — **M-Package** TO-99 (Hermetic)



Top View — **P-Package** Plastic Mini-DIP, **U-Package** Plastic SOIC



PACKAGE INFORMATION

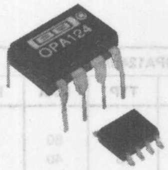
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA121KM	TO-99	001
OPA121KP	8-Pin Plastic DIP	006
OPA121KU	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA121KM	TO-99	0°C to +70°C
OPA121KP	8-Pin Plastic DIP	0°C to +70°C
OPA121KU	8-Pin SOIC	0°C to +70°C

BURR - BROWN®



OPA124

Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- **LOW NOISE: 6nV/√Hz (10kHz)**
- **LOW BIAS CURRENT: 1pA max**
- **LOW OFFSET: 250μV max**
- **LOW DRIFT: 2μV/°C max**
- **HIGH OPEN-LOOP GAIN: 120dB min**
- **HIGH COMMON-MODE REJECTION: 100dB min**
- **AVAILABLE IN 8-PIN PLASTIC DIP AND 8-PIN SOIC PACKAGES**

APPLICATIONS

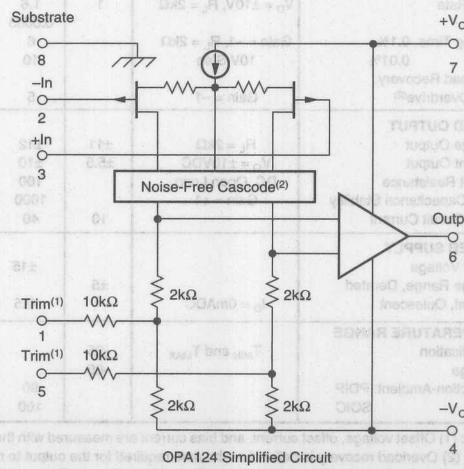
- **PRECISION PHOTODIODE PREAMP**
- **MEDICAL EQUIPMENT**
- **OPTOELECTRONICS**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**

DESCRIPTION

The OPA124 is a precision monolithic FET operational amplifier using a ***Difet*** (dielectrical isolation) manufacturing process. Outstanding DC and AC performance characteristics allow its use in the most critical instrumentation applications.

Bias current, noise, voltage offset, drift, open-loop gain, common-mode rejection and power supply rejection are superior to BIFET and CMOS amplifiers. ***Difet*** fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry. This cascode design also allows high precision input specifications and reduced susceptibility to flicker noise. Laser trimming of thin-film resistors gives very low offset and drift.

Compared to the popular OPA111, the OPA124 gives comparable performance and is available in an 8-pin PDIP and 8-pin SOIC package.



OPA124 Simplified Circuit

NOTES: (1) Omitted on SOIC. (2) Patented.

BIFET® National Semiconductor Corp.,
Difet® Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

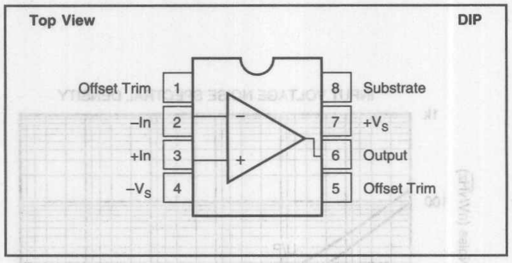
ELECTRICAL

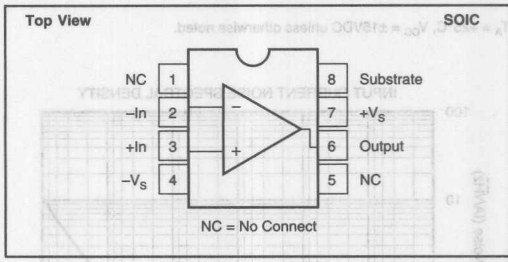
At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

		OPA124U/P			OPA124UA/PA			OPA124UB/PB			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT NOISE											
Voltage, f_O = 10Hz(4)			40	80		40	80		40	80	$nV/\sqrt{Hz}$
f_O = 100Hz(4)			15	40		15	40		15	40	$nV/\sqrt{Hz}$
f_O = 1kHz(4)			8	15		8	15		8	15	$nV/\sqrt{Hz}$
f_O = 10kHz(5)			6	8		6	8		6	8	$nV/\sqrt{Hz}$
f_B = 10Hz to 10kHz(5)			0.7	1.2		0.7	1.2		0.7	1.2	µVrms
f_B = 0.1Hz to 10Hz			1.6	3.3		1.6	3.3		1.6	3.3	µVp-p
Current, f_B = 0.1Hz to 10Hz			9.5	15		9.5	15		9.5	15	fAp-p
f_O = 0.1Hz thru 20kHz			0.5	0.8		0.5	0.8		0.5	0.8	$fA/\sqrt{Hz}$
OFFSET VOLTAGE(1)											
Input Offset Voltage	V_{CM} = 0VDC		±200	±800		±150	±500		±100	±250	µV
vs Temperature	T_A = T_{MIN} to T_{MAX}		±4	±7.5		±2	±4		±1	±2	µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	88	110		90	110		100	110		dB
vs Temperature	T_A = T_{MIN} to T_{MAX}	84	100		86	100		90	100		dB
BIAS CURRENT(1)											
Input Bias Current	V_{CM} = 0VDC		±1	±5		±0.5	±2		±0.35	±1	pA
OFFSET CURRENT(1)											
Input Offset Current	V_{CM} = 0VDC		±1	±5		±0.5	±1		±0.25	±0.5	pA
IMPEDANCE											
Differential			10^{13} ǁ 1			10^{13} ǁ 1			10^{13} ǁ 1		Ω ǁ pF
Common-Mode			10^{14} ǁ 3			10^{14} ǁ 3			10^{14} ǁ 3		Ω ǁ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	92	110		94	110		100	110		dB
vs Temperature	T_A = T_{MIN} to T_{MAX}	86	100		86	100		90	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	106	125		106	125		120	125		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			1.5			1.5			1.5		MHz
Full Power Response	20Vp-p, R_L = 2kΩ	16	32		16	32		16	32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	1.6		1	1.6		1	1.6		V/µs
THD			0.0003			0.0003			0.0003		%
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		6			6			6		µs
0.01%	10V Step		10			10			10		µs
Overload Recovery, 50% Overdrive(2)	Gain = −1		5			5			5		µs
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		±11	±12		V
Current Output	V_O = ±10VDC	±5.5	±10		±5.5	±10		±5.5	±10		mA
Output Resistance	DC, Open Loop		100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		2.5	3.5		2.5	3.5		2.5	3.5	mA
TEMPERATURE RANGE											
Specification	T_{MIN} and T_{MAX}	−25		+85	−25		+85	−25		+85	°C
Storage		−65		+125	−65		+125	−65		+125	°C
θ Junction-Ambient: PDIP			90			90			90		°C/W
SOIC			100			100			100		°C/W

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. For performance at other temperatures see Typical Performance Curves. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (3) For performance at other temperatures see Typical Performance Curves. (4) Sample tested, 98% confidence. (5) Guaranteed by design.

CONNECTION DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation(1)	750mW
Differential Input Voltage(2)	±36VDC
Input Voltage Range(2)	±18VDC
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration(3)	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{JA} = 90°C/W for PDIP and 100°C/W for SOIC. (2) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to $+18V > V_{IN} > -V_{CC} - 6V$. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA124U	8-Pin SOIC	182
OPA124P	8-Pin Plastic DIP	006
OPA124UA	8-Pin SOIC	182
OPA124PA	8-Pin Plastic DIP	006
OPA124UB	8-Pin SOIC	182
OPA124PB	8-Pin Plastic DIP	006

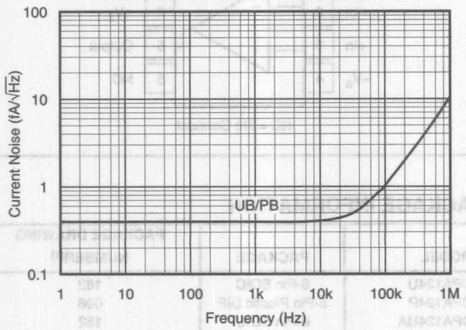
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

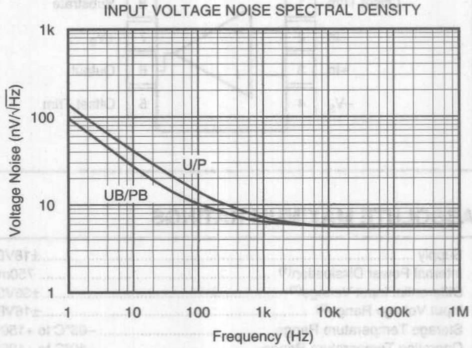
MODEL	PACKAGE	TEMPERATURE RANGE	BIAS CURRENT pA, max	OFFSET DRIFT µV/°C, max
OPA124U	8-PIN SOIC	–25°C TO +85°C	5	7.5
OPA124P	8-Pin Plastic DIP	–25°C to +85°C	5	7.5
OPA124UA	8-Pin SOIC	–25°C to +85°C	2	4
OPA124PA	8-Pin Plastic DIP	–25°C to +85°C	2	4
OPA124UB	8-Pin SOIC	–25°C to +85°C	1	2
OPA124PB	8-Pin Plastic DIP	–25°C to +85°C	1	2

$T_A = +25°C$, $V_{CC} = ±15VDC$ unless otherwise noted.

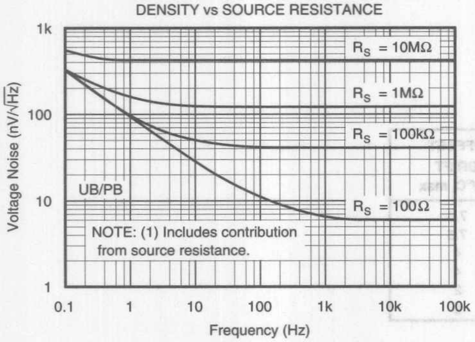
INPUT CURRENT NOISE SPECTRAL DENSITY



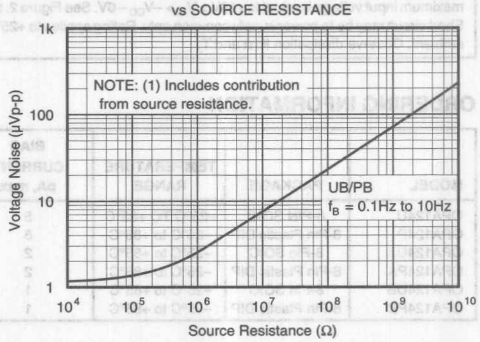
INPUT VOLTAGE NOISE SPECTRAL DENSITY



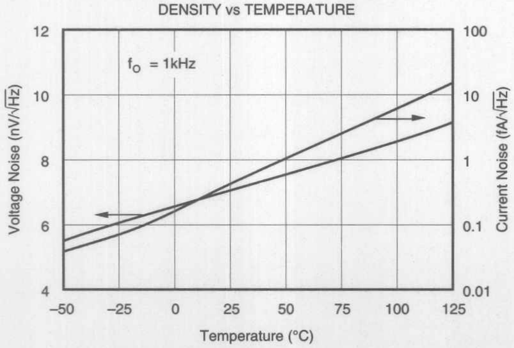
TOTAL[1] INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



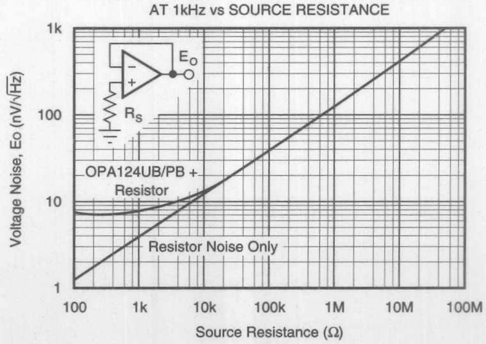
TOTAL[1] INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



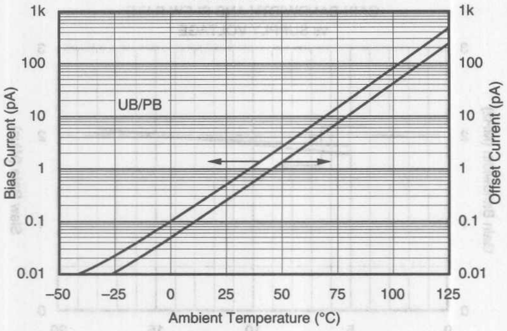
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



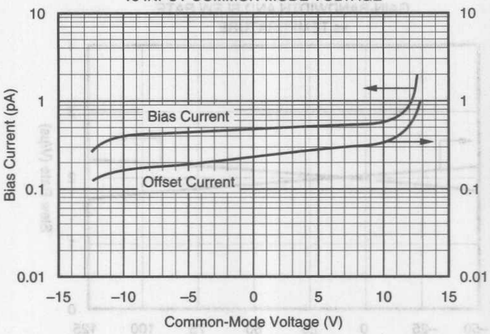
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

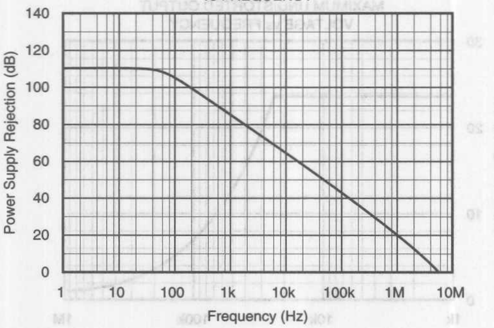
BIAS AND OFFSET CURRENT vs TEMPERATURE



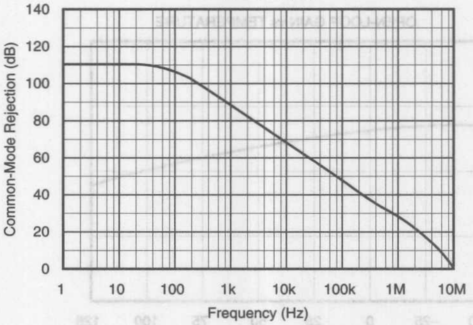
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



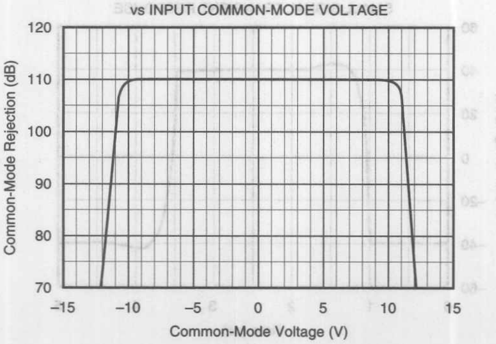
POWER SUPPLY REJECTION vs FREQUENCY



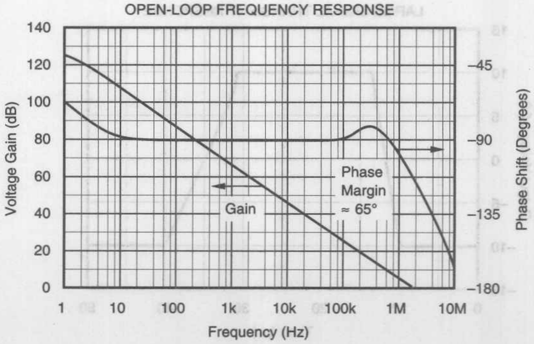
COMMON-MODE REJECTION vs FREQUENCY



COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE

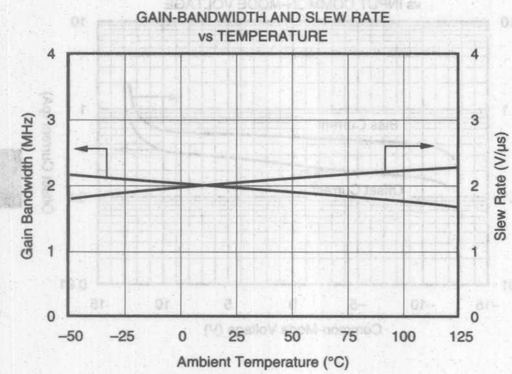


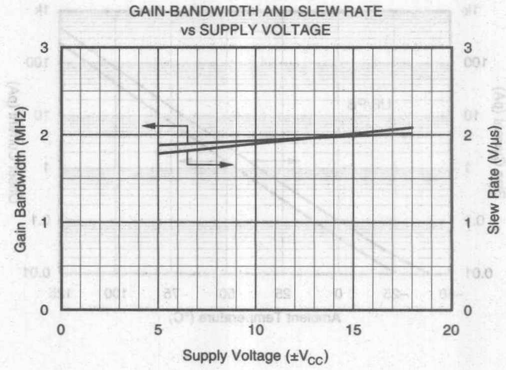
OPEN-LOOP FREQUENCY RESPONSE

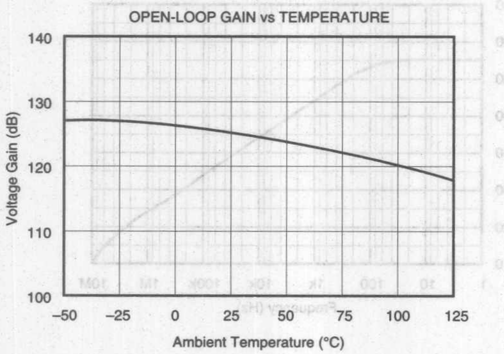


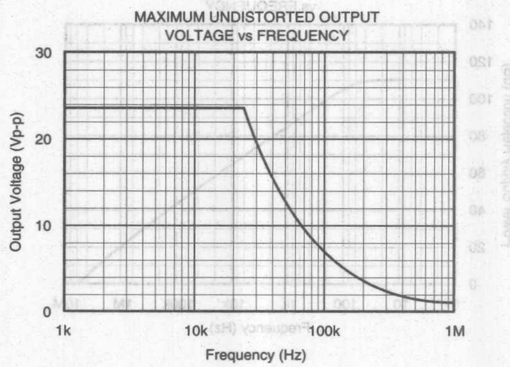
TYPICAL PERFORMANCE CURVES (CONT)

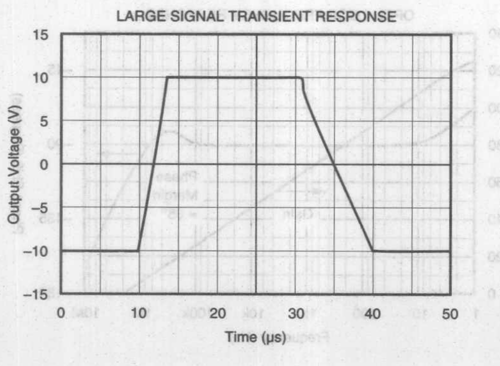
$T_A = +25°C$, $V_{CC} = \pm15VDC$ unless otherwise noted.

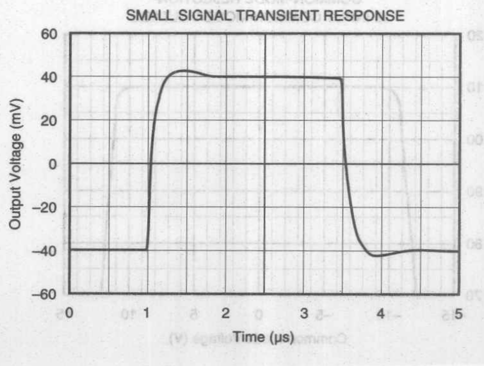








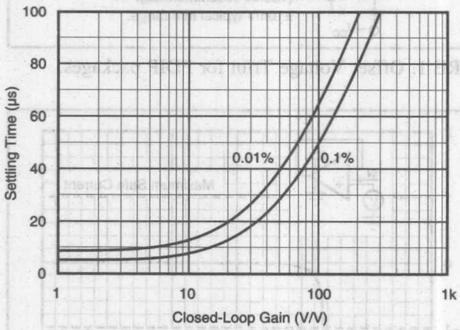




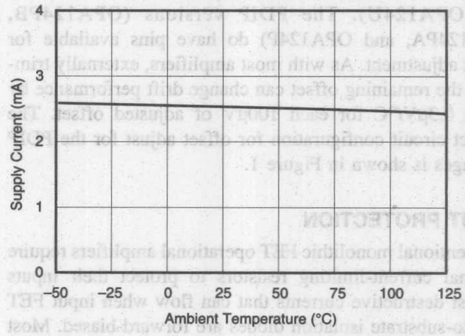
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

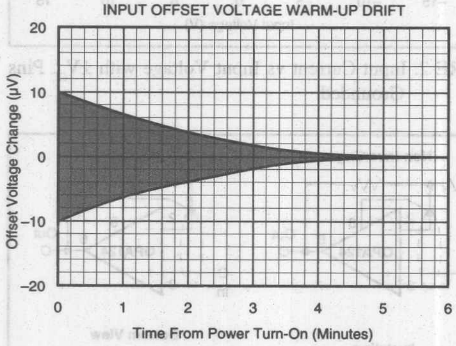
SETTLING TIME vs CLOSED-LOOP GAIN



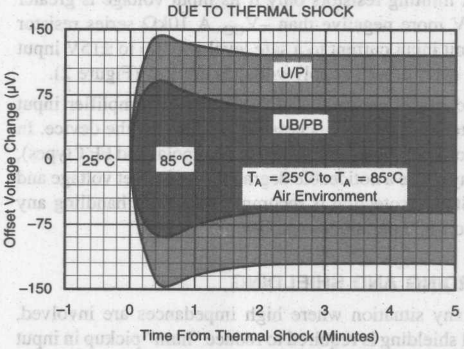
SUPPLY CURRENT vs TEMPERATURE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



OPA124

2

OPERATIONAL AMPLIFIERS

APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA124 offset voltage is laser-trimmed and will require no further trim for most applications. In order to reduce layout leakage errors, the offset adjust capability has been removed from the SOIC versions (OPA124UB, OPA124UA, and OPA124U). The PDIP versions (OPA124PB, OPA124PA, and OPA124P) do have pins available for offset adjustment. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3µV/°C for each 100µV of adjusted offset. The correct circuit configuration for offset adjust for the PDIP packages is shown in Figure 1.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the ***Difet*** OPA124 requires input current limiting resistors only if its input voltage is greater than 6V more negative than $-V_{CC}$. A 10kΩ series resistor will limit input current to a safe level with up to ±15V input levels, even if both supply voltages are lost (Figure 2).

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA124. To avoid leakage problems, the OPA124 should be soldered directly into a printed circuit board. Utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier substrate should be connected to any input shield or guard via pin 8 minimizing both leakage and noise pickup (see Figure 3).

If guarding is not required, pin 8 should be connected to ground.

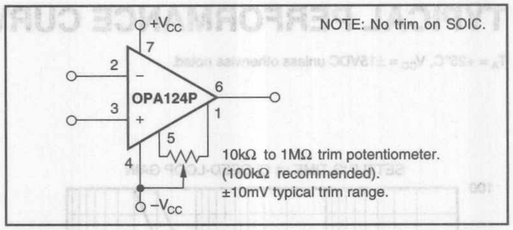


FIGURE 1. Offset Voltage Trim for PDIP packages.

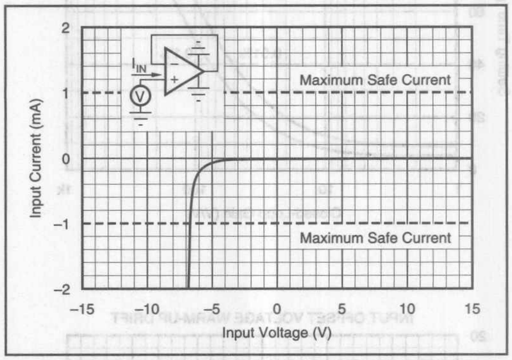


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

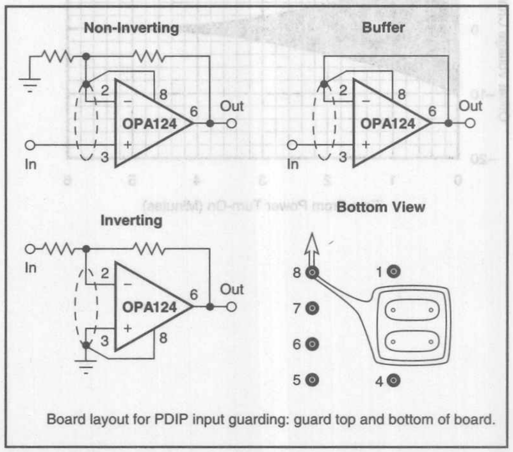
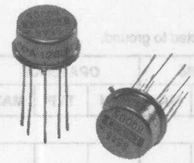


FIGURE 3. Connection of Input Guard.

BURR - BROWN®



OPA128

Difet® Electrometer-Grade OPERATIONAL AMPLIFIER

FEATURES

- ULTRA-LOW BIAS CURRENT: 75fA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 5μV/°C max
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 90dB min
- IMPROVED REPLACEMENT FOR AD515 AND AD549

APPLICATIONS

- ELECTROMETER
- MASS SPECTROMETER
- CHROMATOGRAPH
- ION GAUGE
- PHOTODETECTOR
- RADIATION-HARD EQUIPMENT

DESCRIPTION

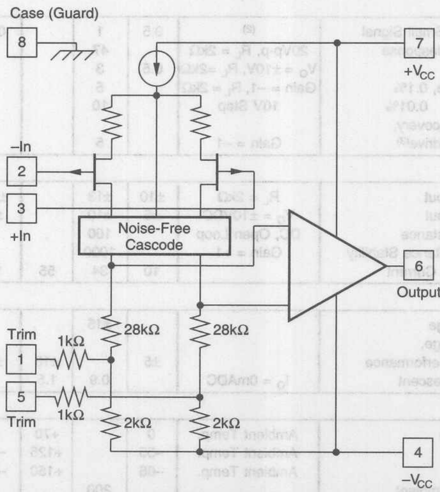
The OPA128 is an ultra-low bias current monolithic operational amplifier. Using advanced geometry dielectrically-isolated FET (***Difet®***) inputs, this monolithic amplifier achieves a performance level exceeding even the best hybrid electrometer amplifiers.

Laser-trimmed thin-film resistors give outstanding voltage offset and drift performance.

A noise-free cascode and low-noise processing give the OPA128 excellent low-level signal handling capabilities. Flicker noise is very low.

The OPA128 is an improved pin-for-pin replacement for the AD515.

Difet® Burr-Brown Corp.



OPA128 Simplified Circuit

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA128JM MIN	OPA128JM TYP	OPA128JM MAX	OPA128KM MIN	OPA128KM TYP	OPA128KM MAX	OPA128LM MIN	OPA128LM TYP	OPA128LM MAX	OPA128SM MIN	OPA128SM TYP	OPA128SM MAX	UNITS
BIAS CURRENT(1)														
Input Bias Current	V_{CM} = 0VDC, $R_L \geq 10k\Omega$		±150	±300		±75	±150		±40	±75		±75	±150	fA
OFFSET CURRENT(1)														
Input Offset Current	V_{CM} = 0VDC, $R_L \geq 10k\Omega$		65			30			30			30		fA
OFFSET VOLTAGE(1)														
Input Offset Voltage	V_{CM} = 0VDC		±260	±1000		±140	±500		±140	±500		±140	±500	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}			±20			±10			±5			±10	µV/°C
Supply Rejection		80	120		90	120		90	120		90	120		dB
			±1	±100		±1	±32		±1	±32		±1	±32	µV/V
NOISE														
Voltage: f_O = 10Hz			92			92			92			92		nV/√Hz
f_O = 100Hz			78			78			78			78		nV/√Hz
f_O = 1kHz			27			27			27			27		nV/√Hz
f_O = 10kHz			15			15			15			15		nV/√Hz
f_B = 10Hz to 10kHz			2.4			2.4			2.4			2.4		µVrms
f_B = 0.1Hz to 10Hz			4			4			4			4		µVp-p
Current: f_B = 0.1Hz to 10Hz			4.2			3			2.3			3		fA, p-p
f_O = 0.1Hz to 20kHz			0.22			0.16			0.12			0.16		fA/√Hz
IMPEDANCE														
Differential			10^{13} ‖ 1			10^{13} ‖ 1			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{15} ‖ 2			10^{15} ‖ 2			10^{15} ‖ 2			10^{15} ‖ 2		Ω ‖ pF
VOLTAGE RANGE(4)														
Common-Mode Input Range		±10	±12		±10	±12		±10	±12		±10	±12		V
Common-Mode Rejection	V_{IN} = ±10VDC	80	118		90	118		90	118		90	118		dB
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	94	128		110	128		110	128		110	128		dB
Unity Gain, Small Signal	(2)	0.5	1		0.5	1		0.5	1		0.5	1		MHz
Full Power Response	20Vp-p, R_L = 2kΩ		47			47			47			47		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	0.5	3		1	3		1	3		1	3		V/µs
Settling Time, 0.1%	Gain = –1, R_L = 2kΩ		5			5			5			5		µs
0.01%	10V Step		10			10			10			10		µs
Overload Recovery, 50% Overdrive(3)	Gain = –1		5			5			5			5		µs
Voltage Output	R_L = 2kΩ	±10	±13		±10	±13		±10	±13		±10	±13		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, Open Loop		100			100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000			1000		pF
Short Circuit Current		10	34	55	10	34	55	10	34	55	10	34	55	mA
Rated Voltage			±15			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		0.9	1.5		0.9	1.5		0.9	1.5		0.9	1.5	mA
Specification	Ambient Temp.	0		+70	0		+70	0		+70	–55		+125	°C
Operating	Ambient Temp.	–55		+125	–55		+125	–55		+125	–55		+125	°C
Storage	Ambient Temp.	–65		+150	–65		+150	–65		+150	–65		+150	°C
θ Junction-Ambient			200			200			200			200		°C/W

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. Bias current doubles approximately every 11°C. (2) Sample tested. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can withstand overload currents of 0.3mA indefinitely without damage.

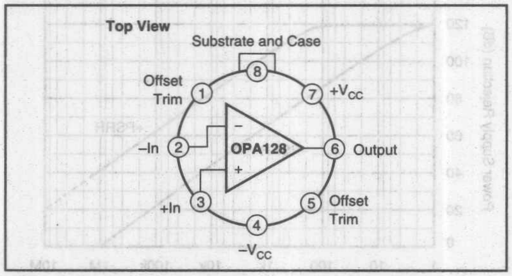
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and T_A = T_{MIN} and T_{MAX} unless otherwise noted.

		OPA128JM			OPA128KM			OPA128LM			OPA128SM			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TEMPERATURE RANGE														
Specification Range	Ambient Temp.	0		+70	0		+70	0		+70	–55		+125	°C
INPUT														
BIAS CURRENT[1]														
Input Bias Current	V_{CM} = 0VDC		±2.5	±8		±1.3	±4		±0.7	±2		±43	±170	pA
OFFSET CURRENT[1]														
Input Offset Current	V_{CM} = 0VDC		1.1			0.6			0.6			18		pA
OFFSET VOLTAGE[1]														
Input Offset Voltage	V_{CM} = 0VDC			±2.2mV			±1mV			±750			±1.5mV	µV
Average Drift				±20			±10			±5			±10	µV/°C
Supply Rejection		74	114		80	114		80	114		80	106		dB
			±2	±200		±2	±100		±2	±100		±5	±100	µV/V
VOLTAGE RANGE[2]														
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		±10	±11		V
Commmon-Mode Rejection	V_{IN} = ±10VDC	74	112		80	112		80	112		74	104		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	90	125		104	125		104	125		90	122		dB
RATED OUTPUT														
Voltage Output	R_L = 2k	±10			±10			±10			±10			V
Current Output	V_O = ±10VDC	±5			±5			±5			±5			mA
Short Circuit Current	V_O = 0VDC	10	22		10	22		10	22		10	18		mA
POWER SUPPLY														
Current, Quiescent	I = 0mADC		0.9	1.8		0.9	1.8		0.9	1.8		0.9	2	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (2) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can withstand overload currents of 0.3mA indefinitely without damage.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration[2]	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{CA} = 150°C/W or θ_{JA} = 200°C/W. (2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

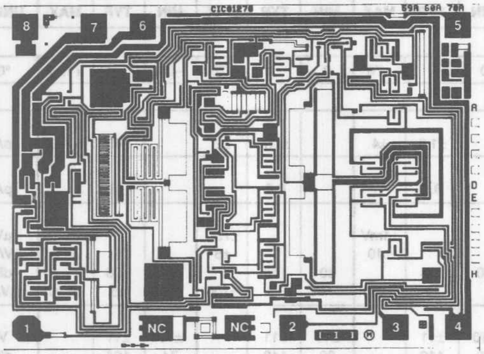
MODEL	PACKAGE	TEMPERATURE RANGE	BIAS CURRENT, max (fA)
OPA128JM	TO-99	0°C to +70°C	±300
OPA128KM	TO-99	0°C to +70°C	±150
OPA128LM	TO-99	0°C to +70°C	±75
OPA128SM	TO-99	–55°C to +125°C	±150

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA128JM	TO-99	001
OPA128KM	TO-99	001
OPA128LM	TO-99	001
OPA128SM	TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

DICE INFORMATION



OPA128 DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	−In
3	+In
4	$-V_{CC}$
5	Offset Trim
6	Output
7	$+V_{CC}$
8	Substrate
NC	No Connection

Substrate Bias: Isolated, normally connected to common.

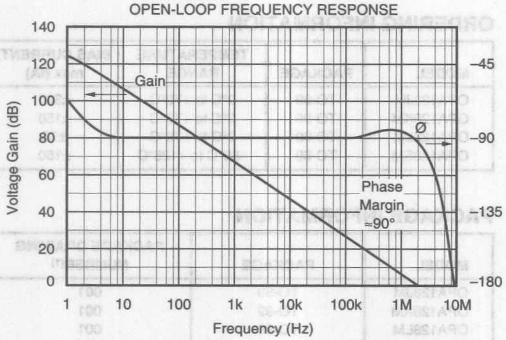
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	96 x 71 ±5	2.44 x 1.80 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None

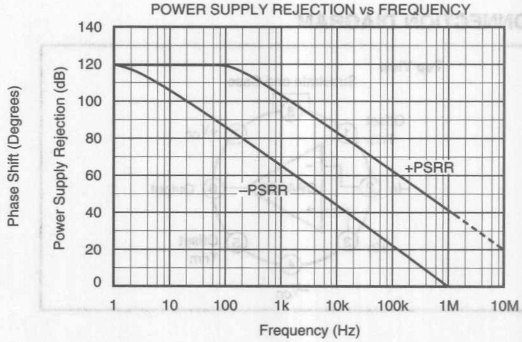
TYPICAL PERFORMANCE CURVES

T_A = +25°C, ±15VDC, unless otherwise noted.

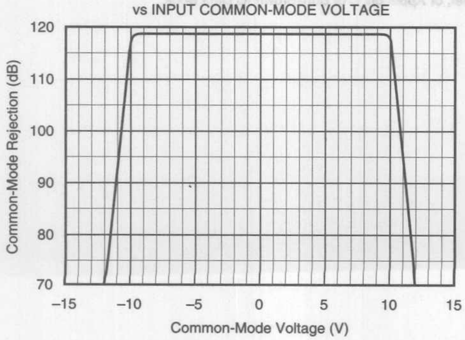
OPEN-LOOP FREQUENCY RESPONSE



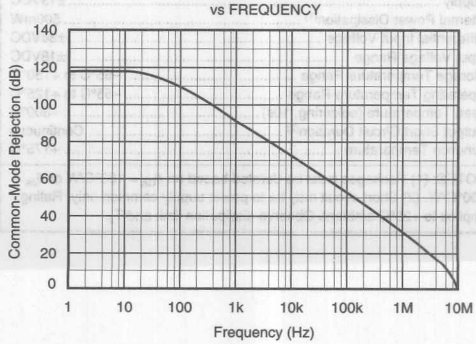
POWER SUPPLY REJECTION vs FREQUENCY



COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE

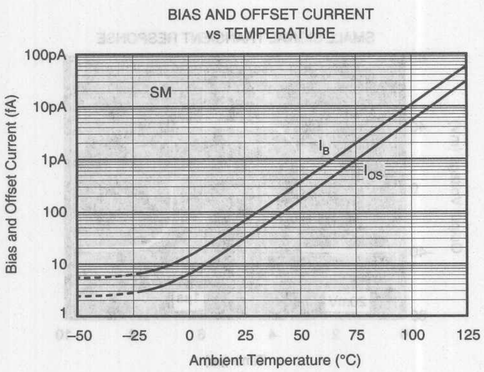


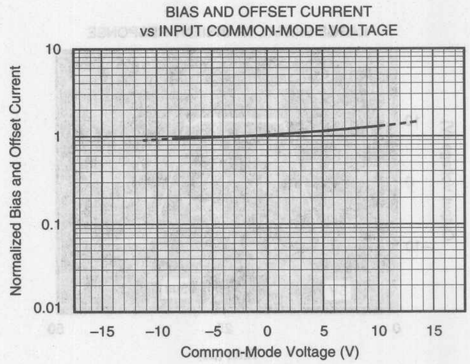
COMMON-MODE REJECTION
vs FREQUENCY

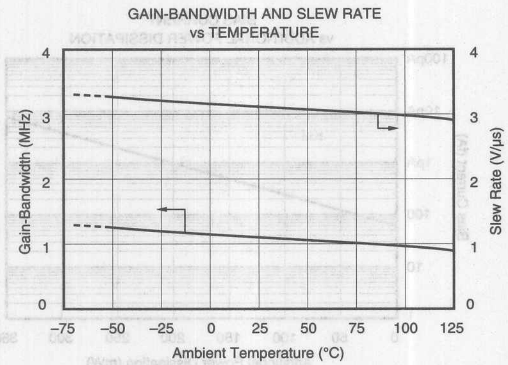


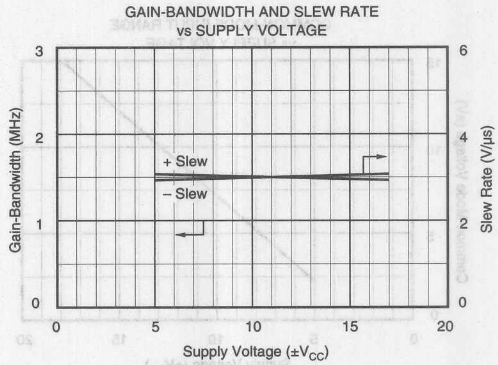
TYPICAL PERFORMANCE CURVES (CONT)

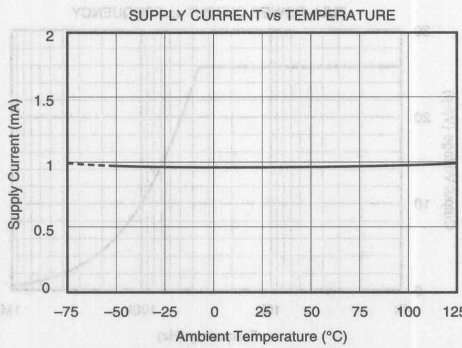
At T_A = +25°C, +15VDC unless otherwise noted.

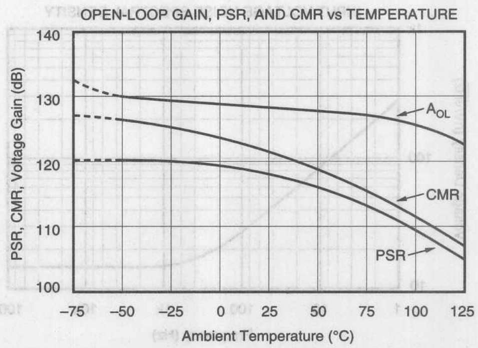












OPA128

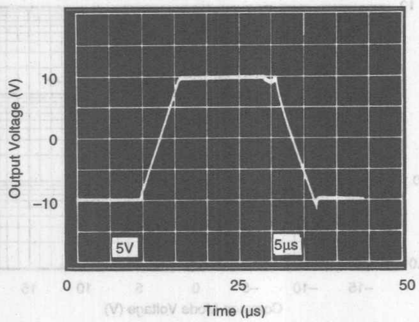
2

OPERATIONAL AMPLIFIERS

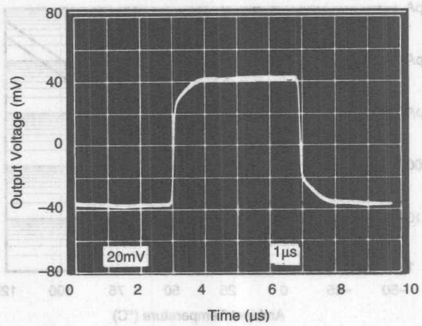
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, +15VDC unless otherwise noted.

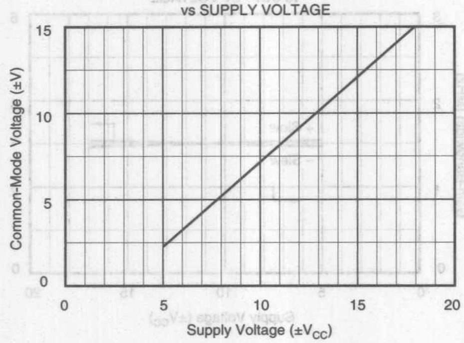
LARGE SIGNAL TRANSIENT RESPONSE



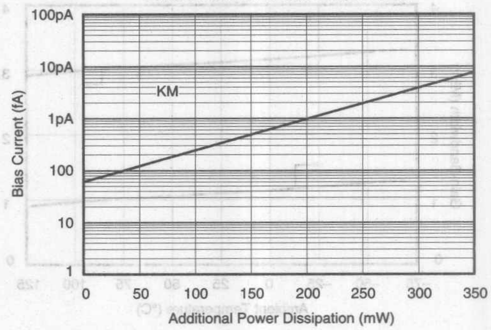
SMALL SIGNAL TRANSIENT RESPONSE



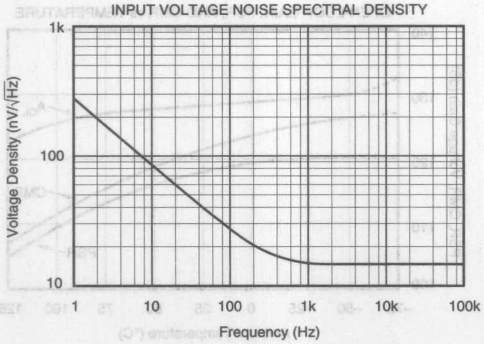
COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE



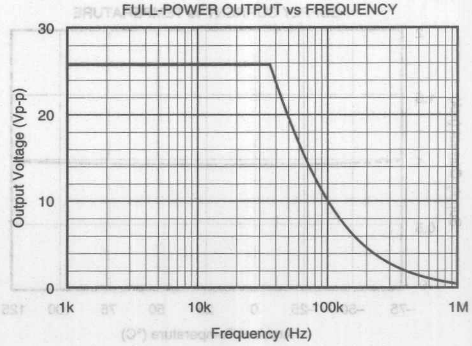
BIAS CURRENT vs ADDITIONAL POWER DISSIPATION



INPUT VOLTAGE NOISE SPECTRAL DENSITY



FULL-POWER OUTPUT vs FREQUENCY



BURR - BROWN®

APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA128 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3μV/°C for each 100μV of adjusted effort. Note that the trim (Figure 1) is similar to operational amplifiers such as HA-5180 and AD515. The OPA128 can replace many other amplifiers by leaving the external null circuit unconnected.

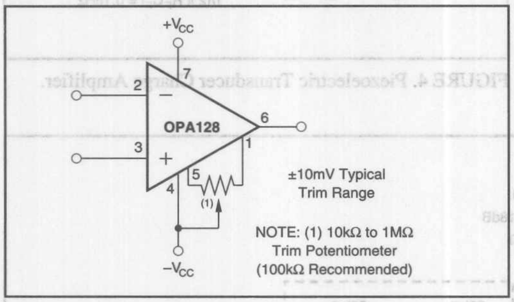


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers' inputs must be protected against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA128. Of course, the differential and common-mode voltage limits should be observed.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. Leakage currents across printed circuit boards can easily exceed the bias current of the OPA128. To avoid leakage problems, it is recommended that the signal input lead of the OPA128 be wired to a Teflon standoff. If the input is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

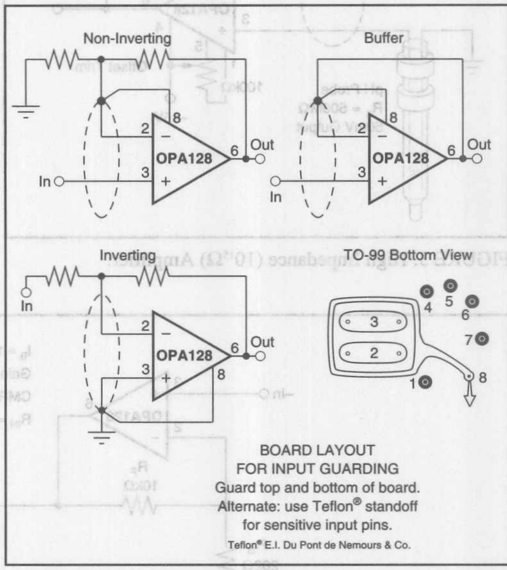


FIGURE 2. Connection of Input Guard.

Triboelectric charge (static electricity generated by friction) can be a troublesome noise source from cables connected to the input of an electrometer amplifier. Special low-noise cable will minimize this effect but the optimum solution is to mount the signal source directly at the electrometer input with short, rigid, wiring to preclude microphonic noise generation.

TESTING

Accurately testing the OPA128 is extremely difficult due to its high level of performance. Ordinary test equipment may not be able to resolve the amplifier's extremely low bias current.

Inaccurate bias current measurements can be due to:

1. Test socket leakage
2. Unclean package
3. Humidity or dew point condensation
4. Circuit contamination from fingerprints or anti-static treatment chemicals
5. Test ambient temperature
6. Load power dissipation

BIFET® National Semiconductor Corp.

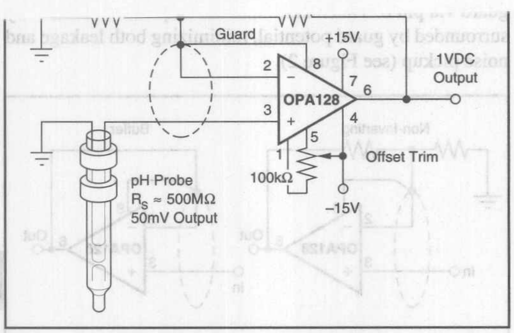


FIGURE 3. High Impedance ($10^{15}\Omega$) Amplifier.

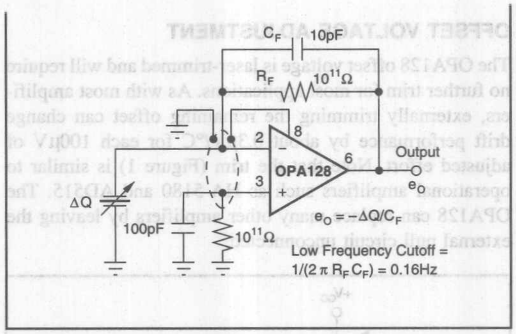


FIGURE 4. Piezoelectric Transducer Charge Amplifier.

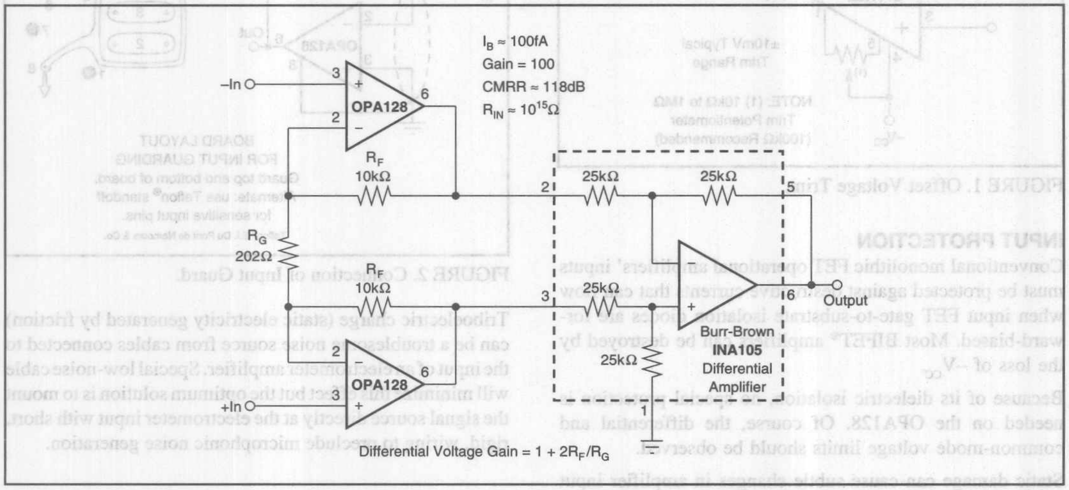


FIGURE 5. FET Input Instrumentation Amplifier for Biomedical Applications.

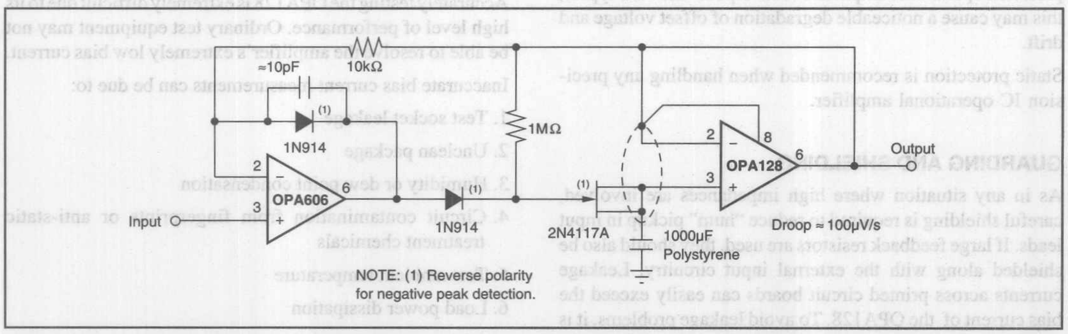


FIGURE 6. Low-Droop Positive Peak Detector.

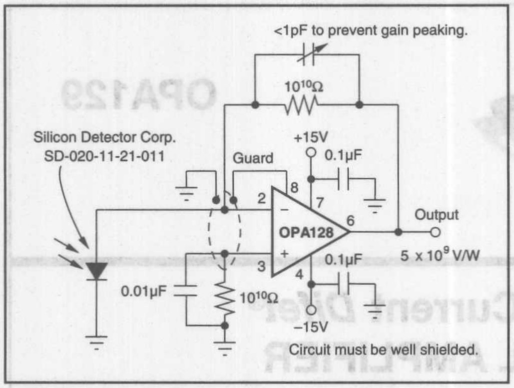


FIGURE 7. Sensitive Photodiode Amplifier.

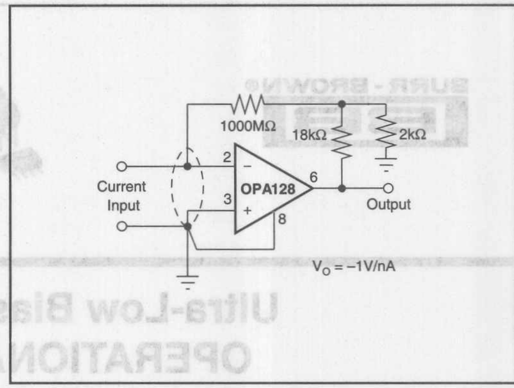


FIGURE 8. Current-to-Voltage Converter.

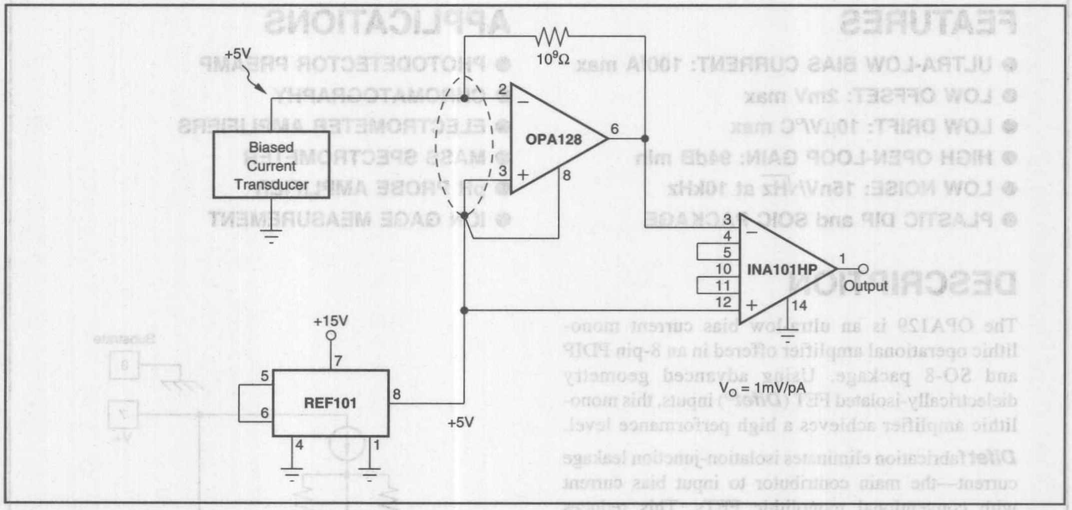
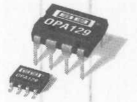


FIGURE 9. Biased Current-to-Voltage Converter.

BURR - BROWN®



OPA129

Ultra-Low Bias Current *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- ULTRA-LOW BIAS CURRENT: 100fA max
- LOW OFFSET: 2mV max
- LOW DRIFT: 10µV/°C max
- HIGH OPEN-LOOP GAIN: 94dB min
- LOW NOISE: 15nV/√Hz at 10kHz
- PLASTIC DIP and SOIC PACKAGE

APPLICATIONS

- PHOTODETECTOR PREAMP
- CHROMATOGRAPHY
- ELECTROMETER AMPLIFIERS
- MASS SPECTROMETER
- pH PROBE AMPLIFIER
- ION GAGE MEASUREMENT

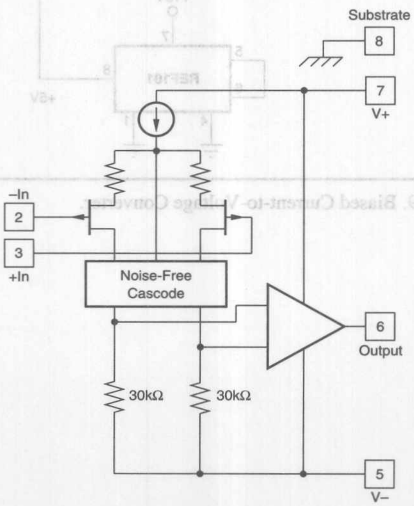
DESCRIPTION

The OPA129 is an ultra-low bias current monolithic operational amplifier offered in an 8-pin PDIP and SO-8 package. Using advanced geometry dielectrically-isolated FET (***Difet***®) inputs, this monolithic amplifier achieves a high performance level.

Difet fabrication eliminates isolation-junction leakage current—the main contributor to input bias current with conventional monolithic FETs. This reduces input bias current by a factor of 10 to 100. Very low input bias current can be achieved without resorting to small-geometry FETs or CMOS designs which can suffer from much larger offset voltage, voltage noise, drift, and poor power supply rejection.

The OPA129's special pinout eliminates leakage current that occurs with other op amps. Pins 1 and 4 have no internal connection, allowing circuit board guard traces—even with the surface-mount package version.

OPA129 is available in 8-pin DIP and SO-8 packages, specified for operation from –40°C to +85°C.



Simplified Circuit

Difet® Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1195A

SPECIFICATIONS

ELECTRICAL

At $V_S = \pm15V$ and $T_A = +25°C$ unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITION	OPA129PB, UB MIN	OPA129PB, UB TYP	OPA129PB, UB MAX	OPA129P, U MIN	OPA129P, U TYP	OPA129P, U MAX	UNITS
INPUT BIAS CURRENT[1]	$V_{CM} = 0V$		±30	±100		*	±250	fA
vs Temperature			Doubles every 10°C			*		
INPUT OFFSET CURRENT	$V_{CM} = 0V$		±30			*		fA
OFFSET VOLTAGE								
Input Offset Voltage	$V_{CM} = 0V$		±0.5	±2		±1	±5	mV
vs Temperature			±3	±10		±5		µV/°C
Supply Rejection	$V_S = \pm5V$ to $\pm18V$		±3	±100		*	*	µV/V
NOISE								
Voltage	f = 10Hz		85			*		nV/√Hz
	f = 100Hz		28			*		nV/√Hz
	f = 1kHz		17			*		nV/√Hz
	f = 10kHz		15			*		nV/√Hz
	f_B = 0.1Hz to 10Hz		4			*		µVp-p
Current	f = 10kHz		0.1			*		fA/√Hz
INPUT IMPEDANCE								
Differential			10^{13} ‖ 1			*		Ω ‖ pF
Common-Mode			10^{15} ‖ 2			*		Ω ‖ pF
VOLTAGE RANGE								
Common-Mode Input Range		±10	±12		*	*		V
Common-Mode Rejection	$V_{IN} = \pm10V$	80	118		*	*		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	94	120		*	*		dB
FREQUENCY RESPONSE								
Unity Gain, Small Signal			1			*		MHz
Full Power Response	20Vp-p, $R_L = 2k\Omega$		47			*		kHz
Slew Rate	$V_O = \pm10V$, $R_L = 2k\Omega$	1	2.5		*	*		V/µs
Settling Time:	G = –1, $R_L = 2k\Omega$, 10V Step							
0.1%			5			*		µs
0.01%			10			*		µs
Overload Recovery, 50% Overdrive[2]	G = –1		5			*		µs
RATED OUTPUT								
Voltage Output	$R_L = 2k\Omega$	±12	±13		*	*		V
Current Output	$V_O = \pm12V$	±6	±10		*	*		mA
Load Capacitance Stability	Gain = +1		1000			*		pF
Short-Circuit Current			±35	±55		*	*	mA
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range, Derated Performance		±5		±18	*		*	V
Current, Quiescent	$I_O = 0mA$		1.2	1.8		*	*	mA
TEMPERATURE								
Specification	Ambient Temperature	–40		+85	*		*	°C
Operating	Ambient Temperature	–40		+125	*		*	°C
Storage		–40		+125	*		*	°C
Thermal Resistance	θ_{JA}, Junction-to-Ambient							
PDIP—"P"			90			*		°C/W
SOIC—"U"			100			*		°C/W

NOTES: (1) High-speed automated test. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

Power Supply Voltage	±18V
Differential Input Voltage	V– to V+
Input Voltage Range	V– to V+
Storage Temperature Range	–40°C to +125°C
Operating Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 10s; SOIC 3s)	+300°C
Output Short Circuit Duration[1]	Continuous
Junction Temperature (T_J)	+150°C

NOTE: (1) Short circuit may be to power supply common at +25°C ambient.

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA129P	8-pin Plastic DIP	006
OPA129PB	8-pin Plastic DIP	006
OPA129U	8-pin SOIC	182
OPA129UB	8-pin SOIC	182

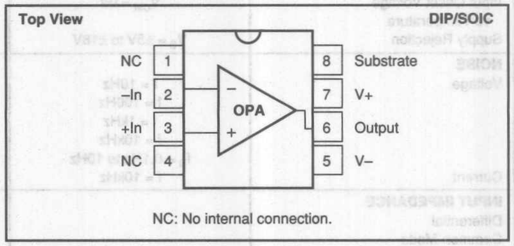
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

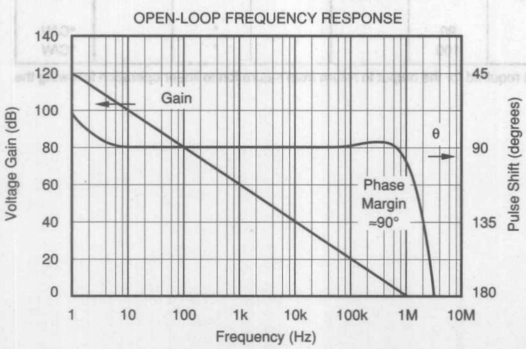
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

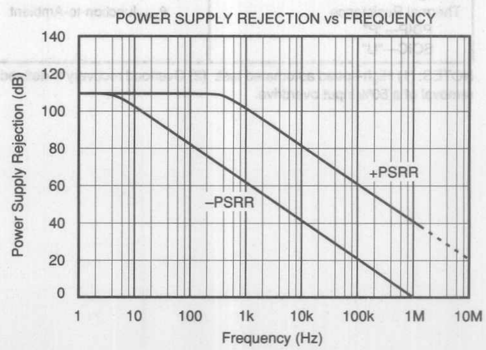
CONNECTION DIAGRAM



TYPICAL PERFORMANCE CURVES

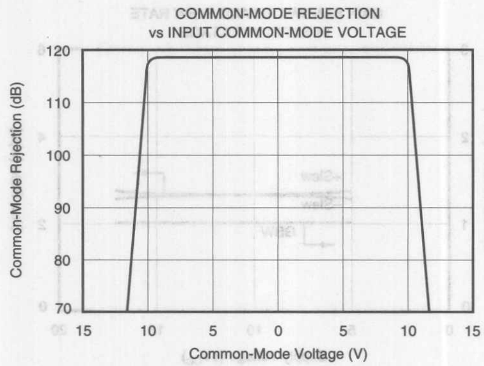
T_A = +25°C, +15VDC, unless otherwise noted.

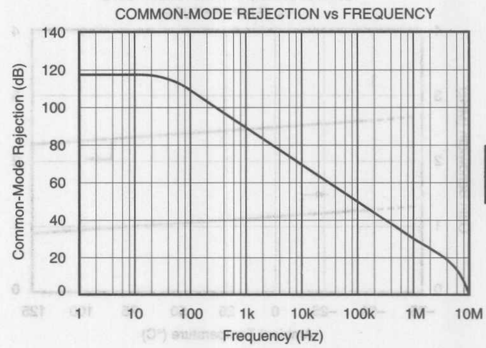


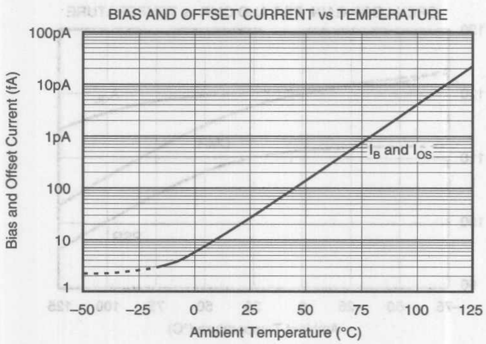


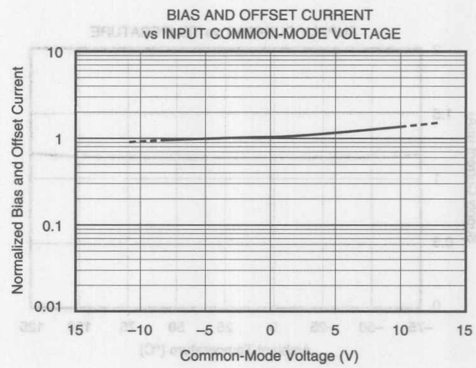
TYPICAL PERFORMANCE CURVES (CONT)

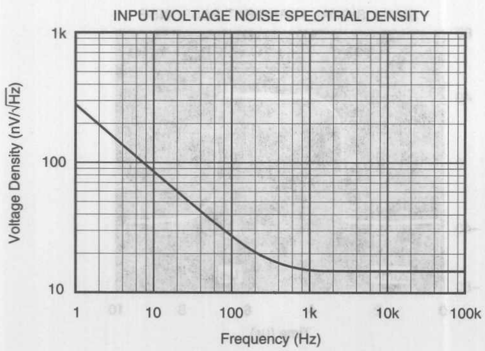
T_A = +25°C, +15VDC, unless otherwise noted.

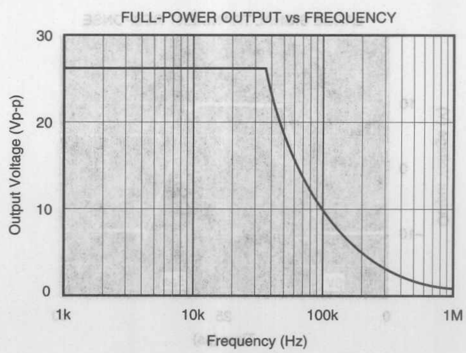










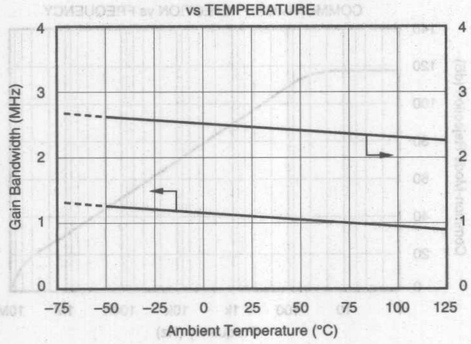


OPERATIONAL AMPLIFIERS 2 OPA129

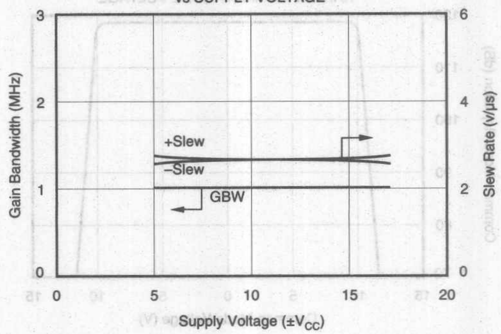
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, +15VDC, unless otherwise noted.

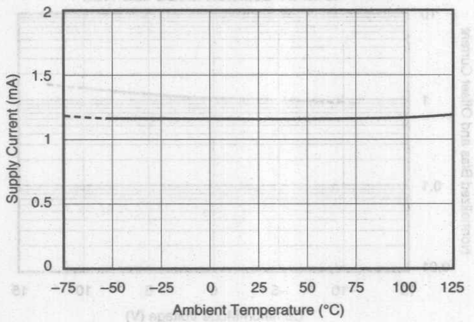
GAIN BANDWIDTH AND SLEW RATE vs TEMPERATURE



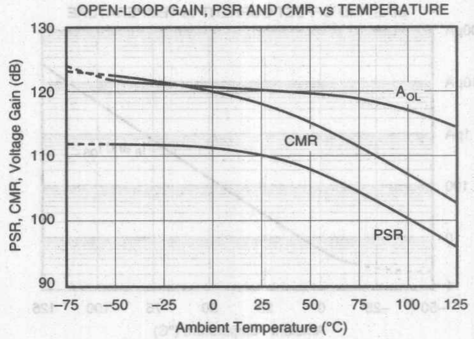
GAIN BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



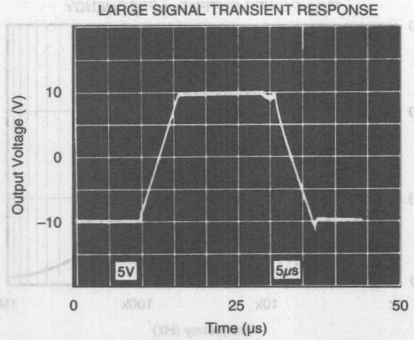
SUPPLY CURRENT vs TEMPERATURE



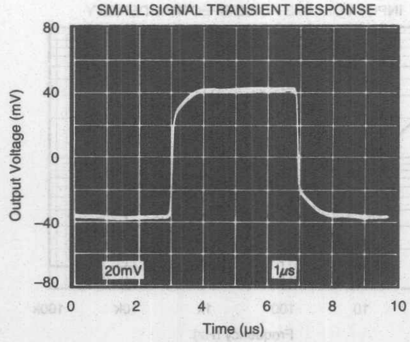
OPEN-LOOP GAIN, PSR AND CMR vs TEMPERATURE



LARGE SIGNAL TRANSIENT RESPONSE



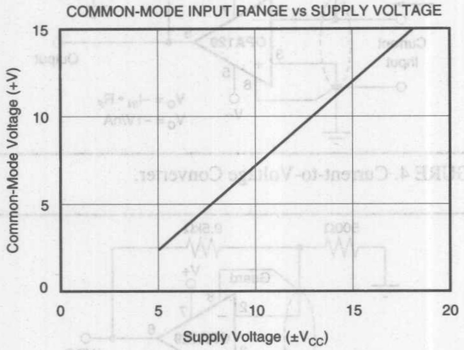
SMALL SIGNAL TRANSIENT RESPONSE

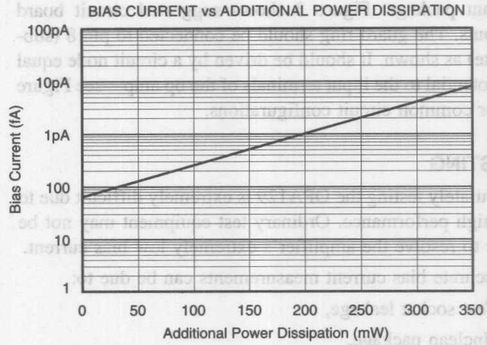


BURR-BROWN®

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, +15VDC, unless otherwise noted.





APPLICATIONS INFORMATION

NON-STANDARD PINOUT

The OPA129 uses a non-standard pinout to achieve lowest possible input bias current. The negative power supply is connected to pin 5—see Figure 1. This is done to reduce the leakage current from the V- supply (pin 4 on conventional op amps) to the op amp input terminals. With this new pinout, sensitive inputs are separated from both power supply pins.

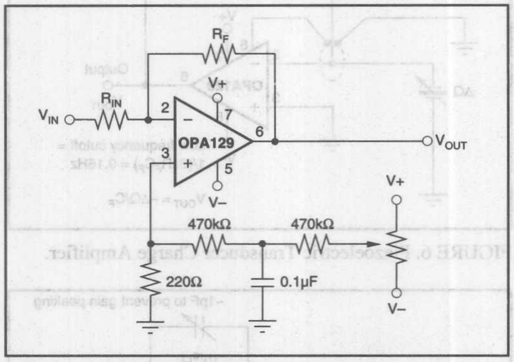


FIGURE 1. Offset Adjust Circuit.

OFFSET VOLTAGE TRIM

The OPA129 has no conventional offset trim connections. Pin 1, next to the critical inverting input, has no internal connection. This eliminates a source of leakage current and allows guarding of the input terminals. Pin 1 and pin 4, next to the two input pins, have no internal connection. This allows an optimized circuit board layout with guarding—see "circuit board layout."

Due to its laser-trimmed input stage, most applications do not require external offset voltage trimming. If trimming is required, the circuit shown in Figure 1 can be used. Power supply voltages are divided down, filtered and applied to the non-inverting input. The circuit shown is sensitive to variation in the supply voltages. Regulation can be added, if needed.

GUARDING AND SHIELDING

Ultra-low input bias current op amps require precautions to achieve best performance. Leakage current on the surface of circuit board can exceed the input bias current of the amplifier. For example, a circuit board resistance of $10^{12}\Omega$ from a power supply pin to an input pin produces a current of 15pA—more than one-hundred times the input bias current of the op amp.

To minimize surface leakage, a guard trace should completely surround the input terminals and other circuitry connecting to the inputs of the op amp. The DIP package should have a guard trace on both sides of the circuit board. The guard ring should be driven by a circuit node equal in potential to the op amp inputs—see Figure 2. The substrate, pin 8, should also be connected to the circuit board guard to assure that the amplifier is fully surrounded by the guard potential. This minimizes leakage current and noise pick-up.

Careful shielding is required to reduce noise pickup. Shielding near feedback components may also help reduce noise pick-up.

Triboelectric effects (friction-generated charge) can be a troublesome source of errors. Vibration of the circuit board, input connectors and input cables can cause noise and drift. Make the assembly as rigid as possible. Attach cables to avoid motion and vibration. Special low noise or low leakage cables may help reduce noise and leakage current. Keep all input connections as short possible. Surface-mount components may reduce circuit board size and allow a more rigid assembly.

The OPA129 uses a new pinout for ultra low input bias current. Pin 1 and pin 4 have no internal connection. This allows ample circuit board space for a guard ring surrounding the op amp input pins—even with the tiny SO-8 surface-mount package. Figure 3 shows suggested circuit board layouts. The guard ring should be connected to pin 8 (substrate) as shown. It should be driven by a circuit node equal in potential to the input terminals of the op amp—see Figure 2 for common circuit configurations.

TESTING

Accurately testing the OPA129 is extremely difficult due to its high performance. Ordinary test equipment may not be able to resolve the amplifier's extremely low bias current.

Inaccurate bias current measurements can be due to:

1. Test socket leakage,
2. Unclean package,
3. Humidity or dew point condensations,
4. Circuit contamination from fingerprints or anti-static treatment chemicals,
5. Test ambient temperature,
6. Load power dissipation,
7. Mechanical stress,
8. Electrostatic and electromagnetic interference.

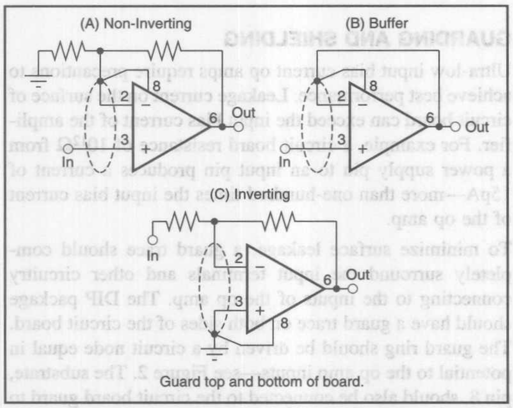


FIGURE 2. Connection of Input Guard.

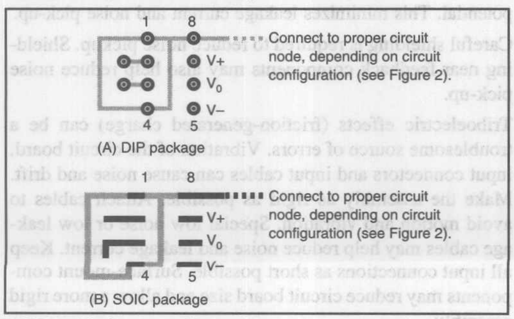


FIGURE 3. Suggested Board Layout for Input Guard.

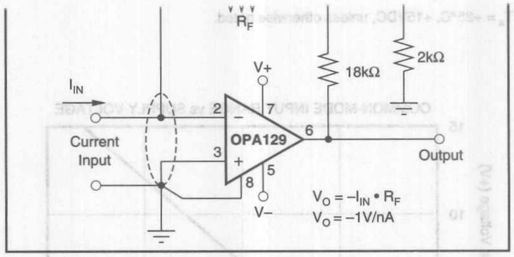


FIGURE 4. Current-to-Voltage Converter.

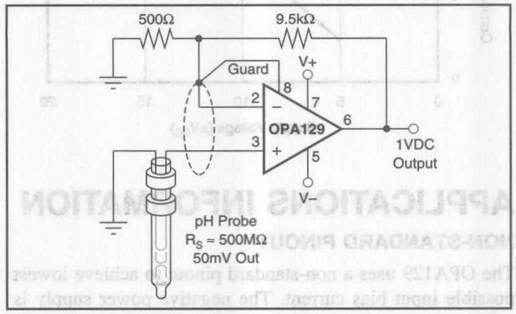


FIGURE 5. High Impedance ($10^{15}\Omega$) Amplifier.

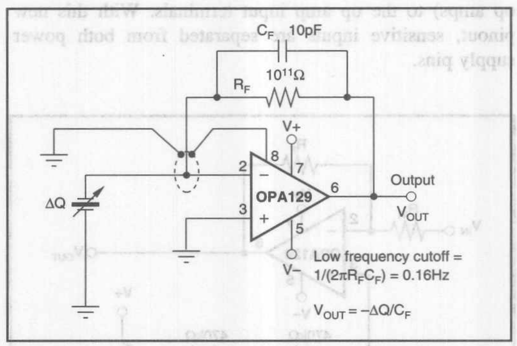


FIGURE 6. Piezoelectric Transducer Charge Amplifier.

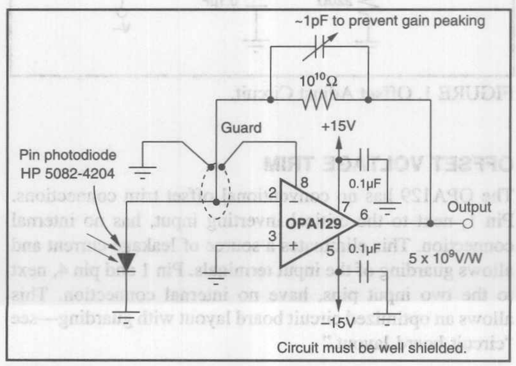
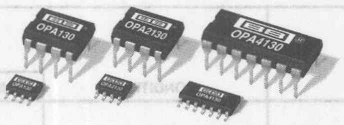


FIGURE 7. Sensitive Photodiode Amplifier.

BURR - BROWN®



OPA130
OPA2130
OPA4130

Low Power, Precision FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

- LOW QUIESCENT CURRENT: 530μA/amp
- LOW OFFSET VOLTAGE: 1mV max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH CMRR: 90dB min
- FET INPUT: I_B = 20pA max
- EXCELLENT BANDWIDTH: 1MHz
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- SINGLE, DUAL, AND QUAD VERSIONS

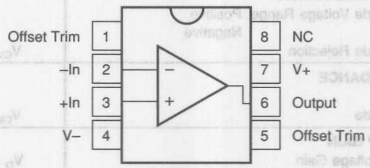
DESCRIPTION

The OPA130 series of FET-input op amps combine precision dc performance with low quiescent current. Single, dual, and quad versions have identical specifications for maximum design flexibility. They are ideal for general-purpose, portable, and battery operated applications, especially with high source impedance.

OPA130 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA130 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

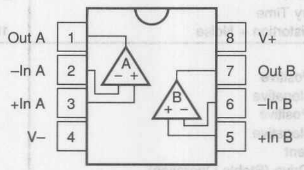
Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages. Quad is available in 14-pin DIP and SO-14 surface-mount packages. All are specified for –40°C to +85°C operation.

OPA130



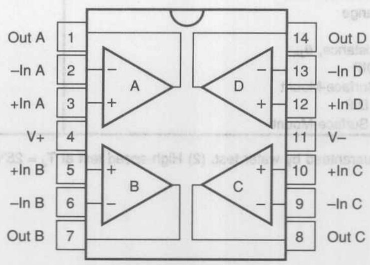
8-Pin DIP, SO-8

OPA2130



8-Pin DIP, SO-8

OPA4130



14-Pin DIP
SO-14

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25°C$, $V_S = \pm 15V$, and $R_L = 10k\Omega$ unless otherwise noted.

PARAMETER	CONDITION	OPA130PA, UA OPA2130PA, UA OPA4130PA, UA			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Input Offset Voltage			±0.2	±1	mV
vs Temperature[1]	Operating Temperature Range		±2	±10	µV/°C
vs Power Supply	$V_S = \pm 2.25V$ to $\pm 18V$		2	20	µV/V
Channel Separation (dual and quad)			0.3		µV/V
INPUT BIAS CURRENT[2]					
Input Bias Current	$V_{CM} = 0V$		+5	±20	pA
vs Temperature			See Typical Curve		
Input Offset Current	$V_{CM} = 0V$		±2	±20	pA
NOISE					
Input Voltage Noise					
Noise Density, f = 10Hz			30		$nV/\sqrt{Hz}$
f = 100Hz			18		$nV/\sqrt{Hz}$
f = 1kHz			16		$nV/\sqrt{Hz}$
f = 10kHz			16		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz			4		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range, Positive		(V+)–2	(V+)–1.5		V
Negative		(V–)+2	(V–)+1.2		V
Common-Mode Rejection	$V_{CM} = -13V$ to $+13V$	90	105		dB
INPUT IMPEDANCE					
Differential			$10^{13} \parallel 1$		Ω ‖ pF
Common-Mode	$V_{CM} = -13V$ to $+13V$		$10^{13} \parallel 3$		Ω ‖ pF
OPEN-LOOP GAIN					
Open-loop Voltage Gain	$V_O = -13.8V$ to $+13V$	120	135		dB
	$R_L = 2k\Omega$, $V_O = -13V$ to $+12V$	120	135		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			1		MHz
Slew Rate			2		V/µs
Settling Time: 0.1%	G = 1, 10V Step, $C_L = 100pF$		5.5		µs
0.01%	G = 1, 10V Step, $C_L = 100pF$		7		µs
Overload Recovery Time	G = 1, $V_{IN} = \pm 15V$		2		µs
Total Harmonic Distortion + Noise	1kHz, G = 1, $V_O = 3.5Vrms$		0.0003		%
OUTPUT					
Voltage Output, Positive		(V+)–2	(V+)–1.5		V
Negative		(V–)+1.2	(V–)+1		V
Positive	$R_L = 2k\Omega$	(V+)–3	(V+)–2.5		V
Negative	$R_L = 2k\Omega$	(V–)+2	(V–)+1.5		V
Short-Circuit Current			±18		mA
Capacitive Load Drive (Stable Operation)			10		nF
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±2.25		±18	V
Quiescent Current (per amplifier)	$I_O = 0$		±530	±650	µA
TEMPERATURE RANGE					
Operating Range		–40		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}					
8-Pin DIP			100		°C/W
SO-8 Surface-Mount			150		°C/W
14-Pin DIP			80		°C/W
SO-14 Surface-Mount			110		°C/W

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at $T_J = 25°C$.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	36V
Input Voltage	(V–) –0.7V to (V+) +0.7V
Output Short-Circuit[1]	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
Single		
OPA130PA	8-Pin Plastic DIP	006
OPA130UA	SO-8 Surface-Mount	182
Dual		
OPA2130PA	8-Pin Plastic DIP	006
OPA2130UA	SO-8 Surface-Mount	182
Quad		
OPA4130PA	14-Pin Plastic DIP	010
OPA4130UA	SO-14 Surface-Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
Single		
OPA130PA	8-Pin Plastic DIP	–40°C to +85°C
OPA130UA	SO-8 Surface-Mount	–40°C to +85°C
Dual		
OPA2130PA	8-Pin Plastic DIP	–40°C to +85°C
OPA2130UA	SO-8 Surface-Mount	–40°C to +85°C
Quad		
OPA4130PA	14-Pin Plastic DIP	–40°C to +85°C
OPA4130UA	SO-14 Surface-Mount	–40°C to +85°C

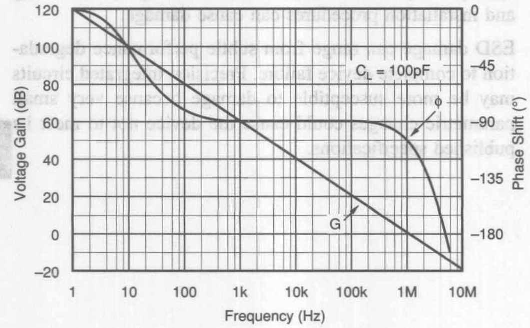
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

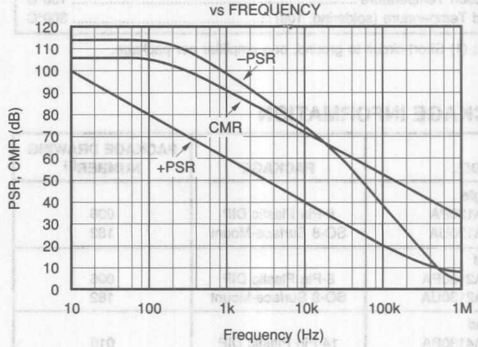
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

At $T_A = +25°C$, $V_S = \pm15V$, and $R_L = 10k\Omega$ unless otherwise noted.

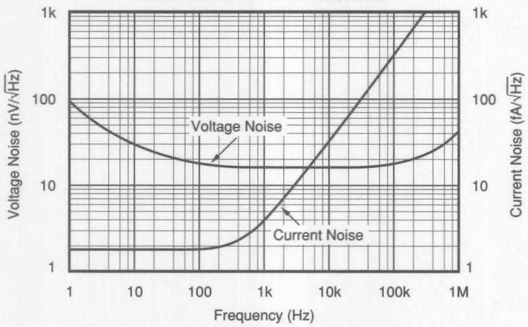
OPEN-LOOP GAIN/PHASE vs FREQUENCY



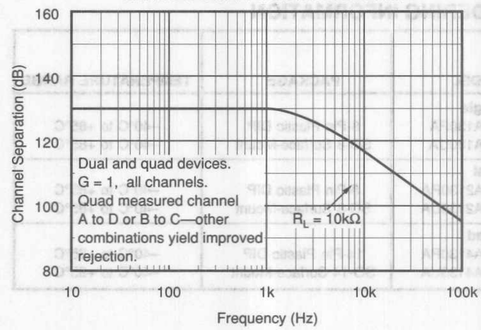
POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



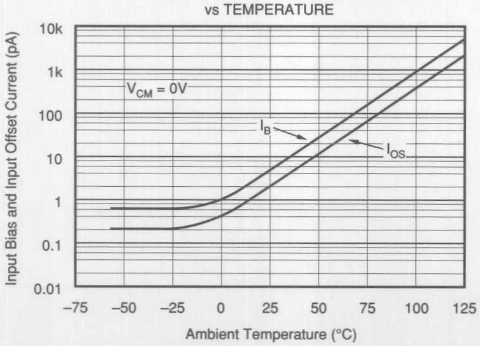
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



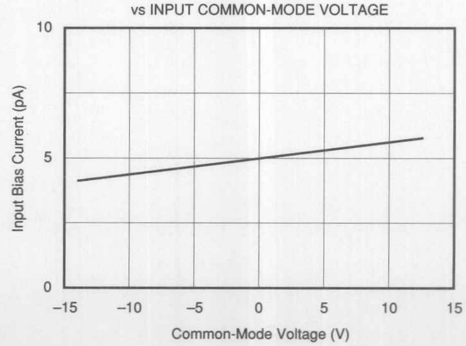
CHANNEL SEPARATION vs FREQUENCY



INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs INPUT COMMON-MODE VOLTAGE

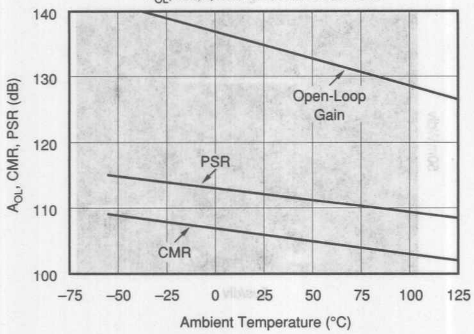


BURR-BROWN®

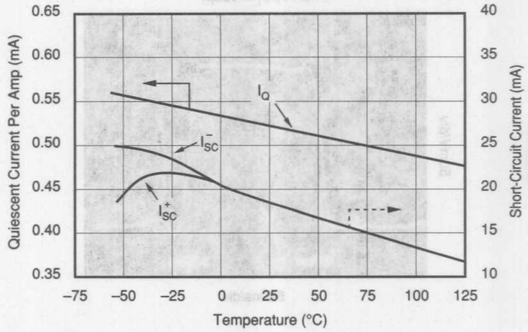
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = \pm15V$, and $R_L = 10k\Omega$ unless otherwise noted.

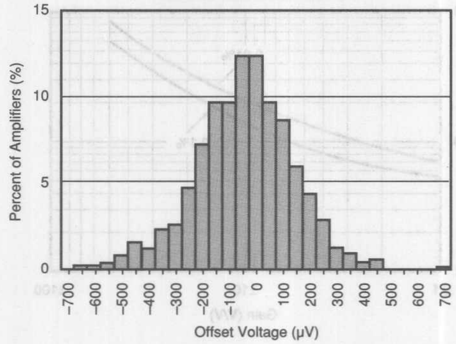
A_{OL}, CMR, PSR vs TEMPERATURE



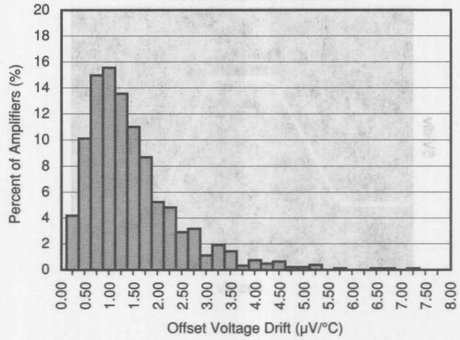
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



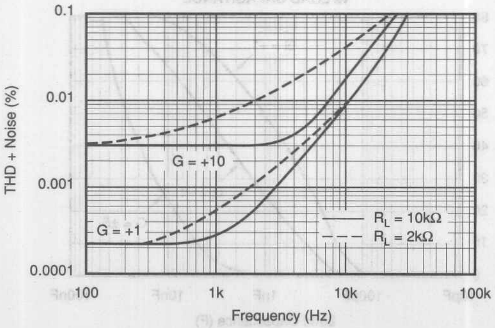
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



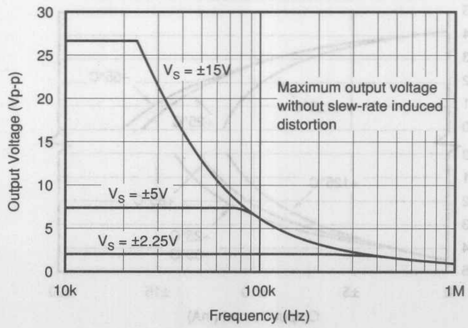
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



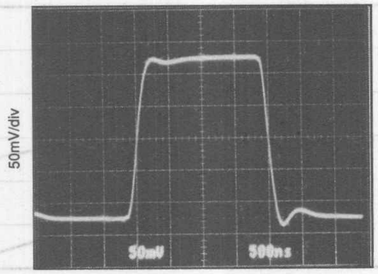
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



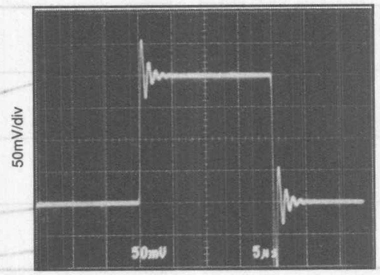
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = \pm15V$, and $R_L = 10k\Omega$ unless otherwise noted.

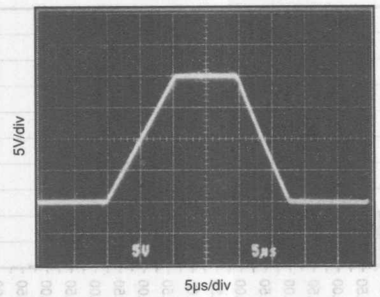
SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF



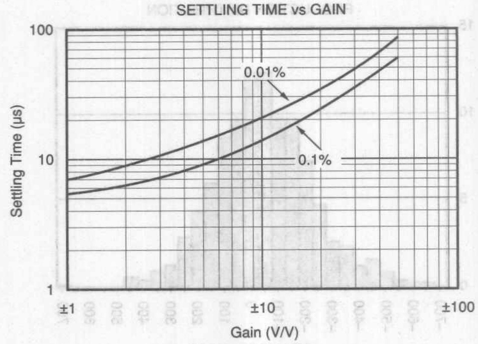
SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 1000pF



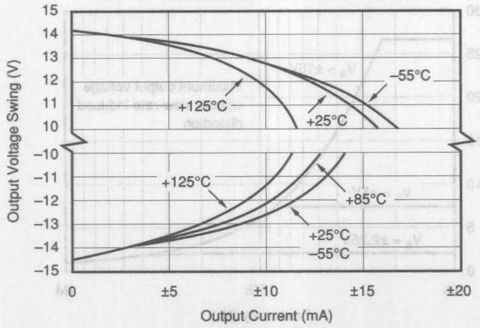
LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF



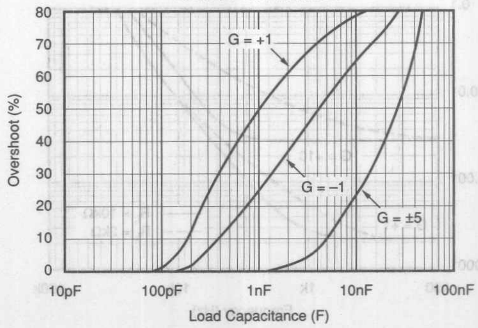
SETTLING TIME vs GAIN



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



APPLICATIONS INFORMATION

OPA130 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA130 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA130 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

OPERATING VOLTAGE

OPA130 series op amps operate with power supplies from ±2.25V to ±18V with excellent performance. Although specifications are production tested with ±15V supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

OFFSET VOLTAGE TRIM

Offset voltage of OPA130 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA130 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset that is not produced by the amplifier will change the offset voltage drift behavior of the op amp.

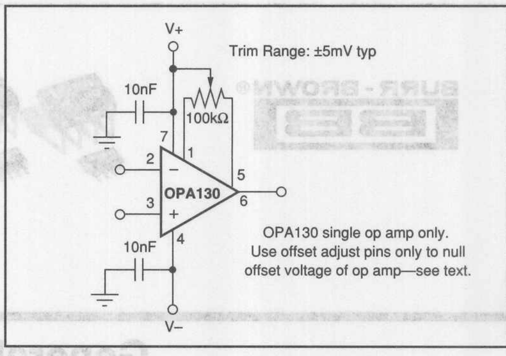


FIGURE 1. OPA130 Offset Voltage Trim Circuit.

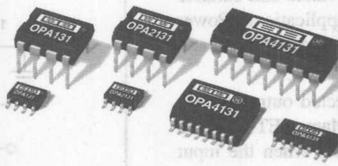
INPUT BIAS CURRENT

The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the typical performance curve "Input Bias Current vs Temperature."

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPA130. See the typical performance curve "Input Bias Current vs Common-Mode Voltage."

BURR - BROWN®

OPA131
OPA2131
OPA4131



General Purpose
FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

- FET INPUT: I_B = 50pA max
- LOW OFFSET VOLTAGE: 750µV max
- WIDE SUPPLY RANGE: ±4.5V to ±18V
- SLEW RATE: 10V/µs
- WIDE BANDWIDTH: 4MHz
- EXCELLENT CAPACITIVE LOAD DRIVE
- SINGLE, DUAL, QUAD VERSIONS

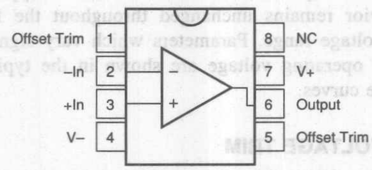
DESCRIPTION

The OPA131 series of FET-input op amps provides high performance at low cost. Single, dual and quad versions in industry-standard pinouts allow cost-effective design options.

The OPA131 series offers excellent general purpose performance, including low offset voltage, drift, and good dynamic characteristics.

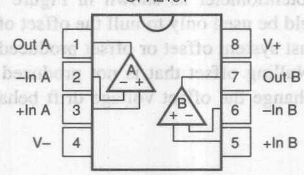
Single, dual and quad versions are available in DIP and SOIC packages. Performance grades include commercial and industrial temperature ranges.

OPA131



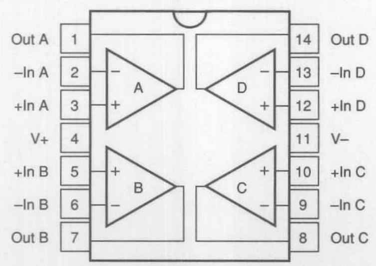
8-Pin DIP, SO-8

OPA2131



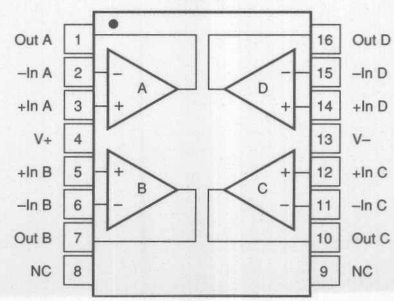
8-Pin DIP, SO-8

OPA4131



14-Pin DIP
SO-14

OPA4131



SOL-16

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

		OPA131PA, UA OPA2131PA, UA OPA4131PA, UA, NA			OPA131PJ, UJ OPA2131PJ, UJ OPA4131PJ, NJ			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE								
Input Offset Voltage			±0.2	±1		*	±1.5	mV
OPA131P, U models only			±0.2	0.75				mV
vs Temperature(1)	Operating Temperature Range		±2	±10		*	*	μV/°C
vs Power Supply	V_S = ±4.5V to ±18V		50	200		*	*	μV/V
OPA131P, U models only			50	100				μV/V
INPUT BIAS CURRENT(2)								
Input Bias Current	V_{CM} = 0V		+5	±50		*	*	pA
vs Temperature			See Typical Curve			*		
Input Offset Current	V_{CM} = 0V		±1	±50		*	*	pA
NOISE								
Input Voltage Noise								
Noise Density, f = 10Hz			21			*		nV/√Hz
f = 100Hz			16			*		nV/√Hz
f = 1kHz			15			*		nV/√Hz
f = 10kHz			15			*		nV/√Hz
Current Noise Density, f = 1kHz			3			*		fA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range		(V–)+3		(V+)–1	*		*	V
Common-Mode Rejection	V_{CM} = –12V to +14V	70	80		*	*		dB
OPA131P, U models only		80	86					dB
INPUT IMPEDANCE								
Differential			10^{10} ǁ 1			*		Ω ǁ pF
Common-Mode	V_{CM} = 0V		10^{12} ǁ 3			*		Ω ǁ pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = –12V to +12V	94	110		*	*		dB
OPA131P, U models only		100	110					dB
FREQUENCY RESPONSE								
Gain-Bandwidth Product			4			*		MHz
Slew Rate			10			*		V/μs
Settling Time 0.1%	G = –1, 10V Step, C_L = 100pF		1.5			*		μs
0.01%	G = –1, 10V Step, C_L = 100pF		2			*		μs
Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5Vrms		0.0008			*		%
OUTPUT								
Voltage Output, Positive		(V+)–3	(V+)–2.5		*	*		V
Negative		(V–)+3	(V–)+2.5		*	*		V
Short-Circuit Current			±25			*		mA
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Quiescent Current (per amplifier)	I_O = 0		±1.5	±1.75		*	±2	mA
TEMPERATURE RANGE								
Operating Range		–40		+85	0		+70	°C
Storage		–40		+125	*		*	°C
Thermal Resistance, θ_{JA}								
8-Pin DIP			100			*		°C/W
SO-8 Surface-Mount			150			*		°C/W
14-Pin DIP			80			*		°C/W
SO-14, SOL-16 Surface-Mount			110			*		°C/W

* Specifications same as OPA131PA, OPA131UA.

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at T_J = 25°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	36V
Input Voltage	(V–) –0.7V to (V+) +0.7V
Output Short-Circuit(1)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
Single		
OPA131PJ	8-Pin Plastic DIP	006
OPA131PA	8-Pin Plastic DIP	006
OPA131P	8-Pin Plastic DIP	006
OPA131UJ	SO-8 Surface-Mount	182
OPA131UA	SO-8 Surface-Mount	182
OPA131U	SO-8 Surface-Mount	182
Dual		
OPA2131PJ	8-Pin Plastic DIP	006
OPA2131PA	8-Pin Plastic DIP	006
OPA2131UJ	SO-8 Surface-Mount	182
OPA2131UA	SO-8 Surface-Mount	182
Quad		
OPA4131PJ	14-Pin Plastic DIP	010
OPA4131PA	14-Pin Plastic DIP	010
OPA4131UA	SOL-16 Surface-Mount	211
OPA4131NJ	SO-14 Surface-Mount	235
OPA4131NA	SO-14 Surface-Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
Single		
OPA131PJ	8-Pin Plastic DIP	0 to +70°C
OPA131PA	8-Pin Plastic DIP	–40°C to +85°C
OPA131P	8-Pin Plastic DIP	–40°C to +85°C
OPA131UJ	SO-8 Surface-Mount	0 to +70°C
OPA131UA	SO-8 Surface-Mount	–40°C to +85°C
OPA131U	SO-8 Surface-Mount	–40°C to +85°C
Dual		
OPA2131PJ	8-Pin Plastic DIP	0 to +70°C
OPA2131PA	8-Pin Plastic DIP	–40°C to +85°C
OPA2131UJ	SO-8 Surface-Mount	0 to +70°C
OPA2131UA	SO-8 Surface-Mount	–40°C to +85°C
Quad		
OPA4131PJ	14-Pin Plastic DIP	0 to +70°C
OPA4131PA	14-Pin Plastic DIP	–40°C to +85°C
OPA4131UA	SOL-16 Surface-Mount	–40°C to +85°C
OPA4131NJ	SO-14 Surface-Mount	0 to +70°C
OPA4131NA	SO-14 Surface-Mount	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

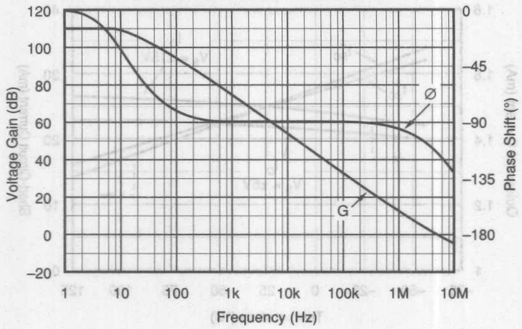
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

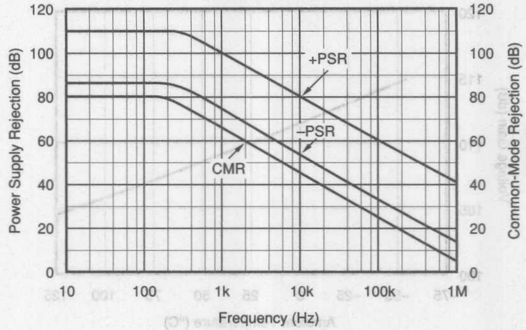
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, $V_S = ±15V$, and $R_L = 2kΩ$, unless otherwise noted.

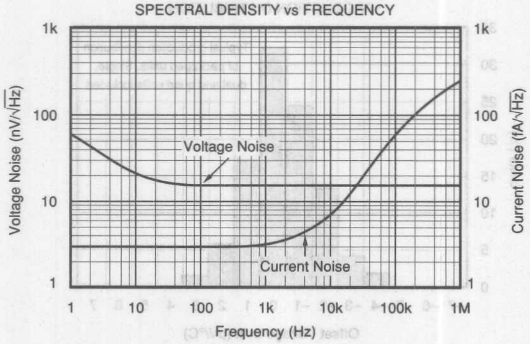
OPEN-LOOP GAIN/PHASE vs FREQUENCY



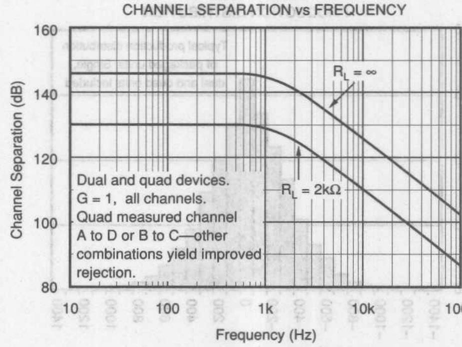
POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



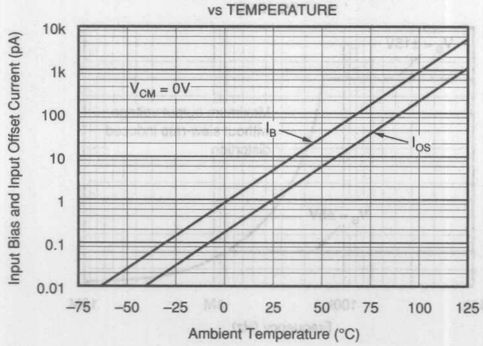
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



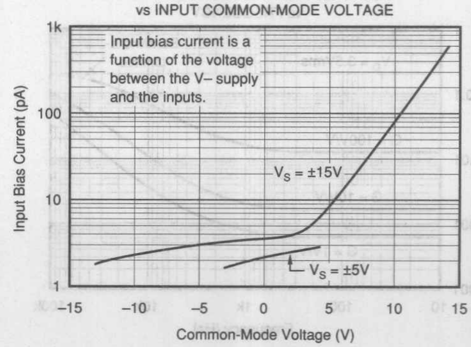
CHANNEL SEPARATION vs FREQUENCY



INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE

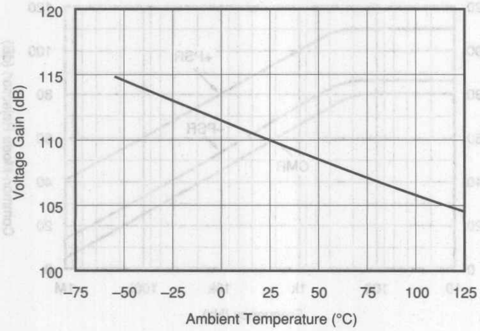


INPUT BIAS CURRENT vs INPUT COMMON-MODE VOLTAGE

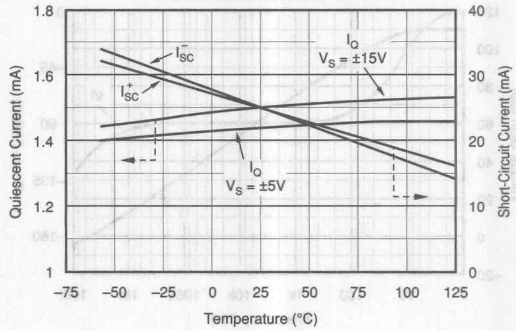


At $T_A = +25°C$, $V_S = ±15V$, and $R_L = 2kΩ$, unless otherwise noted.

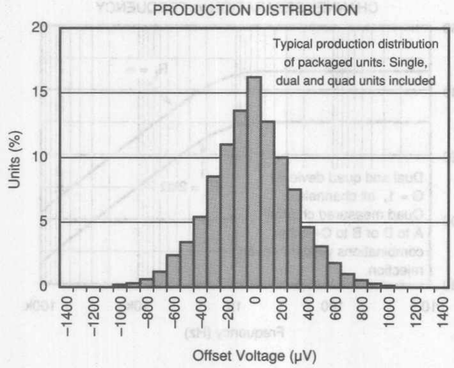
OPEN-LOOP GAIN vs TEMPERATURE



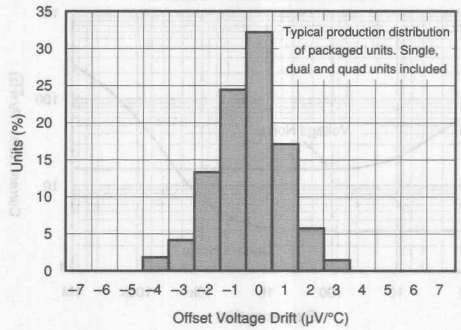
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



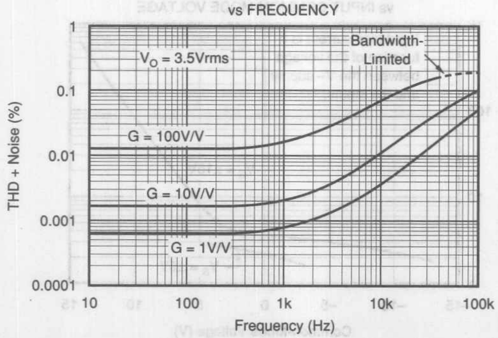
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



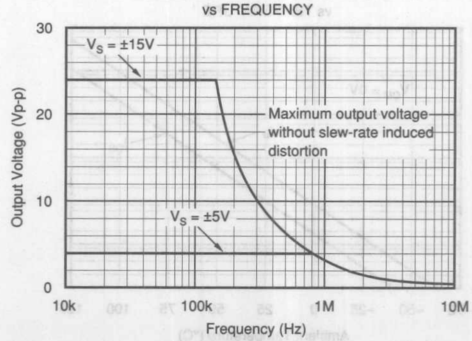
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



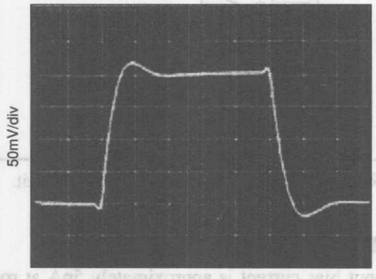
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



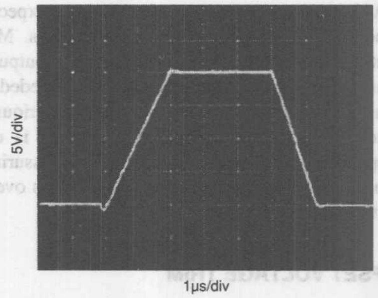
TYPICAL PERFORMANCE CURVES (CONT)

At T_{CASE} = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

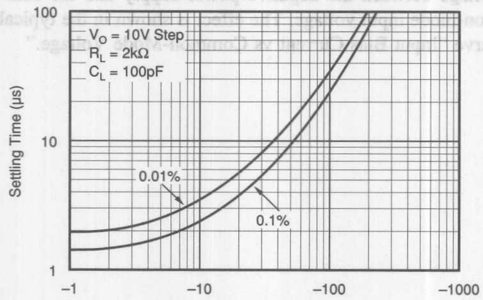
SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 300pF



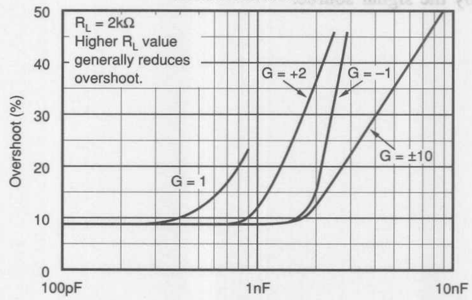
LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 300pF



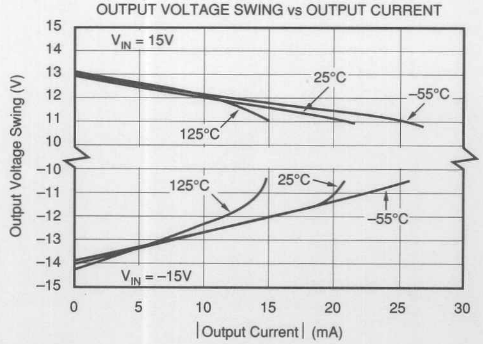
SETTLING TIME vs CLOSED-LOOP GAIN



SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



APPLICATIONS INFORMATION

OPA131 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA131 series op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

OFFSET VOLTAGE TRIM

The OPA131 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not system offset or offset produced by the signal source.

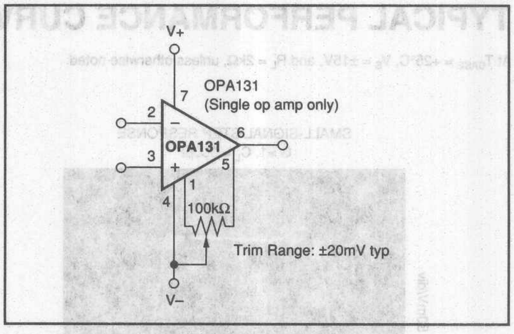


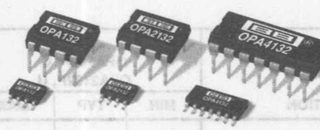
FIGURE 1. OPA131 Offset Voltage Trim Circuit.

INPUT BIAS CURRENT

The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the typical performance curve "Input Bias Current vs Temperature."

Input bias current also varies with common-mode voltage and power supply voltage. This variation is dependent on the voltage between the negative power supply and the common-mode input voltage. The effect is shown in the typical curve "Input Bias Current vs Common-Mode Voltage."

BURR - BROWN®



OPA132
OPA2132
OPA4132

High Speed
FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

- FET INPUT: I_B = 50pA max
- WIDE BANDWIDTH: 8MHz
- HIGH SLEW RATE: 20V/µs
- LOW NOISE: 8nV/√Hz (1kHz)
- LOW DISTORTION: 0.00008%
- HIGH OPEN-LOOP GAIN: 130dB (600Ω load)
- WIDE SUPPLY RANGE: ±2.5 to ±18V
- LOW OFFSET VOLTAGE: 500µV max
- SINGLE, DUAL, AND QUAD VERSIONS

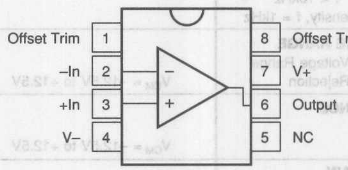
DESCRIPTION

The OPA132 series of FET-input op amps provides high-speed and excellent dc performance. The combination of high slew rate and wide bandwidth provide fast settling time. Single, dual, and quad versions have identical specifications for maximum design flexibility. High performance grades are available in the single and dual versions. All are ideal for general-purpose, audio, data acquisition and communications applications, especially where high source impedance is encountered.

OPA132 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA132 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

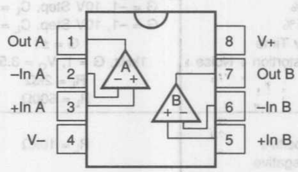
Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages. Quad is available in 14-pin DIP and SO-14 surface-mount packages. All are specified for –40°C to +85°C operation.

OPA132



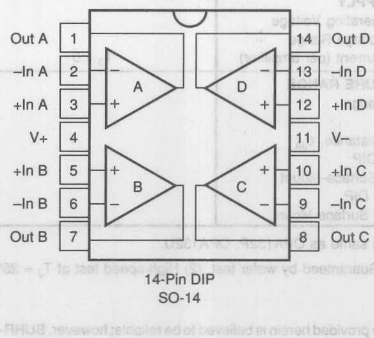
8-Pin DIP, SO-8

OPA2132



8-Pin DIP, SO-8

OPA4132



14-Pin DIP
SO-14

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

PARAMETER	CONDITION	OPA132P, U / OPA2132P, U MIN	TYP	MAX	OPA132PA, UA / OPA2132PA, UA / OPA4132PA, UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE								
Input Offset Voltage			±0.25	±0.5		±0.5	±2	mV
vs Temperature(1)	Operating Temperature Range		±2	±10		*	*	μV/°C
vs Power Supply	V_S = ±2.5V to ±18V		5	15		*	30	μV/V
Channel Separation (dual and quad)	R_L = 2kΩ		0.2			*		μV/V
INPUT BIAS CURRENT								
Input Bias Current(2)	V_{CM} = 0V		+5	±50		*	*	pA
vs Temperature			See Typical Curve			*		
Input Offset Current(2)	V_{CM} = 0V		±2	±50		*	*	pA
NOISE								
Input Voltage Noise								
Noise Density, f = 10Hz			23			*		nV/√Hz
f = 100Hz			10			*		nV/√Hz
f = 1kHz			8			*		nV/√Hz
f = 10kHz			8			*		nV/√Hz
Current Noise Density, f = 1kHz			3			*		fA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range		(V–)+2.5	±13	(V+)–2.5	*		*	V
Common-Mode Rejection	V_{CM} = –12.5V to +12.5V	96	100		86	94		dB
INPUT IMPEDANCE								
Differential			10^{13} || 2			*		Ω || pF
Common-Mode	V_{CM} = –12.5V to +12.5V		10^{13} || 6			*		Ω || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	R_L = 10kΩ, V_O = –14.5V to +13.8V	110	120		104	*		dB
	R_L = 2kΩ, V_O = –13.8V to +13.5V	110	126		104	120		dB
	R_L = 600Ω, V_O = –12.8V to +12.5V	110	130		104	120		dB
FREQUENCY RESPONSE								
Gain-Bandwidth Product			8			*		MHz
Slew Rate			±20			*		V/μs
Settling Time: 0.1%	G = –1, 10V Step, C_L = 100pF		0.7			*		μs
0.01%	G = –1, 10V Step, C_L = 100pF		1			*		μs
Overload Recovery Time	G = ±1		0.5			*		μs
Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5Vrms							
	R_L = 2kΩ		0.00008			*		%
	R_L = 600Ω		0.00009			*		%
OUTPUT								
Voltage Output, Positive	R_L = 10kΩ	(V+)–1.2	(V+)–0.9		*	*		V
Negative		(V–)+0.5	(V–)+0.3		*	*		V
Positive	R_L = 2kΩ	(V+)–1.5	(V+)–1.2		*	*		V
Negative		(V–)+1.2	(V–)+0.9		*	*		V
Positive	R_L = 600Ω	(V+)–2.5	(V+)–2.0		*	*		V
Negative		(V–)+2.2	(V–)+1.9		*	*		V
Short-Circuit Current			±40			*		mA
Capacitive Load Drive (Stable Operation)			See Typical Curve			*		
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±2.5		±18	*		*	V
Quiescent Current (per amplifier)	I_O = 0		±4	±4.8		*	*	mA
TEMPERATURE RANGE								
Operating Range		–40		+85	*		*	°C
Storage		–40		+125	*		*	°C
Thermal Resistance, θ_{JA}								
8-Pin DIP			100			*		°C/W
SO-8 Surface-Mount			150			*		°C/W
14-Pin DIP			80			*		°C/W
SO-14 Surface-Mount			110			*		°C/W

*Specifications same as OPA132P, OPA132U.

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at T_J = 25°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	36V
Input Voltage	(V–) –0.7V to (V+) +0.7V
Output Short-Circuit(1)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
Single		
OPA132PA	8-Pin Plastic DIP	006
OPA132P	8-Pin Plastic DIP	006
OPA132UA	SO-8 Surface-Mount	182
OPA132U	SO-8 Surface-Mount	182
Dual		
OPA2132PA	8-Pin Plastic DIP	006
OPA2132P	8-Pin Plastic DIP	006
OPA2132UA	SO-8 Surface-Mount	182
OPA2132U	SO-8 Surface-Mount	182
Quad		
OPA4132PA	14-Pin Plastic DIP	010
OPA4132UA	SO-14 Surface-Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
Single		
OPA132PA	8-Pin Plastic DIP	–40°C to +85°C
OPA132P	8-Pin Plastic DIP	–40°C to +85°C
OPA132UA	SO-8 Surface-Mount	–40°C to +85°C
OPA132U	SO-8 Surface-Mount	–40°C to +85°C
Dual		
OPA2132PA	8-Pin Plastic DIP	–40°C to +85°C
OPA2132P	8-Pin Plastic DIP	–40°C to +85°C
OPA2132UA	SO-8 Surface-Mount	–40°C to +85°C
OPA2132U	SO-8 Surface-Mount	–40°C to +85°C
Quad		
OPA4132PA	14-Pin Plastic DIP	–40°C to +85°C
OPA4132UA	SO-14 Surface-Mount	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

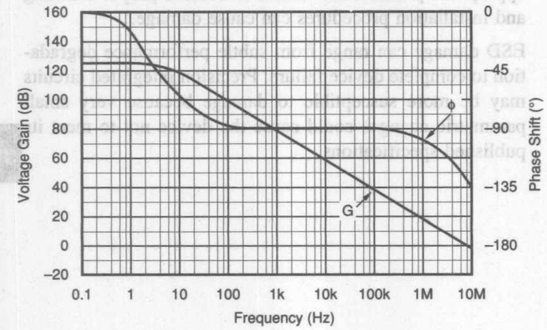
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

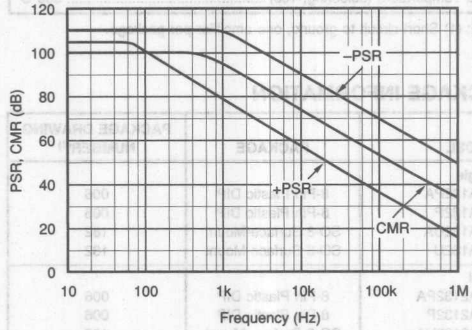
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, $V_S = \pm15V$, $R_L = 2k\Omega$, unless otherwise noted.

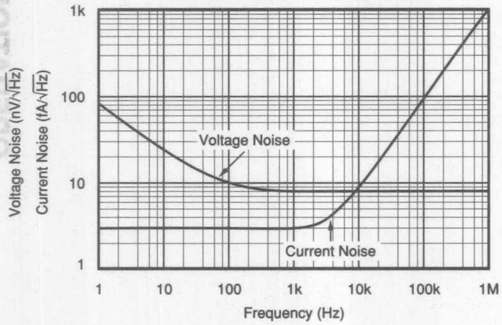
OPEN-LOOP GAIN/PHASE vs FREQUENCY



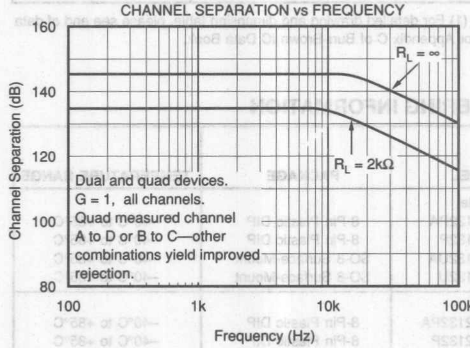
POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



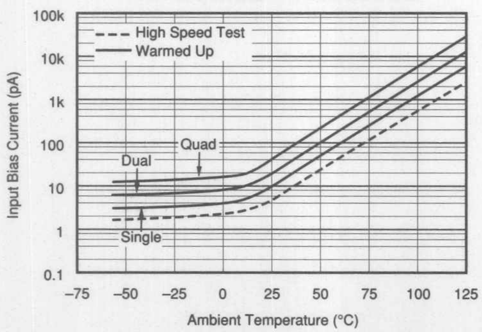
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



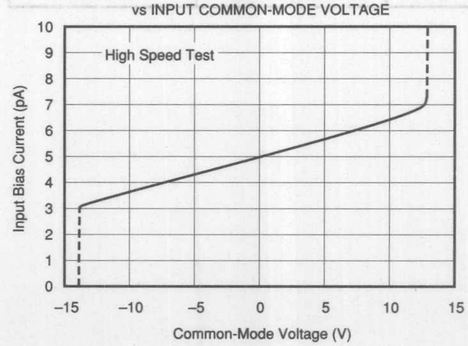
CHANNEL SEPARATION vs FREQUENCY



INPUT BIAS CURRENT vs TEMPERATURE

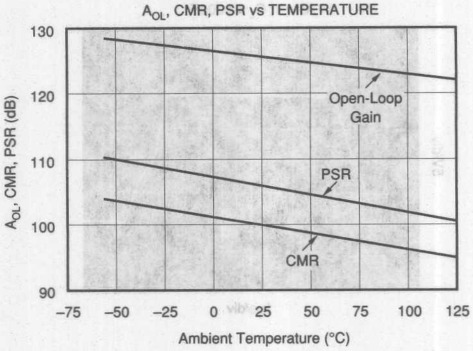


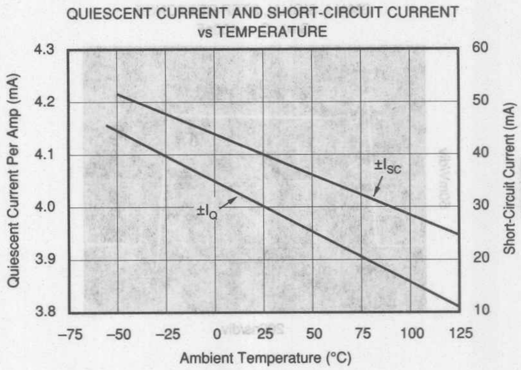
INPUT BIAS CURRENT vs INPUT COMMON-MODE VOLTAGE

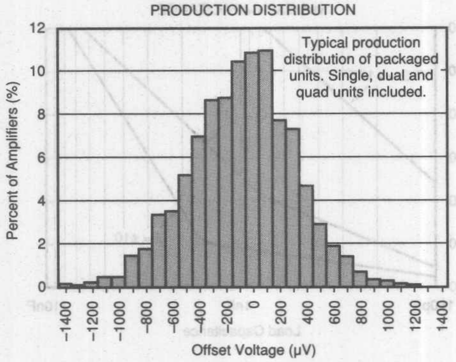


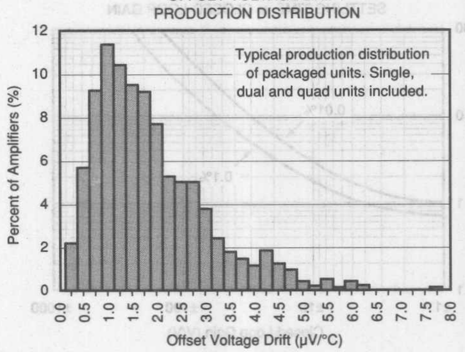
TYPICAL PERFORMANCE CURVES (CONT)

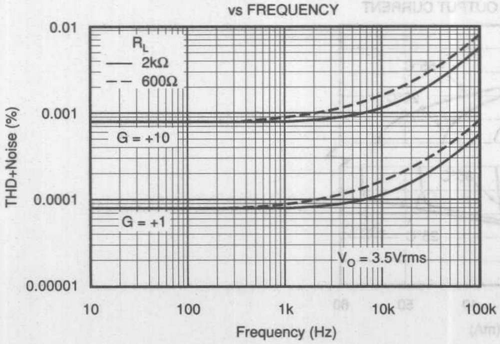
At $T_A = +25°C$, $V_S = \pm15V$, $R_L = 2k\Omega$, unless otherwise noted.

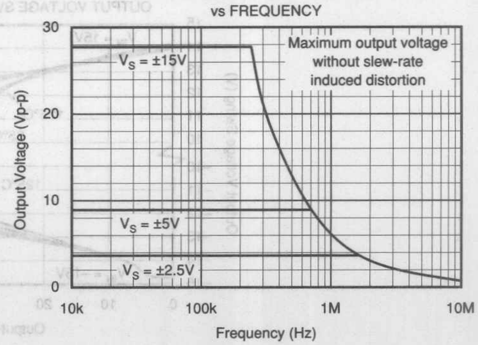








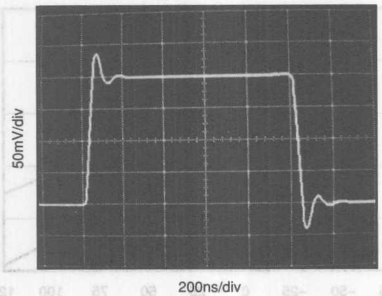




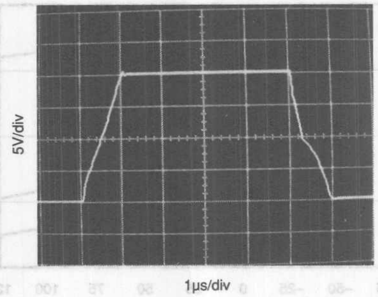
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = ±15V$, $R_L = 2kΩ$, unless otherwise noted.

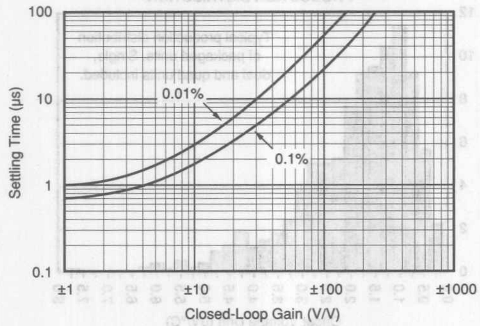
SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF



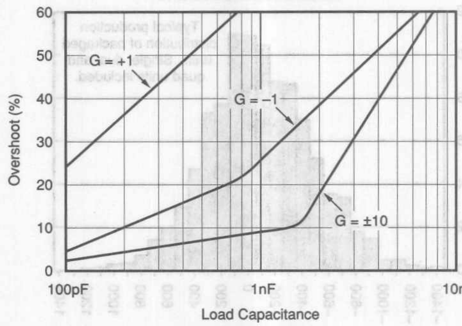
LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF



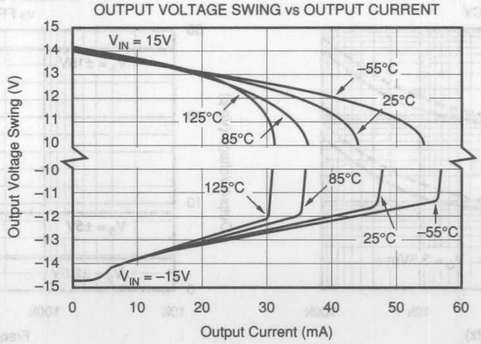
SETTLING TIME vs CLOSED-LOOP GAIN



SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



OPA132 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA132 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA132 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

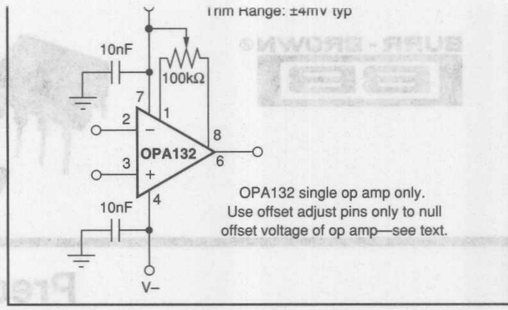


FIGURE 1. OPA132 Offset Voltage Trim Circuit.

OPERATING VOLTAGE

OPA132 series op amps operate with power supplies from ±2.5V to ±18V with excellent performance. Although specifications are production tested with ±15V supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

OFFSET VOLTAGE TRIM

Offset voltage of OPA132 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA132 (single op amp version) provides offset voltage trim connections on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset voltage drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

INPUT BIAS CURRENT

The FET-inputs of the OPA132 series provide very low input bias current and cause negligible errors in most applications. For applications where low input bias current is crucial, junction temperature rise should be minimized. The input bias current of FET-input op amps increases with temperature as shown in the typical performance curve "Input Bias Current vs Temperature."

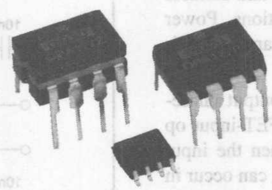
The OPA132 series may be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±3V supplies reduces power dissipation to one-fifth that at ±15V.

The dual and quad versions have higher total power dissipation than the single, leading to higher junction temperature. Thus, a warmed-up quad will have higher input bias current than a warmed-up single. Furthermore, an SOIC will generally have higher junction temperature than a DIP at the same ambient temperature because of a larger θ_{JA}. Refer to the specifications table.

Circuit board layout can also help minimize junction temperature rise. Temperature rise can be minimized by soldering the devices to the circuit board rather than using a socket. Wide copper traces will also help dissipate the heat by acting as an additional heat sink.

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPA132 series. See the typical performance curve "Input Bias Current vs Common-Mode Voltage."

BURR - BROWN®



OPA177
OPA77

Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 10µV max
- LOW DRIFT: 0.1µV/°C
- HIGH OPEN-LOOP GAIN: 130dB min
- LOW QUIESCENT CURRENT: 1.5mA typ
- REPLACES INDUSTRY-STANDARD OP AMPS: OP-07, OP-77, OP-177, AD707, ETC.

APPLICATIONS

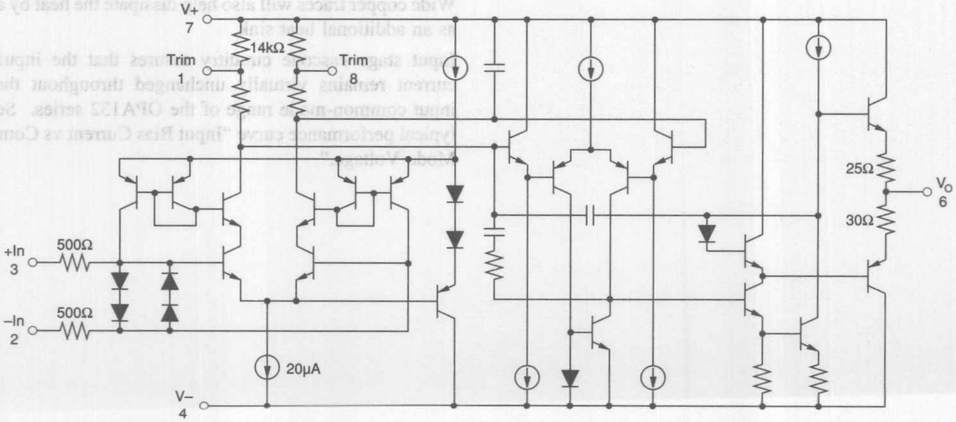
- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER

DESCRIPTION

The OPA177 and OPA77 precision bipolar op amps feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. Their high performance and low cost make them ideally suited to a wide range of precision instrumentation.

The low quiescent current of the OPA177 and OPA77 dramatically reduce warm-up drift and errors due to thermoelectric effects in input interconnections. They provide an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 and OPA77 maintains accuracy.

OPA177 and OPA77 performance gradeouts are available. Packaging options include 8-pin plastic DIP, 8-pin ceramic DIP, and SO-8 surface-mount packages.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

OPA177 SPECIFICATIONS

ELECTRICAL

At $V_S = \pm15V$, $T_A = +25°C$ unless otherwise noted.

		OPA177E			OPA177F			OPA177G			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE											
Input Offset Voltage			4	10		10	25		20	60	µV
Long-Term Input Offset(1) Voltage Stability			0.2			0.3			0.4		µV/Mo
Offset Adjustment Range	$R_P = 20k\Omega$		±3			*			*		mV
Power Supply Rejection Ratio	$V_S = \pm3V$ to $\pm18V$	120	125		115	*		110	120		dB
INPUT BIAS CURRENT											
Input Offset Current			0.3	1		*	1.5		*	2.8	nA
Input Bias Current			0.5	±1.5		*	±2		*	±2.8	nA
NOISE											
Input Noise Voltage	1Hz to 100Hz(2)		85	150		*	*		*	*	nVrms
Input Noise Current	1Hz to 100Hz		4.5			*			*		pArms
INPUT IMPEDANCE											
Input Resistance	Differential Mode(3)	26	45		*	*		18.5	*		MΩ
	Common-Mode		200			*			*		GΩ
INPUT VOLTAGE RANGE											
Common-Mode Input Range(4)		±13	±14		*	*		*	*		V
Common-Mode Rejection	$V_{CM} = \pm13V$	130	140		*	*		115	*		dB
OPEN-LOOP GAIN	$R_L \geq 2k\Omega$										
Large Signal Voltage Gain	$V_O = \pm10V$(5)	5000	12000		*	*		2000	6000		V/mV
OUTPUT											
Output Voltage Swing	$R_L \geq 10k\Omega$	±13.5	±14		*	*		*	*		V
	$R_L \geq 2k\Omega$	±12.5	±13		*	*		*	*		V
	$R_L \geq 1k\Omega$	±12	±12.5		*	*		*	*		V
Open-Loop Output Resistance			60			*			*		Ω
FREQUENCY RESPONSE											
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		*	*		*	*		V/µs
Closed-Loop Bandwidth	G = +1	0.4	0.6		*	*		*	*		MHz
POWER SUPPLY											
Power Consumption	$V_S = \pm15V$, No Load		40	60		*	*		*	*	mW
	$V_S = \pm3V$, No Load		3.5	4.5		*	*		*	*	mW
Supply Current	$V_S = \pm15V$, No Load		1.3	2		*	*		*	*	mA

ELECTRICAL

At $V_S = \pm15V$, $-40°C \leq T_A \leq +85°C$, unless otherwise noted.

		OPA177E			OPA177F			OPA177G			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE											
Input Offset Voltage			10	20		15	40		20	100	µV
Average Input Offset Voltage Drift(6)			0.03	0.1		0.1	0.3		0.7	1.2	µV/°C
Power Supply Rejection Ratio	$V_S = \pm3V$ to $\pm18V$	120	125		110	120		106	115		dB
INPUT BIAS CURRENT											
Input Offset Current			0.5	1.5		*	2.2		*	4.5	nA
Average Input Offset Current Drift(7)			1.5	25		*	40		*	85	pA/°C
Input Bias Current			0.5	±4		*				±6	nA
Average Input Bias Current Drift(7)			8	25		*	40		15	60	pA/°C
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±13	±13.5		*	*		*	*		V
Common-Mode Rejection	$V_{CM} = \pm13V$	120	140		*	*		110	*		dB
OPEN-LOOP GAIN											
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm10V$	2000	6000			*		1000	4000		V/mV
OUTPUT											
Output Voltage Swing	$R_L \geq 2k\Omega$	±12	±13		*	*		*	*		V
POWER SUPPLY											
Power Consumption	$V_S = \pm15V$, No Load		60	75		*	*		*	*	mW
Supply Current	$V_S = \pm15V$, No Load		2	2.5		*	*		*	*	mA

* Same as specification for product to left.

NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2µV. (2) Sample tested. (3) Guaranteed by design. (4) Guaranteed by CMRR test condition. (5) To insure high open-loop gain throughout the ±10V output range, A_{OL} is tested at $-10V \leq V_O \leq 0V$, $0V \leq V_O \leq +10V$, and $-10V \leq V_O \leq +10V$. (6) OP177EZ and OP177FZ: TCV_{OS} is 100% tested. (7) Guaranteed by end-point limits.

OPA77 SPECIFICATIONS

ELECTRICAL

At $V_S = \pm15V$, $T_A = +25°C$ unless otherwise noted.

PARAMETER	CONDITION	OPA77E MIN	OPA77E TYP	OPA77E MAX	OPA77F MIN	OPA77F TYP	OPA77F MAX	OPA77G MIN	OPA77G TYP	OPA77G MAX	UNITS
OFFSET VOLTAGE											
Input Offset Voltage			10	25		20	60		50	100	µV
Long-Term Input Offset Voltage Stability(1)			0.3			0.4			*		µV/Mo
Offset Adjustment Range	$R_{TRIM} = 20kΩ$		±3			*			*		mV
Power Supply Rejection Ratio	$V_S = \pm3V$ to $\pm18V$		0.7	3		*	*		*	*	µV/V
INPUT BIAS CURRENT											
Input Offset Current			0.3	1.5		*	2.8		*	*	nA
Input Bias Current			1.2	±2		*	±2.8		*	*	nA
NOISE											
Input Noise Voltage	0.1Hz to 10Hz(2)		0.35	0.6		0.38	0.65		*	*	µVp-p
Input Noise Voltage Density	f = 10Hz(2)		8.5	18		*	20		*	*	nV/√Hz
	f = 100Hz(2)		7.5	13		*	13.5		*	*	nV/√Hz
	f = 1000Hz(2)		7.5	11		*	11.5		*	*	nV/√Hz
Input Noise Current	0.1Hz to 10Hz		35			*			*		pAp-p
Input Noise Current Density	f = 10Hz		0.73			*			*		pA/√Hz
	f = 100Hz		0.26			*			*		pA/√Hz
	f = 1000Hz		0.22			*			*		pA/√Hz
INPUT RESISTANCE											
Differential Input Resistance(3)		26	45		18.5	*		*	*		MΩ
Common-mode Input Resistance			200			*			*		GΩ
INPUT VOLTAGE RANGE											
Common Mode Input Range		±13	±14		*	*		*	*		V
Common-Mode Rejection	$V_{CM} = \pm13V$		0.1	1		*	1.6		*	*	µV/V
OPEN-LOOP GAIN											
Large-Signal Voltage Gain	$R_L \geq 2kΩ$, $V_O = \pm10V$	5000	12000		2000	6000		*			V/mV
OUTPUT											
Output Voltage Swing	$R_L \geq 10kΩ$	±13.5	±14		*	*		*	*		V
	$R_L \geq 2kΩ$	±12.5	±13		*	*		*	*		V
	$R_L \geq 1kΩ$	±12	±12.5		*	*		*	*		V
Open-Loop Output Resistance			60			*			*		Ω
FREQUENCY RESPONSE											
Slew Rate	$R_L \geq 2kΩ$	0.1	0.3		*	*		*	*		V/µs
Closed-Loop Bandwidth	AVCL = +1	0.4	0.6		*	*		*	*		MHz
POWER SUPPLY											
Power Consumption	$V_S = \pm15V$, No Load		50	60		*	*		*	*	mW
	$V_S = \pm3V$, No Load		3.5	4.5		*	*		*	*	mW

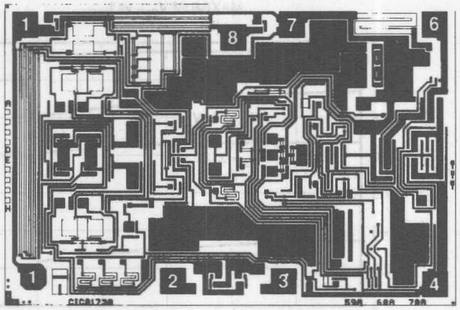
ELECTRICAL

At $V_S = \pm15V$, $-25°C \leq T_A \leq +85°C$ for OPA77EZ and OPA77FZ, $0°C \leq T_A \leq +70°C$ for OPA77FP and OPA77GP, unless otherwise noted.

OFFSET VOLTAGE											
Input Offset Voltage	Z Package		10	45		20	100		*	*	µV
	P Package		10	55		20	100		80	150	µV
Average Input Offset(4) Voltage Drift	Z Package		0.1	0.3		0.2	0.6		*	*	µV/°C
	P Package		0.3	0.6		0.4	1		0.7	1.2	µV/°C
Power Supply Rejection Ratio	$V_S = \pm3V$ to $\pm18V$		1	3		*	5		*	*	µV/V
INPUT BIAS CURRENT											
Input Offset Current			0.5	2.2		*	4.5		*	*	nA
Avg Input Offset Current Drift(5)			1.5	40		*	85		*	*	pA/°C
Input Bias Current			2.4	±4		*	±6		*	*	nA
Avg Input Bias Current Drift(5)			8	40		15	60		*	*	pA/°C
INPUT VOLTAGE RANGE											
Common Mode Input Range		±13	±13.5		*	*		*	*		V
Common-Mode Rejection	$V_{CM} = \pm13V$		0.1	1		*	3		*	*	µV/V
OPEN-LOOP GAIN											
Large Signal Voltage Gain	$R_L \geq 2kΩ$, $V_O = \pm10V$	2000	6000		1000	4000		*	*		V/mV
OUTPUT											
Output Voltage Swing	$R_L \geq 2kΩ$	±12	±13		*	*		*	*		V
POWER SUPPLY											
Power Consumption	$V_S = \pm15V$, No Load		60	75		*	*		*	*	mW

* Same as specification for product to left. NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended period after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV. (2) Sample tested. (3) Guaranteed by design. (4) OPA77E: TCV_{OS} is 100% tested on Z package. (5) Guaranteed by end-point limits.

DICE INFORMATION



OPA177/77 DIE TOPOGRAPHY

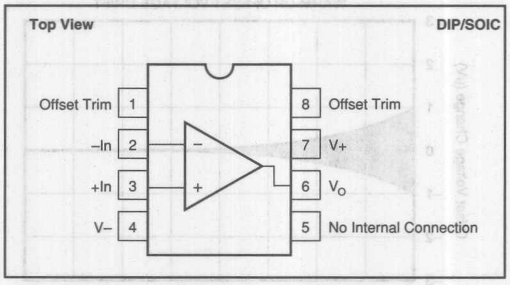
PAD	FUNCTION
1	Offset Trim
2	−In
3	+In
4	V−
5	NC
6	V_O
7	V+
8	Offset Trim

Substrate Bias: $-V_S$
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	63 x 92 ±5	1.60 x 2.34 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count		46
Backing		Gold

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	$\pm V_S$
Output Short Circuit	Continuous
Operating Temperature:	
Ceramic DIP (Z)	−55°C to +125°C
Plastic DIP (P), SO-8 (S)	−40°C to +85°C
θ_{JA} (PDIP)	100°C/W
θ_{JA} (SOIC)	160°C/W
θ_{JA} (Ceramic)	148°C/W
Storage Temperature:	
Ceramic DIP (Z)	−65°C to +150°C
Plastic DIP (P), SO-8 (S)	−65°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) P, Z packages	+300°C
(soldering, 3s) S package	+260°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA177FP	8-Pin Plastic DIP	−40°C to +85°C
OPA177GP	8-Pin Plastic DIP	−40°C to +85°C
OPA177GS	SO-8 Surface-Mount	−40°C to +85°C
OPA177EZ	8-Pin Ceramic DIP	−40°C to +85°C
OPA177FZ	8-Pin Ceramic DIP	−40°C to +85°C
OPA177GZ	8-Pin Ceramic DIP	−40°C to +85°C
OPA77FP	8-Pin Plastic DIP	0°C to +70°C
OPA77GP	8-Pin Plastic DIP	0°C to +70°C
OPA77EZ	8-Pin Ceramic DIP	−25°C to +85°C
OPA77FZ	8-Pin Ceramic DIP	−25°C to +85°C

PACKAGE INFORMATION

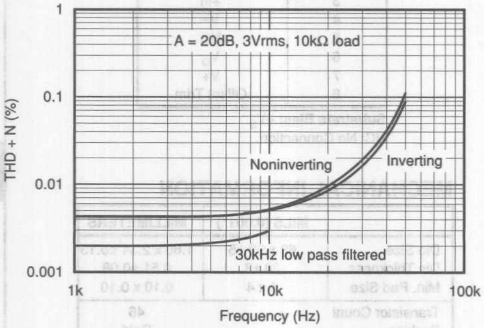
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA177FP	8-Pin Plastic DIP	006
OPA177GP	8-Pin Plastic DIP	006
OPA177GS	SO-8 Surface-Mount	182
OPA177EZ	8-Pin Ceramic DIP	254
OPA177FZ	8-Pin Ceramic DIP	254
OPA177GZ	8-Pin Ceramic DIP	254
OPA77FP	8-Pin Plastic DIP	006
OPA77GP	8-Pin Plastic DIP	006
OPA77EZ	8-Pin Ceramic DIP	254
OPA77FZ	8-Pin Ceramic DIP	254

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

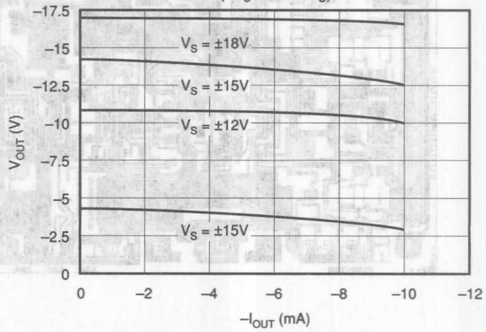
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

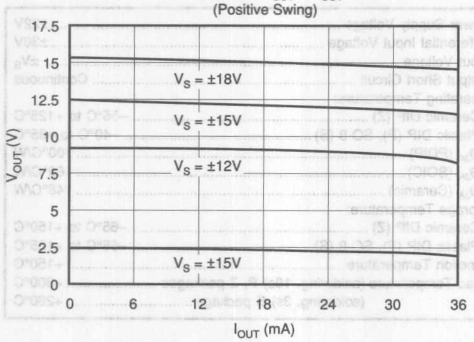
TOTAL HARMONIC DISTORTION AND NOISE vs FREQUENCY



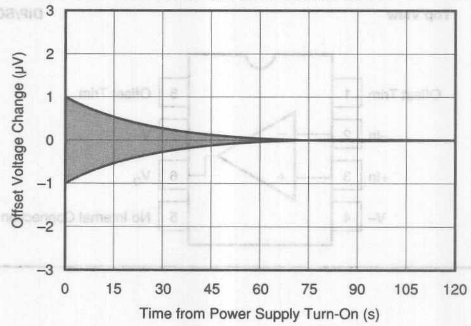
MAXIMUM V_{OUT} vs I_{OUT} (Negative Swing)



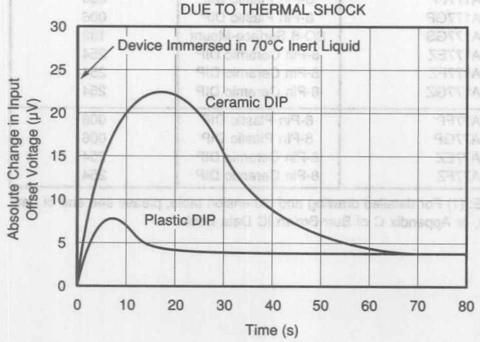
MAXIMUM V_{OUT} vs I_{OUT} (Positive Swing)



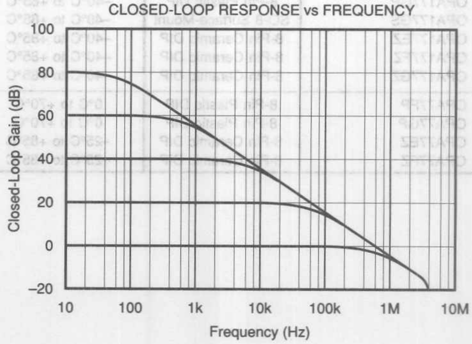
WARM-UP OFFSET VOLTAGE DRIFT



OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK

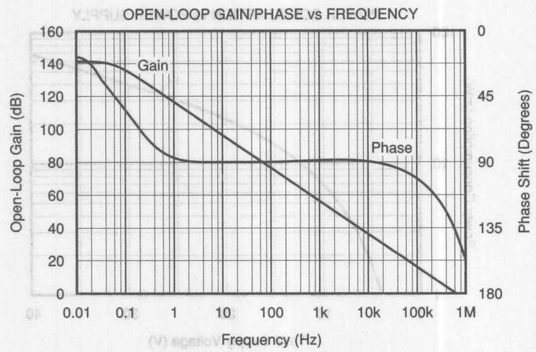


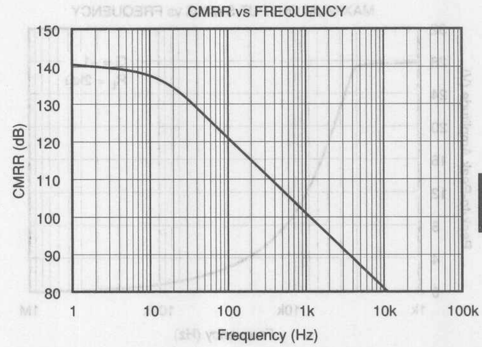
CLOSED-LOOP RESPONSE vs FREQUENCY

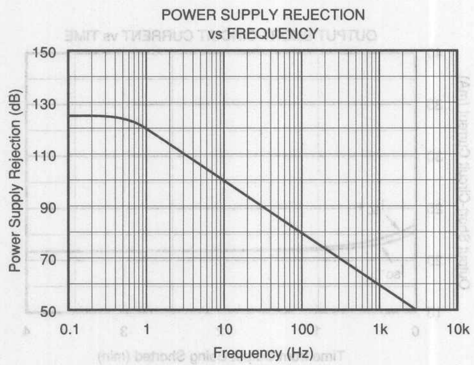


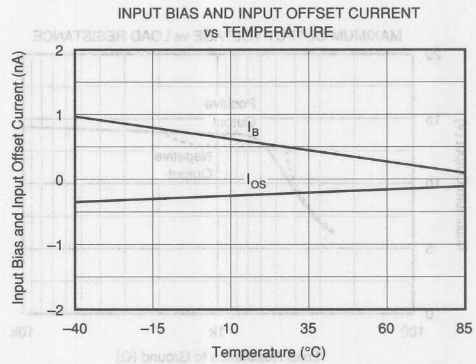
TYPICAL PERFORMANCE CURVES (CONT)

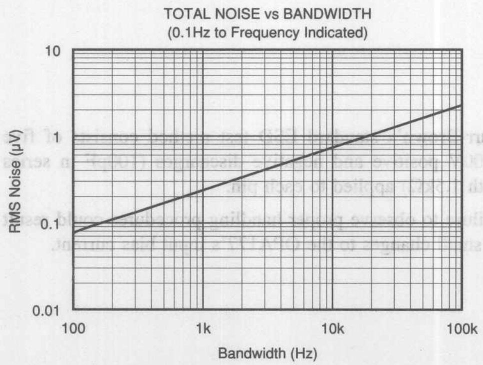
T_A = +25°C, V_S = ±15V unless otherwise noted.

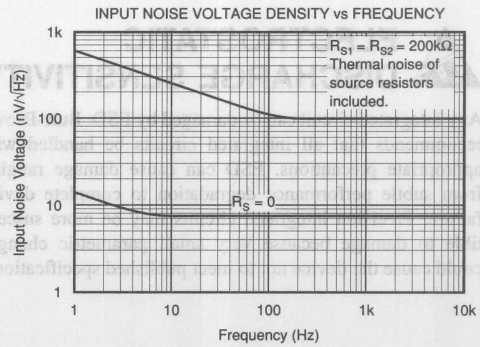






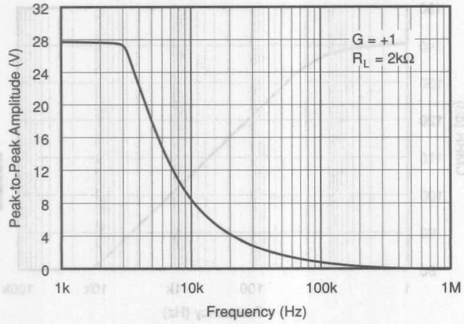




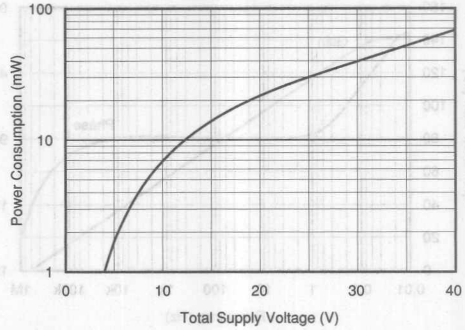


$T_A = +25°C$, $V_S = \pm15V$ unless otherwise noted.

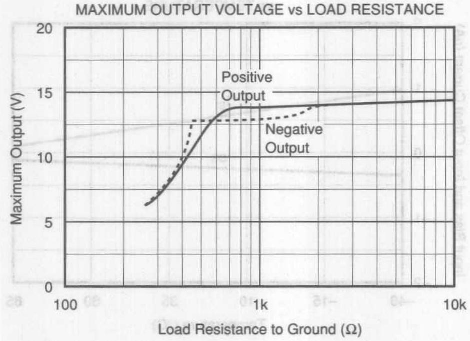
MAXIMUM OUTPUT SWING vs FREQUENCY



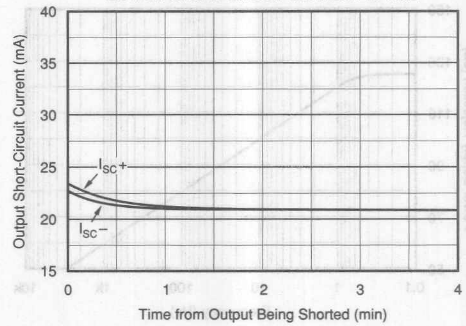
POWER CONSUMPTION vs POWER SUPPLY



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT vs TIME



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5kΩ) applied to each pin.

Failure to observe proper handling procedures could result in small changes to the OPA177's input bias current.

APPLICATIONS INFORMATION

The OPA177 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 0.1μF ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions must be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can mask the ultimate performance of the OPA177. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

1. Keep connections made to the two input terminals close together.
2. Locate heat sources as far as possible from the critical input circuitry.
3. Shield the op amp and input circuitry from air currents such as cooling fans.

OFFSET VOLTAGE ADJUSTMENT

The OPA177 and OPA77 have been laser-trimmed for low offset voltage and drift so most circuits will not require external adjustment. Figure 1 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce excessive temperature drift.

INPUT PROTECTION

The inputs of the OPA177 and OPA77 are protected with 500Ω series input resistors and diode clamps as shown in the simplified circuit diagram. The inputs can withstand ±30V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

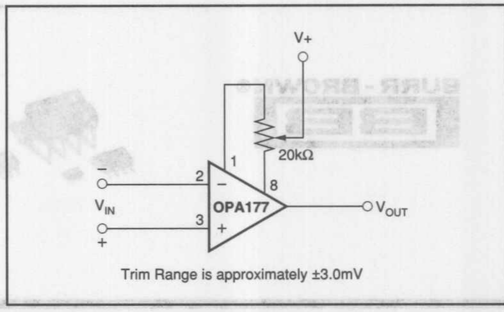


FIGURE 1. Optional Offset Nulling Circuit.

NOISE PERFORMANCE

The noise performance of the OPA177 and OPA77 is optimized for circuit impedances in the range of 2kΩ to 50kΩ. Total noise in an application is a combination of the op amp's input voltage noise and input bias current noise reacting with circuit impedances. For applications with higher source impedance, the OPA627 FET-input op amp will generally provide lower noise. For very low impedance applications, the OPA27 will provide lower noise.

INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to balance the DC resistance seen at the two input terminals (Figure 2). A resistor added to balance the input resistances may actually increase offset and noise.

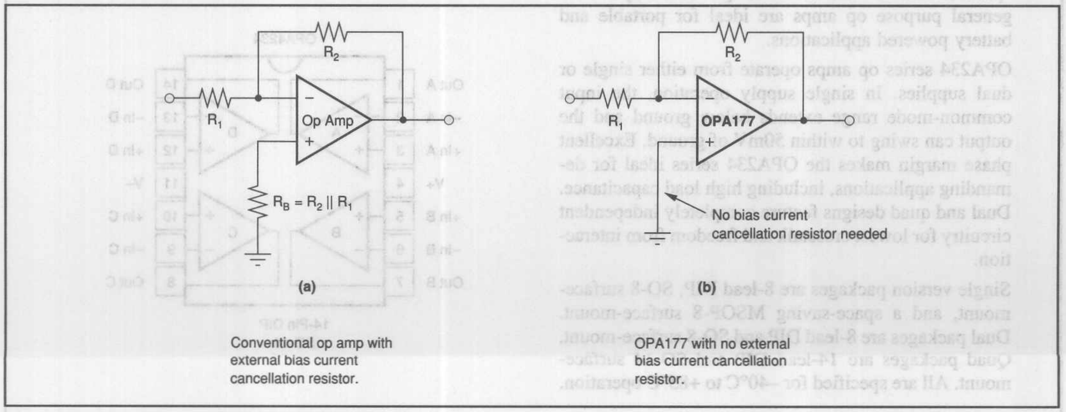
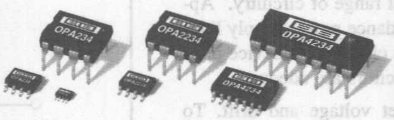


FIGURE 2. Input Bias Current Cancellation.

BURR - BROWN®



OPA234
OPA2234
OPA4234

PRELIMINARY INFORMATION SUBJECT TO CHANGE WITHOUT NOTICE

Low Power, Precision SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

FEATURES

- **WIDE SUPPLY RANGE:**
  Single Supply: V_S = +2.7V to +36V
  Dual Supply: V_S = ±1.35V to ±18V
- **GUARANTEED PERFORMANCE: +2.7V, +5V, and ±15V**
- **LOW QUIESCENT CURRENT: 250µA/amp**
- **LOW INPUT BIAS CURRENT: 20nA max**
- **LOW OFFSET VOLTAGE: 100µV max**
- **HIGH CMRR, PSRR, and A_{OL}**
- **SINGLE, DUAL, and QUAD VERSIONS**

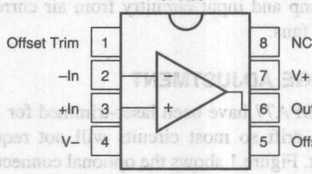
DESCRIPTION

The OPA234 series of low cost op amps is ideal for single supply, low voltage, low power applications. The combination of low offset voltage, high common-mode rejection, high power supply rejection, and a wide supply range provides excellent accuracy and versatility. Single, dual, and quad versions have identical specifications for maximum design flexibility. These general purpose op amps are ideal for portable and battery powered applications.

OPA234 series op amps operate from either single or dual supplies. In single supply operation, the input common-mode range extends below ground and the output can swing to within 50mV of ground. Excellent phase margin makes the OPA234 series ideal for demanding applications, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

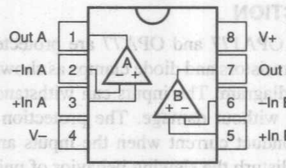
Single version packages are 8-lead DIP, SO-8 surface-mount, and a space-saving MSOP-8 surface-mount. Dual packages are 8-lead DIP and SO-8 surface-mount. Quad packages are 14-lead DIP and SO-14 surface-mount. All are specified for –40°C to +85°C operation.

OPA234



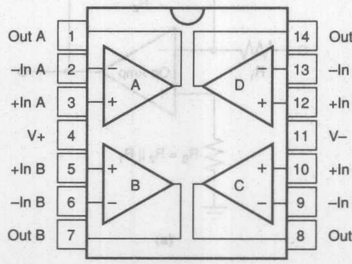
8-Pin DIP, SO-8, MSOP-8

OPA2234



8-Pin DIP, SO-8

OPA4234



14-Pin DIP
SO-14

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

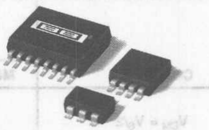
At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

			OPA234P, U OPA2234P, U			OPA234PA, UA OPA2234PA, UA OPA4234PA, UA			
PARAMETER	V_s	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE									
Input Offset Voltage	+5V	V_{CM} = V_S/2		±30	±100		*	±250	µV
	±15V	V_{CM} = 0V		±30	±500		*	*	µV
vs Temperature(1)		Operating Temperature Range		±0.5	±3		*	*	µV/°C
vs Power Supply		V_S = +2.7V to +30V, V_{CM} = 1.7V		3	10		*	20	µV/V
Channel Separation (Dual, Quad)				1			*		µV/V
INPUT BIAS CURRENT		V_{CM} = V_S/2							
Input Bias Current				–15	–20		*	–50	nA
Input Offset Current				±0.5	±2		*	±5	nA
NOISE									
Input Voltage Noise Density, f = 1kHz				25			*		nV/√Hz
Current Noise Density, f = 1kHz				100			*		fA/√Hz
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	+5V		–0.1		(V+)–1	*		*	V
	±15V		(V–)–0.1		(V+)–1	*		*	V
Common-Mode Rejection(2)		V_{CM} = (V–)–0.1V to (V+)–1V	100	106		90	*		dB
INPUT IMPEDANCE									
Differential				10^6 || 10			*		Ω || pF
Common-Mode		V_{CM} = V_S/2		10^8 || 5			*		Ω || pF
OPEN-LOOP GAIN(2)		V_O = (V–)+0.25V to (V+)–1V							
Open-Loop Voltage Gain		R_L = 10kΩ	110	120		*	*		dB
		R_L = 2kΩ	90	94		*	*		dB
FREQUENCY RESPONSE									
Gain-Bandwidth Product				350			*		kHz
Slew Rate				0.2			*		V/µs
Settling Time		G = 1, C_L = 100pF							
0.1%	+5V	3V Step		16			*		µs
	±15V	10V Step		42			*		µs
0.01%	+5V	3V Step		25			*		µs
	±15V	10V Step		46			*		µs
Overload Recovery Time		G = 1, V_{IN} = V_S		16			*		µs
OUTPUT									
Voltage Output, Positive	+5V	R_L = 10kΩ to V_S/2	(V+)–1	(V+)–0.6		*	*		V
Negative	+5V	R_L = 10kΩ to V_S/2	0.25	0.05		*	*		V
Positive	+5V	R_L = 10kΩ to Ground	(V+)–1	(V+)–0.65		*	*		V
Negative	+5V	R_L = 10kΩ to Ground	0.1	0.05		*	*		V
Positive	±15V	R_L = 10kΩ to Ground	(V+)–1	(V+)–0.7		*	*		V
Negative	±15V	R_L = 10kΩ to Ground	(V–)+0.5	(V–)+0.15		*	*		V
Short-Circuit Current	+5V			±11			*		mA
	±15V			±22			*		mA
Capacitive Load Drive (Stable Operation)		G = +1		1000			*		pF
POWER SUPPLY									
Specified Operating Voltage									
Single Supply			+2.7		+36	*		*	V
Dual Supply			±1.35		±18	*		*	V
Quiescent Current (per amplifier)	+5V	I_O = 0		250	300		*	*	µA
	±15V	I_O = 0		275	350		*	*	µA
TEMPERATURE RANGE									
Operating Range			–40		+85	*		*	°C
Storage			–40		+125	*		*	°C
Thermal Resistance, θ_{JA}									
8-Pin DIP				100			*		°C/W
SO-8 Surface-Mount				150			*		°C/W
MSOP-8 Surface-Mount				175			*		°C/W
14-Pin DIP				80			*		°C/W
SO-14 Surface-Mount				110			*		°C/W

*Specifications same as OPA234P, OPA234U.

NOTES: (1) Guaranteed by wafer test. (2) For Single Supply, (V–) = 0V.

BURR - BROWN®



OPA237
OPA2237
OPA4237

PRELIMINARY INFORMATION SUBJECT TO CHANGE WITHOUT NOTICE

SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

MicroAmplifier™ Series

FEATURES

- **MICRO-SIZE, MINIATURE PACKAGES**
  Single: SOT-23-5
  Dual: MSOP-8
  Quad: SSOP-16
- **LOW OFFSET VOLTAGE: 250µV max**
- **WIDE SUPPLY RANGE**
  Single Supply: +2.7V to +36V
  Dual Supply: ±1.35V to ±18V
- **LOW QUIESCENT CURRENT: 200µA**
- **WIDE BANDWIDTH: 1.5MHz**

APPLICATIONS

- **BATTERY POWERED INSTRUMENTS**
- **PORTABLE DEVICES**
- **PCMCIA CARDS**
- **MEDICAL INSTRUMENTS**
- **TEST EQUIPMENT**

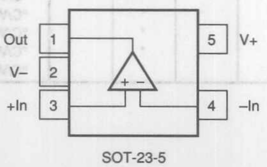
DESCRIPTION

The OPA237 op amp family is one of Burr-Brown's ***MicroAmplifier***™ series of miniature products. In addition to small size, these devices feature low offset voltage, low quiescent current, low bias current, and a wide supply range. Single, dual and quad versions have identical specifications for maximum design flexibility. They are ideal for single supply, battery operated, and space-limited applications, such as PCMCIA cards and other portable instruments.

OPA237 series op amps can operate from either single or dual supplies. When operated from a single supply, the input common-mode range extends below ground and the output can swing to within 50mV of ground. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

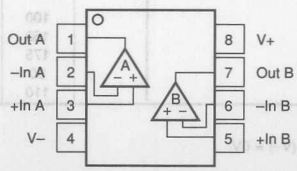
Single, dual, and quad are available in surface-mount packages. The single version's package is the ultra-miniature 5-lead SOT-23. The dual version comes in a miniature MSOP-8. The quad version's package is the SSOP-16. The SSOP-16 is the same size as an SO-8 surface-mount package and the MSOP-8 is half the size of an SO-8. The SOT-23 is even smaller, half the size of an MSOP-8. Operation is specified from –40°C to +85°C.

OPA237



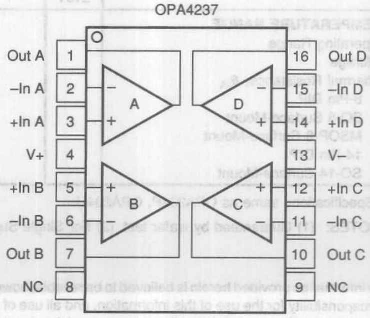
SOT-23-5

OPA2237



MSOP-8

OPA4237



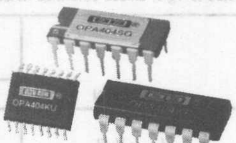
SSOP-16

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PARAMETER	CONDITION	OPA237UA OPA2237UA OPA4237UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage	$V_{CM} = V_S/2$		±100	±250	mV
vs Temperature(1)	Operating Temperature Range		±0.5	±5	μV/°C
vs Power Supply	V_S = +2.7V to +36V		10	30	μV/V
Channel Separation (dual and quad)			1		μV/V
INPUT BIAS CURRENT					
Input Bias Current	V_{CM} = (V–)–0.2V to (V+)–1.5V		–15	–40	nA
Input Offset Current	V_{CM} = (V–)–0.2V to (V+)–1.5V		±5	±10	nA
NOISE					
Input Voltage Noise, f = 0.1 to 10Hz			1		μVp-p
Input Voltage Noise Density, f = 1kHz			30		nV/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range		(V–)–0.2		(V+)–1.5	V
Common-Mode Rejection	V_{CM} = (V–)–0.2V to (V+)–1.5V	85	90		dB
INPUT IMPEDANCE					
Differential			10^8 || 4		Ω || pF
Common-Mode			10^9 || 2		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = (V–)+0.5V to (V+)–1	80	90		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			1.5		MHz
Slew Rate	G = 1		0.5		V/μs
Settling Time: 0.1%	V_S = +5V, G = 1, 3V Step, C_L = 100pF		8		μs
0.01%	V_S = +5V, G = 1, 3V Step, C_L = 100pF		10		μs
VOLTAGE OUTPUT: V_S = +2.7V or +5V					
Positive	R_L = 100kΩ to Ground	(V+)–1	(V+)–0.75		V
Negative	R_L = 100kΩ to Ground	0.05	0.01		V
Positive	R_L = 100kΩ to $V_S/2$	(V+)–1	(V+)–0.75		V
Negative	R_L = 100kΩ to $V_S/2$	0.1	0.05		V
Positive	R_L = 10kΩ to $V_S/2$	(V+)–1	(V+)–0.75		V
Negative	R_L = 10kΩ to $V_S/2$	0.5	0.35		V
VOLTAGE OUTPUT: V_S = ±15V					
Positive	R_L = 100kΩ to Ground	(V+)–1	(V+)–0.75		V
Negative	R_L = 100kΩ to Ground	(V–)+0.5	(V–)+0.3		V
Positive	R_L = 10kΩ to Ground	(V+)–1.5	(V+)–1		V
Negative	R_L = 10kΩ to Ground	(V–)+1.2	(V–)+0.8		V
OUTPUT					
Short-Circuit Current			±4		mA
Caoacitive Load Drive (stable operation)	G = 1		200		pF
	G = 5		1000		pF
POWER SUPPLY					
Specified Operating Voltage, Single Supply		+2.7		+36	V
Specified Operating Voltage, Dual Supply		±1.35		±18	V
Quiescent Current (per amplifier)	V_S = +2.7V to +5V		200	350	μA
	V_S = ±15V		250	450	μA
TEMPERATURE RANGE					
Operating Range		–40		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}					
5-Lead SOT-23 Surface-Mount			200		°C/W
MSOP-8 Surface-Mount			200		°C/W
SSOP-16 Surface Mount			150		°C/W

NOTES: (1) Guaranteed by wafer-level test.

BURR - BROWN®



OPA404

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10677

Quad High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±750μV max
- LOW BIAS CURRENT: ±4pA max
- LOW SETTLING: 1.5μs to 0.01%
- STANDARD QUAD PINOUT

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

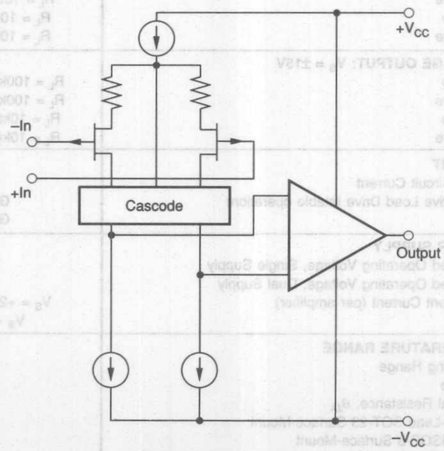
The OPA404 is a high performance monolithic ***Difet***®(dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias current together with wide bandwidth and fast slew rate.

Noise, bias current, voltage offset, drift, and speed are superior to BIFET® amplifiers.

Laser-trimming of thin-film resistors gives very low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.



OPA404 Simplified Circuit
(Each Amplifier)

Difet®, Burr-Brown Corp.
BIFET®, National Semiconductor Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU [1] MIN	TYP	MAX	OPA404BG MIN	TYP	MAX	OPA404SG MIN	TYP	MAX	UNITS
INPUT											
NOISE											
Voltage: f_O = 10Hz			32			*			*		nV/√Hz
f_O = 100Hz			19			*			*		nV/√Hz
f_O = 1kHz			15			*			*		nV/√Hz
f_O = 10kHz			12			*			*		nV/√Hz
f_B = 10Hz to 10kHz			1.4			*			*		µVrms
f_B = 0.1Hz to 10Hz			0.95			*			*		µVp-p
Current: f_B = 0.1Hz to 10Hz			12			*			*		fA, p-p
f_O = 0.1Hz thru 20kHz			0.6			*			*		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage	V_{CM} = 0VDC		±260	±1mV		*	±750		*	*	µV
KP, KU			±750	±2.5mV							µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3			*			*		µV/°C
KP, KU			±5								µV/°C
Supply Rejection	±V_{CC} = 12V to 18V	80	100		86	*			*		dB
KP, KU		76	100								dB
Channel Separation	100Hz, R_L = 2kΩ		125			*			*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±1	±8		*	±4		*	*	pA
KP, KU			±1	±12							pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.5	8		*	4		*	*	pA
KP, KU			0.5	12							pA
IMPEDANCE											
Differential			10^{13} || 1			*			*		Ω || pF
Common-Mode			10^{14} || 3			*			*		Ω || pF
VOTAGE RANGE											
Common-Mode Input Range		±10.5	+13, −11		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	88	100		92	*		*	*		dB
KP, KU		84	100								dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	88	100		92	*		*	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	4	6.4		5	*		*	*		MHz
Full Power Response	20Vp-p, R_L = 2kΩ		570			*			*		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	24	35		28	*		*	*		V/µs
Settling Time: 0.1%	Gain = −1, R_L = 2kΩ		0.6			*			*		µs
0.01%	C_L = 100 pF, 10V Step		1.5			*			*		µs
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11.5	+13.2, −13.8		*	*		*	*		V
Current Output	V_O = ±10VDC	±5	±10		*	*		*	*		mA
Output Resistance	1MHz, Open Loop		80			*			*		Ω
Load Capacitance Stability	Gain = +1		1000			*			*		pF
Short Circuit Current		±10	±27	±40	*	*	*	*	*	*	mA
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range, Derated Performance		±5		±18	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		9	10		*	*		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient Temperature	−25		+85	*		*	−55		+125	°C
KP, KU		0		+70							°C
Operating	Ambient Temperature	−55		+125	*		*	*		*	°C
KP, KU		−25		+85							°C
Storage	Ambient Temperature	−65		+150	*		*	*		*	°C
KP, KU		−40		+125							°C
θ Junction-Ambient			100			*			*		°C/W
KP, KU			120/100								°C/W

*Specifications same as OPA404AG.

NOTE: (1) OPA404KU may be marked OPA404U.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

		OPA404AG, KP, KU			OPA404BG			OPA404SG			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TEMPERATURE RANGE											
Specification Range	Ambient Temperature	–25		+85	*		*	–55		+125	°C
KP, KU		0		+70							°C
INPUT											
OFFSET VOLTAGE											
Input Offset Voltage	V_{CM} = 0VDC		±450	2mV		*	±1.5mV		±550	±2.5mV	µV
KP KU			±1	±3.5							mV
Average Drift			±3			*			*		µV/°C
KP, KU			±5								µV/°C
Supply Rejection		75	96		80	*		70	93		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±32	±200		*	±100		±500	±5nA	pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		17	100		*	50		260	2.5nA	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10	+12.7, –10.6		*	*		±10	+12.6, –10.5		V
Common-Mode Rejection	V_{IN} = ±10VDC	82	99		86	*		80	88		dB
KP, KU		80	99								dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	82	94		86	*		80	88		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11.5	+12.9, –13.8		*	*		±11	+12.7, –13.8		V
Current Output	V_O = ±10VDC	±5	±9		*	*		*	±8		mA
Short Circuit Current	V_O = 0VDC	±8	±20	±50	*	*	*	*	*	*	mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		9.3	10.5		*	*		9.4	11	mA

* Specification same as OPA404AG.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA404KP	14-Pin Plastic DIP	0°C to +70°C
OPA404KU(1)	16-Pin Plastic SOIC	0°C to +70°C
OPA404AG	14-Pin Ceramic DIP	–25°C to +85°C
OPA404BG	14-Pin Ceramic DIP	–25°C to +85°C
OPA404SG	14-Pin Ceramic DIP	–55°C to +125°C

NOTE: (1) OPA404KU may be marked OPA404U.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA404KP	14-Pin Plastic DIP	010
OPA404KU(2)	16-Pin Plastic SOIC	211
OPA404AG	14-Pin Ceramic DIP	169
OPA404BG	14-Pin Ceramic DIP	169
OPA404SG	14-Pin Ceramic DIP	169

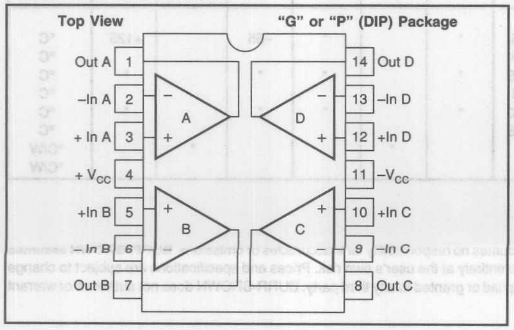
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) OPA404KU may be marked OPA404U.

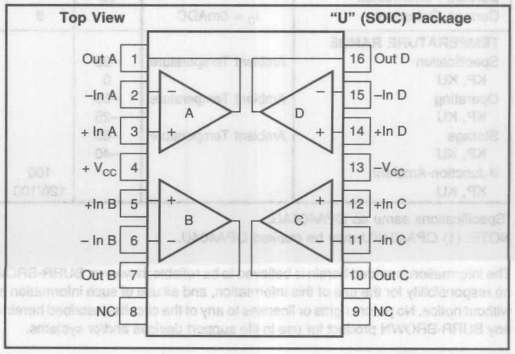
ABSOLUTE MAXIMUM RATINGS

Supply .... ±18VDC
Internal Power Dissipation(1) 1000mW
Differential Input Voltage(2) .... ±36VDC
Input Voltage Range(2) .... ±18VDC
Storage Temperature Range ... P, U = –40°C/+125°C, G = –65°C/+150°C
Operating Temperature Range .. P, U = –25°C/+85°C, G = –55°C/+125°C
Lead Temperature (soldering, 10s) .... 300°C
SOIC (soldering, 3s) .... +260°C
Output Short-Circuit Duration(3) .... Continuous
Junction Temperature .... +175°C

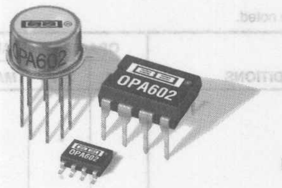
NOTES: (1) Packages must be derated based on θ_{JC} = 30°C/W or θ_{JA} = 120°C/W. (2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to: 18V > V_{IN} > $-V_{CC}$ – 8V. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

PIN CONFIGURATION





BURR - BROWN®



OPA602

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10753

High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±250μV max
- LOW BIAS CURRENT: ±1pA max
- FAST SETTLING TIME: 1μs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION

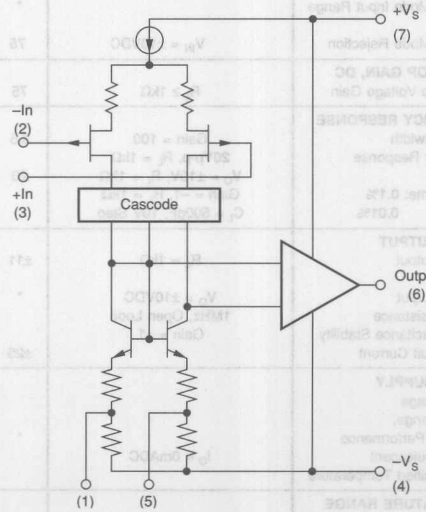
DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic ***Difet*** (dielectrically isolated FET) construction provides an unusual combination of high speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1kΩ resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. ***Difet*** construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.



Difet® Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At $V_S = \pm15VDC$ and $T_A = +25°C$ unless otherwise noted.

		OPA602AM/AP/AU			OPA602BM/SM/BP			OPA602CM			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT NOISE											
Voltage: f_O = 10Hz			*			23			*		nV/√Hz
f_O = 100Hz			*			19			*		nV/√Hz
f_O = 1kHz			*			13			*		nV/√Hz
f_O = 10kHz			*			12			*		nV/√Hz
f_B = 10Hz to 10kHz			*			1.4			*		µVrms
f_B = 0.1Hz to 10Hz			*			0.95			*		µVp-p
Current: f_B = 0.1Hz to 10Hz			*			12			*		fAp-p
f_O = 0.1Hz to 20kHz			*			0.6			*		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage:											
M Package	V_{CM} = 0VDC		±300	±1000		±150	±500		±100	±250	µV
P Package			1	2		0.5	1				mV
U Package			1	3							mV
Over Specified Temperature											
M Package			±550			±250	±1000		±200	±500	µV
P, U Packages			±1.5			±0.75	±1.5				mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		*	±15		±3	±5		*	±2	µV/°C
Supply Rejection	$\pm V_S$ = 12V to 18V	70	*		80	100		86	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±2	±10		±1	±2		±0.5	±1	pA
Over Specified Temperature			±20	±500		±20	±200		±10	±100	pA
SM Grade						±200	±2000				pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		1	10		0.5	2		0.5	1	pA
Over Specified Temperature			20	500		20	200		10	100	pA
SM Grade						200	1000				pA
INPUT IMPEDANCE											
Differential			*			10^{13} ‖ 1			*		Ω ‖ pF
Common-Mode			*			10^{14} ‖ 3			*		Ω ‖ pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		*	*		±10.2	+13, –11		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	75	*		88	100		92	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 1k\Omega$	75	*		88	100		92	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	3.5	*		4	6.5		5	*		MHz
Full Power Response	20Vp-p, R_L = 1kΩ		*			570			*		kHz
Slew Rate	V_O = ±10V, R_L = 1kΩ	20	*		24	35		28	*		V/µs
Settling Time: 0.1%	Gain = –1, R_L = 1kΩ		*			0.6			*		µs
0.01%	C_L = 500pF, 10V Step		*			1.0			*		µs
RATED OUTPUT											
Voltage Output	R_L = 1kΩ	±11	*		±11.5	+12.9, –13.8		*	*		V
Current Output	V_O = ±10VDC	*	*		±15	±20		*	*		mA
Output Resistance	1MHz, Open Loop		*			80			*		Ω
Load Capacitance Stability	Gain = +1		*			1500			*		pF
Short Circuit Current		±25	*		±30	±50		*	*		mA
POWER SUPPLY											
Rated Voltage			*			±15			*		VDC
Voltage Range, Derated Performance		*		*	±5		±18	*		*	VDC
Current, Quiescent	I_O = 0mADC		*	*		3	4		*	*	mA
Over Specified Temperature			*	*		3.5	4.5		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient Temperature	*		*	–25		+85	*		*	°C
SM Grade					–55		+125				°C
Operating: M Package	Ambient Temperature	*		*	–55		+125	*		*	°C
P, U Packages		–25		+85	–25		+85				°C
Storage: M Package	Ambient Temperature	*		*	–65		+150	*		*	°C
P, U Packages		–40		+125	–40		+125				°C
θ_{JA}			*			200			*		°C/W

* Same specifications as OPA602BM.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Internal Power Dissipation ($T_J \leq +175°C$)	1000mW
Differential Input Voltage	Total V_S
Input Voltage Range	$\pm V_S$
Storage Temperature Range	
M Package	–65°C to +150°C
P and U Packages	–40°C to +125°C
Operating Temperature Range	
M Package	–55°C to +125°C
P and U Packages	–25°C to + 85°C
Lead Temperature	
M and P Packages (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA602AM	TO-99	001
OPA602BM	TO-99	001
OPA602CM	TO-99	001
OPA602SM	TO-99	001
OPA602AP	Plastic DIP	006
OPA602BP	Plastic DIP	006
OPA602AU	Plastic SOIC	182

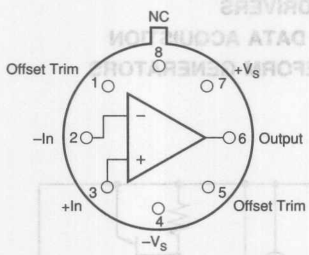
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (μV) AT 25°C
OPA602AM	TO-99	–25 to +85°C	±1000
OPA602BM	TO-99	–25 to +85°C	±500
OPA602CM	TO-99	–25 to +85°C	±250
OPA602SM	TO-99	–55 to +125°C	±500
OPA602AP	Plastic DIP	–25 to +85°C	±2000
OPA602BP	Plastic DIP	–25 to +85°C	±1000
OPA602AU	Plastic SOIC	–25 to +85°C	±3000

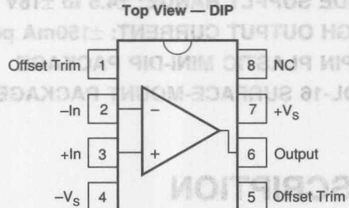
PIN CONFIGURATIONS

Top View — TO-99

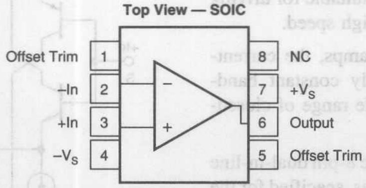


Case Connected to $+V_S$.

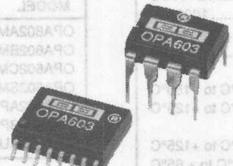
Top View — DIP



Top View — SOIC



BURR - BROWN®



OPA603

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11026

High Speed, Current-Feedback OPERATIONAL AMPLIFIER

FEATURES

- BANDWIDTH: 100MHz, G = 1 to 10
- SLEW RATE: 1000V/μs
- FAST SETTLING TIME: 50ns to 0.1%
- WIDE SUPPLY RANGE: ±4.5 to ±18V
- HIGH OUTPUT CURRENT: ±150mA peak
- 8-PIN PLASTIC MINI-DIP PACKAGE
- SOL-16 SURFACE-MOUNT PACKAGE

APPLICATIONS

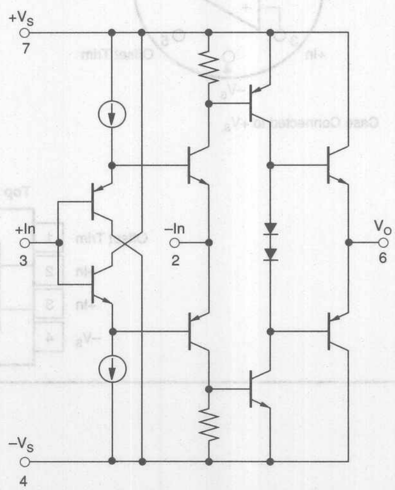
- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- SONAR, ULTRASOUND CIRCUITRY
- ATE PIN DRIVERS
- LINE DRIVERS
- FAST DATA ACQUISTION
- WAVEFORM GENERATORS

DESCRIPTION

The OPA603 is a high-speed current-feedback op amp with guaranteed specifications at both ±5V and ±15V power supplies. It can deliver full ±10V signals into 150Ω loads with up to 1000V/μs slew rate. This allows it to drive terminated 75Ω cables. With 150mA peak output current capability it is suitable for driving load capacitance or long lines at high speed.

In contrast with conventional op amps, the current-feedback approach provides nearly constant bandwidth and settling time over a wide range of closed-loop voltage gains.

The OPA603 is available in a plastic 8-pin dual-in-line and SOL-16 surface-mount packages, specified for the industrial temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

$T_A = +25°C$, $R_L = 150\Omega$ unless otherwise noted.

		OPA603AP/AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT OFFSET VOLTAGE					
Initial				5	mV
vs Temperature			8		µV/°C
vs Common-Mode Voltage	$V_{CM} = \pm10V$	50	60		dB
vs Supply (tracking) Voltage	$V_S = \pm12V$ to $\pm18V$	80	85		dB
vs Supply (non-tracking)(1)	$\lvert V_S\rvert = 12V$ to $18V$	55	60		dB
+INPUT BIAS CURRENT					
Initial				5	µA
vs Temperature			30		nA/°C
vs Common-Mode	$V_{CM} = \pm10V$		200	500	nA/V
vs Supply (tracking)	$V_S = \pm12V$ to $\pm18V$		50	100	nA/V
vs Supply (non-tracking)(1)	$\lvert V_S\rvert = 12V$ to $18V$		150	300	nA/V
–INPUT BIAS CURRENT					
Initial				25	µA
vs Temperature			300		nA/°C
vs Common-Mode	$V_{CM} = \pm10V$		200	600	nA/V
vs Supply (tracking)	$V_S = \pm12V$ to $\pm18V$		300	500	nA/V
vs Supply (non-tracking)(1)	$\lvert V_S\rvert = 12V$ to $18V$		1500	2000	nA/V
INPUT IMPEDANCE					
+Input			5 || 2		MΩ || pF
–Input			30 || 2		Ω || pF
OPEN LOOP CHARACTERISTICS					
Transresistance	$V_O = \pm10V$	300	440		kΩ
Transcapacitance			1.8		pF
OUTPUT CHARACTERISTICS					
Voltage	$R_L = 150\Omega$	±10	±12		V
Peak Current			150		mA
Short-Circuit Current(2)	$V_O = 0V$		250		mA
Output Resistance, Open-Loop			70		Ω
FREQUENCY RESPONSE	G = +2				
Small-Signal Bandwidth(3)		70	160		MHz
Gain Flatness, ±0.5dB		35	75		MHz
Full-Power Bandwidth	$V_O = 20Vp\text{-}p$		10		MHz
Differential Gain	f = 4.43MHz, $V_O = 1V$		0.03		%
Differential Phase	f = 4.43MHz, $V_O = 1V$		0.025		Degrees
TIME DOMAIN RESPONSE	G = +2				
Propagation Delay			10		ns
Rise and Fall Time			10		ns
Settling Time to 0.10%	10V Step		50		ns
Slew Rate			1000		V/µs
DISTORTION	G = +2, $R_L = 100\Omega$, f = 10MHz				
2nd Harmonic Distortion	$V_O = 0.2Vp\text{-}p$	–60	–65		dBc
3rd Harmonic Distortion	$V_O = 0.2Vp\text{-}p$	–70	–90		dBc
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±18	V
Current			±21	±25	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+150	°C
THERMAL RESISTANCE, $\theta_{JUNCTION\text{-}AMBIENT}$	Soldered to Printed Circuit		90		°C/W

NOTES: (1) One power supply fixed at 15V; the other supply varied from 12V to 18V. (2) Observe power derating curve. (3) See bandwidth versus gain curve, Figure 5.

SPECIFICATIONS, $V_S = \pm 5V$

ELECTRICAL

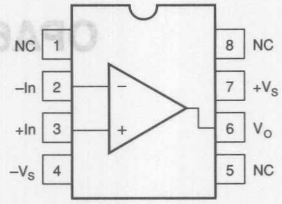
$T_A = +25°C$, $R_L = 75\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA603AP/AU MIN	TYP	MAX	UNITS
INPUT OFFSET VOLTAGE					
Initial				6	mV
vs Temperature			8		µV/°C
vs Common-Mode	$V_{CM} = \pm 3V$	50	55		dB
vs Supply (tracking)	$V_S = \pm 4V$ to $\pm 6V$	75	80		dB
vs Supply (non-tracking)(1)	$\lvert V_S \rvert = 4V$ to $6V$	55	60		dB
+INPUT BIAS CURRENT					
Initial				5	µA
vs Temperature			30		nA/°C
vs Common-Mode	$V_{CM} = \pm 3V$		350	600	nA/V
vs Supply (tracking)	$V_S = \pm 4V$ to $\pm 6V$		100	200	nA/V
vs Supply (non-tracking)(1)	$\lvert V_S \rvert = 4V$ to $6V$		200	300	nA/V
–INPUT BIAS CURRENT					
Initial				25	µA
vs Temperature			300		nA/°C
vs Common-Mode	$V_{CM} = \pm 3V$		300	600	nA/V
vs Supply (tracking)	$V_S = \pm 4V$ to $\pm 6V$		500	700	nA/V
vs Supply (non-tracking)(1)	$\lvert V_S \rvert = 4V$ to $6V$		2500	3000	nA/V
INPUT IMPEDANCE					
+Input			3.3 || 2		MΩ || pF
–Input			30 || 2		Ω || pF
OPEN LOOP CHARACTERISTICS					
Transresistance	$V_O = \pm 2V$	225	330		kΩ
Transcapacitance			2.4		pF
OUTPUT CHARACTERISTICS					
Voltage	$R_L = 75\Omega$	±2	±2.75		V
Peak Current			150		mA
Short-Circuit Current(2)	$V_O = 0V$		250		mA
Output Resistance, Open-Loop			80		Ω
FREQUENCY RESPONSE	G = +2				
Small-Signal Bandwidth(3)			140		MHz
Gain Flatness, ±0.5dB			65		MHz
Full-Power Bandwidth			20		MHz
Differential Gain	f = 4.43MHz, $V_O = 1V$, $R_L = 150\Omega$		0.03		%
Differential Phase	f = 4.43MHz, $V_O = 1V$, $R_L = 150\Omega$		0.025		Degrees
TIME DOMAIN RESPONSE	G = +2, $R_L = 100\Omega$				
Propagation Delay			15		ns
Rise and Fall Time			20		ns
Settling Time to 0.10%			60		ns
Slew Rate			750		V/µs
DISTORTION	G = +2, $R_L = 100\Omega$, f = 10MHz				
2nd Harmonic Distortion	$V_O = 0.2Vp\text{-}p$		–67		dBc
3rd Harmonic Distortion	$V_O = 0.2Vp\text{-}p$		–78		dBc
POWER SUPPLY					
Specified Operating Voltage			±5		V
Operating Voltage Range		±4.5		±18	V
Current			±21	±25	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+150	°C
THERMAL RESISTANCE, $\theta_{JUNCTION\text{-}AMBIENT}$	Soldered to Printed Circuit		90		°C/W

NOTES: (1) One power supply fixed at 5V; the other supply varied from 4V to 6V. (2) Observe power derating curve. (3) See bandwidth versus gain curves, Figure 5.

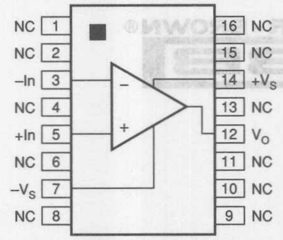
PIN CONFIGURATION

Top View — DIP



NC: No Internal Connection.
Solder to ground plane for
improved heat dissipation.

Top View — SOL-16



NC: No Internal Connection.
Solder to ground plane for
improved heat dissipation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$\pm V_S$
Differential Input Voltage	±6V
Power Dissipation	See derating curve
Operating Temperature	+100°C
Storage Temperature	+150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
(soldering SOL-16 package, 3s)	+260°C

ORDERING INFORMATION

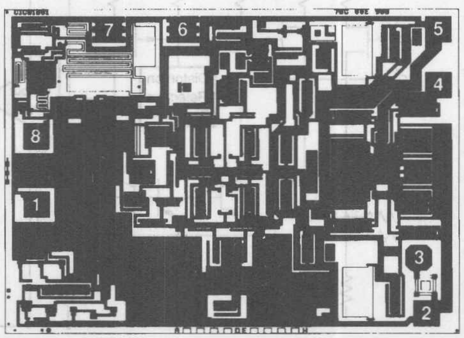
MODEL	PACKAGE	SPECIFIED TEMPERATURE RANGE
OPA603AP	Plastic DIP	–25°C to +85°C
OPA603AU	SOL-16	–25°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA603AP	Plastic DIP	006
OPA603AU	SOL-16	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

DICE INFORMATION



OPA603 DIE TOPOGRAPHY

PAD	FUNCTION
1	Noninverting Input
2	$-V_S$
3	Laser Alignment
4	V_O (Output)
5	$+V_S$
6	RT (Trim Sense Point)
7	CE (Compensation Capacitor)
8	Inverting Input

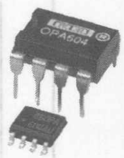
Substrate Bias: Dielectrically Isolated. Recommend tying to $+V_S$.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	94 x 69 ±5	2.39 x 1.75 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

BURR - BROWN®

OPA604



FET-Input, Low Distortion OPERATIONAL AMPLIFIER

FEATURES

- LOW DISTORTION: 0.0003% at 1kHz
- LOW NOISE: $10nV/\sqrt{Hz}$
- HIGH SLEW RATE: 25V/µs
- WIDE GAIN-BANDWIDTH: 20MHz
- UNITY-GAIN STABLE
- WIDE SUPPLY RANGE: $V_S = \pm 4.5$ to $\pm 24V$
- DRIVES 600Ω LOAD
- DUAL VERSION AVAILABLE (OPA2604)

APPLICATIONS

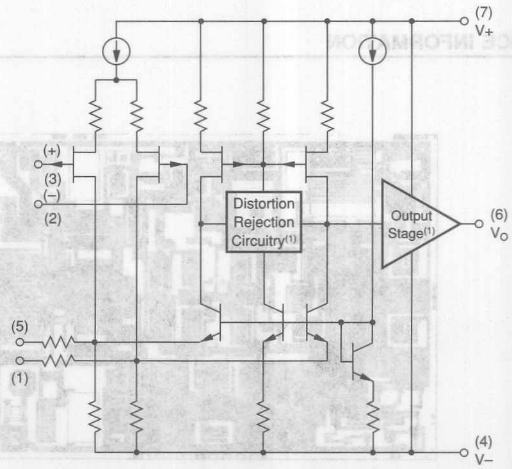
- PROFESSIONAL AUDIO EQUIPMENT
- PCM DAC I/V CONVERTER
- SPECTRAL ANALYSIS EQUIPMENT
- ACTIVE FILTERS
- TRANSDUCER AMPLIFIER
- DATA ACQUISITION

DESCRIPTION

The OPA604 is a FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio and other applications requiring excellent dynamic performance.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

The OPA604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the –25°C to +85°C temperature range.



NOTE: (1) Patents Granted: #5053718, 5019789

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

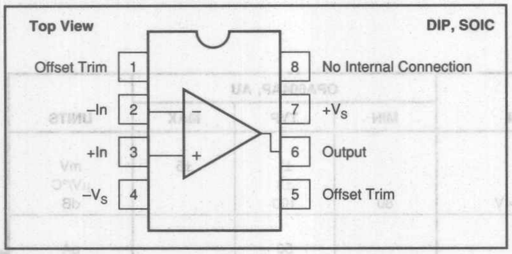
ELECTRICAL

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA604AP, AU MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±1	±5	mV
Average Drift			±8		μV/°C
Power Supply Rejection	V_S = ±5 to ±24V	80	100		dB
INPUT BIAS CURRENT[1]					
Input Bias Current	V_{CM} = 0V		50		pA
Input Offset Current	V_{CM} = 0V		±3		pA
NOISE					
Input Voltage Noise					
Noise Density: f = 10Hz			25		nV/√Hz
f = 100Hz			15		nV/√Hz
f = 1kHz			11		nV/√Hz
f = 10kHz			10		nV/√Hz
Voltage Noise, BW = 20Hz to 20kHz			1.5		μVp-p
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			4		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±12	±13		V
Common-Mode Rejection	V_{CM} = ±12V	80	100		dB
INPUT IMPEDANCE					
Differential			10^{12} || 8		Ω || pF
Common-Mode			10^{12} || 10		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	80	100		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product	G = 100		20		MHz
Slew Rate	20Vp-p, R_L = 1kΩ	15	25		V/μs
Settling Time: 0.01%	G = –1, 10V Step		1.5		μs
0.1%			1		μs
Total Harmonic Distortion + Noise (THD+N)	G = 1, f = 1kHz V_O = 3.5Vrms, R_L = 1kΩ		0.0003		%
OUTPUT					
Voltage Output	R_L = 600Ω	±11	±12		V
Current Output	V_O = ±12V		±35		mA
Short Circuit Current			±40		mA
Output Resistance, Open-Loop			25		Ω
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±24	V
Current			±5.3	±6	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+125	°C
Thermal Resistance[2], θ_{JA}			90		°C/W

NOTES: (1) Typical performance, measured fully warmed-up. (2) Soldered to circuit board—see text.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±25V
Input Voltage	(V–)–1V to (V+)+1V
Output Short Circuit to Ground	Continuous
Operating Temperature	–40°C to +100°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) AP	+300°C
Lead Temperature (soldering, 3s) AU	+260°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA604AP	8-Pin Plastic DIP	–25°C to +85°C
OPA604AU	SO-8 Surface-Mount	–25°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

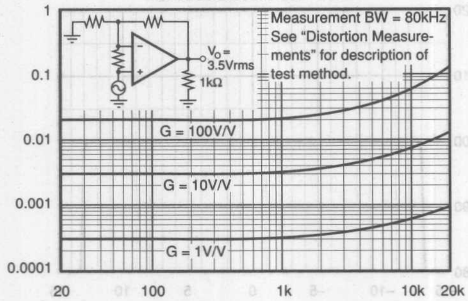
PACKAGE INFORMATION

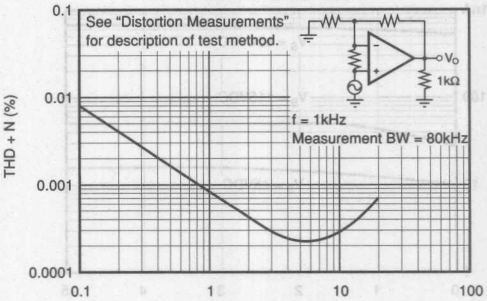
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA604AP	8-Pin Plastic DIP	006
OPA604AU	SO-8 Surface-Mount	182

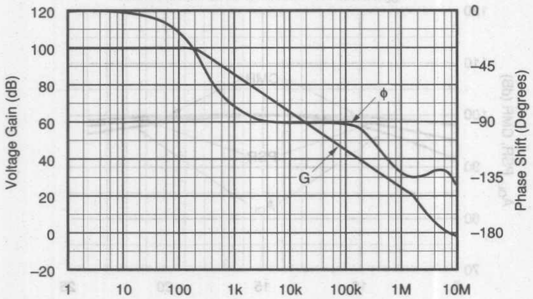
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

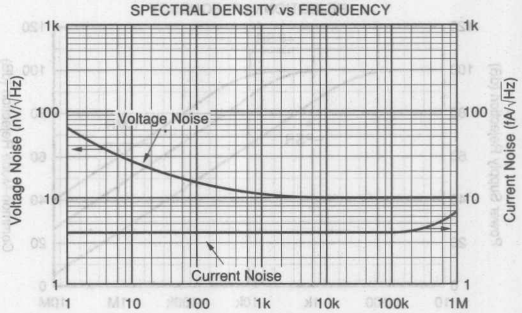
TYPICAL PERFORMANCE CURVES

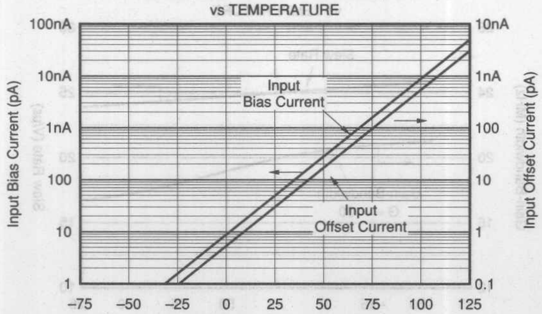
T_A = +25°C, V_S = ±15V unless otherwise noted.

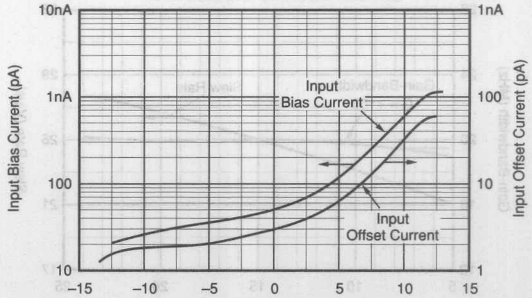




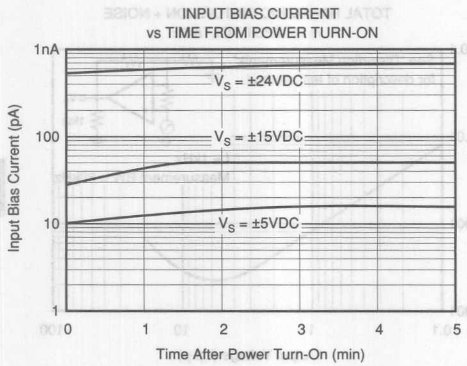


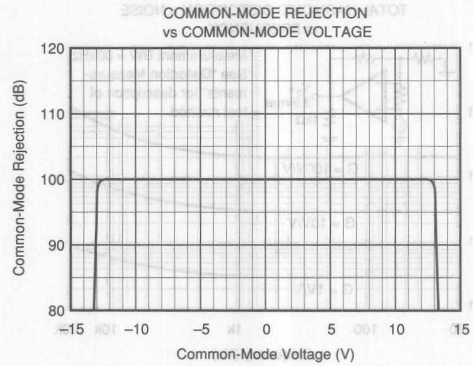


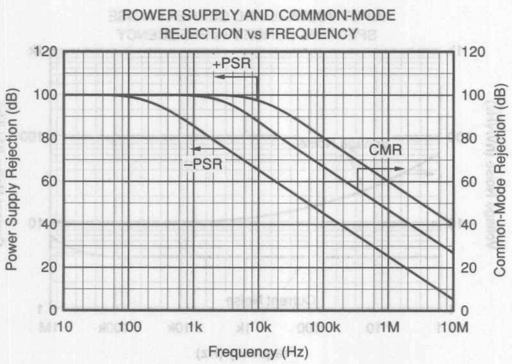


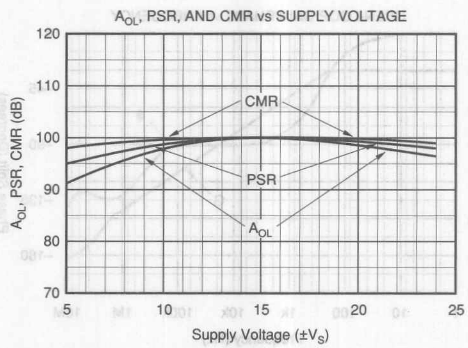


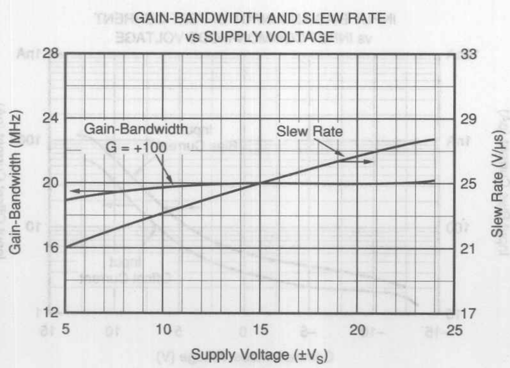
$T_A = +25°C$, $V_S = \pm15V$ unless otherwise noted.

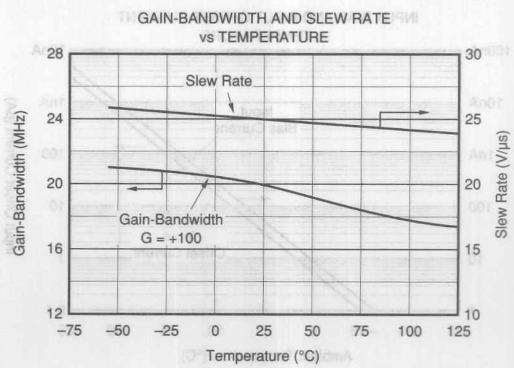




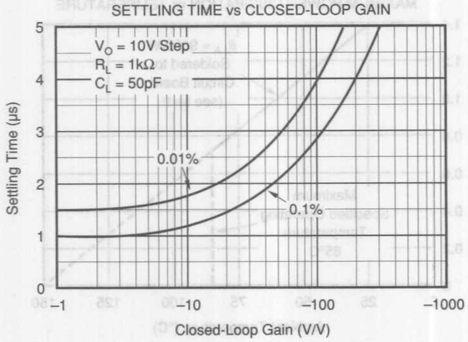




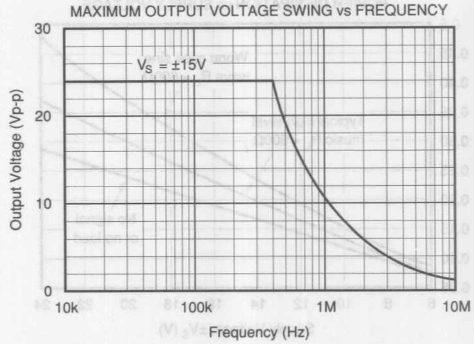




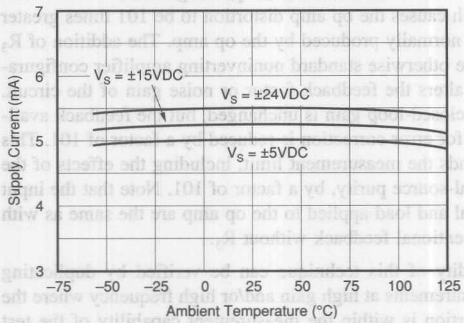
SETTLING TIME vs CLOSED-LOOP GAIN



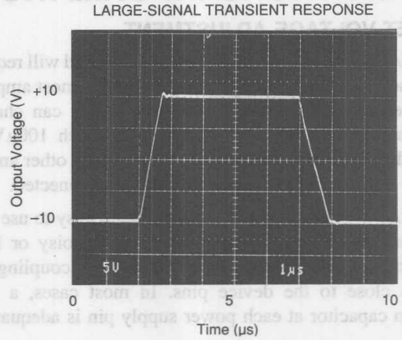
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



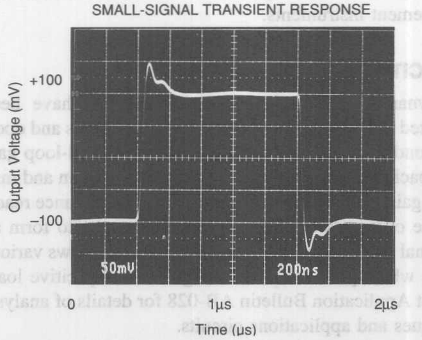
SUPPLY CURRENT vs TEMPERATURE



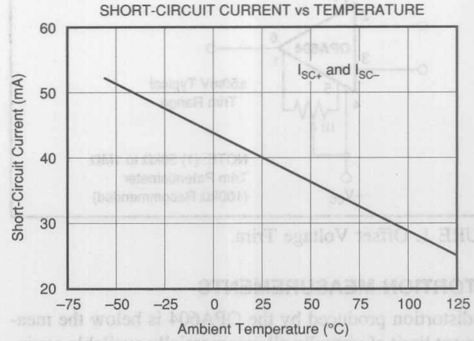
LARGE-SIGNAL TRANSIENT RESPONSE



SMALL-SIGNAL TRANSIENT RESPONSE

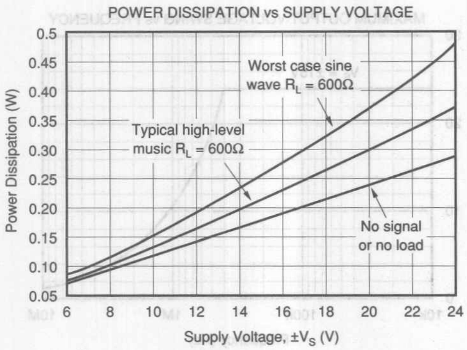


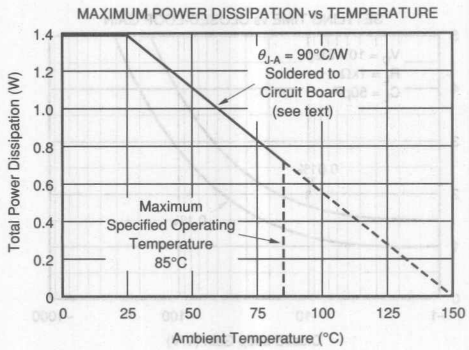
SHORT-CIRCUIT CURRENT vs TEMPERATURE



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm15V$ unless otherwise noted.





APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA604 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3µV/°C for each 100µV of adjusted offset. The OPA604 can replace many other amplifiers by leaving the external null circuit unconnected.

The OPA604 is unity-gain stable, making it easy to use in a wide range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases, a 1µF tantalum capacitor at each power supply pin is adequate.

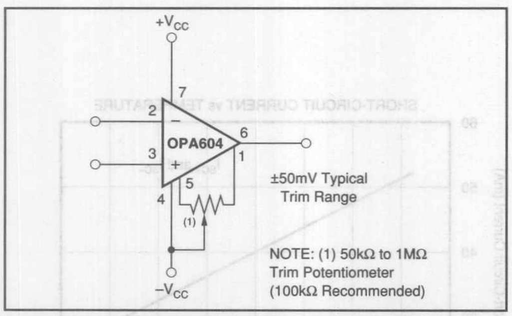


FIGURE 1. Offset Voltage Trim.

DISTORTION MEASUREMENTS

The distortion produced by the OPA604 is below the measurement limit of virtually all commercially available equipment. A special test circuit, however, can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source which can be referred to the input. Figure 2 shows a circuit which causes the op amp distortion to be 101 times greater than normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101. This extends the measurement limit, including the effects of the signal-source purity, by a factor of 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with the Audio Precision System One which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

CAPACITIVE LOADS

The dynamic characteristics of the OPA604 have been optimized for commonly encountered gains, loads and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. Figure 3 shows various circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details of analysis techniques and applications circuits.

For the unity-gain buffer, Figure 3a, stability is preserved by adding a phase-lead network, R_C and C_C. Voltage drop

across R_C will reduce output voltage swing with heavy loads. An alternate circuit, Figure 3b, does not limit the output with low load impedance. It provides a small amount of positive feedback to reduce the net feedback factor. Input impedance of this circuit falls at high frequency as op amp gain rolloff reduces the bootstrap action on the compensation network.

Figures 3c and 3d show compensation techniques for noninverting amplifiers. Like the follower circuits, the circuit in Figure 3d eliminates voltage drop due to load current, but at the penalty of somewhat reduced input impedance at high frequency.

Figures 3e and 3f show input lead compensation networks for inverting and difference amplifier configurations.

NOISE PERFORMANCE

Op amp noise is described by two parameters—noise voltage and noise current. The voltage noise determines the noise performance with low source impedance. Low noise bipolar-input op amps such as the OPA27 and OPA37 provide very low voltage noise. But if source impedance is greater than a few thousand ohms, the current noise of bipolar-input op amps react with the source impedance and will dominate. At a few thousand ohms source impedance and above, the OPA604 will generally provide lower noise.

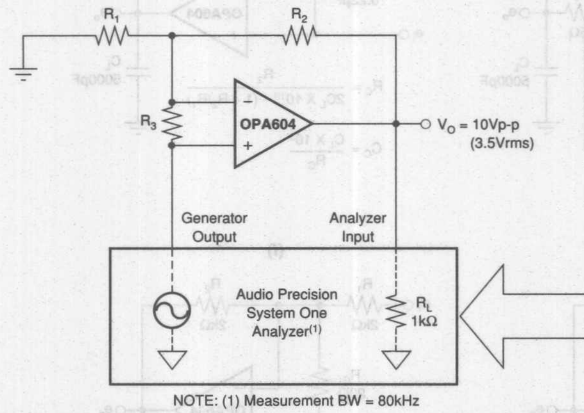
POWER DISSIPATION

The OPA604 is capable of driving a 600Ω load with power supply voltages up to ±24V. Internal power dissipation is increased when operating at high power supply voltage. The typical performance curve, Power Dissipation vs Power Supply Voltage, shows quiescent dissipation (no signal or no load) as well as dissipation with a worst case continuous sine wave. Continuous high-level music signals typically produce dissipation significantly less than worst case sine waves.

Copper leadframe construction used in the OPA604 improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately ±40mA at 25°C. The limit current decreases with increasing temperature as shown in the typical curves.



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	5kΩ	50Ω
10	101	500Ω	5kΩ	500Ω
100	101	50Ω	5kΩ	∞

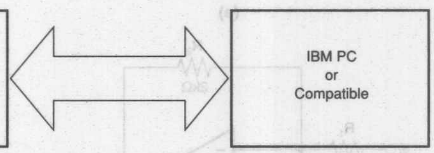
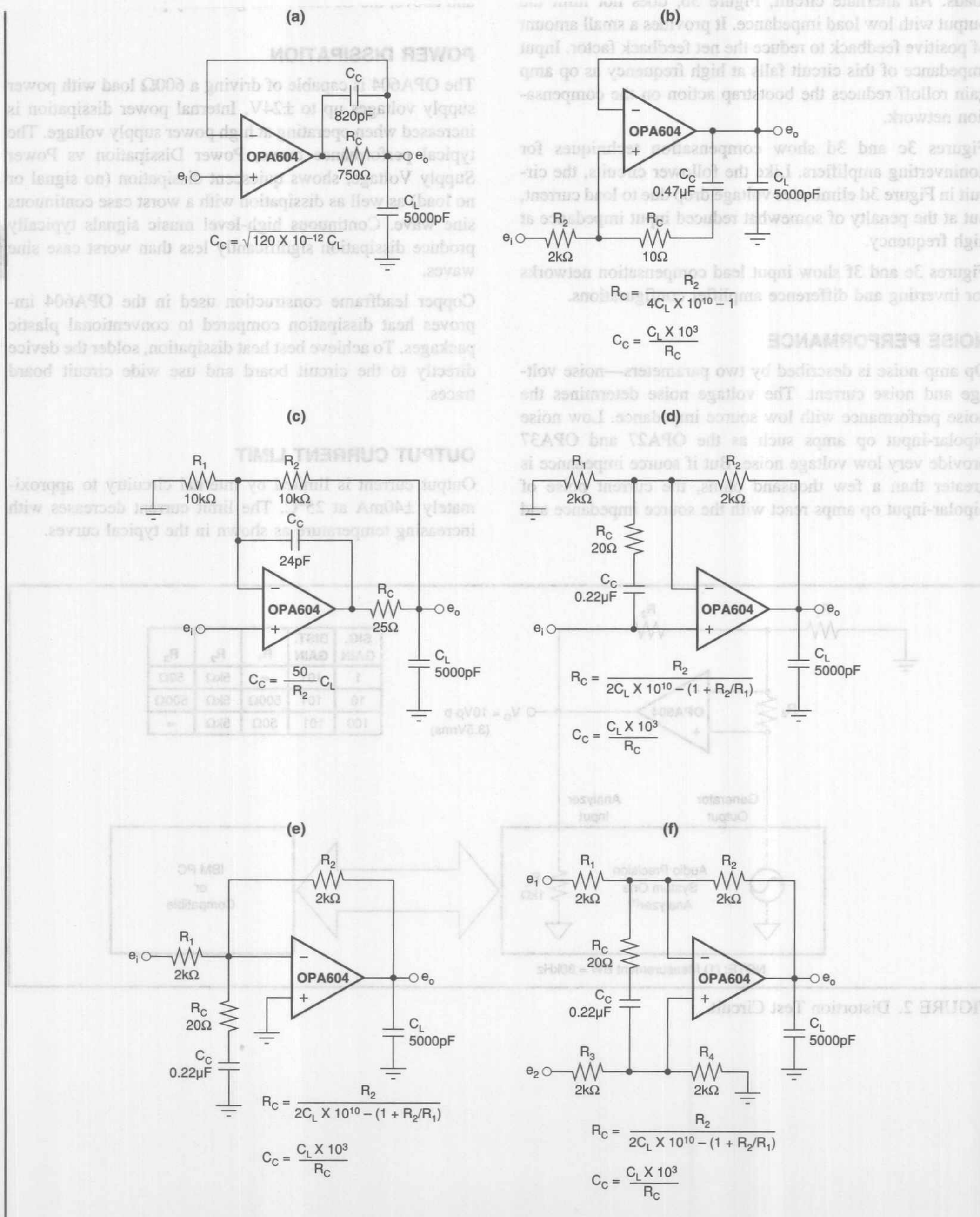


FIGURE 2. Distortion Test Circuit.



NOTE: Design equations and component values are approximate. User adjustment is required for optimum performance.

FIGURE 3. Driving Large Capacitive Loads.

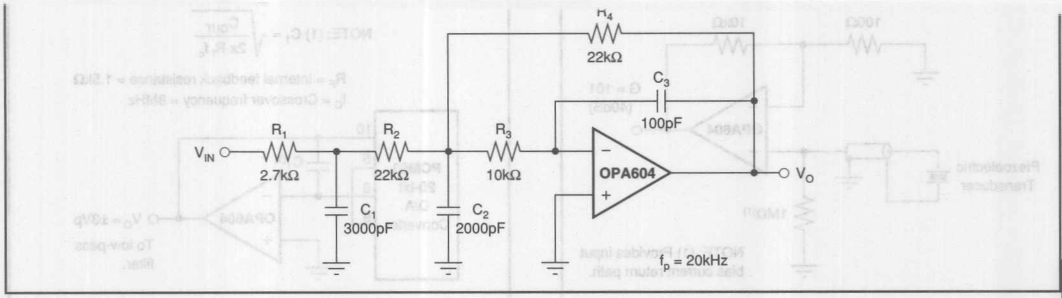


FIGURE 4. Three-Pole Low-Pass Filter.

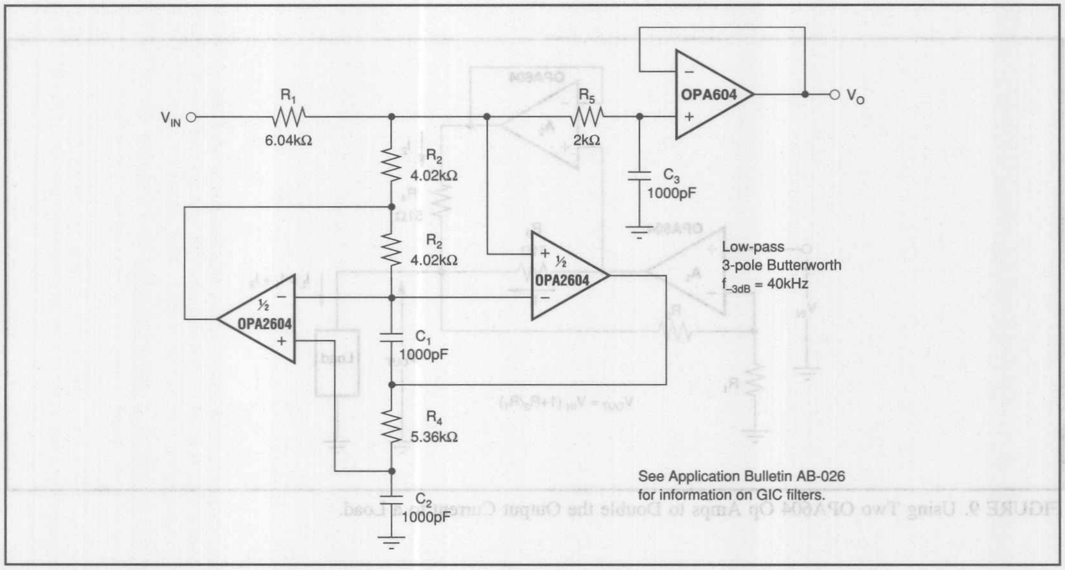


FIGURE 5. Three-Pole Generalized Immittance Converter (GIC) Low-Pass Filter.

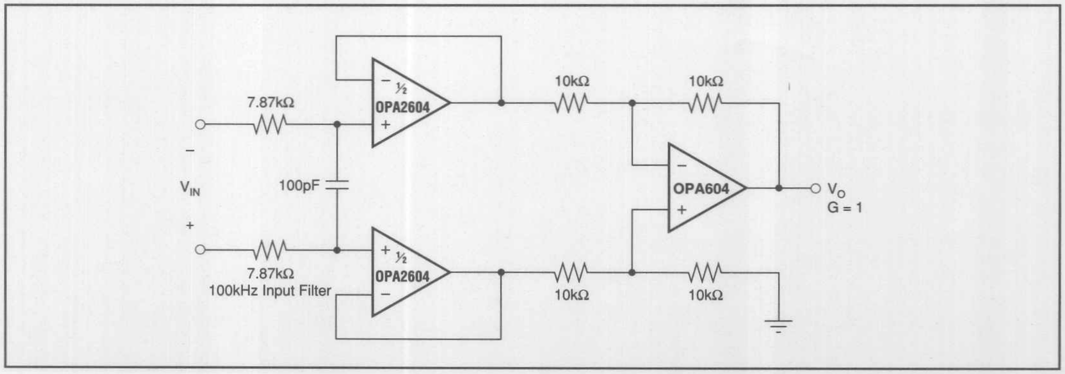


FIGURE 6. Differential Amplifier with Low-Pass Filter.

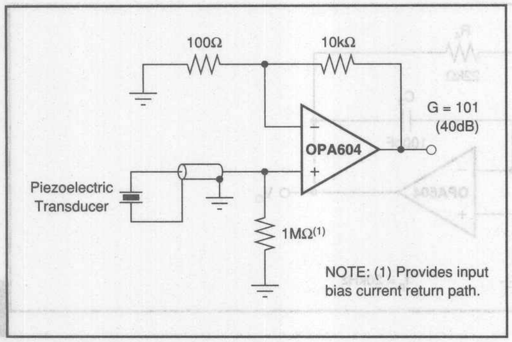


FIGURE 7. High Impedance Amplifier.

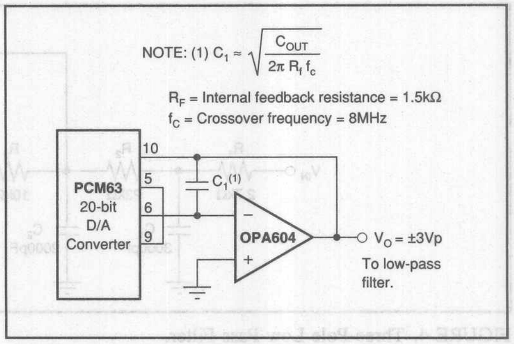


FIGURE 8. Digital Audio DAC I-V Amplifier.

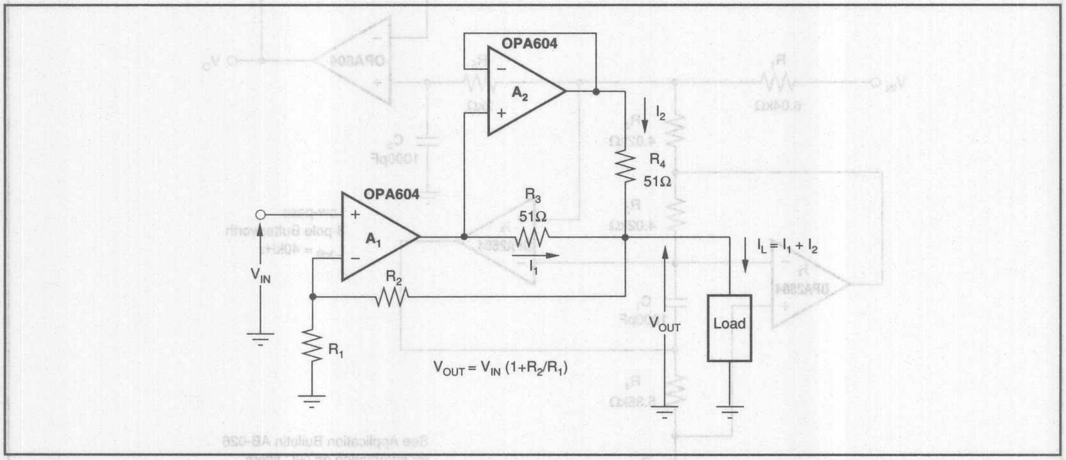


FIGURE 9. Using Two OPA604 Op Amps to Double the Output Current to a Load.

SOUND QUALITY

The following discussion is provided, recognizing that not all measured performance behavior explains or correlates with listening tests by audio experts. The design of the OPA604 included consideration of both objective performance measurements, as well as an awareness of widely held theory on the success and failure of previous op amp designs.

SOUND QUALITY

The sound quality of an op amp is often the crucial selection criteria—even when a data sheet claims exceptional distortion performance. By its nature, sound quality is subjective. Furthermore, results of listening tests can vary depending on application and circuit configuration. Even experienced listeners in controlled tests often reach different conclusions.

Many audio experts believe that the sound quality of a high performance FET op amp is superior to that of bipolar op amps. A possible reason for this is that bipolar designs generate greater odd-order harmonics than FETs. To the human ear, odd-order harmonics have long been identified as sounding more unpleasant than even-order harmonics. FETs, like vacuum tubes, have a square-law I-V transfer function which is more linear than the exponential transfer function of a bipolar transistor. As a direct result of this square-law characteristic, FETs produce predominantly even-order harmonics. Figure 10 shows the transfer function of a bipolar transistor and FET. Fourier transformation of both transfer functions reveals the lower odd-order harmonics of the FET amplifier stage.

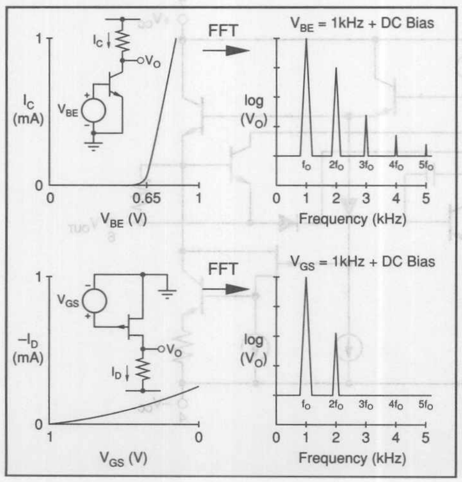
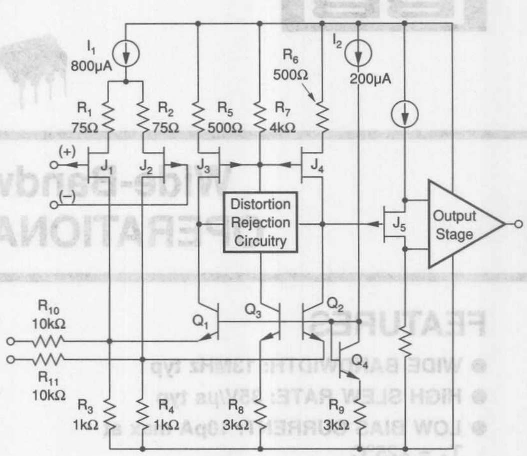


FIGURE 10. I-V and Spectral Response of NPN and JFET.



THE OPA604 DESIGN

The OPA604 uses FETs throughout the signal path, including the input stage, input-stage load, and the important phase-splitting section of the output stage. Bipolar transistors are used where their attributes, such as current capability are important, and where their transfer characteristics have minimal impact.

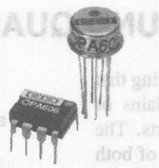
The topology consists of a single folded-cascode gain stage followed by a unity-gain output stage. Differential input transistors J_1 and J_2 are special large-geometry, P-channel JFETs. Input stage current is a relatively high 800μA, providing high transconductance and reducing voltage noise. Laser trimming of stage currents and careful attention to symmetry yields a nearly symmetrical slew rate of ±25V/μs.

The JFET input stage holds input bias current to approximately 50pA or roughly 3000 times lower than common bipolar-input audio op amps. This dramatically reduces noise with high-impedance circuitry.

The drains of J_1 and J_2 are cascoded by Q_1 and Q_2, driving the input stage loads, FETs J_3 and J_4. Distortion reduction circuitry (patented) linearizes the open-loop response and increases voltage gain. The 20MHz bandwidth of the OPA604 further reduces distortion through the user-connected feedback loop.

The output stage consists of a JFET phase-splitter loaded into high speed all-NPN output drivers. Output transistors are biased by a special circuit to prevent cutoff, even with full output swing into 600Ω loads.

BURR - BROWN®



OPA606

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10598

Wide-Bandwidth *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 13MHz typ
- HIGH SLEW RATE: 35V/µs typ
- LOW BIAS CURRENT: 10pA max at T_A = +25°C
- LOW OFFSET VOLTAGE: 500µV max
- LOW DISTORTION: 0.0035% typ at 10kHz

APPLICATIONS

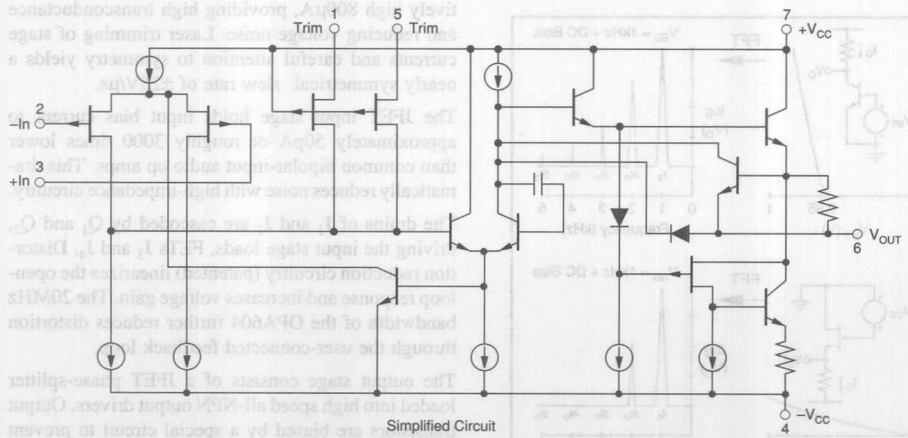
- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- AUDIO AMPLIFIERS

DESCRIPTION

The OPA606 is a wide-bandwidth monolithic dielectrically-isolated FET (*Difet*®) operational amplifier featuring a wider bandwidth and lower bias current than BIFET® LF156A amplifiers. Bias current is specified under warmed-up and operating conditions, as opposed to a junction temperature of +25°C.

Laser-trimmed thin-film resistors offer improved offset voltage and noise performance.

The OPA606 is internally compensated for unity-gain stability.



Simplified Circuit

Difet®; Burr-Brown Corp.

BIFET®; National Semiconductor Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA606KM MIN	OPA606KM TYP	OPA606KM MAX	OPA606LM MIN	OPA606LM TYP	OPA606LM MAX	OPA606KP MIN	OPA606KP TYP	OPA606KP MAX	UNITS
FREQUENCY RESPONSE											
Gain Bandwidth	Small Signal	10	12.5		11	13		9	12		MHz
Full Power Response	20Vp-p, R_L = 2kΩ		515			550			470		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	22	33		25	35		20	30		V/µs
Settling Time(1): 0.1%	Gain = –1, R_L = 2kΩ		1.0			1.0			1.0		µs
0.01%	10V Step		2.1			2.1			2.1		µs
Total Harmonic Distortion	G = +1, 20Vp-p, R_L = 2kΩ, f = 10kHz		0.0035			0.0035			0.0035		%
INPUT OFFSET VOLTAGE(2)											
Input Offset Voltage	V_{CM} = 0VDC		±180	±1.5mV		±100	±500		±300	±3mV	µV
Average Drift	T_A = T_{MIN} to T_{MAX}		±5			±3	±5		±10		µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	82	100		90	104		80	90		dB
			±10	±79		±6	±32		±32	±100	µV/V
BIAS CURRENT(2)											
Input Bias Current	V_{CM} = 0VDC		±7	±15		±5	±10		±8	±25	pA
OFFSET CURRENT(2)											
Input Offset Current	V_{CM} = 0VDC		±0.6	±10		±0.4	±5		±1	±15	pA
NOISE											
Voltage, f_O = 10Hz	100% tested (L)		37			30	40		37		nV/√Hz
100Hz	100% tested (L)		21			20	28		21		nV/√Hz
1kHz	100% tested (L)		14			13	16		14		nV/√Hz
10kHz	(3)		12			11	13		12		nV/√Hz
20kHz	(3)		11			10.5	13		11		nV/√Hz
f_B = 10Hz to 10kHz	(3)		1.3			1.2	1.5		1.3		µVrms
Current, f_O = 0.1Hz thru 20kHz	(3)		1.5			1.3	2		1.7		fA/√Hz
IMPEDANCE											
Differential			10^{13} ∥ 1			10^{13} ∥ 1			10^{13} ∥ 1		Ω ∥ pF
Common-Mode			10^{14} ∥ 3			10^{14} ∥ 3			10^{14} ∥ 3		Ω ∥ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10.5	±11.5		±11	±11.6		±10.2	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	80	95		85	96		78	90		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	95	115		100	118		90	110		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11	±12.2		±12	±12.6		±11	±12		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, Open Loop		40			40			40		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	20		10	20		10	20		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		6.5	9.5		6.2	9		6.5	10	mA
TEMPERATURE RANGE											
Specification	Ambient Temperature KM, KP, LM	0		+70	0		+70	0		+70	°C
Operating	Ambient Temperature	–55		+125	–55		+125	–40		+85	°C
θ_{JA}			200			200			155		°C/W

NOTES: (1) See settling time test circuit in Figure 2. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Sample tested–this parameter is guaranteed on L grade only.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

		OPA606KM			OPA606LM			OPA606KP			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TEMPERATURE RANGE											
Specification Range	Ambient Temp.	0		+70	0		+70	0		+70	°C
INPUT OFFSET VOLTAGE(1)											
Input Offset Voltage	V_{CM} = 0VDC		±400	±2mV		±335	±750		±750	±3.5mV	μV
Average Drift			±5			±3	±5		±10		μV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	80	98		85	100		78	95		dB
			±13	±100		±10	±56		±18	±126	μV/V
BIAS CURRENT(1)											
Input Bias Current	V_{CM} = 0VDC		±158	±339		±113	±226		±181	±566	pA
OFFSET CURRENT(1)											
Input Offset Current	V_{CM} = 0VDC		±14	±226		±9	±113		±23	±339	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10.4	±11.4		±10.9	±11.5		±10	±10.9		V
Common-Mode Rejection	V_{IN} = ±10VDC	78	92		82	95		75	88		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	90	106		95	112		88	104		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10.5	±12		±11.5	±12.4		±10.4	±11.8		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		6.6	10		6.4	9.5		6.6	10.5	mA

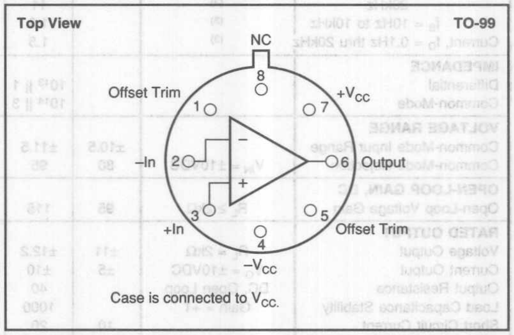
NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

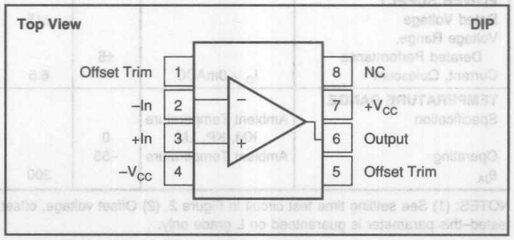
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Internal Power Dissipation (1)	500mW
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	M = –65°C to +150°C
	P = –40°C to +85°C
Operating Temperature Range	M = –55°C to +125°C
	P = –40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit Duration(3)	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{JC} = 15°C/W or θ_{JA}. (2) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to the negative supply voltage. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

CONNECTION DIAGRAMS





PACKAGE INFORMATION

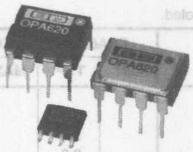
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA606KM	TO-99	001
OPA606LM	TO-99	001
OPA606KP	Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA606KM	TO-99	0°C to 70°C
OPA606LM	TO-99	0°C to 70°C
OPA606KP	Plastic DIP	0°C to 70°C

BURR - BROWN®



OPA620

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 2.3nV/√Hz
- HIGH OUTPUT CURRENT: 100mA
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH: 200MHz
- UNITY-GAIN STABLE
- LOW OFFSET VOLTAGE: ±100µV
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- 8-PIN DIP, SOIC PACKAGES

APPLICATIONS

- LOW NOISE PREAMPLIFIER
- LOW NOISE DIFFERENTIAL AMPLIFIER
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- LINE DRIVER
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- ACTIVE FILTERS

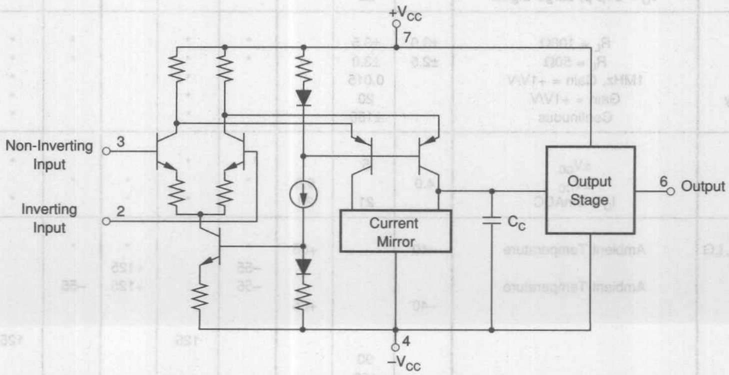
DESCRIPTION

The OPA620 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA620 is internally compensated for unity-gain stability. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA620 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short-circuit protection is provided by an internal current-limiting circuit.

The OPA620 is available in plastic, ceramic, and SOIC packages. Two temperature ranges are offered: –40°C to +85°C and –55°C to +125°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

		OPA620KP, KU, KG			OPA620SG			OPA620LG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT NOISE											
Voltage: f_O = 100Hz	R_S = 0Ω		10			*			*		nV/√Hz
f_O = 1kHz			5.5			*			*		nV/√Hz
f_O = 10kHz			3.3			*			*		nV/√Hz
f_O = 100kHz			2.5			*			*		nV/√Hz
f_O = 1MHz to 100MHz			2.3			*			*		nV/√Hz
f_B = 100Hz to 10MHz			8.0			*			*		μV, rms
Current: f_O = 10kHz to 100MHz			2.3			*			*		pA/√Hz
OFFSET VOLTAGE(1)											
Input Offset Voltage	V_{CM} = 0VDC		±200	±1mV		*	*		±100	±500	μV
Average Drift	T_A = T_{MIN} to T_{MAX}		±8			*			*		μV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	50	60		*	*		55	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		15	30		*	*		*	25	μA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	*		*	*	μA
INPUT IMPEDANCE											
Differential	Open-Loop		15 || 1			*			*		kΩ || pF
Common-Mode			1 || 1			*			*		MΩ || pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±3.0	±3.5		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	65	75		*	*		70	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	50	60		*	*		55	*		dB
	R_L = 50Ω	48	58		*	*		53	*		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth	Gain = +1V/V		300			*			*		MHz
(–3dB)	Gain = +2V/V		100			*			*		MHz
	Gain = +5V/V		40			*			*		MHz
	Gain = +10V/V		20			*			*		MHz
Gain-Bandwidth	Gain = +10V/V		200			*			*		MHz
Differential Gain	3.58MHz, G = +1V/V		0.05			*			*		%
Differential Phase	3.58MHz, G = +1V/V		0.05			*			*		Degrees
Harmonic Distortion(2)	G = +2V/V, f = 10MHz, V_O = 2Vp-p										
	Second Harmonic		–61	–50		*	*		*	*	dBc(3)
	Third Harmonic		–65	–55		*	*		*	*	dBc
Full Power Response(2)	V_O = 5Vp-p, Gain = +1V/V	11	16		*	*		*	*		MHz
	V_O = 2Vp-p, Gain = +1V/V	27	40		*	*		*	*		MHz
Slew Rate(2)	2V Step, Gain = –1V/V	175	250		*	*		*	*		V/μs
Overshoot	2V Step, Gain = –1V/V		10			*			*		%
Settling Time: 0.1%	2V Step, Gain = –1V/V		13			*			*		ns
0.01%			25			*			*		ns
Phase Margin	Gain = +1V/V		60			*			*		Degrees
Rise Time	Gain = +1V/V, 10% to 90%					*			*		
	V_O = 100mVp-p; Small Signal		2			*			*		ns
	V_O = 6Vp-p; Large Signal		22			*			*		ns
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
Output Resistance	1MHz, Gain = +1V/V		0.015			*			*		Ω
Load Capacitance Stability	Gain = +1V/V		20			*			*		pF
Short Circuit Current	Continuous		±150			*			*		mA
POWER SUPPLY											
Rated Voltage	±V_{CC}		5			*			*		VDC
Derated Performance	±V_{CC}	4.0		6.0	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		21	23		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	–40		+85	*		*	*		*	°C
SG					–55		+125				°C
Operating: KG, LG, SG	Ambient Temperature				–55		+125	–55		+125	°C
KP, KU		–40		+85							°C
θ_{JA}											
KG, LG, SG						125			125		°C/W
KP			90								°C/W
KU			100								°C/W

* Same specifications as for KP/KU.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = T_{MIN} to T_{MAX} unless noted.

		OPA620KP, KU, KG			OPA620SG			OPA620LG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	–40		+85	*		*	*		*	°C
SG					–55		+125				°C
OFFSET VOLTAGE(1)											
Average Drift	Full Temp.		±8			*			*		μV/°C
Supply Rejection	0°C to +70°C ±V_{CC} = 4.5V to 5.5V	45	60		*	*		50	*		dB
	Full Temp., ±V_{CC} = 4.5 to 5.5V	40	55		*	*		45	*		dB
BIAS CURRENT											
Input Bias Current	Full Temp., V_{CM} = 0VDC		15	40		*	*		*	35	μA
OFFSET CURRENT											
Input Offset Current	Full Temp., V_{CM} = 0VDC		0.2	5		*	*		*	*	μA
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±2.5	±3.0		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	60	75		*	*		65	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	46	60		*	*		52	*		dB
	R_L = 50Ω	44	58		*	*		50	*		dB
RATED OUTPUT											
Voltage Output	0°C to +70°C, R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	–40°C to +85°C, R_L = 100Ω	±2.75	±3.25		*	*		*	*		V
	0°C to +70°C, R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
	–40°C to +85°C, R_L = 50Ω	±2.25	±2.7		*	*		*	*		V
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		21	25		*	*		*	*	mA

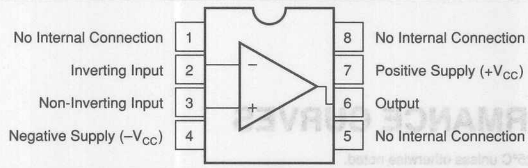
* Same specifications as for KP/KU.

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is sample tested. (3) dBc = dB referred to carrier-input signal.

PIN CONFIGURATION

Top View

8-Pin DIP
8-Pin SOIC



ORDERING INFORMATION

OPA620 ( ) ( ) (Q)

Basic Model Number
Performance Grade Code
- K, L = –40°C to +85°C
- S = –55°C to +125°C

Package Code
- G = 8-pin Ceramic DIP
- P = 8-pin Plastic DIP
- U = 8-pin Plastic SOIC

Reliability Screening
- Q = Q-Screened

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA620KP	8-Pin Plastic DIP	006
OPA620KU	8-pin Plastic SOIC	182
OPA602KG	8-pin Ceramic DIP	157
OPA620LG	8-Pin Ceramic DIP	157
OPA620SG	8-Pin Ceramic DIP	157

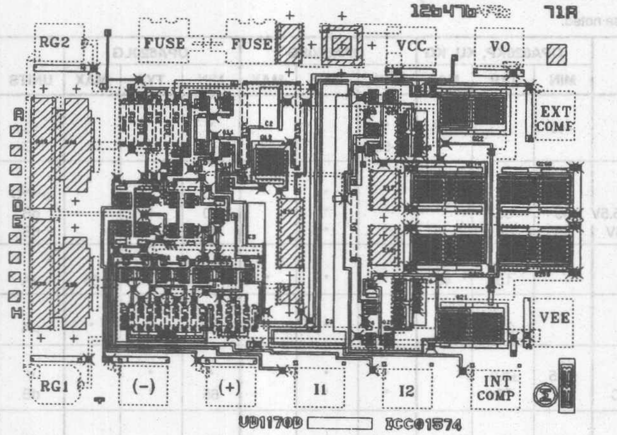
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply .... ±7VDC
Internal Power Dissipation(1) .... See Applications Information
Differential Input Voltage .... Total V_{CC}
Input Voltage Range .... See Applications Information
Storage Temperature Range: KG, LG, SG .... –65°C to +150°C
KP, KU .... –40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
(soldering, SOIC 3s) .... +260°C
Output Short Circuit to Ground (+25°C) .... Continuous to Ground
Junction Temperature (T_J) .... +175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

DICE INFORMATION



OPA620 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	NC	7	$-V_{CC}$
2	–Input	8	NC
3	+Input	9	V_{OUT}
4	NC	10	$+V_{CC}$
5	NC	11	NC
6	NC	12	NC
		13	NC

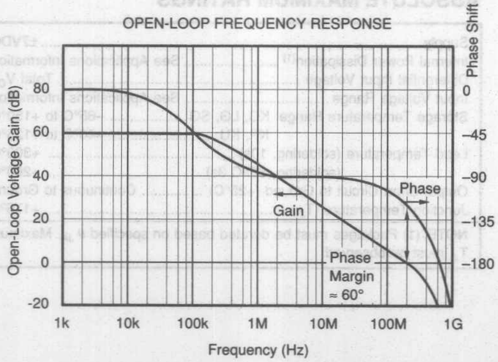
Substrate Bias: Negative Supply $-V_{CC}$.

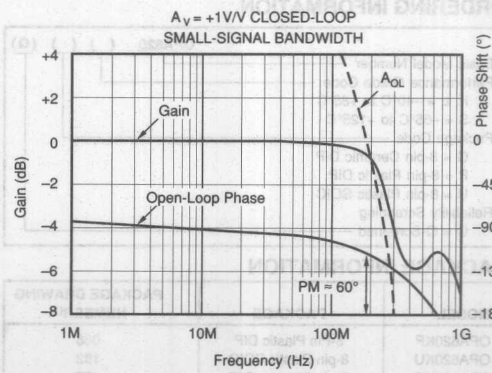
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	63 x 47 ±5	1.22 x 1.83 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold
Metalization		Gold

TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

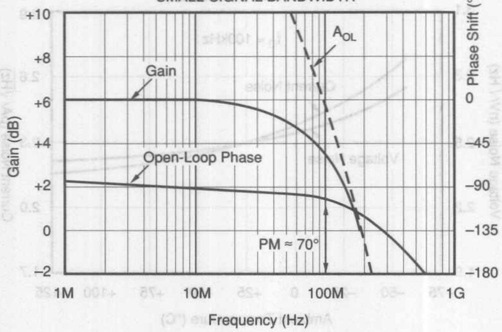




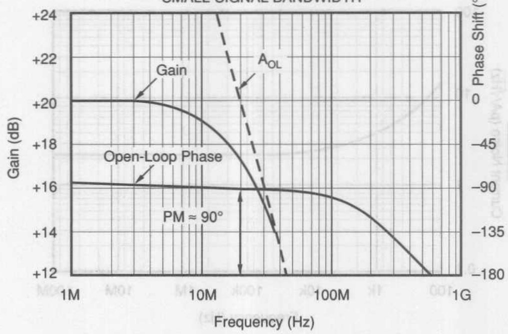
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

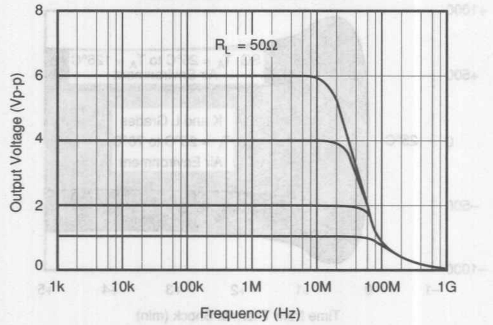
A_V = +2V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



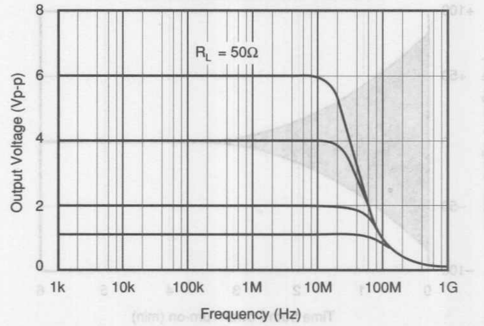
A_V = +10V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



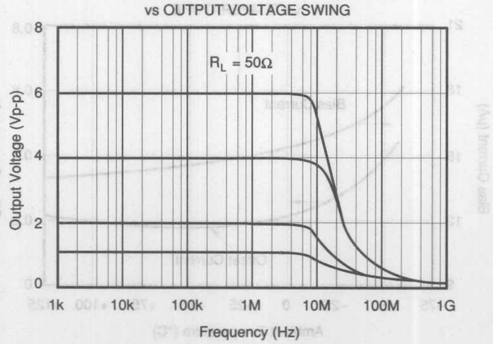
A_V = +1V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



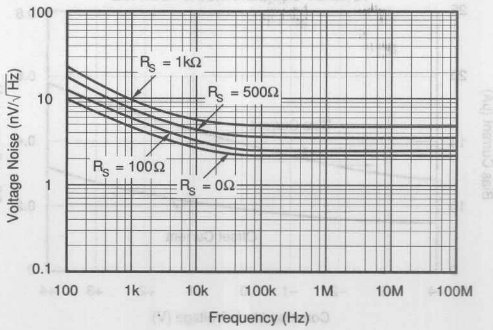
A_V = +2V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



A_V = +10V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING

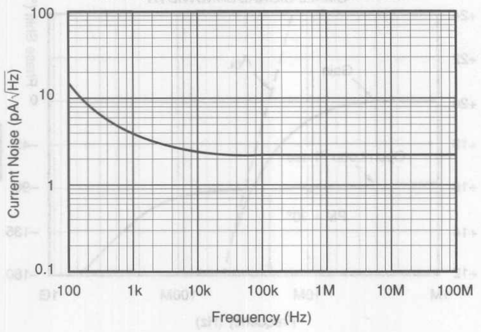


TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE

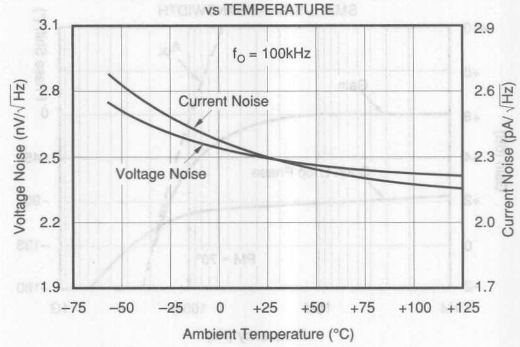


At $V_{CC} = \pm5VDC$, $R_L = 100\Omega$, and $T_A = +25°C$ unless otherwise noted.

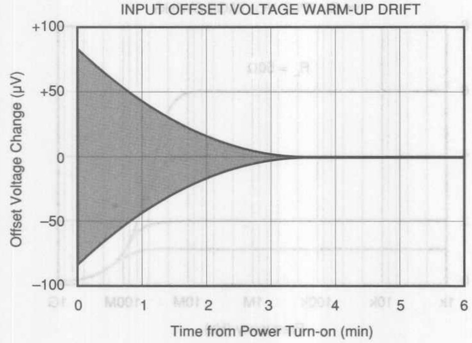
INPUT CURRENT NOISE SPECTRAL DENSITY



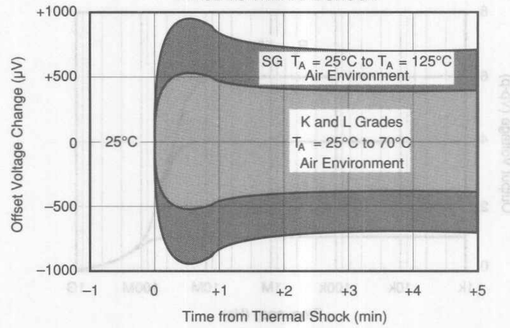
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



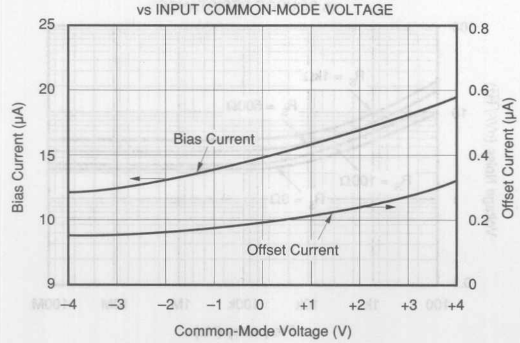
INPUT OFFSET VOLTAGE WARM-UP DRIFT



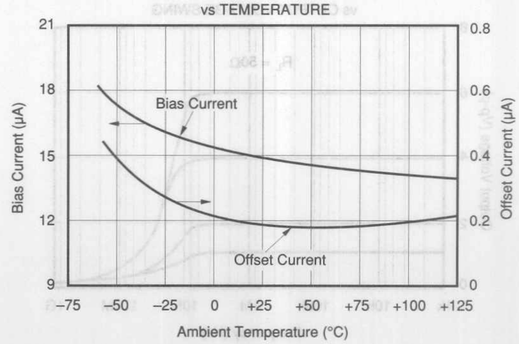
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



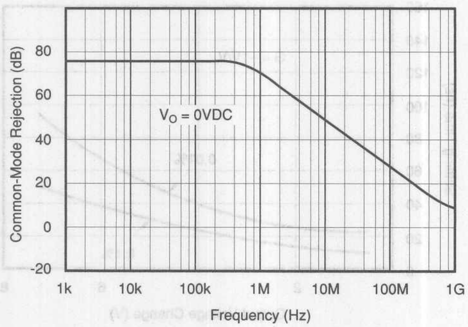
BIAS AND OFFSET CURRENT vs TEMPERATURE



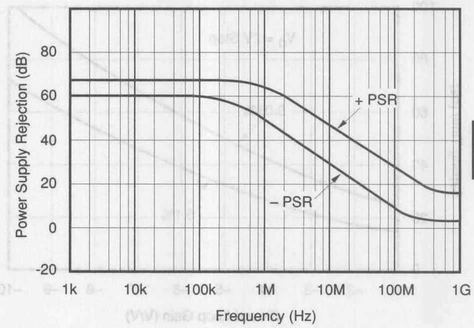
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

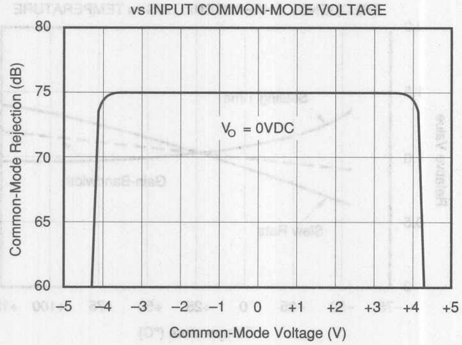
COMMON-MODE REJECTION vs FREQUENCY



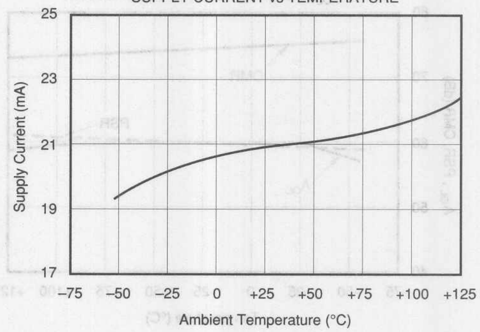
POWER SUPPLY REJECTION vs FREQUENCY



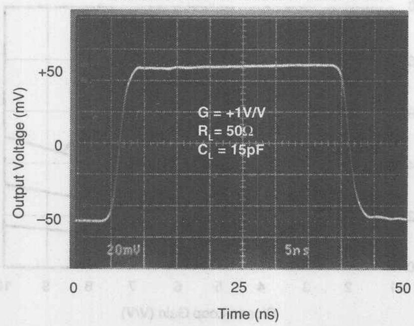
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



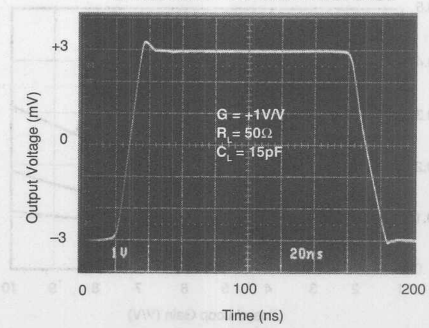
SUPPLY CURRENT vs TEMPERATURE



SMALL-SIGNAL TRANSIENT RESPONSE

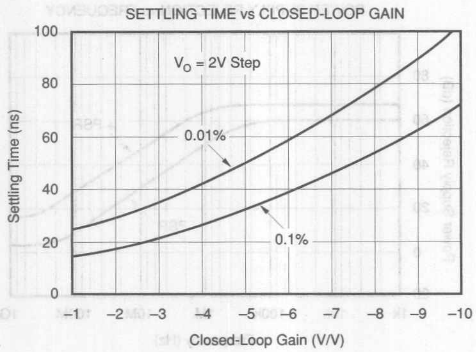


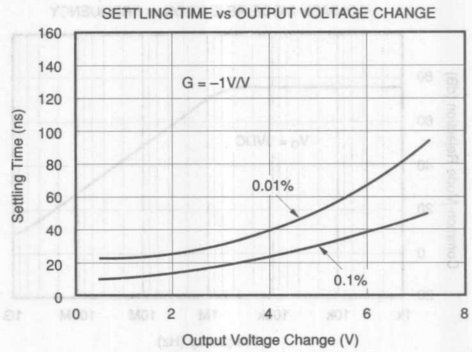
LARGE-SIGNAL TRANSIENT RESPONSE

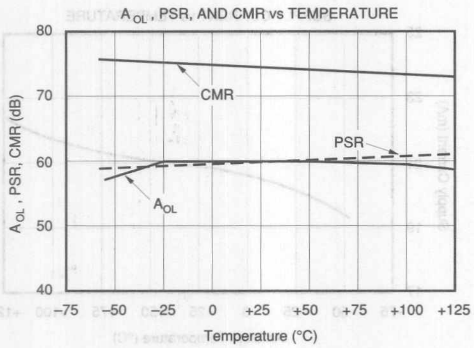


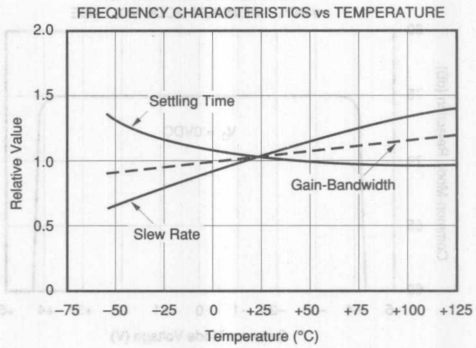
TYPICAL PERFORMANCE CURVES (CONT)

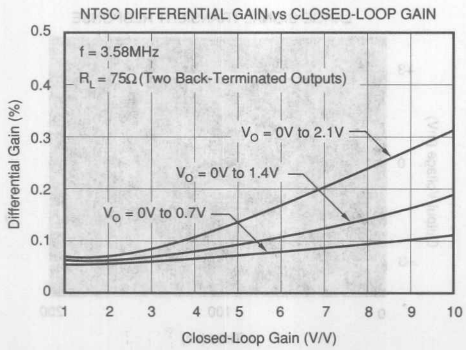
At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

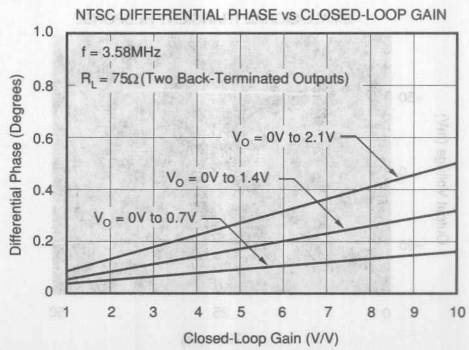








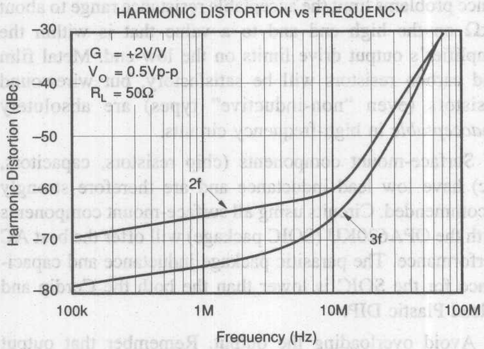




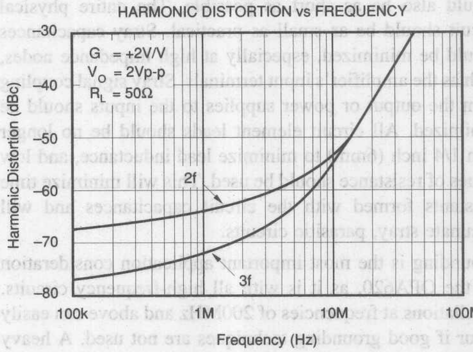
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

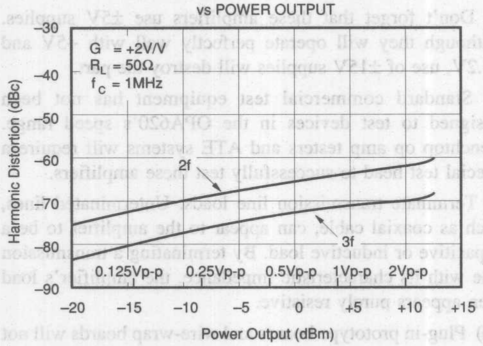
SMALL-SIGNAL HARMONIC DISTORTION vs FREQUENCY



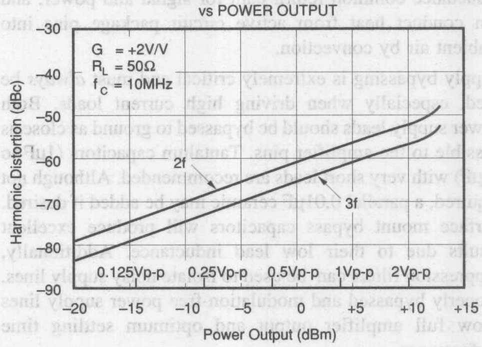
LARGE-SIGNAL HARMONIC DISTORTION vs FREQUENCY



1MHz HARMONIC DISTORTION vs POWER OUTPUT



10MHz HARMONIC DISTORTION vs POWER OUTPUT



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA620 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA620's design uses a "classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e., one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA620's "classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA620. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwidth product of 200MHz, a 0.01% settling time of 25ns, and an input offset voltage of 100µV.

WIRING PRECAUTIONS

Maximizing the OPA620's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain

high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA620, as it is with all high-frequency circuits. Oscillations at frequencies of 200MHz and above can easily occur if good grounding techniques are not used. A heavy ground plane (2 oz. copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1µF to 10µF) with very short leads are recommended. Although not required, a parallel 0.01µF ceramic may be added if desired. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

3) Whenever possible, solder the OPA620 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® stand-mount feedback components.

4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits.

5) Surface-mount components (chip resistors, capacitors, etc) have low lead inductance and are therefore strongly recommended. Circuits using all surface-mount components with the OPA620KU (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA620's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

The OPA620's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current, which is typically only 0.2µA.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA620 incorporates on-chip ESD protection diodes as shown in Figure 2.

Teflon® E. I. Du Pont de Nemours & Co.

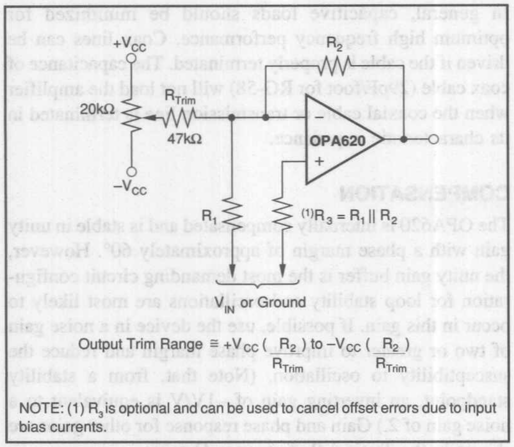


FIGURE 1. Offset Voltage Trim.

This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA620 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

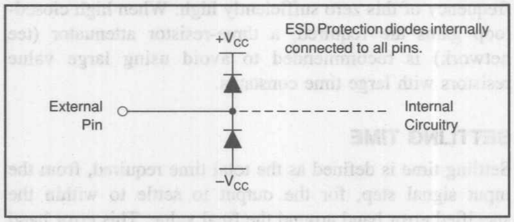


FIGURE 2. Internal ESD Protection.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA620.

OUTPUT DRIVE CAPABILITY

The OPA620's design uses large output devices and has been optimized to drive 50Ω and 75Ω resistive loads. The device can easily drive 6Vp-p into a 50Ω load. This high-output drive capability makes the OPA620 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about 150mA at 25°C. This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA620 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

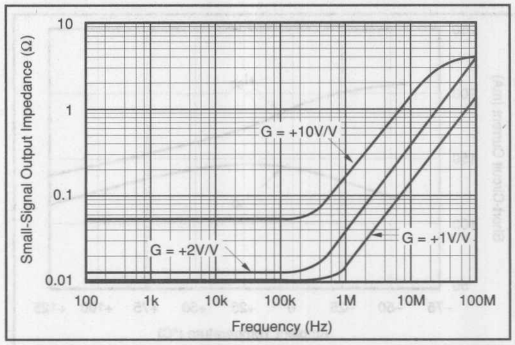


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA620 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 4.

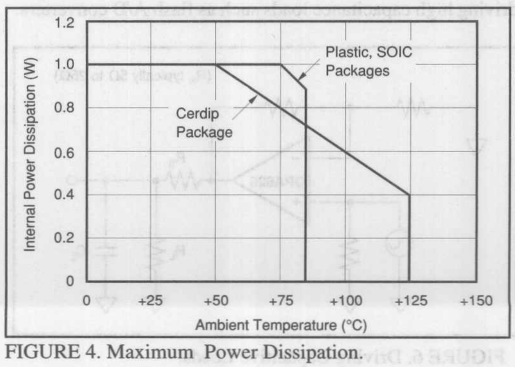


FIGURE 4. Maximum Power Dissipation.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 23mA = 230mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max $= (\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common $P_{DL} = 5V \times 150mA = 750mW$. Thus, $P_D = 230mW + 750mW \approx 1W$. Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, θ_{JA}, of each package. The variation of short-circuit current with temperature is shown in Figure 5.

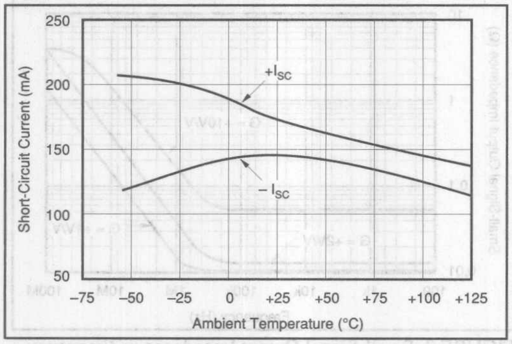


FIGURE 5. Short-Circuit Current vs Temperature.

CAPACITIVE LOADS

The OPA620's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 20pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

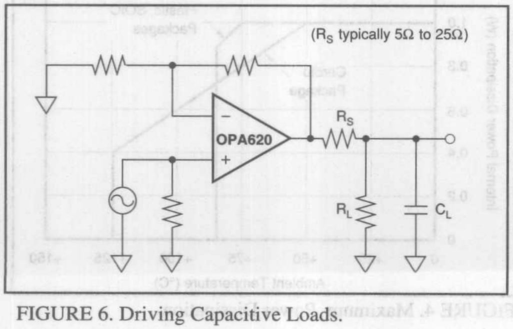


FIGURE 6. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA620 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA620 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 25ns to 0.01% for a 2V step, making the OPA620 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA620 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results, a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA620. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA620's harmonic distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Two-tone third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA620's two-tone third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA620 to operate in a gain of +2V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +40dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm

P_O = output level/tone, dBm/tone

Third IMD = third-order intermodulation ratio below each output tone, dB

For this case OPI^3P = 40dBm, P_O = 10dBm, and the third-order IMD = 2(40 – 10) = 60dB below either 10dBm tone. The OPA620's low IMD makes the device an excellent choice for a variety of RF signal processing applications.

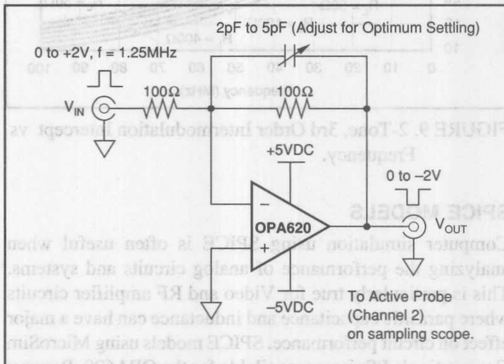


FIGURE 7. Settling Time Test Circuit.

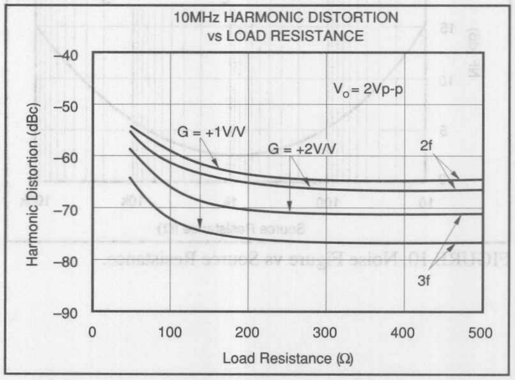


FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

NOISE FIGURE

The OPA620's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA620's Noise Figure vs Source Resistance is shown in Figure 10.

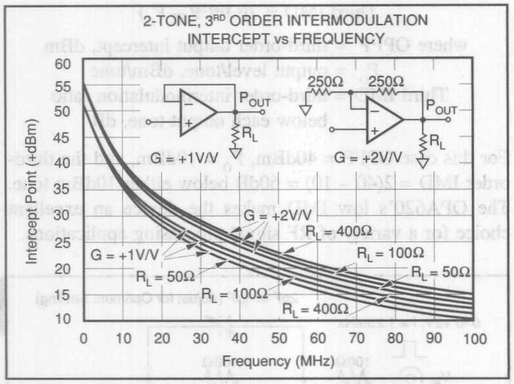


FIGURE 9. 2-Tone, 3rd Order Intermodulation Intercept vs Frequency.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA620. Request Burr-Brown Application Bulletin AB-167.

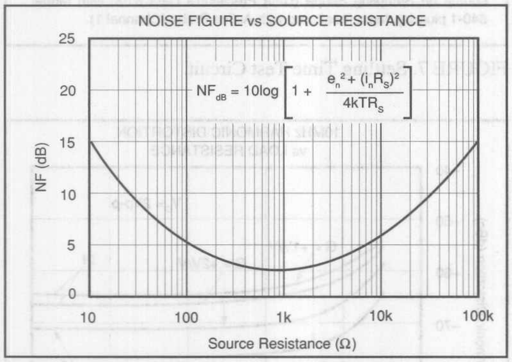


FIGURE 10. Noise Figure vs Source Resistance.

RELIABILITY DATA

Extensive reliability testing has been performed on the OPA620. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: Cerdip package = 1.31E+9 Hours, Plastic DIP = 5.02E+7 Hours, and SOIC = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 125°C, 24 hrs
Temperature Cycling	Temperature = –55°C to 125°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Hermetic Seal	Fine: He leak rate < 1 X 10 atm cc/s Gross: per Fluorocarbon bubble test
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on SG package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM1135 for 8-Pin DIP, and DEM1136 for SOIC package.

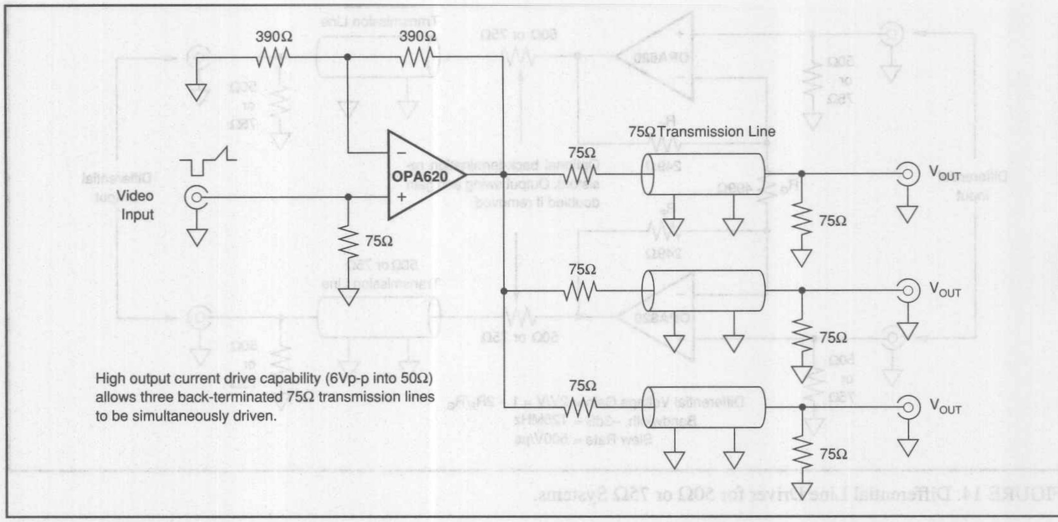


FIGURE 11. Video Distribution Amplifier.

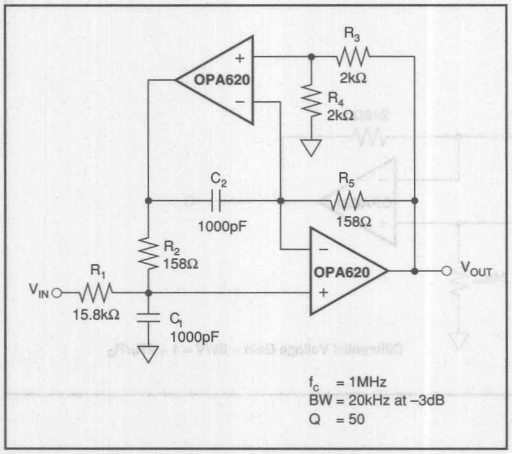


FIGURE 12. High-Q 1MHz Bandpass Filter.

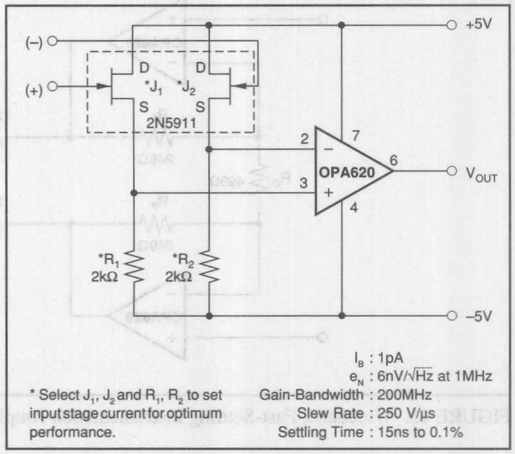


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

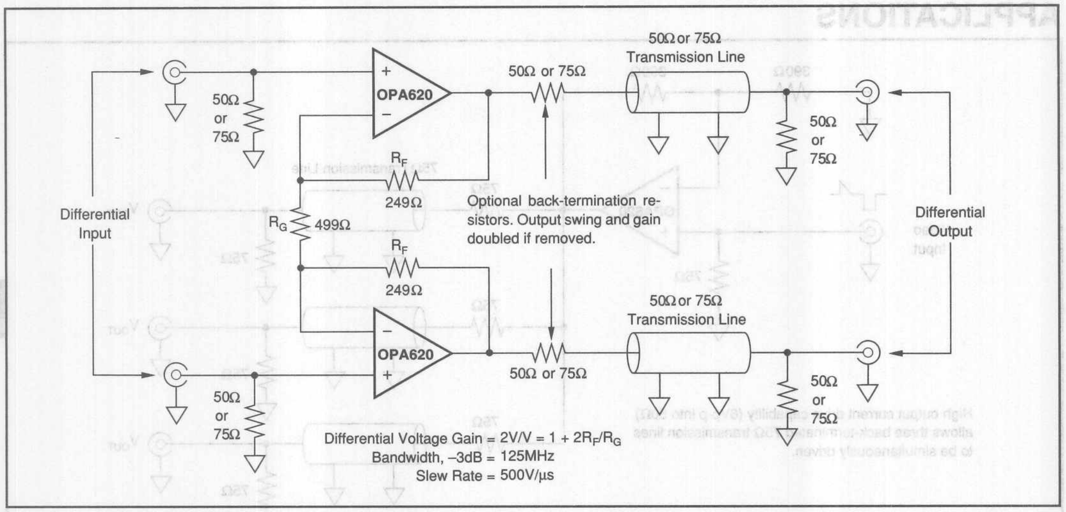


FIGURE 14. Differential Line Driver for 50Ω or 75Ω Systems.

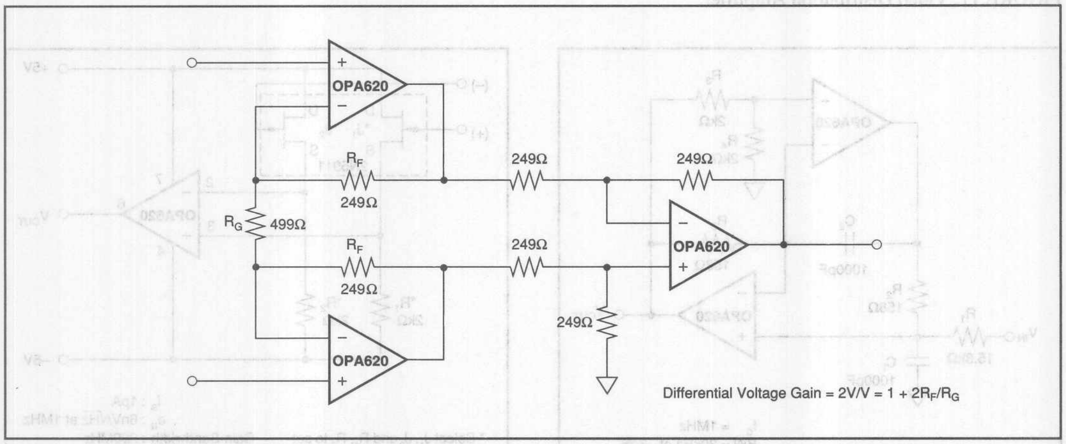


FIGURE 15. Wideband, Fast-Settling Instrumentation Amplifier.

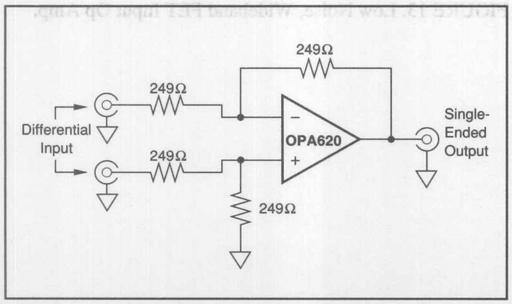


FIGURE 16. Unity Gain Difference Amplifier.

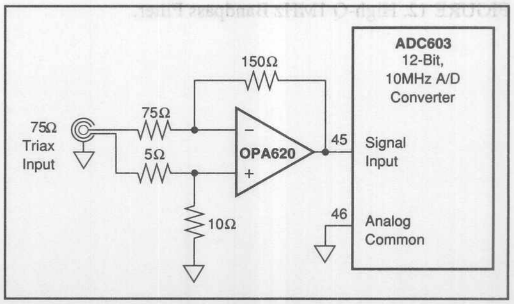
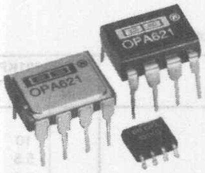


FIGURE 17. Differential Input Buffer Amplifier (G = –2V/V).

BURR - BROWN®



OPA621

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 2.3nV/√Hz
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- HIGH OUTPUT CURRENT: 150mA
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH: 500MHz
- STABLE IN GAINS: ≥ 2V/V
- LOW OFFSET VOLTAGE: ±100μV
- SLEW RATE: 500V/μs
- 8-PIN DIP, SOIC PACKAGES

APPLICATIONS

- LOW NOISE PREAMPLIFIER
- LOW NOISE DIFFERENTIAL AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LINE DRIVER
- HIGH-SPEED SIGNAL PROCESSING
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- ACTIVE FILTERS

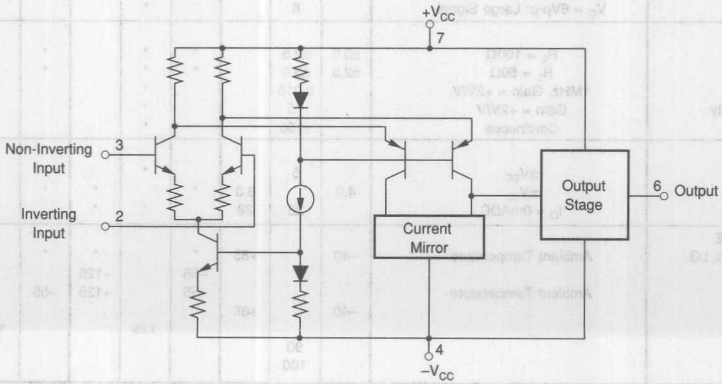
DESCRIPTION

The OPA621 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA621 is stable in gains of ±2V/V or higher. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA621 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The OPA621 is available in plastic, ceramic, and SOIC packages. Two temperature ranges are offered: –40°C to +85°C and –55°C to +125°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP, KU MIN	OPA621KP, KU TYP	OPA621KP, KU MAX	OPA621KG, SG MIN	OPA621KG, SG TYP	OPA621KG, SG MAX	OPA621LG MIN	OPA621LG TYP	OPA621LG MAX	UNITS
INPUT NOISE											
Voltage: f_O= 100Hz	R_S = 0Ω		10			*			*		nV/√Hz
f_O= 1kHz			5.5			*			*		nV/√Hz
f_O= 10kHz			3.3			*			*		nV/√Hz
f_O= 100kHz			2.5			*			*		nV/√Hz
f_O= 1MHz to 100MHz			2.3			*			*		nV/√Hz
f_B= 100Hz to 10MHz			8.0			*			*		μV, rms
Current: f_O= 10kHz to 100MHz			2.3			*			*		pA/√Hz
OFFSET VOLTAGE(1)											
Input Offset Voltage	V_{CM} = 0VDC		±200	±1mV		*	*		±100	±500	μV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±12			*			*		μV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	50	60		*	*		55	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		18	30		*	*		*	25	μA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	*		*	*	μA
INPUT IMPEDANCE											
Differential	Open-Loop		15 || 1			*			*		kΩ || pF
Common-Mode			1 || 1			*			*		MΩ || pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±3.0	±3.5		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	65	75		*	*		70	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	50	60		*	*		55	*		dB
	R_L = 50Ω	48	58		*	*		53	*		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth (–3dB)	Gain = +2V/V		500			*			*		MHz
	Gain = +5V/V		100			*			*		MHz
	Gain = +10V/V		50			*			*		MHz
Gain-Bandwidth	Gain = +10V/V		500			*			*		MHz
Differential Gain	3.58MHz, G = +2V/V		0.05			*			*		%
Differential Phase	3.58MHz, G = +2V/V		0.05			*			*		Degrees
Harmonic Distortion(2)	G = +2V/V, f = 10MHz, VO = 2Vp-p										
	f = 10MHz, Second Harmonic		–62	–50		*	*		*	*	dBc(3)
	Third Harmonic		–80	–70		*	*		*	*	dBc
Full Power Response(2)	V_O = 5Vp-p, Gain = +2V/V	22	32		*	*		*	*		MHz
	V_O = 2Vp-p, Gain = +2V/V	55	80		*	*		*	*		MHz
Slew Rate(2)	2V Step, Gain = –2V/V	350	500		*	*		*	*		V/μs
Overshoot	2V Step, Gain = –2V/V		15			*			*		%
Settling Time: 0.1%	2V Step, Gain = –2V/V		15			*			*		ns
0.01%			25			*			*		ns
Phase Margin	Gain = +2V/V		50			*			*		Degrees
Rise Time	Gain = +2V/V, 10% to 90%								*		
	V_O = 100mVp-p; Small Signal		1.8			*			*		ns
	V_O = 6Vp-p; Large Signal		8			*			*		ns
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
Output Resistance	1MHz, Gain = +2V/V		0.015			*			*		Ω
Load Capacitance Stability	Gain = +2V/V		15			*			*		pF
Short Circuit Current	Continuous		±150			*			*		mA
POWER SUPPLY											
Rated Voltage	$\pm V_{CC}$		5			*			*		VDC
Derated Performance	$\pm V_{CC}$	4.0		6.0	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		26	28		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	–40		+85	*		*	*		*	°C
SG					–55		+125				°C
Operating: KG, LG, SG	Ambient Temperature				–55		+125	–55		+125	°C
KP, KU		–40		+85							°C
θ_{JA} KG, LG, SG						125			125		°C/W
KP			90								°C/W
KU			100								°C/W

* Same Specifications as for KP, KU.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

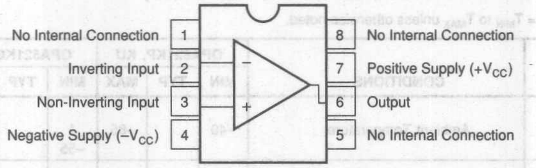
PARAMETER	CONDITIONS	OPA621KP, KU MIN	OPA621KP, KU TYP	OPA621KP, KU MAX	OPA621KG, SG MIN	OPA621KG, SG TYP	OPA621KG, SG MAX	OPA621LG MIN	OPA621LG TYP	OPA621LG MAX	UNITS
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	–40		+85	*		*	*		*	°C
SG					–55		+125				°C
OFFSET VOLTAGE(1)											
Average Drift	Full Temperature Range		±12			*			*		µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	45	60		*	*		50	*		dB
BIAS CURRENT											
Input Bias Current	Full Temperature, V_{CM} = 0VDC		18	40		*	*		*	35	µA
OFFSET CURRENT											
Input Offset Current	Full Temperature, V_{CM} = 0VDC		0.2	5		*	*		*	*	µA
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±2.5	±3.0		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	60	75		*	*		65	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	46	60		*	*		52	*		dB
	R_L = 50Ω	44	58		*	*		50	*		dB
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		26	30		*	*		*	*	mA

* Same specifications as for KP/KU.

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is sample tested. (3) dBc = dB referred to carrier-input signal.

PIN CONFIGURATION

Top View | 8-Pin DIP



ORDERING INFORMATION

OPA621 ( ) ( ) (Q)

- Basic Model Number
- Performance Grade Code
  - K, L = −40°C to +85°C
  - S = −55°C to +125°C
- Package Code
  - G = 8-pin Ceramic DIP
  - P = 8-pin Plastic DIP
  - U = 8-pin Plastic SOIC
- Reliability Screening
  - Q = Q-Screening

ABSOLUTE MAXIMUM RATINGS

Supply .... ±7VDC
Internal Power Dissipation(1) .... See Applications Information
Differential Input Voltage .... Total V_{CC}
Input Voltage Range .... See Applications Information
Storage Temperature Range KG, LG, SG: .... −65°C to +150°C
KP, KU: .... −40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
(soldering, SOIC 3s) .... +260°C
Output Short Circuit to Ground (+25°C) .... Continuous to Ground
Junction Temperature (T_J) .... +175°C

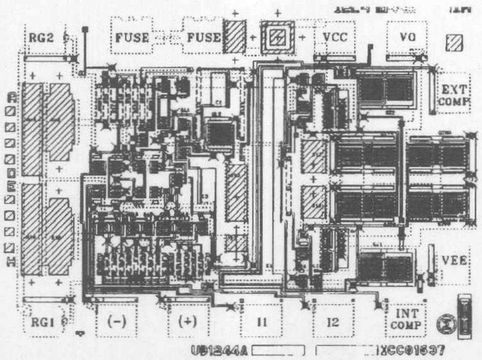
NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA621KP	8-Pin Plastic DIP	006
OPA621KU	8-Pin Surface Mount	182
OPA621KG	8-Pin Ceramic DIP	157
OPA621SG	8-Pin Ceramic DIP	157
OPA621LG	8-Pin Ceramic DIP	157

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

DICE INFORMATION



OPA621 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	NC	7	−V_{CC}
2	−Input	8	NC
3	+Input	9	V_{OUT}
4	NC	10	+V_{CC}
5	NC	11	NC
6	NC	12	NC
		13	NC

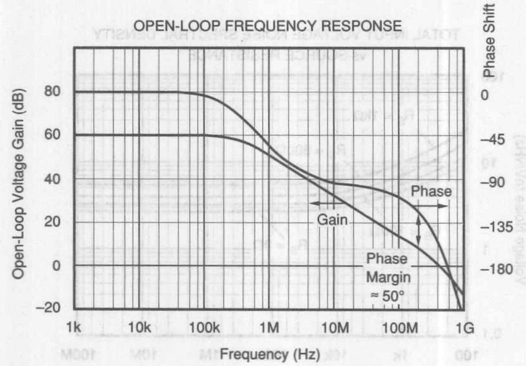
Substrate Bias: Negative Supply −V_{CC}.

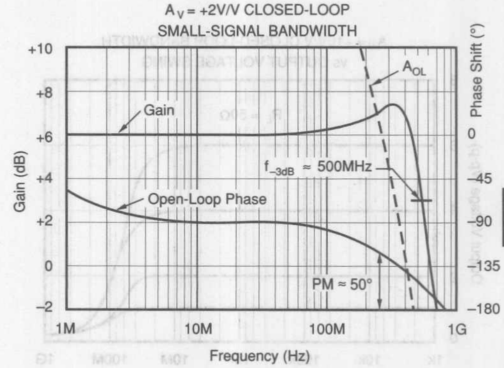
MECHANICAL INFORMATION

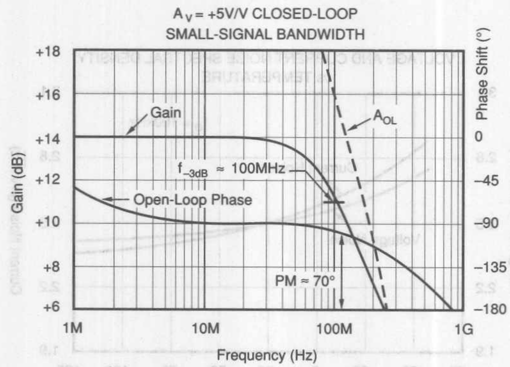
	MILS (0.001")	MILLIMETERS
Die Size	63 x 47 ±5	1.60 x 1.20 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold
Top Metalization		Gold

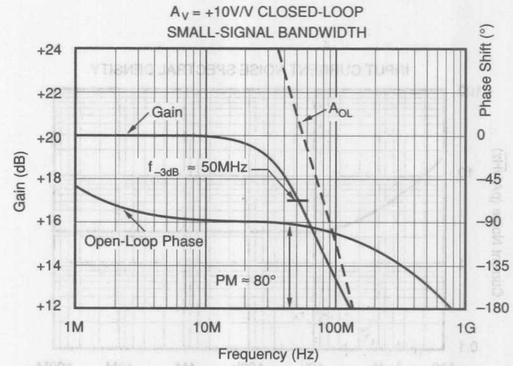
TYPICAL PERFORMANCE CURVES

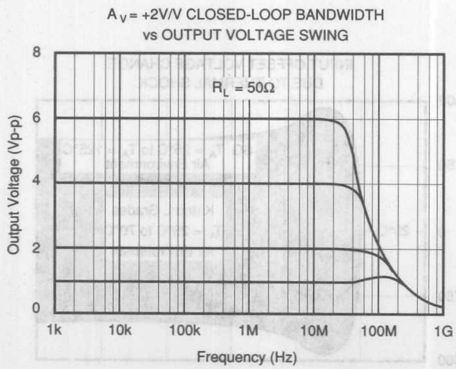
At $V_{CC} = \pm5VDC$, $R_L = 100\Omega$, and $T_A = +25°C$ unless otherwise noted.

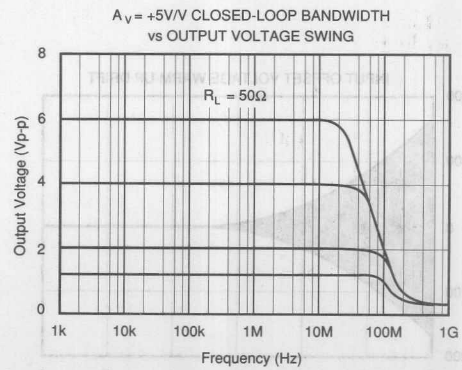








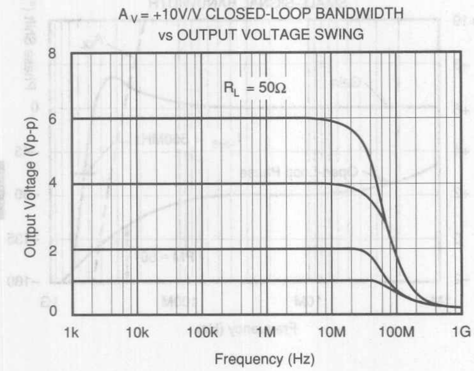


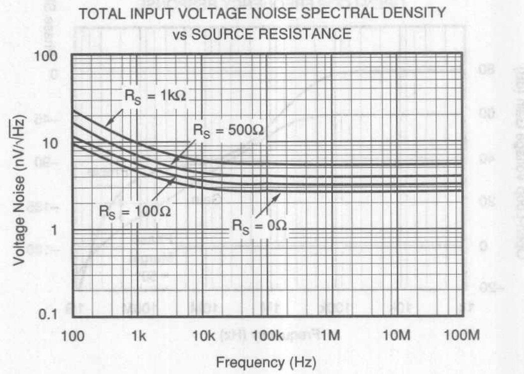


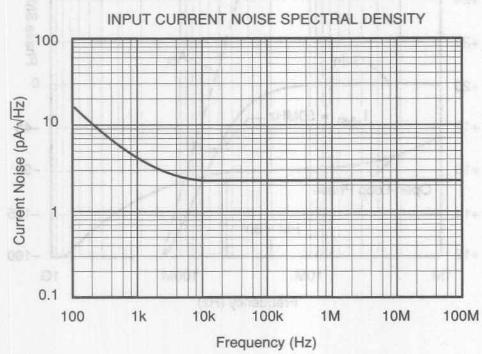
OPA621

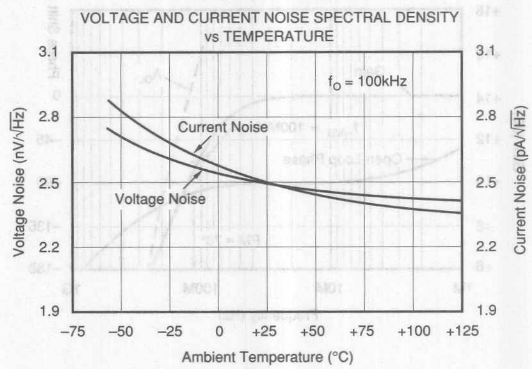
2

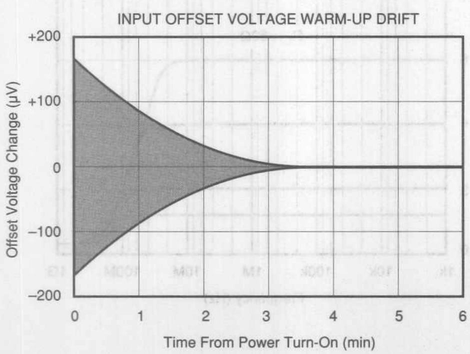
OPERATIONAL AMPLIFIERS

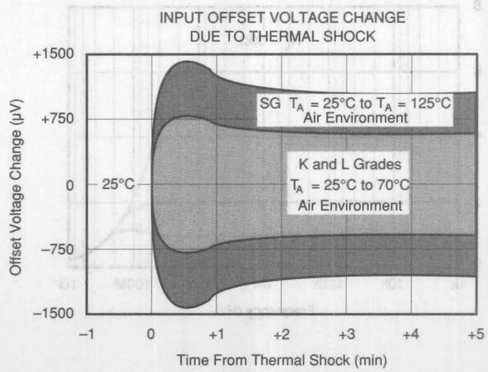

A V = +10V/V CLOSED-LOOP BANDWIDTH
vs OUTPUT VOLTAGE SWING
R L = 50Ω
Output Voltage (Vp-p)
8
6
4
2
0
1k
10k
100k
1M
10M
100M
1G
Frequency (Hz)


TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY
vs SOURCE RESISTANCE
R S = 1kΩ
R S = 500Ω
R S = 100Ω
R S = 0Ω
Voltage Noise (nV/√Hz)
100
10
1
0.1
100
1k
10k
100k
1M
10M
100M
Frequency (Hz)


INPUT CURRENT NOISE SPECTRAL DENSITY
Current Noise (pA/√Hz)
100
10
1
0.1
100
1k
10k
100k
1M
10M
100M
Frequency (Hz)

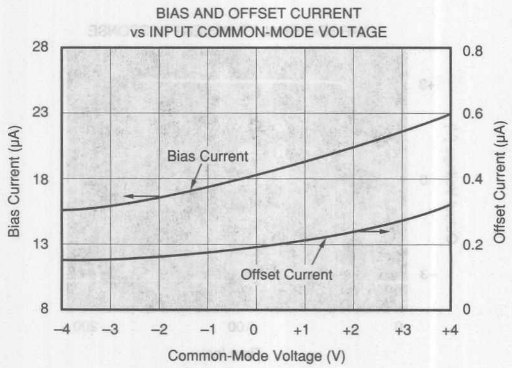

VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY
vs TEMPERATURE
f O = 100kHz
Current Noise
Voltage Noise
Voltage Noise (nV/√Hz)
Current Noise (pA/√Hz)
3.1
2.8
2.5
2.2
1.9
–75
–50
–25
0
+25
+50
+75
+100
+125
Ambient Temperature (°C)

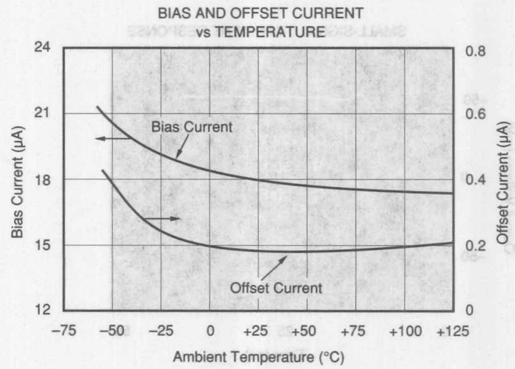

INPUT OFFSET VOLTAGE WARM-UP DRIFT
Offset Voltage Change (µV)
+200
+100
0
–100
–200
0
1
2
3
4
5
6
Time From Power Turn-On (min)

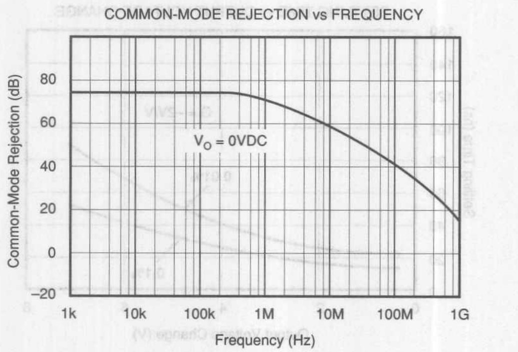

INPUT OFFSET VOLTAGE CHANGE
DUE TO THERMAL SHOCK
SG T A = 25°C to T A = 125°C
Air Environment
K and L Grades
T A = 25°C to 70°C
Air Environment
25°C
Offset Voltage Change (µV)
+1500
+750
0
–750
–1500
–1
0
+1
+2
+3
+4
+5
Time From Thermal Shock (min)

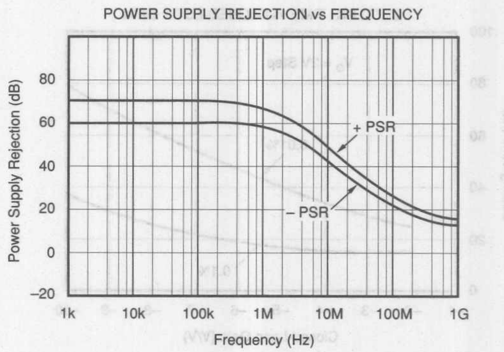
TYPICAL PERFORMANCE CURVES (CONT)

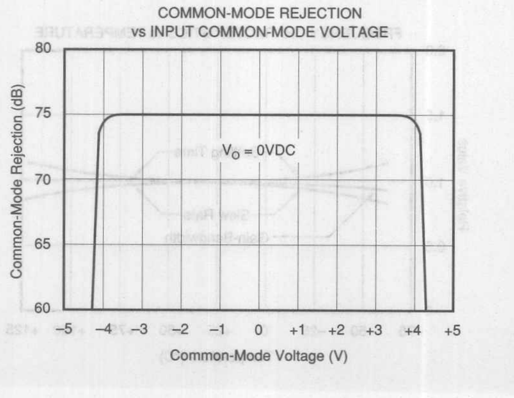
At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

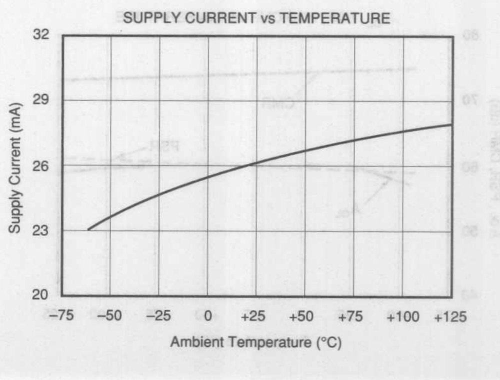








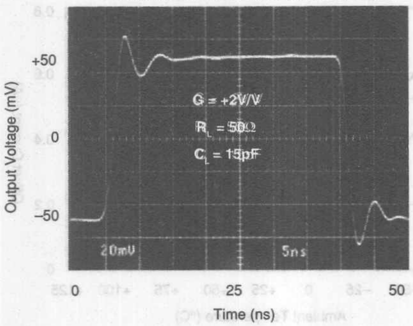




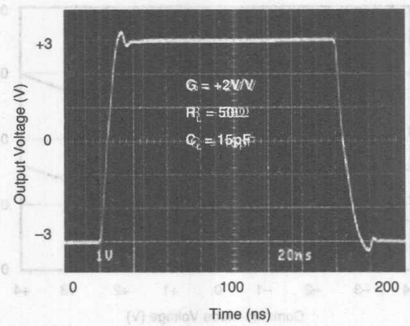
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

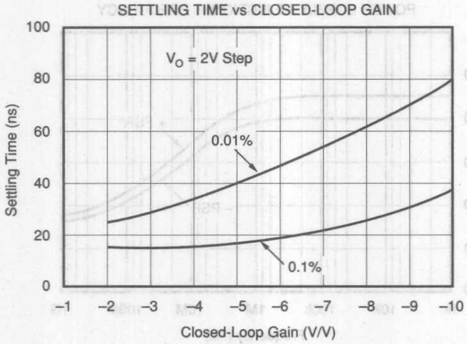
SMALL-SIGNAL TRANSIENT RESPONSE



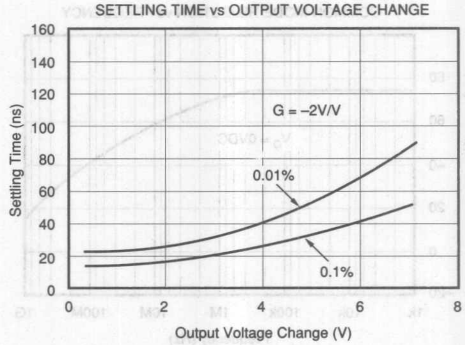
LARGE-SIGNAL TRANSIENT RESPONSE



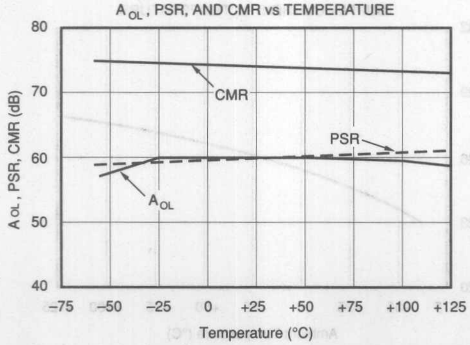
SETTLING TIME vs CLOSED-LOOP GAIN



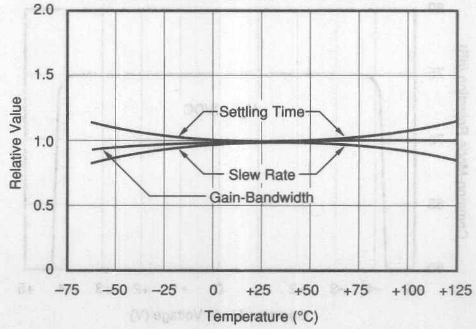
SETTLING TIME vs OUTPUT VOLTAGE CHANGE



A_{OL}, PSR, AND CMR vs TEMPERATURE



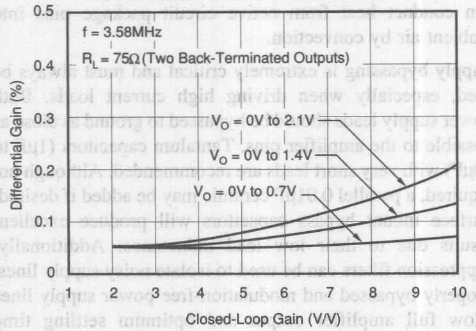
FREQUENCY CHARACTERISTICS vs TEMPERATURE



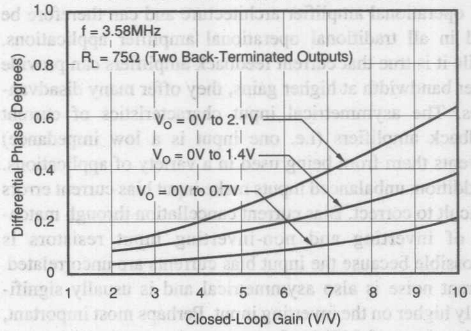
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

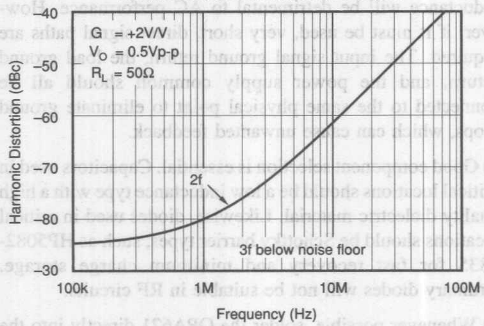
NTSC DIFFERENTIAL GAIN vs CLOSED-LOOP GAIN



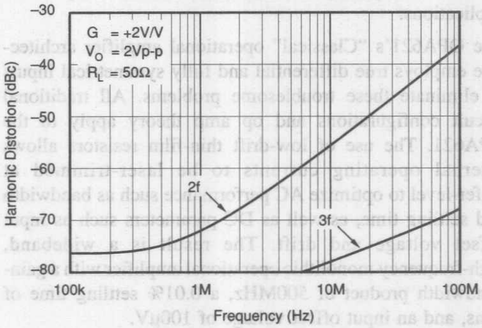
NTSC DIFFERENTIAL PHASE vs CLOSED-LOOP GAIN



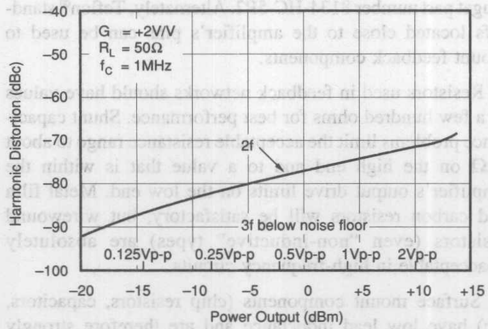
SMALL-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



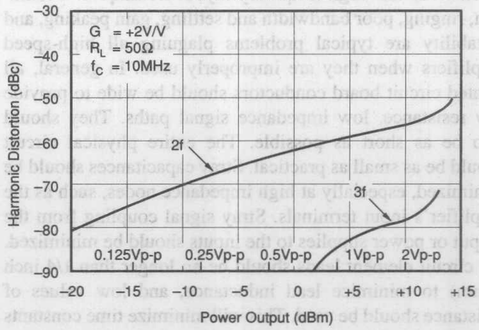
LARGE-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



1MHz HARMONIC DISTORTION
vs POWER OUTPUT



10MHz HARMONIC DISTORTION
vs POWER OUTPUT



DISCUSSION OF PERFORMANCE

The OPA621 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA621's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 microseconds even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA621's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA621. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwidth product of 500MHz, a 0.01% settling time of 25ns, and an input offset voltage of 100μV.

WIRING PRECAUTIONS

Maximizing the OPA621's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA621, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must always be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1μF to 10μF) with very short leads are recommended. Although not required, a parallel 0.01μF ceramic may be added if desired. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

3) Whenever possible, solder the OPA621 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® standoffs located close to the amplifier's pins can be used to mount feedback components.

4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high-frequency circuits.

5) Surface mount components (chip resistors, capacitors, etc) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA621AU (SOIC package) will offer the best AC performance. The parasitic package inductance and capaci-

tance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA621's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

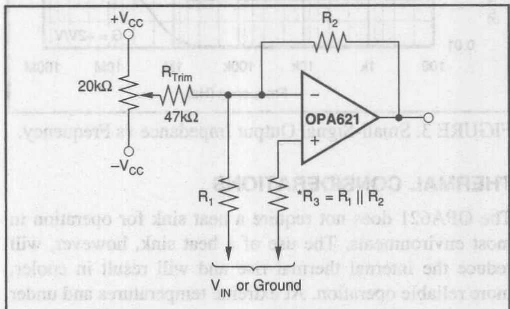
The OPA621's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R3. This will reduce input bias current errors to the amplifier's offset current, which is typically only 0.2µA.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA621 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA621 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA621.



Output Trim Range $\equiv +V_{CC}\left(\frac{R_2}{R_{Trim}}\right)$ to $-V_{CC}\left(\frac{R_2}{R_{Trim}}\right)$

* R_3 is optional and can be used to cancel offset errors due to input bias currents.

FIGURE 1. Offset Voltage Trim.

OUTPUT DRIVE CAPABILITY

The OPA621's design uses large output devices and has been optimized to drive 50Ω and 75Ω resistive loads. The device can easily drive 6Vp-p into a 50Ω load. This high-output drive capability makes the OPA621 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about 150mA at 25°C. This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA621 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

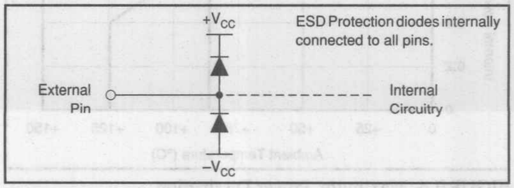


FIGURE 2. Internal ESD Protection.

Teflon® E. I. Du Pont de Nemours & Co.

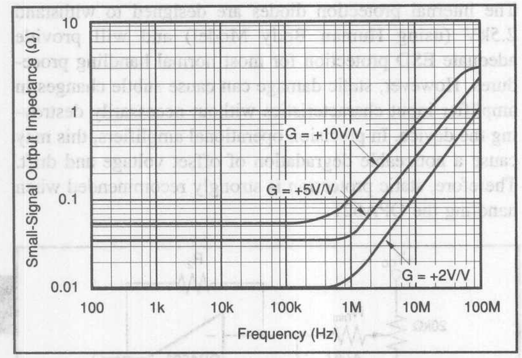


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA621 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 4.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 28mA = 280mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max = $(\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common $P_{DL} = 5V \times 150mA = 750mW$. Thus, $P_D = 280mW + 750mW = 1W$. Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, θ_{JA}, of each package. The variation of short-circuit current with temperature is shown in Figure 5.

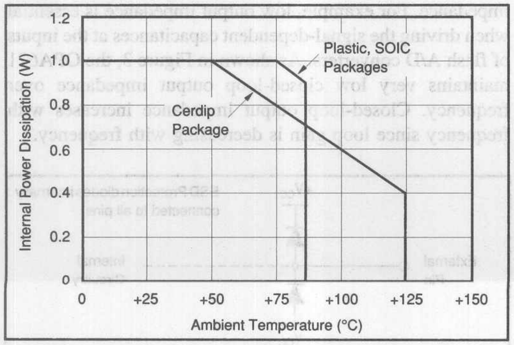


FIGURE 4. Maximum Power Dissipation.

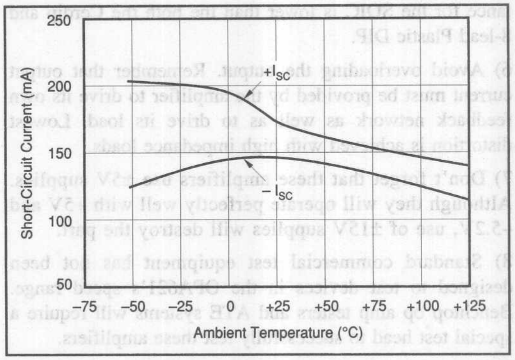


FIGURE 5. Short-Circuit Current vs Temperature.

CAPACITIVE LOADS

The OPA621's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 15pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

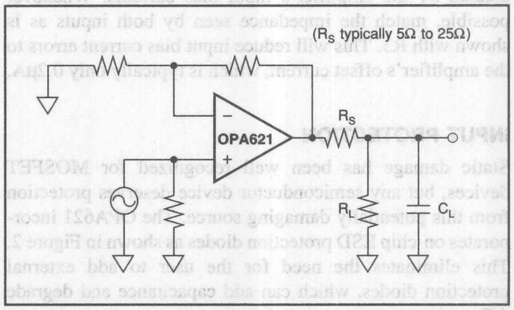


FIGURE 6. Driving Capacitive Loads.

COMPENSATION

The OPA621 is stable in inverting gains of ≥–2V/V and in non-inverting gains ≥+2V/V. Phase margin for both configurations is approximately 50°. Inverting and non-inverting gains of unity should be avoided. The minimum stable gains of +2V/V and –2V/V are the most demanding circuit configurations for loop stability and oscillations are most

likely to occur in these gains. If possible, use the device in a noise gain greater than three to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –2V/V is equivalent to a noise gain of 3.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA621 in a good layout is flat with frequency for higher-gain circuits. However, low-gain circuits and configurations where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

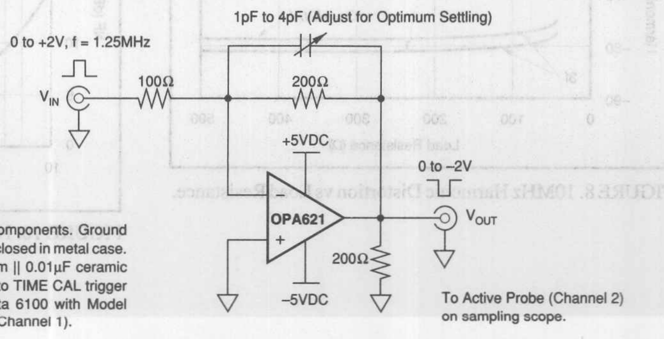
Settling time, specified in an inverting gain of two, occurs in only 25ns to 0.01% for a 2V step, making the OPA621 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA621 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA621. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.



NOTE: Test fixture built using all surface-mount components. Ground plane used on component side and entire fixture enclosed in metal case. Both power supplies bypassed with 10µF Tantalum || 0.01µF ceramic capacitors. It is directly connected (without cable) to TIME CAL trigger source on Sampling Scope (Data Precision's Data 6100 with Model 640-1 plug-in). Input monitored with Active Probe (Channel 1).

FIGURE 7. Settling Time Test Circuit.

The OPA621's Harmonic Distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA621's two-tone, third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA621 to operate in a gain of +2V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +47dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level/tone, dBm/tone
Third IMD = third-order intermodulation ratio below each output tone, dB

For this case OPI^3P = 47dBm, P_O = 10dBm, and the third-order IMD = 2(47 – 10) = 74dB below either 10dBm tone. The OPA621's low IMD makes the device an excellent choice for a variety of RF signal processing applications.

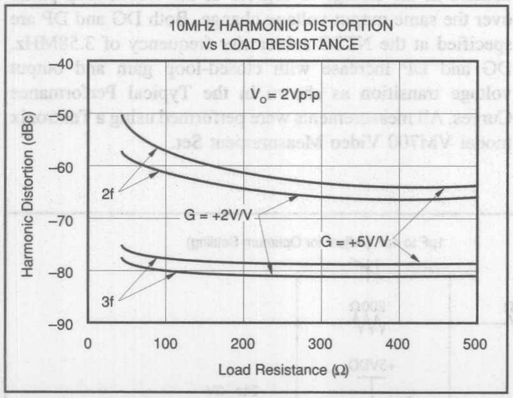


FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

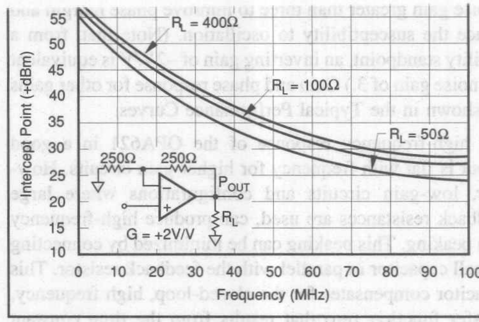


FIGURE 9. Two-Tone Third-Order Intermodulation Intercept vs Frequency.

NOISE FIGURE

The OPA621's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA621's Noise Figure vs Source Resistance is shown in Figure 10.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA621. Request Burr-Brown Application Bulletin AB-167.

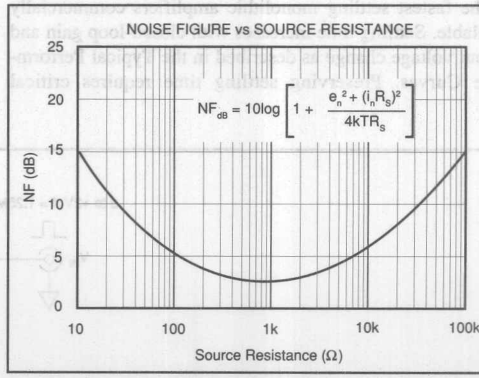


FIGURE 10. Noise Figure vs Source Resistance.

OPA621. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: Cerdip package = 1.31E+9 Hours, Plastic DIP = 5.02E+7 Hours, and SOIC = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 125°C, 24 hrs
Temperature Cycling	Temperature = –55°C to 125°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Hermetic Seal	Fine: He leak rate < 1 X 10 atm cc/s Gross: Perfluorocarbon bubble test
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on SG package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM1135 for 8-Pin DIP, and DEM1136 for SOIC package.

APPLICATIONS

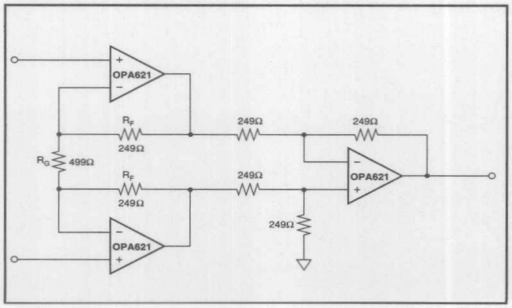


FIGURE 11. Unity Gain Difference Amplifier.

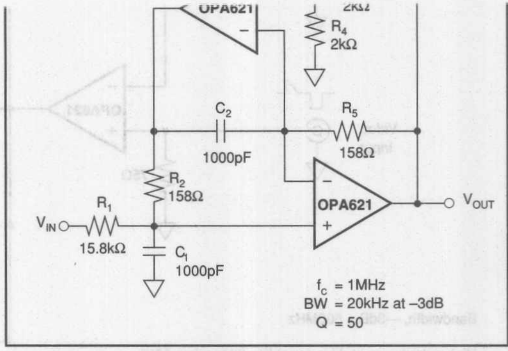


FIGURE 12. High-Q 1MHz Bandpass Filter

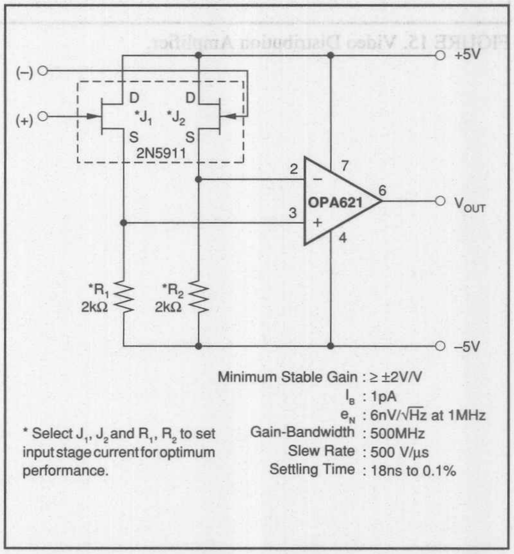


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

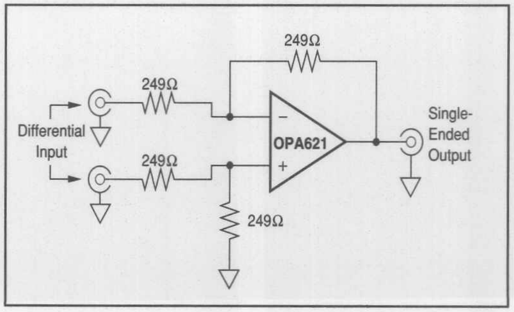


FIGURE 14. Differential Input Buffer Amplifier (G = –2V/V).

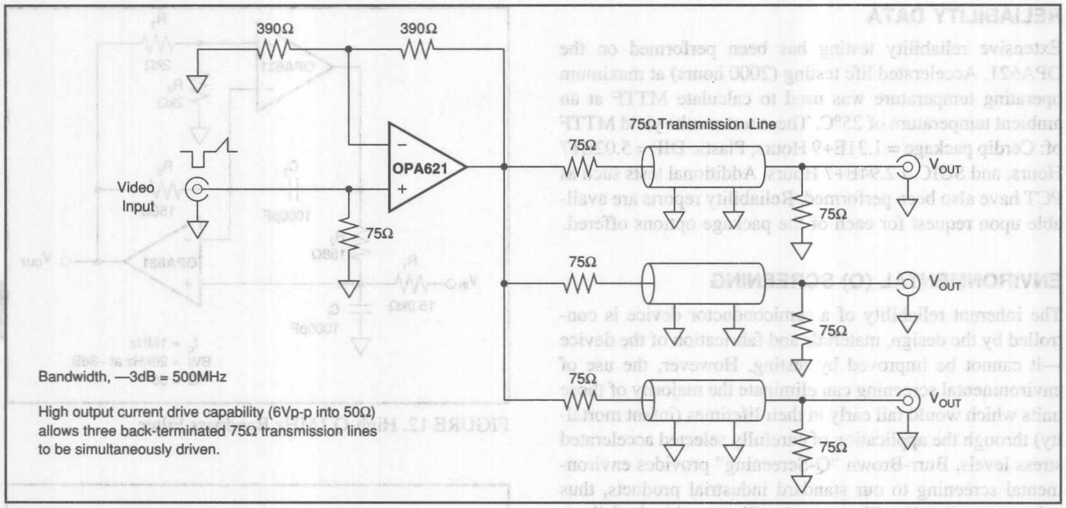
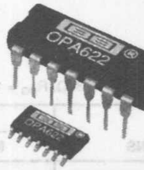


FIGURE 15. Video Distribution Amplifier.

BURR - BROWN®



OPA622

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11131

Wide-Bandwidth OPERATIONAL AMPLIFIER

FEATURES

- LARGE SIGNAL BANDWIDTH: 150MHz (AP), 200MHz (AU) (Voltage-Feedback)
- HIGH OUTPUT CURRENT: ±70mA
- SLEW RATE: 1500V/μs (AP), 1700V/μs (AU)
- DIFFERENTIAL GAIN: 0.15%
- DIFFERENTIAL PHASE: 0.08°
- EXCELLENT BANDWIDTH/SUPPLY CURRENT RATIO: 200MHz/5mA
- LOW INPUT BIAS CURRENT: –1.2μA

APPLICATIONS

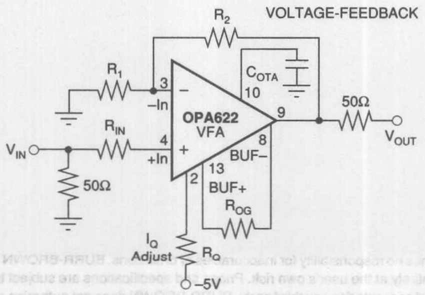
- BROADCAST/HDTV EQUIPMENT
- COMMUNICATIONS
- PULSE/RF AMPLIFIERS
- ACTIVE FILTER
- HIGH SPEED ANALOG SIGNAL PROCESSING
- MULTIPLIER OUTPUT AMP
- DIFFERENTIATOR FOR DIGITIZED VIDEO SIGNALS

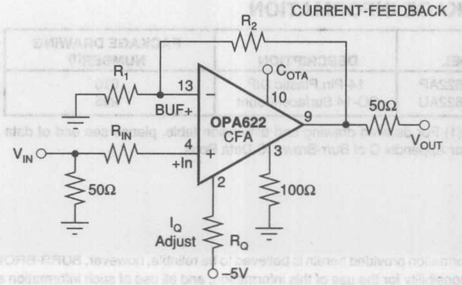
DESCRIPTION

The OPA622 is a monolithic amplifier component designed for precision wide-bandwidth systems including high-resolution video, RF and IF circuitry, and communications equipment. It includes a monolithic integrated current-feedback operational amplifier block and a voltage buffer block, which, when combined, form a voltage-feedback operational amplifier.

When combined as a current-feedback amplifier, it provides a 280MHz large-signal bandwidth at ±2.5V output level and a 1700V/μs slew rate. The output buffer stage can deliver ±70mA output current. The high output current capability allows the OPA622 to drive two 50Ω or 75Ω lines with ±3V output swing, making it ideal along with the low differential gain/phase errors for RF, IF, and video applications.

The feedback buffer stage provides 700MHz bandwidth, a very high slew rate, and a very short signal delay time. It is designed primarily for interstage buffering and not for driving long cables. When combined with the current-feedback amplifier section, the OPA622 can be interconnected as a voltage-feedback amplifier with two identical high-impedance inputs. In this configuration, it features a low common-mode gain, low input offset, and, due to the delay time of the additional feedback buffer, a decrease in frequency bandwidth compared with the current-feedback configuration. Unlike "classical" operational amplifiers, the OPA622 achieves a nearly constant bandwidth over a wide gain and output voltage range. The external setting of the open-loop gain with R_{OG} avoids a large compensation capacitor, improves the slew rate, and allows a frequency response adaption to various gains and load conditions.





International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

DC-SPECIFICATION
VOLTAGE-FEEDBACK AMPLIFIER (Figure 5)

At V_{CC} = ±5V, I_Q = ±5mA, G_{CL} = +2V/V, R_{LOAD} = 100Ω, R_{SOURCE} = 50Ω, R_Q = 430Ω, R_{OG} = 150Ω and T_A = +25°C, unless otherwise specified.

		OPA622AP, AU			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOSED-LOOP OUTPUT OFFSET VOLTAGE					
Initial			1	±15	mV
vs Temperature			210		μV/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V	–46	–50		dB
vs Supply (non-tracking)	V_{CC} = +4.5V to +5.5V		–43		dB
vs Supply (non-tracking)	V_{CC} = –4.5V to –5.5V		–51		dB
INPUT BIAS CURRENT					
Initial			–1.2	±4	μA
vs Temperature			7		nA/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V		29		nA/V
vs Supply (non-tracking)	V_{CC} = +4.5V to +5.5V		170		nA/V
vs Supply (non-tracking)	V_{CC} = –4.5V to –5.5V		58		nA/V
OFFSET CURRENT					
Input Offset Current	V_{CM} = 0V		0.1		μA
INPUT IMPEDANCE					
Differential Mode			2.4 || 1		MΩ || pF
INPUT NOISE					
Voltage Noise Density	f = 100kHz to 100MHz		11		nV/√MHz
Signal-to-Noise Ratio	S/N = 20 log 0.7/(V_N • √5MHz)		89		dB
INPUT VOLTAGE RANGE					
Common-Mode Input Range			±3.2		V
Common-Mode Rejection	V_I = +2.5V, V_O = 0V		78		dB
RATED OUTPUT	G_{CL} = +1				
Voltage Output		±3	±3.2		V
Closed-Loop Output Impedance			0.2		Ω
Current Output			70		mA
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	R_Q = 430Ω, I_O = 0mA	±4.4	±5	±5.6	mA
Quiescent Current (programmable)	Useful Range, I_O = 0mA		3 to 8		mA
TEMPERATURE					
Operating	Ambient Temperature	–40		85	°C
Storage	Ambient Temperature	–40		125	°C

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage(1)	$\pm V_{CC}$ to ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
OPA622AP	14-Pin Plastic DIP	–40°C to +85°C
OPA622AU	SO-14 Surface-Mount	–40°C to +85°C

PACKAGE INFORMATION

MODEL	DESCRIPTION	PACKAGE DRAWING NUMBER(1)
OPA622AP	14-Pin Plastic DIP	010
OPA622AU	SO-14 Surface-Mount	235

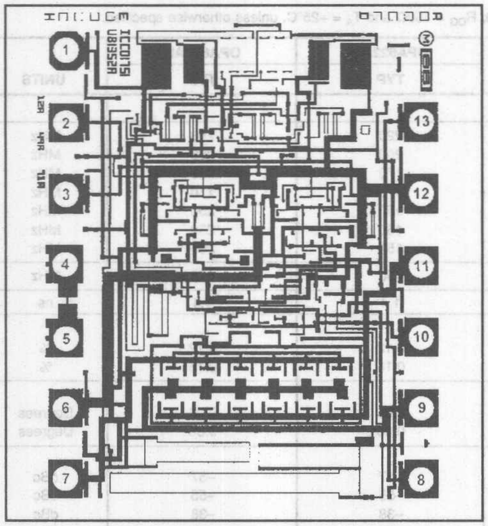
NOTE:(1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

AC-SPECIFICATION
VOLTAGE-FEEDBACK AMPLIFIER (Figure 5)

At $V_{CC} = \pm 5V$, $I_Q = \pm 5mA$, $G_{CL} = +2V/V$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_Q = 430\Omega$, $R_{OG} = 150\Omega$ and $T_A = +25°C$, unless otherwise specified.

PARAMETER	CONDITIONS	OPA622AP TYP	OPA622AU TYP	UNITS
FREQUENCY DOMAIN				
LARGE SIGNAL	V_O = 2.8Vp-p, Gain = +1V/V	220	250	MHz
Closed-Loop Bandwidth (–3dB)	V_O = 2.8Vp-p, Gain = +2V/V	200	250	MHz
	V_O = 2.8Vp-p, Gain = +5V/V	170	230	MHz
	V_O = 2.8Vp-p, Gain = +10V/V	110	110	MHz
	V_O = 2.8Vp-p, Gain = –1V/V	150	250	MHz
	V_O = 2.8Vp-p, Gain = –2V/V	160	250	MHz
	V_O = 5.0Vp-p, Gain = +2V/V	150	200	MHz
SMALL SIGNAL BANDWIDTH	V_O = 0.2Vp-p, Gain = +2V/V	150	170	MHz
GROUP DELAY TIME		1.4	1.4	ns
DIFFERENTIAL GAIN	f = 4.43MHz, R_{LOAD} = 150Ω			
	V_O = 0.7V, Gain = +1V/V	0.12	0.12	%
	V_O = +1.4V, Gain = +2V/V	0.15	0.15	%
DIFFERENTIAL PHASE	f = 4.43MHz, R_{LOAD} = 150Ω			
	V_O = 0.7V, Gain = +1V/V	0.06	0.06	Degrees
	V_O = +1.4V, Gain = +2V/V	0.08	0.08	Degrees
HARMONIC DISTORTION	Gain = +2V/V			
Second Harmonic 2f	f = 10MHz, V_O = 2.8Vp-p	–57	–57	dBc
Third Harmonic 3f		–55	–55	dBc
Second Harmonic 2f	f = 30MHz, V_O = 2.8Vp-p	–38	–38	dBc
Third Harmonic 3f		–43	–43	dBc
Second Harmonic 2f	f = 50MHz, V_O = 2.8Vp-p	–33	–33	dBc
Third Harmonic 3f		–30	–30	dBc
GAIN FLATNESS PEAKING	Gain = +2V/V			
	V_O = 2.8Vp-p, DC to 30MHz	0.12	0.12	dB
	V_O = 2.8Vp-p, DC to 100MHz	0.3	0.3	dB
TIME DOMAIN				
Rise Time	Gain = +2V/V, 10% to 90% V_O = 5Vp-p, C_L = 2pF	2.4	2.7	ns
Fall Time	Gain = +2V/V, 10% to 90% V_O = 5Vp-p, C_L = 2pF	3.5	3.2	ns
SLEW RATE	Gain = +2V/V, Rise Time = 2ns V_O = 6.2Vp-p			
Positive		1500	1700	V/µs
Negative		1300	1600	Vµs
SETTLING TIME	Gain = +2V/V, Rise Time = 2ns V_O = 2Vp-p, 0.1%	17	17	ns

DICE INFORMATION



OPA622AD DIE TOPOGRAPHY

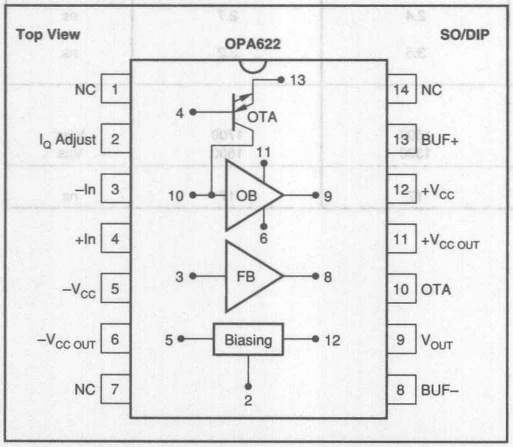
PAD	FUNCTION
1	Quiescent Current Adjustment
2	Inverting Analog Input
3	Non-Inverting Analog Input
4	NC
5	NC
6	–5V Supply
7	–5V Supply, Output
8	Inverting Buffer Output
9	Analog Output
10	Analog OTA Output
11	+5V Supply, Output
12	+5V Supply
13	Non-Inverting Buffer Output

Substrate Bias: Negative Supply
NC: No Connection
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	57 x 69 ±5	1.44 x 1.76 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02+0.05,–0.0	0.0005+0.0013, –0.0
Gold	0.30 ±0.05	0.0076 ±0.0013

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

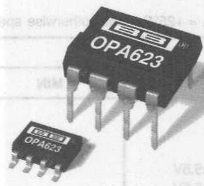
PIN NO.	DESCRIPTION	FUNCTION
1	NC	No Connection
2	I_Q Adjust	Quiescent Current Adjustment; typical 3-8mA
3	–In	Inverting Analog Input
4	+In	Noninverting Analog Input
5	$-V_{CC}$	Negative Supply Voltage; typical –5VDC
6	$-V_{CC\ OUT}$	Negative Supply Voltage Output Buffer; typical –5VDC
8	BUF–	Analog Output Feedback Buffer
9	V_{OUT}	Analog Output
10	OTA	Analog Output OTA
11	$+V_{CC\ OUT}$	Positive Supply Voltage Output Buffer; typical +5VDC
12	$+V_{CC}$	Positive Supply Voltage; typical +5VDC
13	BUF+	Analog Output/Input
14	NC	No Connection

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

BURR - BROWN®



OPA623

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11132

Wide Bandwidth, Current-Feedback OPERATIONAL AMPLIFIER

FEATURES

- BANDWIDTH: 350MHz, 2.8Vp-p
- HIGH OUTPUT CURRENT: ±70mA
- SLEW RATE: 2100V/µs, 5Vp-p
- DIFFERENTIAL GAIN/PHASE: 0.12%/0.05°
- LOW QUIESCENT CURRENT: ±4mA
- LOW INPUT BIAS CURRENT: 1.2µA
- RISE TIME: 1.9ns, 5Vp-p
- SETTLING TIME: 9ns, 0.1%

APPLICATIONS

- BROADCAST/HDTV EQUIPMENT
- HIGH-SPEED DIGITAL COMMUNICATIONS
- PULSE/RF AMPLIFIERS
- HIGH-SPEED ANALOG SIGNAL PROCESSING
- LINE DRIVING (50Ω, 75Ω)
- DISTRIBUTION AMP
- CRT OUTPUT STAGE DRIVER
- ACTIVE FILTER

DESCRIPTION

The OPA623 is a current-feedback operational amplifier designed for precision wide-bandwidth systems including high-resolution video, RF and IF circuitry, and communications equipment.

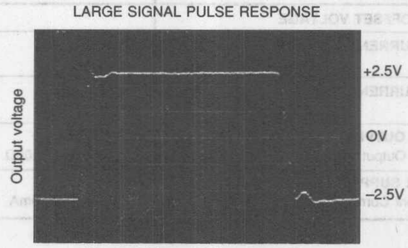
The new circuit design, together with the complementary bipolar process, achieves performance previously unattainable in monolithic integrated circuit technology.

The current-feedback op amp is optimized for wide bandwidth, excellent pulse response, gain flatness, low distortion, and operation at a low quiescent current of ±4mA.

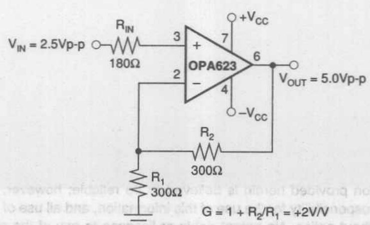
It provides a 350MHz large-signal bandwidth at 2.8Vp-p output voltage, as well as a 2100V/µs slew rate. The gain flatness of 0.05dB over a 30MHz bandwidth makes it suitable for HDTV designs. Another feature of the op amp is its high output current of ±70mA, enabling it to drive two back-terminated 75Ω cables when using the amplifier as a line driver in video routers, distribution amplifiers, and analog and digital communications equipment.

The OPA623 operates from a ±5V supply, is specified for the extended industrial temperature range (–40°C to +85°C), and is available in 8-pin plastic SOIC and 8-pin plastic DIP.

LARGE SIGNAL PULSE RESPONSE



Output Voltage - 5Vp-p, 5ns/DIV



$G = 1 + R_2/R_1 = +2V/V$

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

DC-SPECIFICATION

At V_{CC} = ±5VDC, I_Q = ±4mA, R_L = 100Ω, R_{IN} = 210Ω, and T_{AMB} = +25°C unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP, AU MIN	TYP	MAX	UNITS
INPUT OFFSET VOLTAGE					
Initial			−8	±25	mV
vs Temperature			125		µV/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V	45	50		dB
vs Supply (non-tracking)	V_{CC} = +4.5V to +5.5V		47		dB
vs Supply (non-tracking)	V_{CC} = −4.5V to −5.5V		39		dB
+INPUT BIAS CURRENT					
Initial			−1.2	±4	µA
vs Temperature			7		nA/°C
−INPUT BIAS CURRENT					
Initial			+4.5	±20	µA
vs Temperature			340		nA/°C
INPUT IMPEDANCE					
+Input			2.74 ||1		MΩ || pF
INPUT NOISE	f = 100kHz to 100MHz				
Voltage Noise Density			10		nV/√Hz
Signal-to-Noise Ratio	S/N = 0.7/(Vn • √5MHz)		89		dB
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±3	±3.2		V
Common-Mode Rejection		43	50		dB
RATED OUTPUT					
Voltage Output	R_L = 100Ω	±3	±3.1		V
Output Current			±70		mA
Closed-Loop Output Impedance	Gain = +2		0.12 || 1.5		Ω || pF
POWER SUPPLY					
Rated Voltage		±4.5		±5.5	VDC
Derated Performance		±4		±6	VDC
Quiescent Current	I_O = 0mA	±3.5	±4	±4.5	mA
Rejection Ratio		45	50		dB

ELECTRICAL (FULL TEMPERATURE RANGE, −40°C to +85°C)

At V_{CC} = ±5VDC, I_Q = ±4mA, R_L = 100Ω, and R_{IN} = 210Ω unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP, AU MIN	TYP	MAX	UNITS
INPUT OFFSET VOLTAGE				±30	mV
BIAS CURRENT					
+Input			−1.5	±5	µA
BIAS CURRENT					
−Input			27	±50	µA
RATED OUTPUT					
Voltage Output	R_L = 100Ω	±3	±3.1		V
POWER SUPPLY					
Quiescent Current	I_O = 0mA	±2	±4	±7	mA

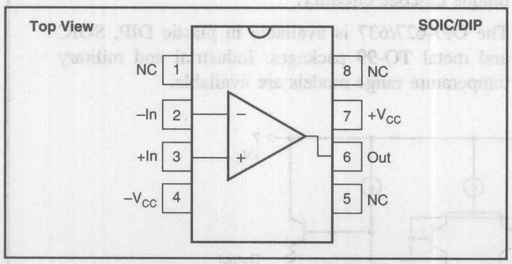
SPECIFICATIONS

AC-SPECIFICATION

At V_{CC} = ±5VDC, I_Q = ±4mA, R_L = 100Ω, R_{IN} = 210Ω, and T_{AMB} = +25°C unless otherwise specified.

		OPA623AP, AU			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY DOMAIN					
Large Signal Closed-Loop Bandwidth (–3dB)	V_O = 2.8Vp-p, Gain = +1V/V V_O = 2.8Vp-p, Gain = +2V/V V_O = 2.8Vp-p, Gain = +5V/V V_O = 2.8Vp-p, Gain = +10V/V V_O = 2.8Vp-p, Gain = –1V/V V_O = 2.8Vp-p, Gain = –2V/V V_O = 5.0Vp-p, Gain = +2V/V		340 350 260 210 360 330 240		MHz MHz MHz MHz MHz MHz MHz
SMALL SIGNAL BANDWIDTH	V_O = 0.2Vp-p, Gain = +2V/V		290		MHz
GROUP DELAY TIME	Pin 3 to Pin 6, Gain = +2V/V		1.2		ns
DIFFERENTIAL GAIN	G = +2V/V, f = 4.43MHz, R_L = 150Ω V_O = +1.4V		0.12		%
DIFFERENTIAL PHASE	G = +2V/V, f = 4.43MHz, R_L = 150Ω V_O = +1.4V		0.05		Degrees
HARMONIC DISTORTION Second Harmonic Third Harmonic Second Harmonic Third Harmonic Second Harmonic Third Harmonic	Gain = +2V/V f = 10MHz, V_O = 2.0Vp-p f = 30MHz, V_O = 2.0Vp-p f = 50MHz, V_O = 2.0Vp-p		–56 –59 –30 –37 –30 –33		dBc dBc dBc dBc dBc dBc
GAIN FLATNESS PEAKING	Gain = +2V/V V_O = 2.0Vp-p, DC to 30MHz V_O = 2.0Vp-p, DC to 100MHz		0.05 0.20		dB dB
TIME DOMAIN					
Rise Time	Gain = +2V/V, 10% to 90% V_O = 2.0Vp-p V_O = 5.0Vp-p		1.4 1.9		ns ns
Fall Time	Gain = +2V/V, 10% to 90% V_O = 2.0Vp-p V_O = 5.0Vp-p		1.4 2.6		ns ns
SLEW RATE	Gain = +2V/V, Rise Time = 1ns V_O = 0.2Vp-p V_O = 5.0Vp-p		140 2100		V/µs V/µs
SETTLING TIME	Gain = +2V/V, Rise Time = 2ns V_O = $2V_{p-p}$, 0.1%		9		ns

PIN CONFIGURATION



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA623AP	Plastic DIP	006
OPA623AU	Plastic SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

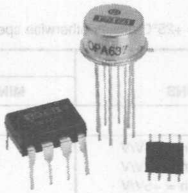
MODEL	PACKAGE	TEMPERATURE RANGE
OPA623AP	8-Pin Plastic DIP	–40°C to +85°C
OPA623AU	8-Pin SOIC	–40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage[1]	$\pm V_{CC}$ ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

BURR - BROWN®



OPA627
OPA637

Precision High-Speed *Difet*® OPERATIONAL AMPLIFIERS

FEATURES

- VERY LOW NOISE: 4.5nV/$\sqrt{Hz}$ at 10kHz
- FAST SETTLING TIME:
  OPA627—550ns to 0.01%
  OPA637—450ns to 0.01%
- LOW V_{OS}: 100µV max
- LOW DRIFT: 0.8µV/°C max
- LOW I_B: 5pA max
- OPA627: Unity-Gain Stable
- OPA637: Stable in Gain ≥ 5

APPLICATIONS

- PRECISION INSTRUMENTATION
- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- ACTIVE FILTERS

DESCRIPTION

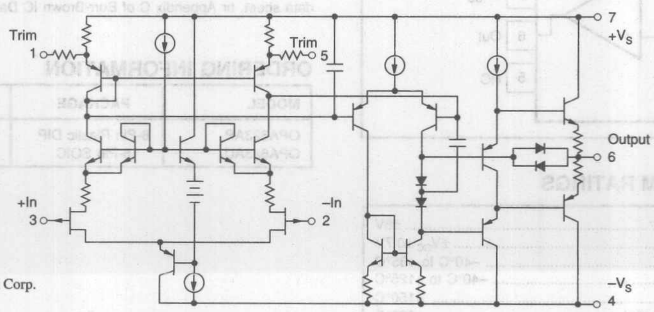
The OPA627 and OPA637 ***Difet*** operational amplifiers provide a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627/637 has lower noise, lower offset voltage, and much higher speed. It is useful in a broad range of precision and high speed analog circuitry.

The OPA627/637 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage—±4.5V to ±18V. Laser-trimmed ***Difet*** input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

Difet fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627/637 is available in plastic DIP, SOIC and metal TO-99 packages. Industrial and military temperature range models are available.



Difet®, Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

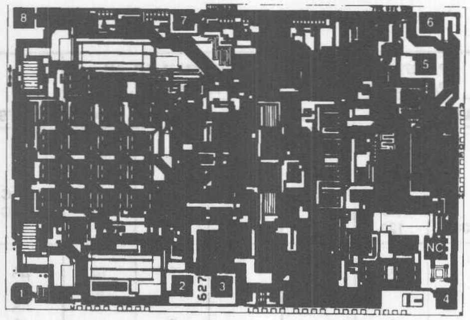
ELECTRICAL

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

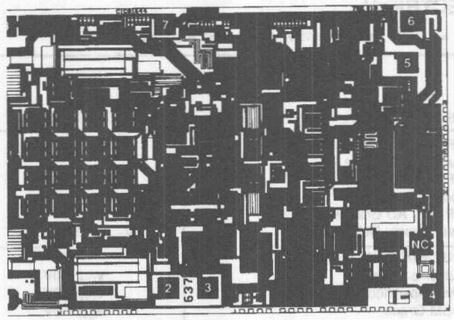
PARAMETER	CONDITIONS	OPA627BM, BP, SM OPA637BM, BP, SM MIN	TYP	MAX	OPA627AM, AP, AU OPA637AM, AP, AU MIN	TYP	MAX	UNITS
OFFSET VOLTAGE (1)								
Input Offset Voltage			40	100		130	250	μV
AP, BP, AU Grades			100	250		280	500	μV
Average Drift			0.4	0.8		1.2	2	μV/°C
AP, BP, AU Grades			0.8	2		2.5		μV/°C
Power Supply Rejection	V_S = ±4.5 to ±18V	106	120		100	116		dB
INPUT BIAS CURRENT (2)								
Input Bias Current	V_{CM} = 0V		1	5		2	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade	V_{CM} = 0V			50				nA
Over Common-Mode Voltage	V_{CM} = ±10V		1			2		pA
Input Offset Current	V_{CM} = 0V		0.5	5		1	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade				50				nA
NOISE								
Input Voltage Noise								
Noise Density: f = 10Hz			15	40		20		nV/√Hz
f = 100Hz			8	20		10		nV/√Hz
f = 1kHz			5.2	8		5.6		nV/√Hz
f = 10kHz			4.5	6		4.8		nV/√Hz
Voltage Noise, BW = 0.1Hz to 10Hz			0.6	1.6		0.8		μVp-p
Input Bias Current Noise								
Noise Density, f = 100Hz			1.6	2.5		2.5		fA/√Hz
Current Noise, BW = 0.1Hz to 10Hz			30	60		48		fAp-p
INPUT IMPEDANCE								
Differential			10^{13} || 8			*		Ω || pF
Common-Mode			10^{13} || 7			*		Ω || pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±11	±11.5		*	*		V
Over Specified Temperature		±10.5	±11		*	*		V
Common-Mode Rejection	V_{CM} = ±10.5V	106	116		100	110		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	112	120		106	116		dB
Over Specified Temperature	V_O = ±10V, R_L = 1kΩ	106	117		100	110		dB
SM Grade	V_O = ±10V, R_L = 1kΩ	100	114					dB
FREQUENCY RESPONSE								
Slew Rate: OPA627	G = –1, 10V Step	40	55		*	*		V/μs
OPA637	G = –4, 10V Step	100	135		*	*		V/μs
Settling Time: OPA627 0.01%	G = –1, 10V Step		550			*		ns
0.1%	G = –1, 10V Step		450			*		ns
OPA637 0.01%	G = –4, 10V Step		450			*		ns
0.1%	G = –4, 10V Step		300			*		ns
Gain-Bandwidth Product: OPA627	G = 1		16			*		MHz
OPA637	G = 10		80			*		MHz
Total Harmonic Distortion + Noise	G = +1, f = 1kHz		0.00003			*		%
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Current			±7	±7.5		*	*	mA
OUTPUT								
Voltage Output	R_L = 1kΩ	±11.5	±12.3		*	*		
Over Specified Temperature		±11	±11.5		*	*		V
Current Output	V_O = ±10V		±45			*		mA
Short-Circuit Current		±35	+70/–55	±100	*	*	*	mA
Output Impedance, Open-Loop	1MHz		55			*		Ω
TEMPERATURE RANGE								
Specification: AP, BP, AM, BM, AU		–25		+85	*		*	°C
SM		–55		+125				°C
Storage: AM, BM, SM		–60		+150	*		*	°C
AP, BP, AU		–40		+125	*		*	°C
θ_{J-A}: AM, BM, SM			200			*		°C/W
AP, BP			100			*		°C/W
AU			160					°C/W

* Specifications same as "B" grade.

NOTES: (1) Offset voltage measured fully warmed-up. (2) High-speed test at T_J = +25°C. See Typical Performance Curves for warmed-up performance.



OPA627 DIE TOPOGRAPHY



OPA637 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Trim	5	Offset Trim
2	–In	6	Output
3	+In	7	$+V_S$
4	$-V_S$	8	Substrate
		NC	No Connection

Substrate Bias: Dielectrically isolated. See data sheet for connection options.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	117 x 80 ±5	2.97 x 2.03 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count	46	
Backing:	None	

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA627AP	Plastic DIP	–25°C to +85°C
OPA627BP	Plastic DIP	–25°C to +85°C
OPA627AU	SOIC	–25°C to +85°C
OPA627AM	TO-99 Metal	–25°C to +85°C
OPA627BM	TO-99 Metal	–25°C to +85°C
OPA627SM	TO-99 Metal	–55°C to +125°C
OPA637AP	Plastic DIP	–25°C to +85°C
OPA637BP	Plastic DIP	–25°C to +85°C
OPA637AU	SOIC	–25°C to +85°C
OPA637AM	TO-99 Metal	–25°C to +85°C
OPA637BM	TO-99 Metal	–25°C to +85°C
OPA637SM	TO-99 Metal	–55°C to +125°C

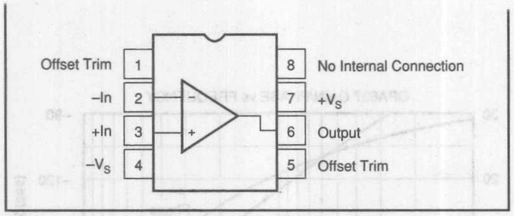
ABSOLUTE MAXIMUM RATINGS

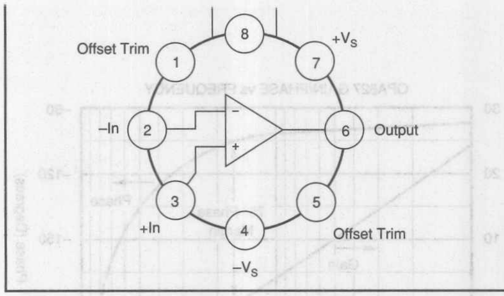
Supply Voltage .... ±18V
Input Voltage Range .... $+V_S + 2V$ to $-V_S - 2V$
Differential Input Range .... Total $V_S + 4V$
Power Dissipation 1000mW
Operating Temperature
  M Package .... –55°C to +125°C
  P, U Package .... –40°C to +125°C
Storage Temperature
  M Package .... –65°C to +150°C
  P, U Package .... –40°C to +125°C
Junction Temperature
  M Package .... +175°C
  P, U Package .... +150°C
Lead Temperature (soldering, 10s) .... +300°C
  SOIC (soldering, 3s) .... +260°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA627AP	Plastic DIP	006
OPA627BP	Plastic DIP	006
OPA627AU	SOIC	182
OPA627AM	TO-99 Metal	001
OPA627BM	TO-99 Metal	001
OPA627SM	TO-99 Metal	001
OPA637AP	Plastic DIP	006
OPA637BP	Plastic DIP	006
OPA637AU	SOIC	182
OPA637AM	TO-99 Metal	001
OPA637BM	TO-99 Metal	001
OPA637SM	TO-99 Metal	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

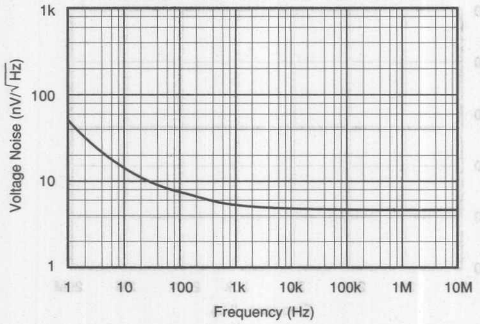




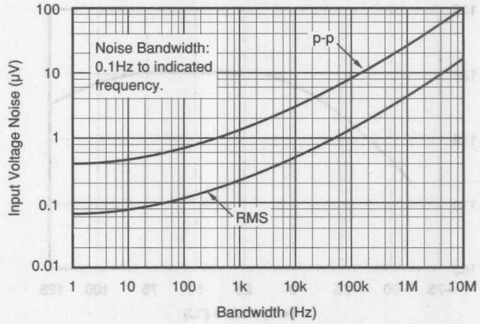
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

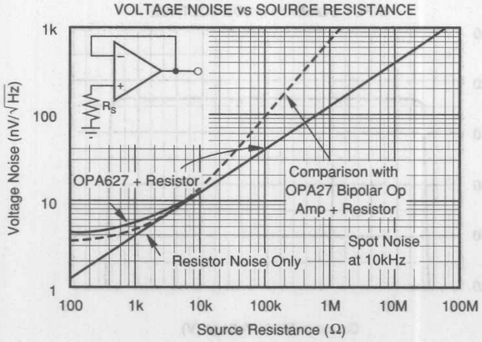
INPUT VOLTAGE NOISE SPECTRAL DENSITY



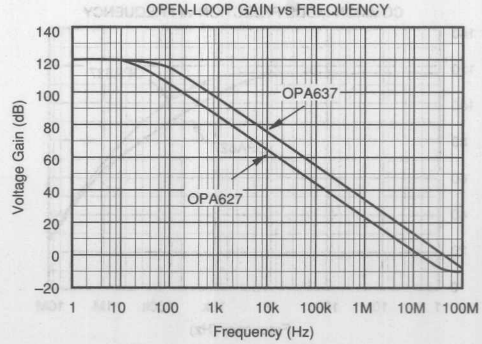
TOTAL INPUT VOLTAGE NOISE vs BANDWIDTH



VOLTAGE NOISE vs SOURCE RESISTANCE

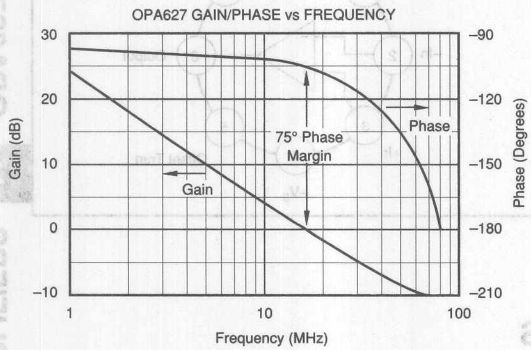


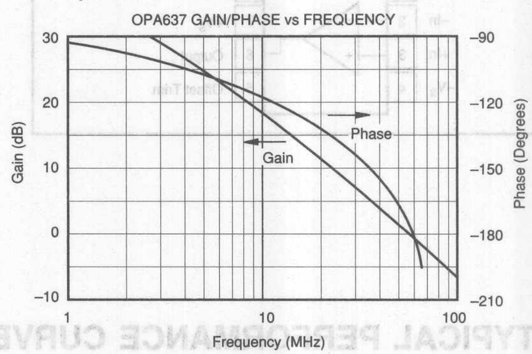
OPEN-LOOP GAIN vs FREQUENCY

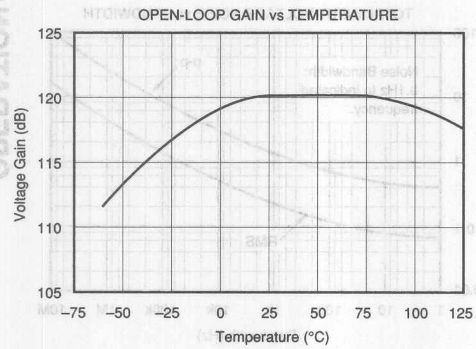


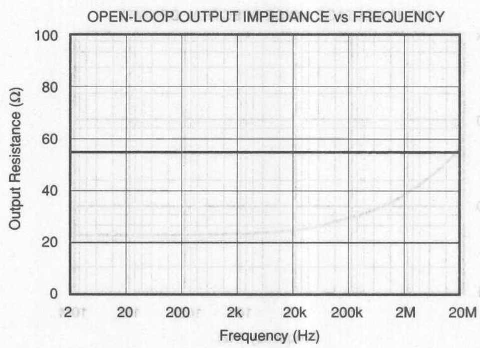
TYPICAL PERFORMANCE CURVES (CONT)

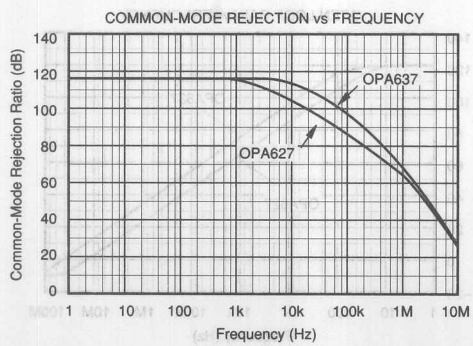
At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

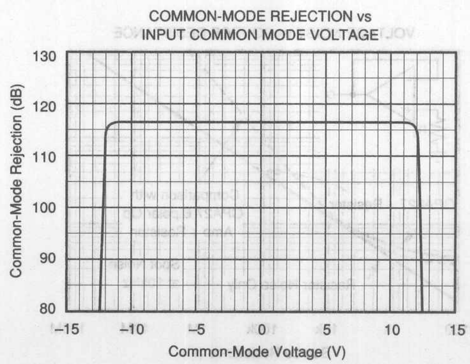






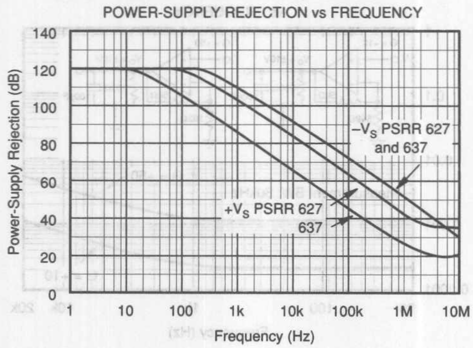


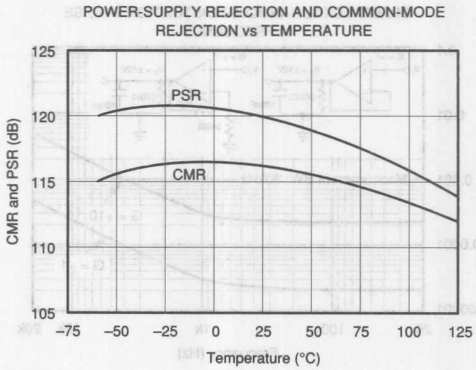


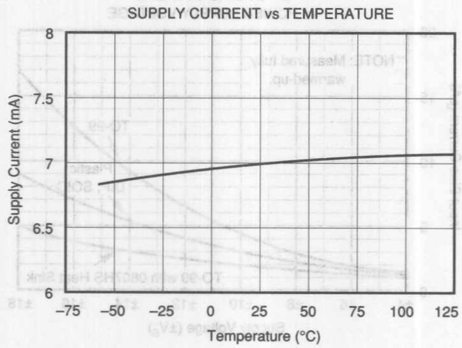


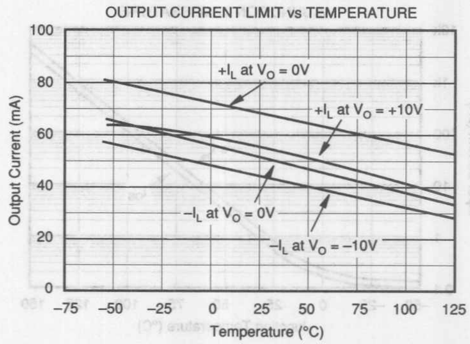
TYPICAL PERFORMANCE CURVES (CONT)

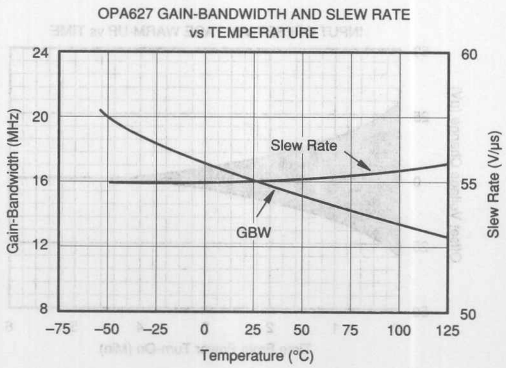
At $T_A = +25°C$, and $V_S = ±15V$, unless otherwise noted.

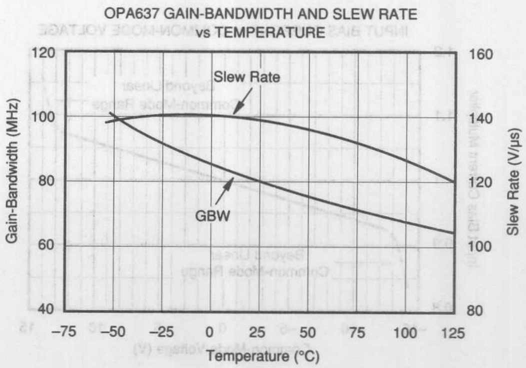






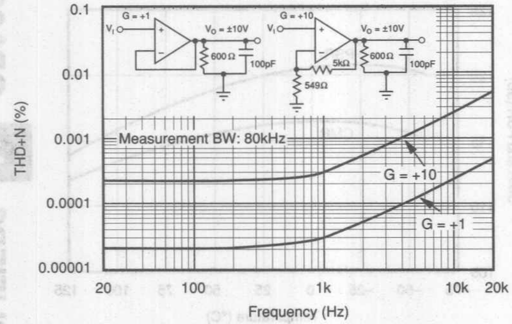




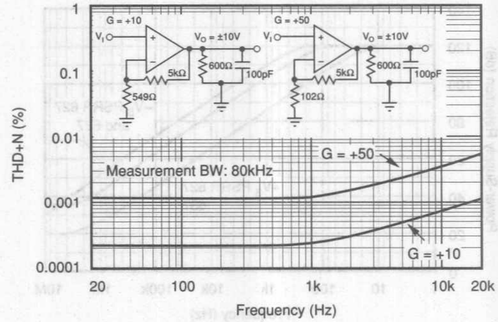


At $T_A = +25°C$, and $V_S = ±15V$, unless otherwise noted.

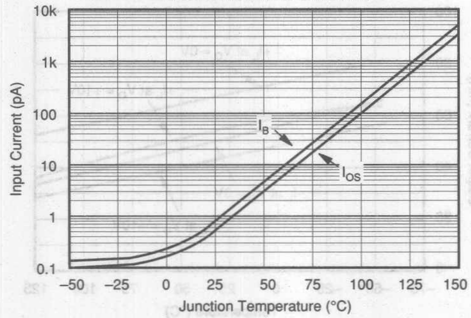
OPA627 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



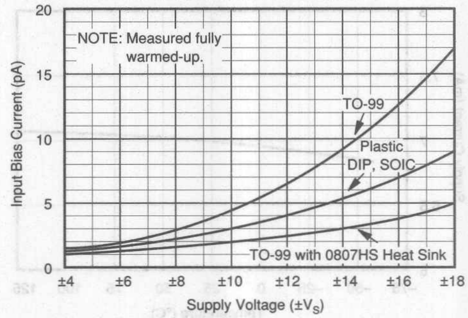
OPA637 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



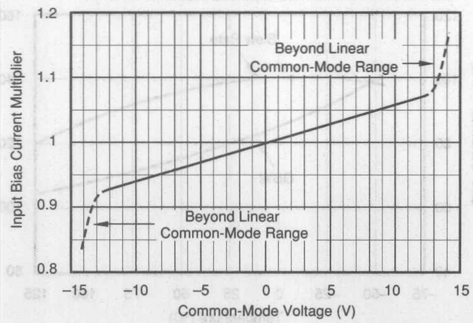
INPUT BIAS AND OFFSET CURRENT vs JUNCTION TEMPERATURE



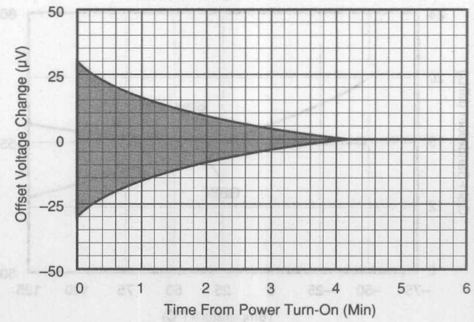
INPUT BIAS CURRENT vs POWER SUPPLY VOLTAGE

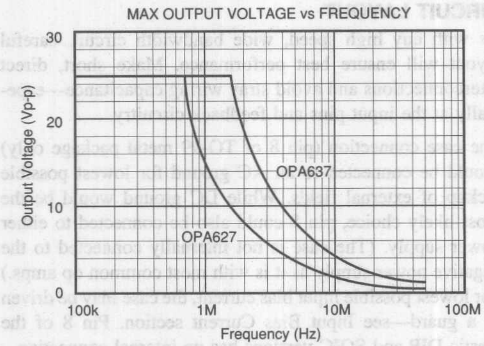


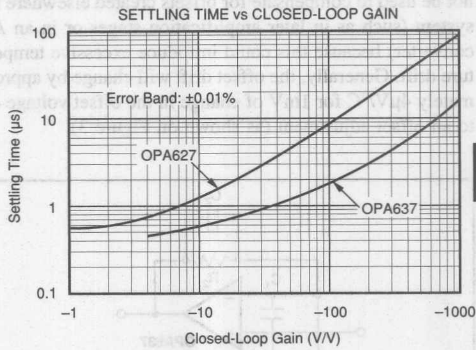
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

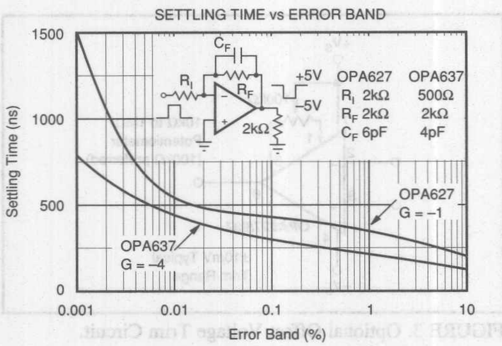


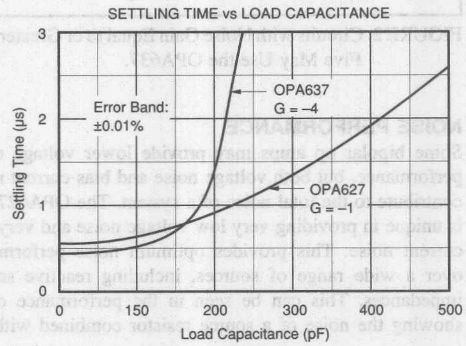
INPUT OFFSET VOLTAGE WARM-UP vs TIME











APPLICATIONS INFORMATION

The OPA627 is unity-gain stable. The OPA637 may be used to achieve higher speed and bandwidth in circuits with noise gain greater than five. Noise gain refers to the closed-loop gain of a circuit as if the non-inverting op amp input were being driven. For example, the OPA637 may be used in a non-inverting amplifier with gain greater than five, or an inverting amplifier of gain greater than four.

When choosing between the OPA627 or OPA637, it is important to consider the high frequency noise gain of your circuit configuration. Circuits with a feedback capacitor (Figure 1) place the op amp in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 2, where a small feedback capacitance is used to compensate for the input capacitance at the op amp's inverting input. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to five or greater, the OPA637 may be used.

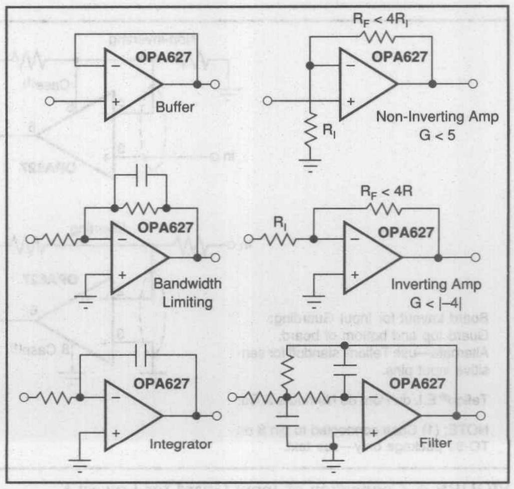


FIGURE 1. Circuits with Noise Gain Less than Five Require the OPA627 for Proper Stability.

OFFSET VOLTAGE ADJUSTMENT

The OPA627/637 is laser-trimmed for low offset voltage and drift, so many circuits will not require external adjustment. Figure 3 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system (such as in later amplification stages or in an A/D converter) because this could introduce excessive temperature drift. Generally, the offset drift will change by approximately 4µV/°C for 1mV of change in the offset voltage due to an offset adjustment (as shown on Figure 3).

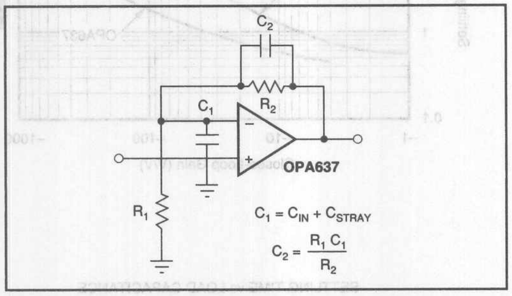


FIGURE 2. Circuits with Noise Gain Equal to or Greater than Five May Use the OPA637.

NOISE PERFORMANCE

Some bipolar op amps may provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA627/637 is unique in providing very low voltage noise and very low current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances. This can be seen in the performance curve showing the noise of a source resistor combined with the noise of an OPA627. Above a 2kΩ source resistance, the op amp contributes little additional noise. Below 1kΩ, op amp noise dominates over the resistor noise, but compares favorably with precision bipolar op amps.

CIRCUIT LAYOUT

As with any high speed, wide bandwidth circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the input pins and feedback circuitry.

The case connection (pin 8 of TO-99 metal package only) should be connected to an AC ground for lowest possible pickup of external fields. While DC ground would be the most likely choice, pin 8 could also be connected to either power supply. (The case is not internally connected to the negative power supply as it is with most common op amps.) For lowest possible input bias current, the case may be driven as a guard—see Input Bias Current section. Pin 8 of the plastic DIP and SOIC versions has no internal connection.

Power supply connections should be bypassed with good high frequency capacitors positioned close to the op amp

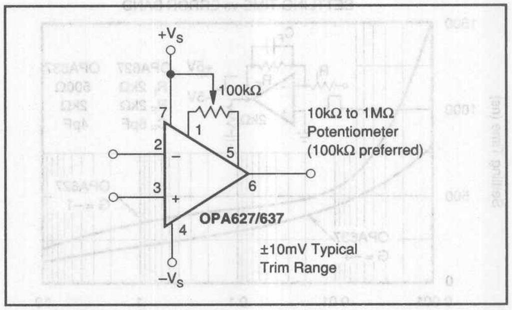


FIGURE 3. Optional Offset Voltage Trim Circuit.

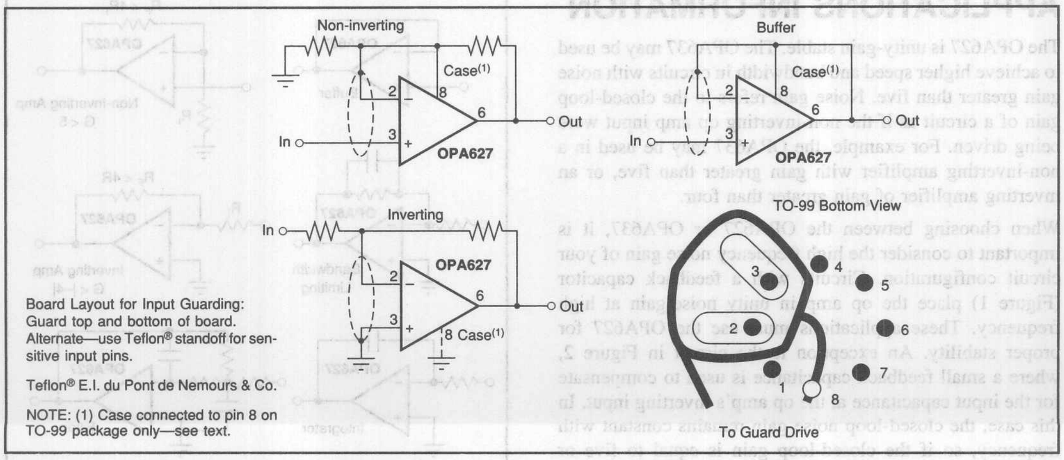


FIGURE 4. Connection of Input Guard for Lowest I_B.

pins. In most cases 0.1μF ceramic capacitors are adequate. The OPA627/637 is capable of high output current (in excess of 45mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1μF solid tantalum capacitors may improve dynamic performance in these applications.

INPUT BIAS CURRENT

Difet fabrication of the OPA627/637 provides very low input bias current. Since the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, the die temperature should be kept as low as possible. The high speed and therefore higher quiescent current of the OPA627/637 can lead to higher chip temperature. A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the I_B to one-third its warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects. See the data sheet on the 807HS for details.

Temperature rise in the plastic DIP and SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces will also help dissipate heat.

The OPA627/637 may also be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±5V power supplies reduces power dissipation to one-third of that at ±15V. This reduces the I_B of TO-99 metal package devices to approximately one-fourth the value at ±15V.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the OPA627/637. A circuit board "guard" pattern (Figure 4) reduces leakage effects. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage current will flow harmlessly to the low-impedance node. The case connection (TO-99 metal package only) may also be driven at guard potential to minimize any leakage which might occur from the input pins to the case. The case is not internally connected to $-V_S$.

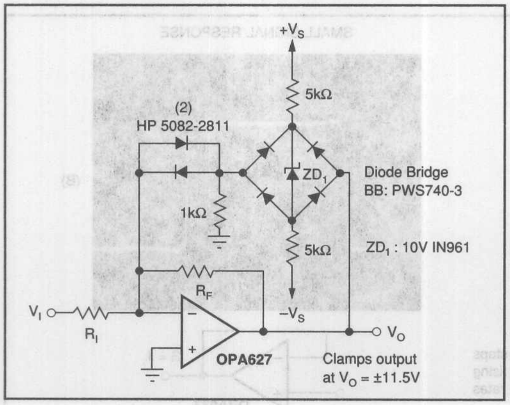


FIGURE 5. Clamp Circuit for Improved Overload Recovery.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be removed with cleaning solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at 85°C.

Many FET-input op amps exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA627/637 virtually constant with wide common-mode voltage changes. This is ideal for accurate high input-impedance buffer applications.

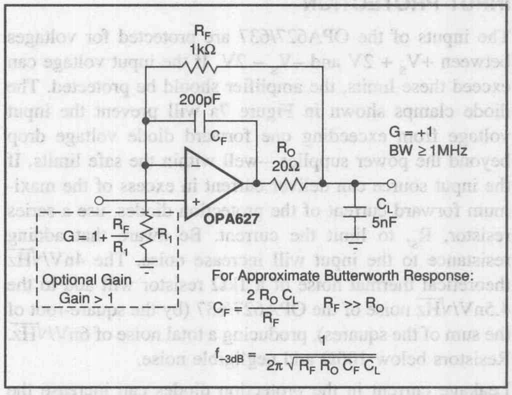


FIGURE 6. Driving Large Capacitive Loads.

PHASE-REVERSAL PROTECTION

The OPA627/637 has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This is most often encountered in non-inverting circuits when the input is driven below –12V, causing the output to reverse into the positive rail. The input circuitry of the OPA627/637 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

OUTPUT OVERLOAD

When the inputs to the OPA627/637 are overdriven, the output voltage of the OPA627/637 smoothly limits at approximately 2.5V from the positive and negative power supplies. If driven to the negative swing limit, recovery takes approximately 500ns. When the output is driven into the positive imit, recovery takes approximately 6μs. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 5. Diodes at the inverting input prevent degradation of input bias current.

As with any high-speed op amp, best dynamic performance can be achieved by minimizing the capacitive load. Since a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow op amp can cause a high-speed op amp to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth of the OPA627 makes it the better choice for driving large capacitive loads. Figure 6 shows a circuit for driving very large load capacitance. This circuit's two-pole response can also be used to sharply limit system bandwidth. This is often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

INPUT PROTECTION

The inputs of the OPA627/637 are protected for voltages between $+V_S + 2V$ and $-V_S - 2V$. If the input voltage can exceed these limits, the amplifier should be protected. The diode clamps shown in Figure 7a will prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies—well within the safe limits. If the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor, R_S, to limit the current. Be aware that adding resistance to the input will increase noise. The $4nV/\sqrt{Hz}$ theoretical thermal noise of a $1k\Omega$ resistor will add to the $4.5nV/\sqrt{Hz}$ noise of the OPA627/637 (by the square-root of the sum of the squares), producing a total noise of $6nV/\sqrt{Hz}$. Resistors below 100Ω add negligible noise.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately 25nA—more than a thousand times larger than the input bias current of the OPA627/637. Leakage current of these diodes is typically much lower and may be adequate in many applications. Light falling on the

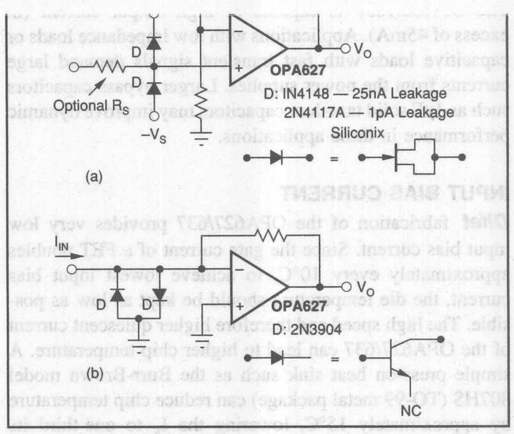
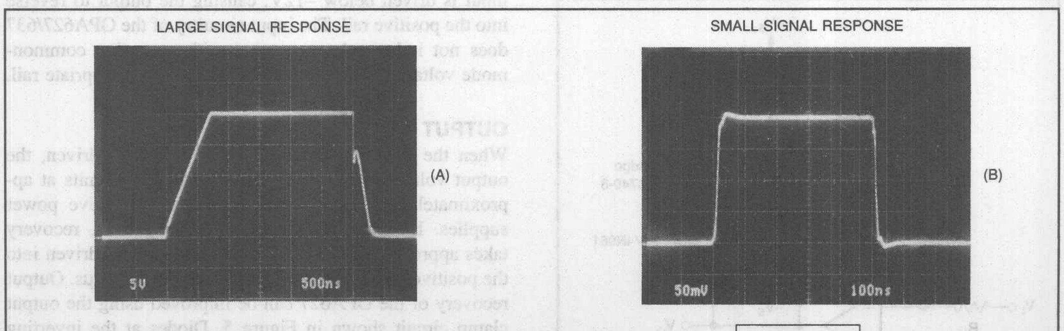


FIGURE 7. Input Protection Circuits.

junction of the protection diodes can dramatically increase leakage current, so common glass-packaged diodes should be shielded from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at 1pA and its metal case shields the junction from light.

Sometimes input protection is required on I/V converters of inverting amplifiers (Figure 7b). Although in normal operation, the voltage at the summing junction will be near zero (equal to the offset voltage of the amplifier), large input transients may cause this node to exceed 2V beyond the power supplies. In this case, the summing junction should be protected with diode clamps connected to ground. Even with the low voltage present at the summing junction, common signal diodes may have excessive leakage current. Since the reverse voltage on these diodes is clamped, a diode-connected signal transistor can be used as an inexpensive low leakage diode (Figure 7b).



When used as a unity-gain buffer, large common-mode input voltage steps produce transient variations in input-stage currents. This causes the rising edge to be slower and falling edges to be faster than nominal slew rates observed in higher-gain circuits.

FIGURE 8. OPA627 Dynamic Performance, G = +1.

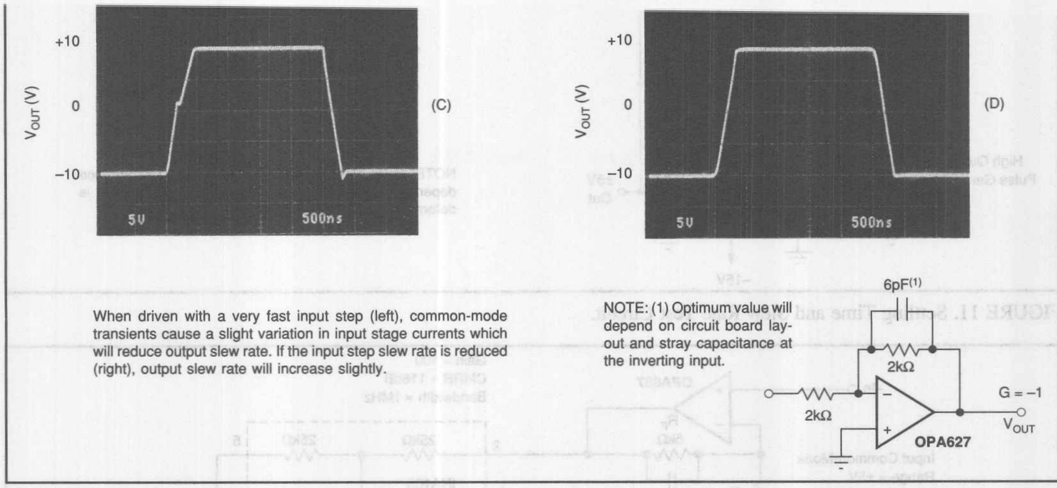


FIGURE 9. OPA627 Dynamic Performance, G = –1.

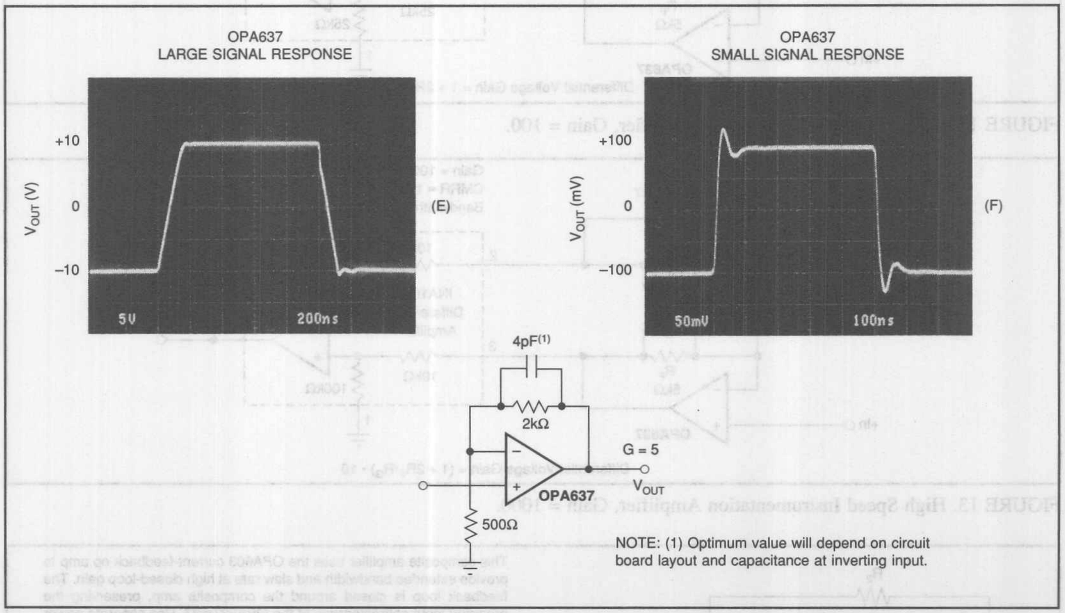
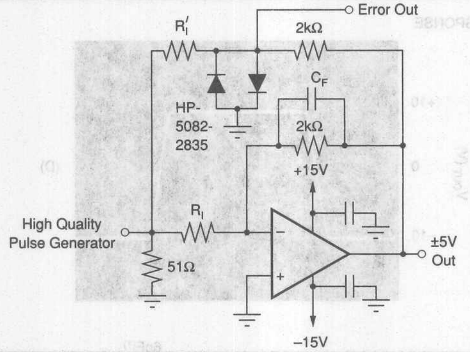


FIGURE 10. OPA637 Dynamic Response, G = 5.



	OPA627	OPA637
R_I, R_I'	2kΩ	500Ω
C_F	6pF	4pF
Error Band (0.01%)	±0.5mV	±0.2mV

NOTE: C_F is selected for best settling time performance depending on test fixture layout. Once optimum value is determined, a fixed capacitor may be used.

FIGURE 11. Settling Time and Slew Rate Test Circuit.

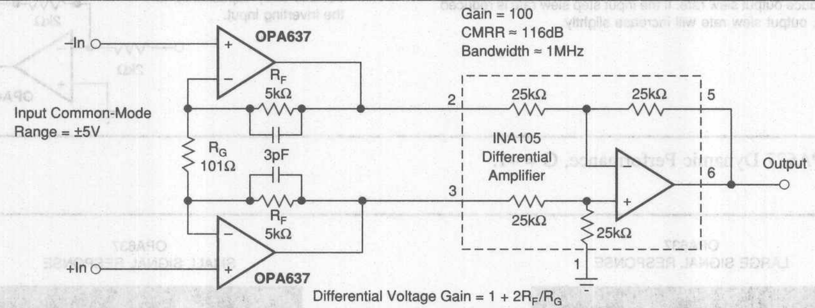
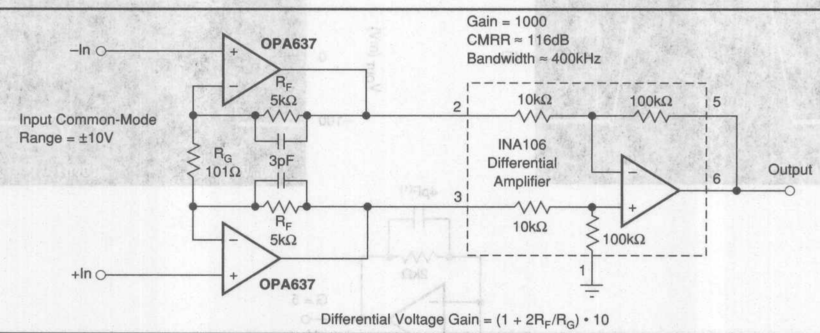


FIGURE 12. High Speed Instrumentation Amplifier, Gain = 100.



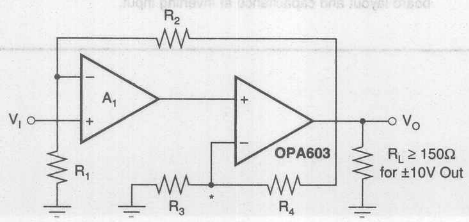


FIGURE 13. High Speed Instrumentation Amplifier, Gain = 1000.

This composite amplifier uses the OPA603 current-feedback op amp to provide extended bandwidth and slew rate at high closed-loop gain. The feedback loop is closed around the composite amp, preserving the precision input characteristics of the OPA627/637. Use separate power supply bypass capacitors for each op amp.

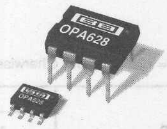
*Minimize capacitance at this node.

GAIN (V/V)	A_1 OP AMP	R_1 (Ω)	R_2 (kΩ)	R_3 (Ω)	R_4 (kΩ)	–3dB (MHz)	SLEW RATE (V/µs)
100	OPA627	50.5(1)	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500

NOTE: (1) Closest 1/2% value.

FIGURE 14. Composite Amplifier for Wide Bandwidth.

BURR-BROWN®



OPA628

Low Distortion Wideband OPERATIONAL AMPLIFIER

FEATURES

- EXCELLENT DIFFERENTIAL GAIN: 0.015%
- EXCELLENT DIFFERENTIAL PHASE: 0.015°
- LOW DISTORTION: 90dB SFDR
- TWO-TONE THIRD-ORDER INTERCEPT: 60dBm
- LOW NOISE: $2.5nV/\sqrt{Hz}$
- LOW NOISE FIGURE: 9dB
- BANDWIDTH (Gain = +1): 160MHz
- 0.1dB GAIN FLATNESS: 30MHz
- LOW OFFSET VOLTAGE: 500µV

APPLICATIONS

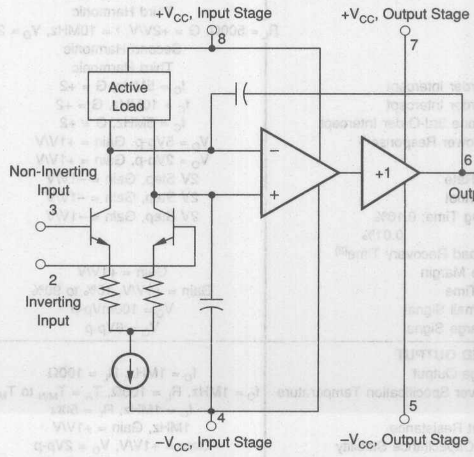
- BROADCAST QUALITY VIDEO
- MEDICAL IMAGING
- LOW NOISE PREAMPLIFIER
- PRECISION ADC/DAC BUFFER
- TELECOMMUNICATIONS
- ANALYTICAL INSTRUMENTS
- ACTIVE FILTERS
- DC RESTORATION CIRCUITS

DESCRIPTION

The OPA628 is a low distortion, wideband operational amplifier. It features low differential gain error of 0.015% and low differential phase error of 0.015° at NTSC and PAL frequencies with a 150Ω load (a back-terminated 75Ω cable). The 0.1dB gain flatness to 30MHz, and the excellent differential gain and phase make the OPA628 ideal for broadcast quality video applications. In addition, the spurious free dynamic range of 90dB makes the OPA628 an excellent choice to buffer the input of precision Analog-to-Digital converters. It can also be used to provide a buffer for the output of precision high speed Digital-to-Analog converters. The two-tone third-order intercept of the OPA628 is 60dBm.

The OPA628 is a unity gain stable, voltage feedback operational amplifier. It has all of the benefits associated with voltage feedback amplifiers including high input impedance, high common mode rejection, and symmetrical differential input flexibility. The unity gain bandwidth of the OPA628 is 160MHz. The low noise of $2.5nV/\sqrt{Hz}$ and low noise figure of 9dB ($R_S = 50\Omega$) make the OPA628 very useful in precision applications requiring wide dynamic range.

The superior distortion performance of the OPA628 is achieved by its multistage architecture which provides high open-loop gain. The distortion performance is additionally enhanced by separating the power supplies to the input and output stages requiring four power supply connections as shown in the block diagram below. This separation of supplies eliminates the effects of package and wire bond parasitic capacitance and inductance. The OPA628 is powered with ±5VDC supplies for low power dissipation. The OPA628 is available in 8-pin plastic DIP and SOIC packages. The temperature range is –40°C to +85°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

At V_{CC} = ±5VDC, R_L=100Ω (including feedback impedance), and T_A = +25°C, unless otherwise noted.

		OPA628AP, AU			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT NOISE					
Voltage: R_S = 0Ω	f_O = 100Hz		8.3		nV/√Hz
	f_O = 1kHz		3.5		nv/√Hz
	f_O = 10kHz		2.6		nV/√Hz
	f_O = 100kHz		2.5		nV/√Hz
	f_O = 1MHz to 100MHz		2.5		nV/√Hz
	f_B = 100Hz to 10MHz		8.1		µVrms
Current	f_O = 100kHz to 100MHz		2.2		pA/√Hz
Noise Figure	R_S = 50Ω, f_O = 1MHz to 100MHz		9.3		dB
OFFSET VOLTAGE					
Input Offset Voltage	V_{CM} = 0VDC		±0.5	±1	mV
Average Drift	T_A = T_{MIN} to T_{MAX}		±6		µV/°C
Supply Rejection (PSRR)	±V_{CC} = ±4.5V to ±5.5V	90	105		dB
Over Specification Temperature	±V_{CC} = ±4.5V to ±5.5V, T_A = T_{MIN} to T_{MAX}		100		dB
INPUT BIAS CURRENT					
Input Bias Current	V_{CM} = 0VDC		15	30	µA
Over Specification Temperature	V_{CM} = 0VDC, T_A = T_{MIN} to T_{MAX}		22		µA
Input Offset Current	V_{CM} = 0VDC		±0.3	±2	µA
Over Specification Temperature	T_A = T_{MIN} to T_{MAX}		±0.8		µA
INPUT IMPEDANCE					
Differential	Open–Loop		30 ‖ 2		kΩ ‖ pF
Common-Mode			10 ‖ 6		MΩ ‖ pF
INPUT VOLTAGE RANGE					
Common-Mode Input Range			±2.5		V
Common-Mode Rejection (CMRR)	V_{CM} = ±2.5V	90	110		dB
Over Specification Temperature	V_{CM} = ±2.5V, T_A = T_{MIN} to T_{MAX}		105		dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain		90	100		dB
Over Specification Temperature	T_A = T_{MIN} to T_{MAX}		96		dB
FREQUENCY RESPONSE					
Closed-Loop Bandwidth	Gain = +1V/V		160		MHz
(–3dB)	Gain = +2V/V		77		MHz
	Gain = +5V/V		24		MHz
Bandwidth 0.1dB Flat	Gain = +2V/V		30		MHz
Differential Gain	3.58MHz, Gain = +2, V_O = 1.4V Ramp		0.015		%
Differential Phase	3.58MHz, Gain = +2, V_O = 1.4V Ramp		0.015		degrees
Harmonic Distortion	R_L = 100Ω, G = +1V/V, f = 5MHz, V_O = 2Vp-p				
	Second Harmonic		–91		dBc
	Third Harmonic		–98		dBc
	R_L = 500Ω, G = +2V/V, f = 5MHz, V_O = 2Vp-p				
	Second Harmonic		–90		dBc
	Third Harmonic		–97		dBc
	R_L = 500Ω, G = +2V/V, f = 10MHz, V_O = 2Vp-p				
	Second Harmonic		–83		dBc
	Third Harmonic		–87		dBc
3rd-Order Intercept	f_C = 5MHz, G = +2		70		dBm
3rd-Order Intercept	f_C = 10MHz, G = +2		60		dBm
Two-tone 3rd-Order Intercept	f_C = 5MHz, G = +2		60		dBm
Full Power Response(1)	V_O = 5Vp-p, Gain = +1V/V		20		MHz
	V_O = 2Vp-p, Gain = +1V/V		49		MHz
Slew Rate	2V Step, Gain = –1V/V		310		V/µs
Overshoot	2V Step, Gain = –1V/V		2		%
Settling Time: 0.10%	2V Step, Gain = –1V/V		20		ns
0.01%			64		ns
Overload Recovery Time(2)			60		ns
Phase Margin	Gain = +1V/V		60		degrees
Rise Time	Gain = +1V/V, 10% to 90%				
Small Signal	V_O = 100mVp-p		3		ns
Large Signal	V_O = 6Vp-p		15		ns
RATED OUTPUT					
Voltage Output	f_O = 1MHz, R_L = 100Ω	±3			V
Over Specification Temperature	f_O = 1MHz, R_L = 100Ω, T_A = T_{MIN} to T_{MAX}		±3		V
	f_O = 1MHz, R_L = 50Ω		±3		V
Output Resistance	1MHz, Gain = +1V/V		0.0005		Ω
Load Capacitance Stability	Gain = +1V/V, V_O = 2Vp-p		20		pF
Short Circuit Current	Continuous, Source		+180		mA
Short Circuit Current	Continuous, Sink		–130		mA

ELECTRICAL

At V_{CC} = ±5VDC, R_L=100Ω (including feedback impedance), and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA628AP, AU MIN	TYP	MAX	UNITS
POWER SUPPLY					
Rated Voltage	$\pm V_{CC}$		±5		VDC
Derated Performance	$\pm V_{CC}$	±4.5		±6	VDC
Current, Quiescent	I_O = 0mADC		29	32	mA
Current, Quiescent	I_O = 0mADC, T_A = T_{MIN} to T_{MAX}		31	35	mA
TEMPERATURE RANGE					
Specification: AP, AU	T_{MIN} and T_{MAX}	–40		+85	°C
Storage: AP, AU	Ambient Temperature	–55		+125	°C
θ_{JA} AP			90		°C/W
AU			100		°C/W

NOTES: (1) Full power response = slew rate/(2πVpeak). (2) Time for output to resume linear operation after saturation.

ORDERING INFORMATION

MODEL	PACKAGE
OPA628AP	8-Pin Plastic DIP
OPA628AU	8-Pin SOIC

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA628AP	8-Pin Plastic DIP	006
OPA628AU	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

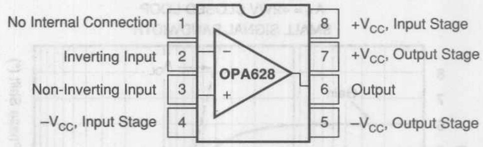
ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation(1)	See Applications Information
Differential Input Voltage	5V
Input Voltage Range	See Applications Information
Storage Temperature Range: AP, AU	–55°C to +125°C
Lead Temperature (soldering, DIP 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PIN CONFIGURATION

Top View **8-Pin Plastic DIP** **8-Pin Plastic SOIC**



ELECTROSTATIC DISCHARGE SENSITIVITY

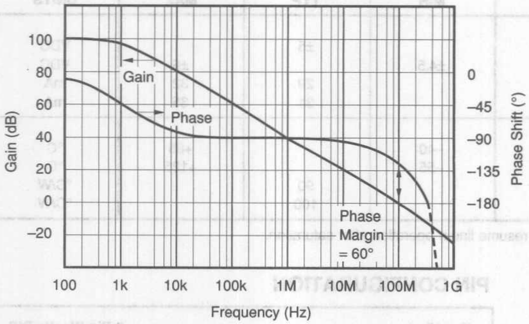
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

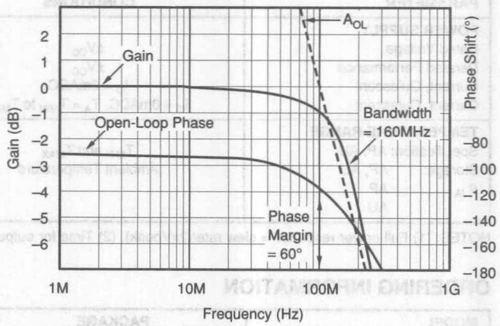
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_L = 100Ω (including feedback impedance), and T_A = +25°C unless otherwise noted.

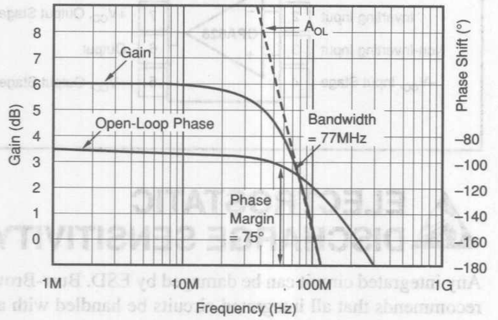
OPEN-LOOP FREQUENCY RESPONSE



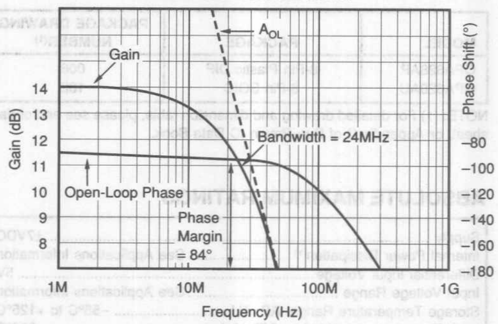
A_V = +1V/V CLOSED-LOOP SMALL SIGNAL BANDWIDTH



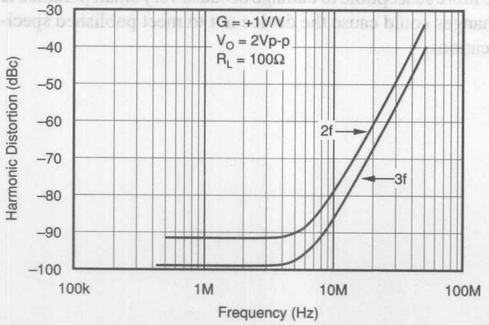
A_V = +2V/V CLOSED-LOOP SMALL SIGNAL BANDWIDTH



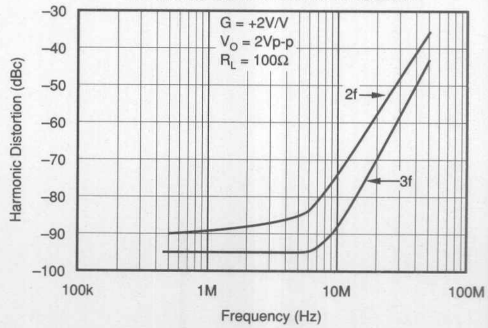
A_V = +5V/V CLOSED-LOOP SMALL SIGNAL BANDWIDTH



HARMONIC DISTORTION vs FREQUENCY

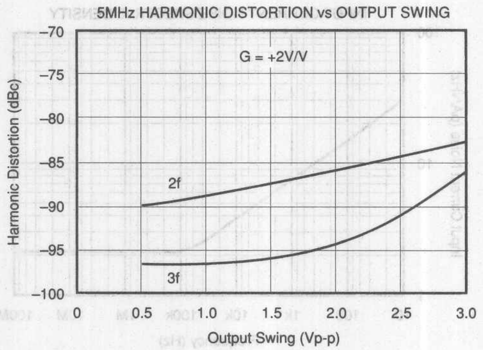


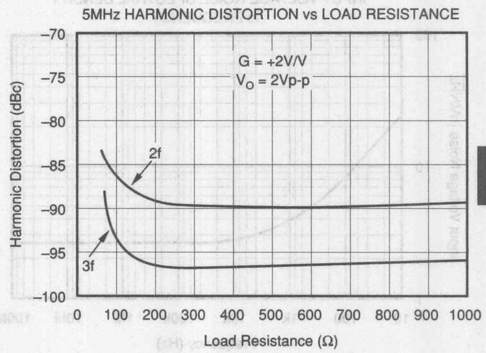
HARMONIC DISTORTION vs FREQUENCY

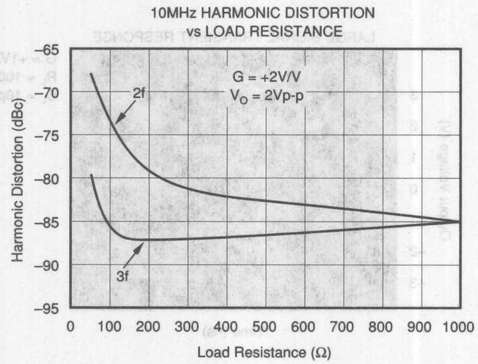


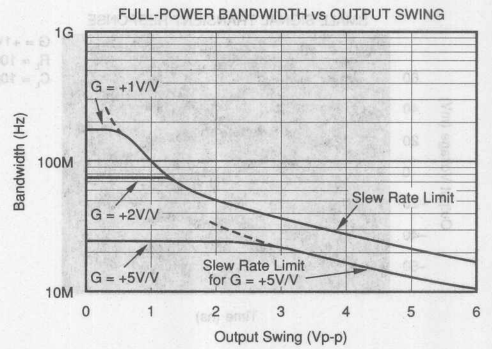
TYPICAL PERFORMANCE CURVES (CONT)

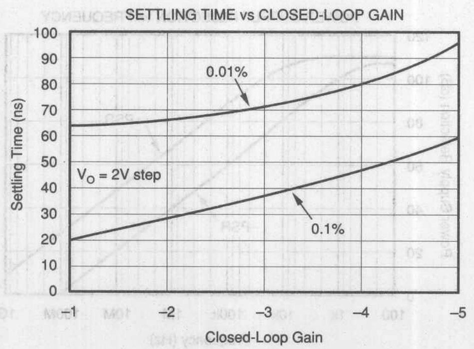
At V_{CC} = ±5VDC, and R_L = 100Ω (including feedback impedance), and T_A = +25°C unless otherwise noted.

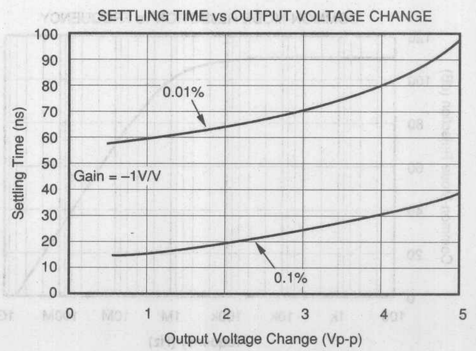




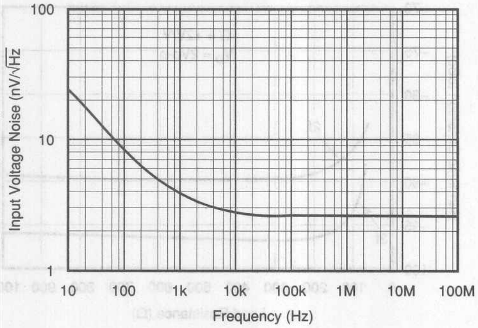


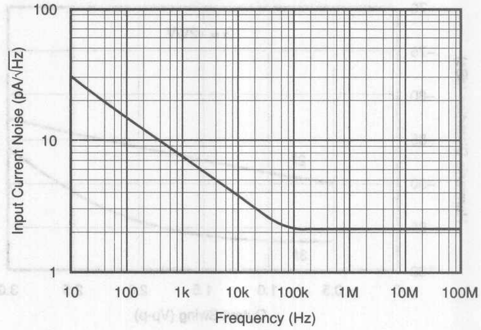


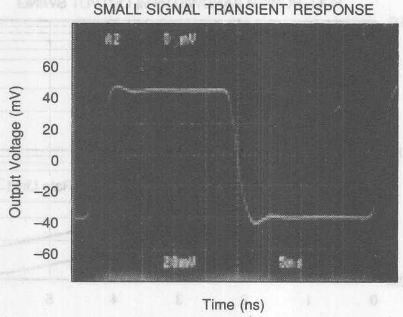


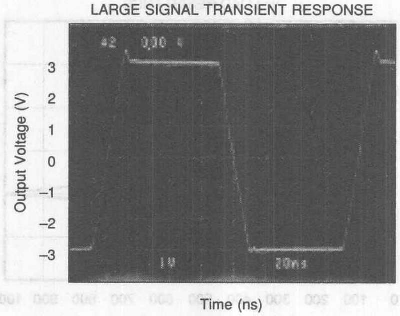


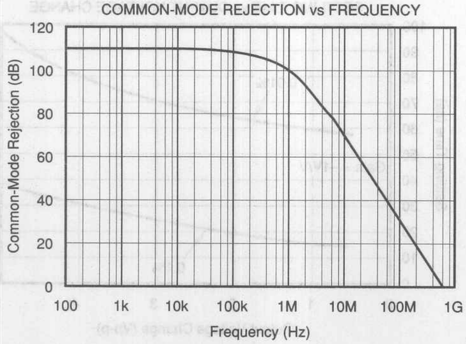
At V_{CC} = ±5VDC, R_L = 100Ω (including feedback impedance), and T_A = +25°C unless otherwise noted.

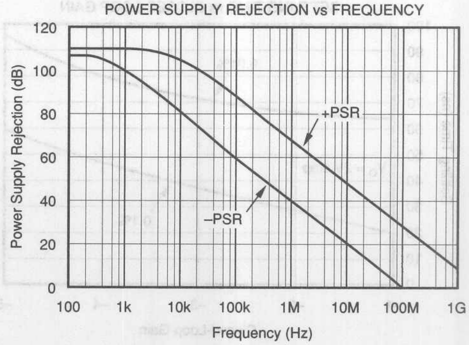








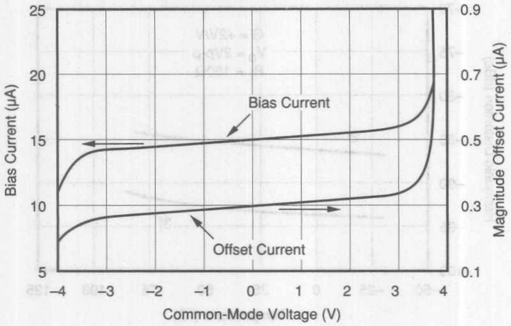




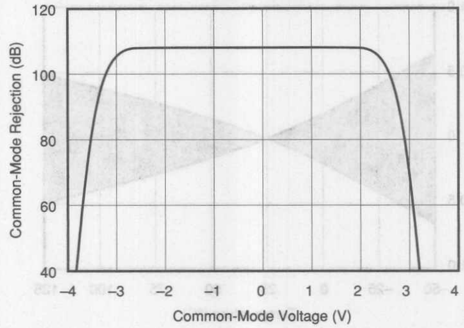
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω (including feedback impedance), and T_A = +25°C unless otherwise noted.

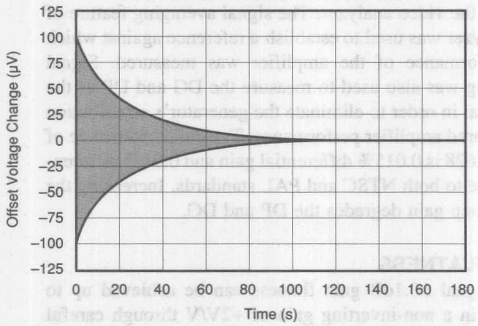
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



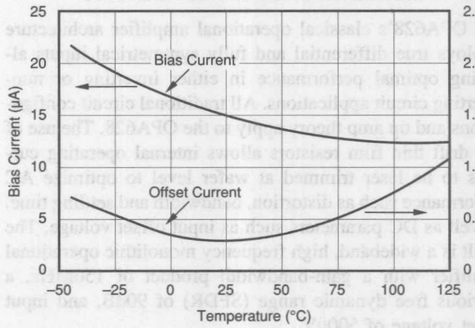
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



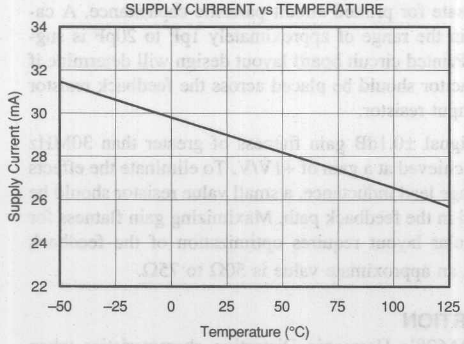
INPUT OFFSET VOLTAGE WARM-UP DRIFT



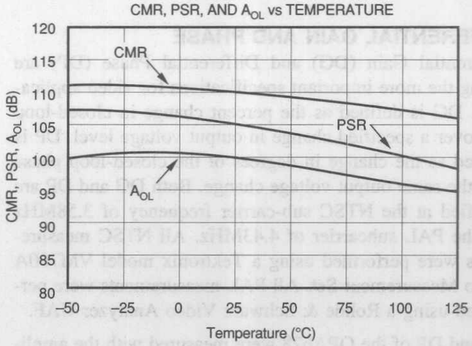
BIAS AND OFFSET CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



CMR, PSR, AND A_{OL} vs TEMPERATURE



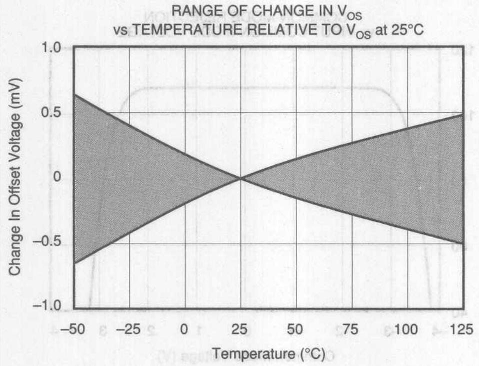
OPA628

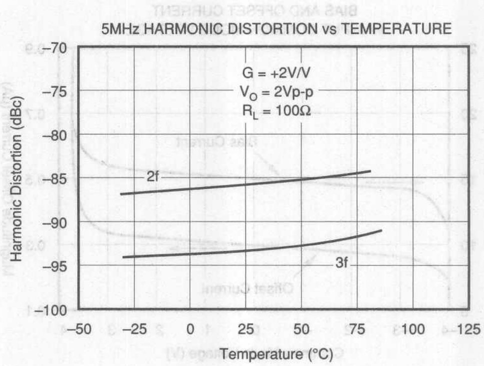
2

OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω (including feedback impedance), and T_A = +25°C unless otherwise noted.





DISCUSSION OF PERFORMANCE

The OPA628's classical operational amplifier architecture employs true differential and fully symmetrical inputs allowing optimal performance in either inverting or non-inverting circuit applications. All traditional circuit configurations and op amp theory apply to the OPA628. The use of low drift thin film resistors allows internal operating currents to be laser trimmed at wafer level to optimize AC performance such as distortion, bandwidth and settling time, as well as DC parameters such as input offset voltage. The result is a wideband, high frequency monolithic operational amplifier with a gain-bandwidth product of 150MHz, a spurious free dynamic range (SFDR) of 90dB, and input offset voltage of 500µV.

The layout considerations described in the "Printed Circuit Board Guidelines" section must be followed to achieve the best possible performance of the OPA628.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set. All PAL measurements were performed using a Rohde & Schwarz Video Analyzer UAF.

DG and DP of the OPA628 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 1 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA628 is 0.015% differential gain and 0.015° differential phase to both NTSC and PAL standards. Increasing the closed-loop gain degrades the DP and DG.

GAIN FLATNESS

Small signal ±0.1dB gain flatness can be achieved up to 30MHz in a non-inverting gain of +2V/V through careful layout of the printed circuit board and frequency shaping of the feedback network. Frequency shaping is achieved empirically by placing a small capacitor in parallel with either the feedback resistor or the input resistor of the OPA628 to compensate for printed circuit parasitic capacitance. A capacitor in the range of approximately 1pF to 20pF is suggested. Printed circuit board layout design will determine if the capacitor should be placed across the feedback resistor or the input resistor.

Small signal ±0.1dB gain flatness of greater than 30MHz can be achieved at a gain of +1V/V. To eliminate the effects of package lead inductance, a small value resistor should be included in the feedback path. Maximizing gain flatness for a particular layout requires optimization of the feedback resistor; an approximate value is 50Ω to 75Ω.

DISTORTION

The OPA628's Harmonic Distortion characteristics when driving a 100Ω load are shown vs frequency and vs voltage output in the Typical Performance Curves. Distortion can be further optimized by decreasing output loading as also

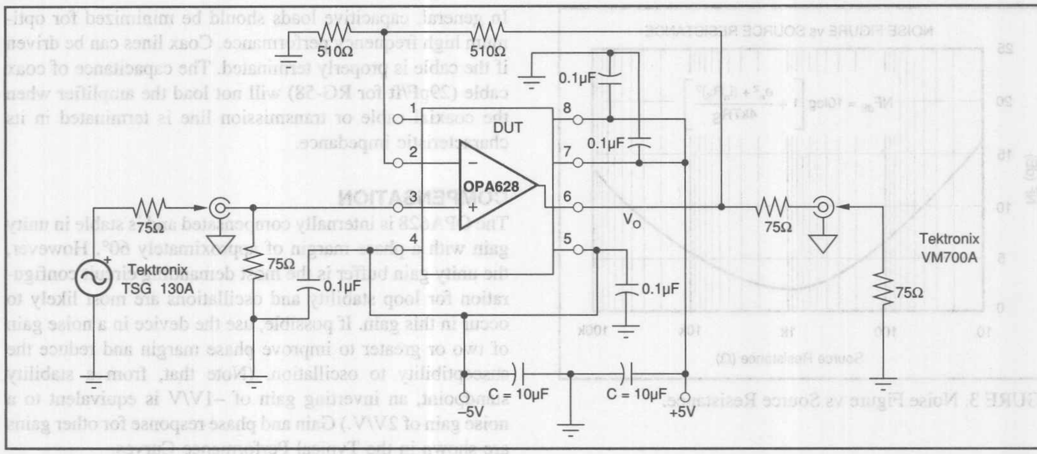


FIGURE 1. Configuration For Testing Differential Gain/Phase.

shown in Typical Performance Curves. Include the contribution of the feedback resistance when calculating the effective load resistance at the amplifier output. A high performance spectrum analyzer such as the HP3585B should be used to measure distortion.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. The specification table shows the OPA628's two-tone, third order IM intercept at 5MHz and 10MHz. For these measurements, tones were spaced 200kHz apart. This data is particularly useful for determining the magnitude of the third-order IM products. The magnitude of the third-order IM products can be easily calculated from the expression:

$$\text{Third IM} = 2(OPI^3P - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level/tone, dBm/tone
Third IM = third-order intermodulation ratio below each output tone, dB

As an example, with OPI^3P = 60dBm, for P_O = 10dBm, the third order IM = 2(60 – 10) = 100dB below either 10dBm tone. The OPA628's low IM makes the device an excellent choice for a variety of RF signal processing applications. In order to obtain the full low distortion performance of the OPA628, it is imperative to follow the recommendations described in the "Printed Circuit Board Guidelines" section.

OUTPUT DRIVE CAPABILITY

The OPA628 has been optimized for low distortion performance with back terminated 50Ω and 75Ω loads (R_{LOAD} = 100Ω and 150Ω, respectively). However, it is capable of driving 6Vpp into a 50Ω load with a sacrifice in distortion. This high-output drive capability makes the OPA628 an ideal choice for a wide range of RF, IF, and video applications. All transmission lines should be terminated with the characteristic impedance of the transmission line.

Internal current-limiting circuitry limits output current to about 130mA at 25°C. This prevents damage from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 2, the OPA628 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

NOISE FIGURE

The OPA628's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA628's Noise Figure vs Source Resistance is shown in Figure 3 for frequencies above 1MHz.

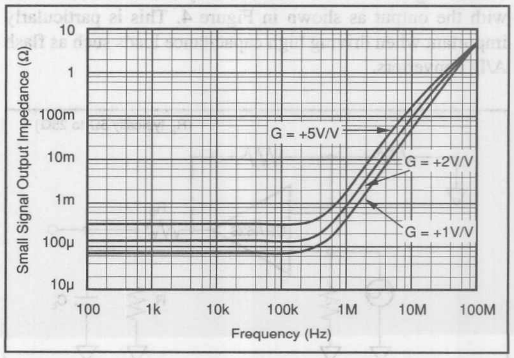


FIGURE 2. Small Signal Output Impedance vs Frequency.

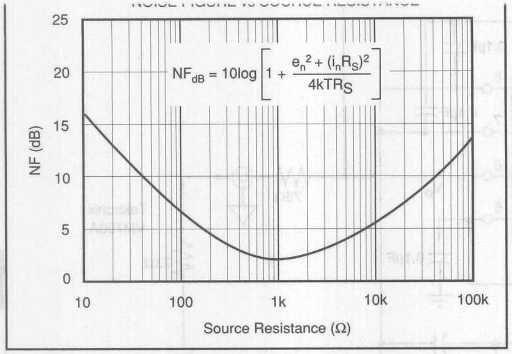


FIGURE 3. Noise Figure vs Source Resistance.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V. Settling time, specified in an inverting gain of one, is only 64ns to 0.01% for a 2V step. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Printed Circuit Board Guidelines." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 60ns. Settling time measurements for the OPA628 were performed in the circuit configuration of Figure 5. A sampling oscilloscope was used with signal averaging.

CAPACITIVE LOADS

Capacitive loads will decrease the OPA628's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 20pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters.

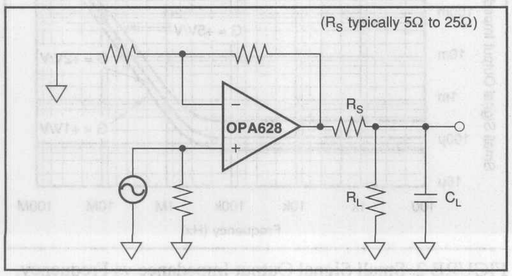


FIGURE 4. Driving Capacitive Loads.

mum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/ft for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA628 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2V/V.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA628 in a good layout is very flat with frequency. However, some circuit configurations, such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

THERMAL CONSIDERATIONS

The OPA628 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 6.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, P_{DQ} = 10V X 32mA = 320mW, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage (V_{OUT}) the maximum valueofP_{DL}occurs at $V_{OUT} = V_{CC}/2$, and is equal to P_{DL}, max = $(V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common P_{DL} = 5V X 180mA = 900mW. Thus, P_D, max = 320mW + 900mW ≈ 1.2W.

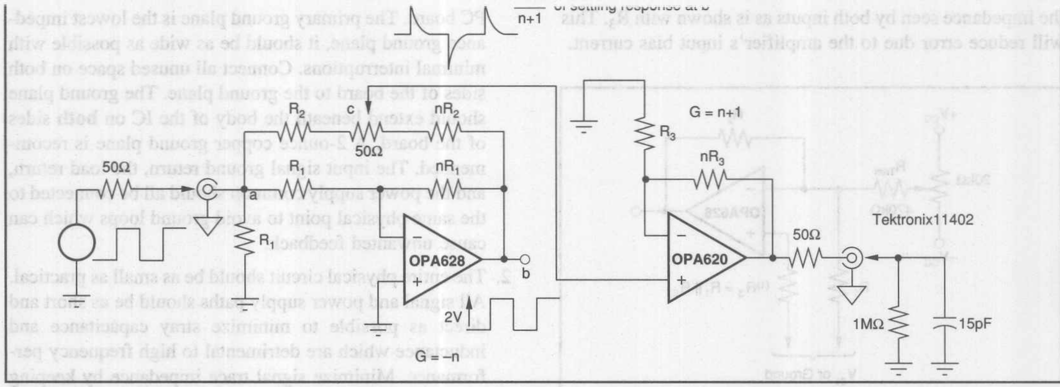


FIGURE 5. Settling Time Test Circuit.

Note that the short circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1.2W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, θ_{JA}, of each package. The variation of short circuit current with temperature is shown in Figure 7.

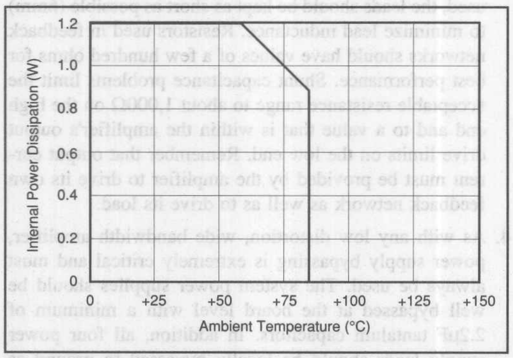


FIGURE 6. Maximum Power Dissipation.

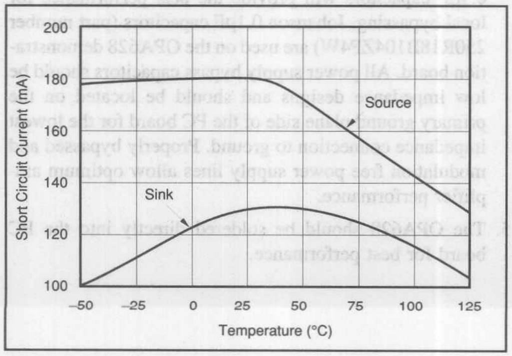


FIGURE 7. Short Circuit Current vs Temperature.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA628 incorporates on-chip ESD protection diodes as shown in Figure 8. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

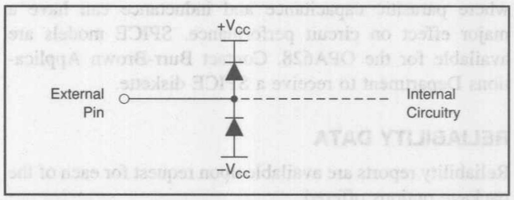


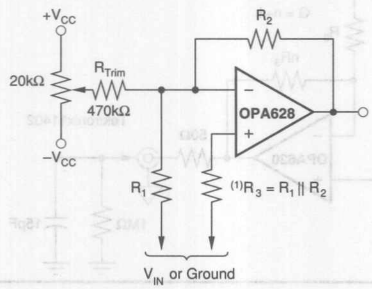
FIGURE 8. Internal ESD Protection.

All pins on the OPA628 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to approximately 10mA whenever possible.

OFFSET VOLTAGE ADJUSTMENT

The OPA628's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 9 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by

the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce error due to the amplifier's input bias current.



Output Trim Range $\equiv +V_{CC}\left(\frac{R_2}{R_{Trim}}\right)$ to $-V_{CC}\left(\frac{R_2}{R_{Trim}}\right)$

NOTE: (1) R_3 is optional and can be used to reduce error due to input bias currents.

FIGURE 9. Offset Voltage Trim.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA628. Contact Burr-Brown Applications Department to receive a SPICE diskette.

RELIABILITY DATA

Reliability reports are available upon request for each of the package options offered.

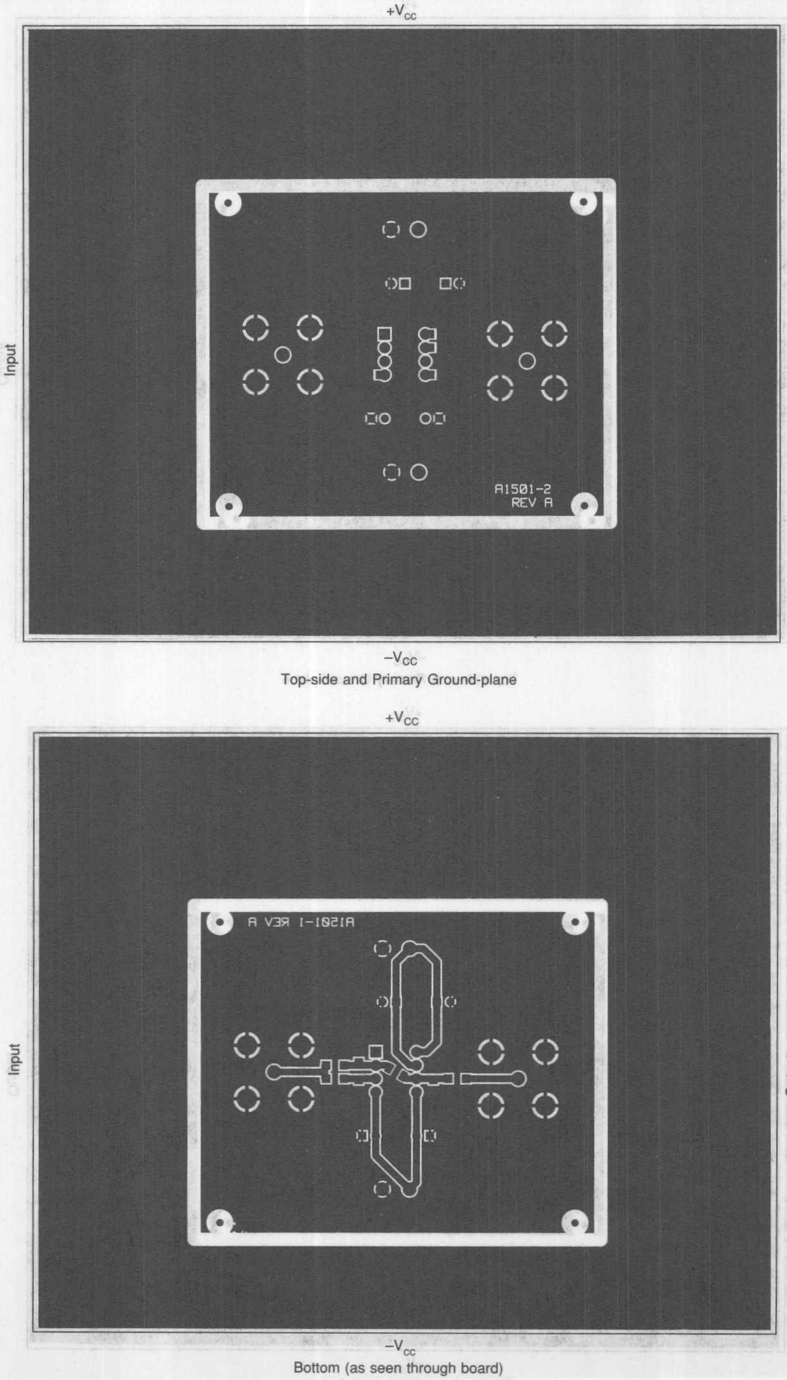
DEMONSTRATION BOARDS

Contact Burr-Brown Applications Department for availability of demonstration boards for the OPA628. There are separate demonstration boards for the DIP and SOIC packages. These demonstration boards use the PC board layouts shown in Figures 10a and 10b. They are carefully designed for optimum low distortion performance as described in the wiring precaution section.

PRINTED CIRCUIT BOARD GUIDELINES

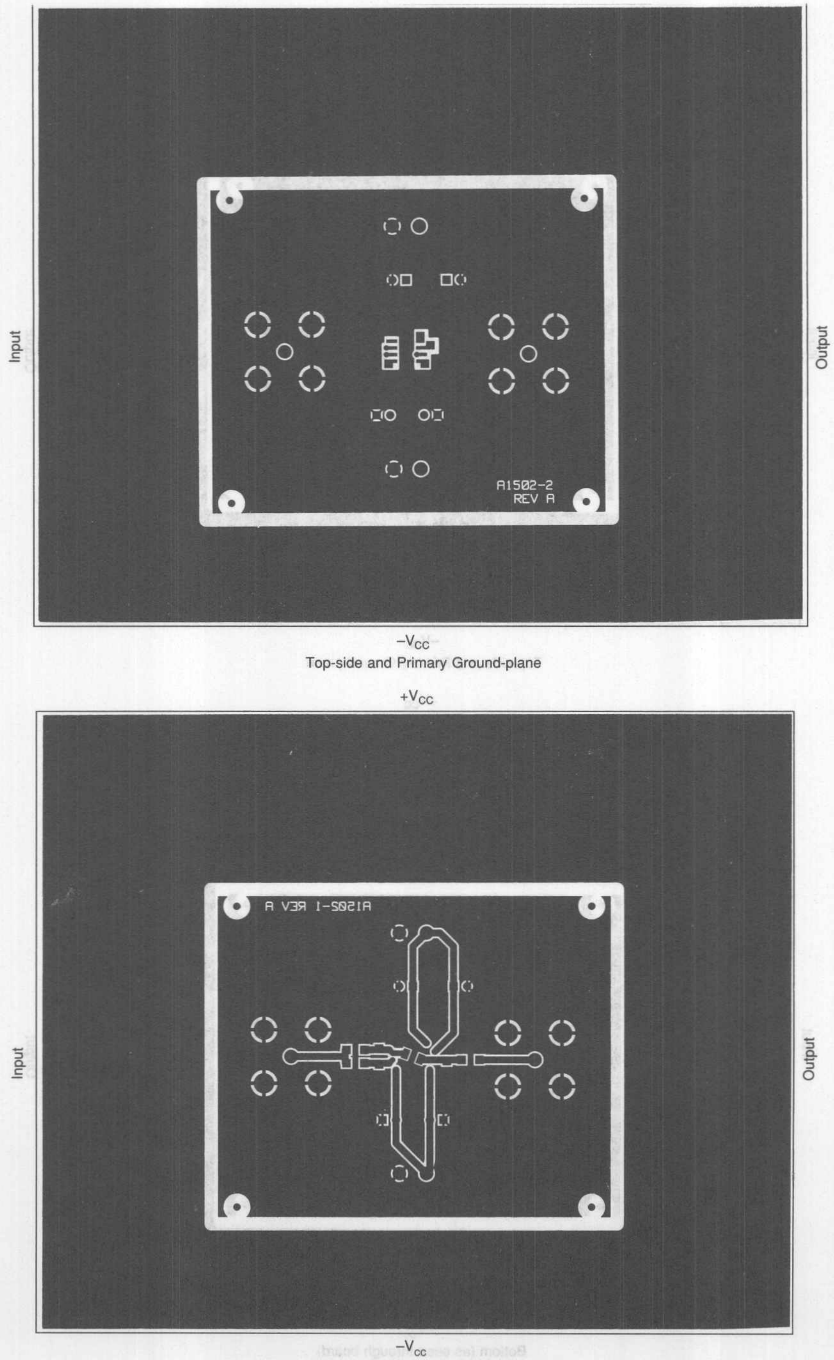
The printed circuit board layout is critical to obtaining the full performance of the OPA628, particularly optimum distortion and gain flatness. The guidelines below should be employed to design the OPA628 printed circuit board. Conceptual layouts illustrating these guidelines for the DIP and SOIC packages are shown in Figures 10a and 10b.

1. Establish the primary ground plane on the IC side of the PC board. The primary ground plane is the lowest impedance ground plane, it should be as wide as possible with minimal interruptions. Connect all unused space on both sides of the board to the ground plane. The ground plane should extend beneath the body of the IC on **both** sides of the board. A 2-ounce copper ground plane is recommended. The input signal ground return, the load return, and the power supply common should all be connected to the same physical point to avoid ground loops which can cause unwanted feedback.
2. The entire physical circuit should be as small as practical. All signal and power supply paths should be as short and direct as possible to minimize stray capacitance and inductance which are detrimental to high frequency performance. Minimize signal trace impedance by keeping traces as wide and short as possible. Stray capacitance should be minimized, especially at high impedance nodes such as the amplifier's input terminals. In addition, stray signal coupling from the output of the amplifier back to the input should be minimized.
3. In general, the use of surface mount components improves performance over through-hole components by minimizing parasitics. (However, it should be noted that use of the DIP version of the OPA628 will not compromise amplifier performance.) If circuit elements with leads are used, the leads should be kept as short as possible (6mm) to minimize lead inductance. Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1,000Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load.
4. As with any low distortion, wide bandwidth amplifier, power supply bypassing is extremely critical and must always be used. The system power supplies should be well bypassed at the board level with a minimum of 2.2µF tantalum capacitors. In addition, all four power supply leads should be locally bypassed to ground as close as possible to the amplifier pins. Surface mount 0.1µF capacitors will provide the best performance for local bypassing. Johanson 0.1µF capacitors (part number 250R18B104ZP4W) are used on the OPA628 demonstration board. All power supply bypass capacitors should be low impedance designs and should be located on the primary ground plane side of the PC board for the lowest impedance connection to ground. Properly bypassed and modulation free power supply lines allow optimum amplifier performance.
5. The OPA628 should be soldered directly into the PC board for best performance.



NOTES: (1) Pin 1 designated by rectangular pad. (2) DUT inserted Top-side. (3) Power supply by-pass caps installed at pin locations on Top-side. (4) All unused area on both sides connected to primary ground-plane. (5) Continue ground-plane under DUT both sides.

FIGURE 10a. Conceptual PCB Layout (8-pin DIP).



Top-side and Primary Ground-plane

Bottom (as seen through board)

NOTES: (1) Pad 1 designated by smallest rectangle. (2) DUT installed Top-side. (3) Power supply bypass caps installed at pad locations on Top-side. (4) All unused area on both sides connected to primary ground-plane. (5) Continue ground-plane under DUT both sides.

FIGURE 10b. Conceptual PCB Layout (8-pin SOIC).

APPLICATIONS

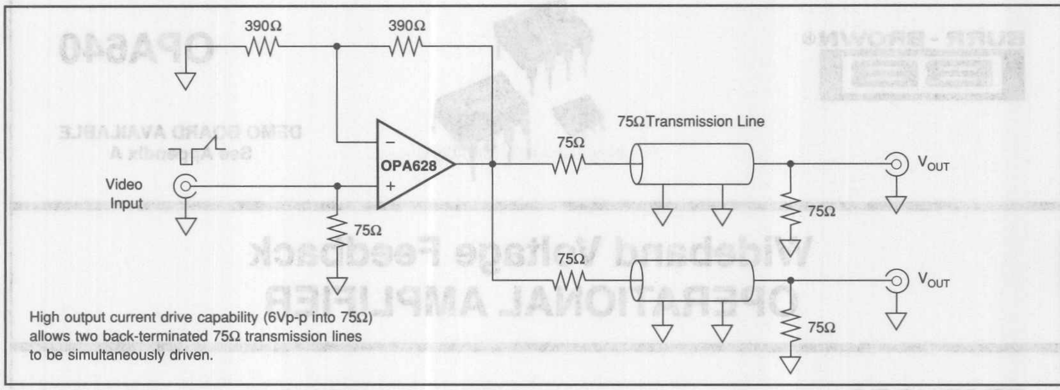
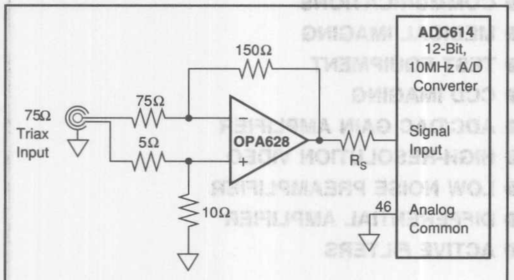


FIGURE 11. Video Distribution Amplifier.



NOTE: The value of R_S varies with the value of the input capacitance of the A/D converter. R_S is 0Ω for the ADC614 since the input capacitance in only 5pF.

ADC INPUT CAPACITANCE	R_S
C_{IN} < 20pF	0Ω
C_{IN} > 20pF	30Ω to 50Ω

FIGURE 12. Differential Input Buffer Amplifier (G = 2V/V).

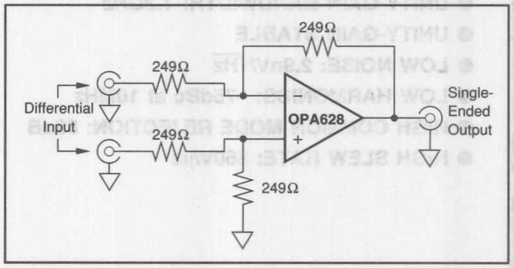
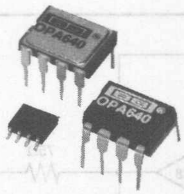


FIGURE 13. Low Distortion Unity Gain Difference Amplifier.

BURR - BROWN®



OPA640

DEMO BOARD AVAILABLE
See Appendix A

Wideband Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- UNITY-GAIN BANDWIDTH: *1.3GHz*
- UNITY-GAIN STABLE
- LOW NOISE: $2.9nV/\sqrt{Hz}$
- LOW HARMONICS: –75dBc at 10MHz
- HIGH COMMON MODE REJECTION: 85dB
- HIGH SLEW RATE: 350V/μs

APPLICATIONS

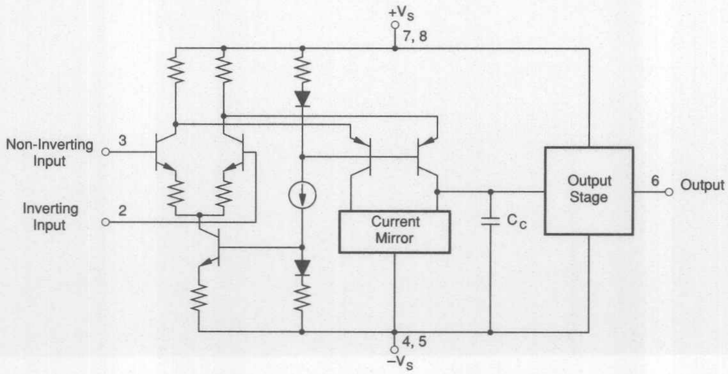
- COMMUNICATIONS
- MEDICAL IMAGING
- TEST EQUIPMENT
- CCD IMAGING
- ADC/DAC GAIN AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LOW NOISE PREAMPLIFIER
- DIFFERENTIAL AMPLIFIER
- ACTIVE FILTERS

DESCRIPTION

The OPA640 is an extremely wideband operational amplifier featuring low noise, high common mode rejection and high spurious free dynamic range.

The OPA640 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. This allows the OPA640 to be used in all op amp applications requiring high speed and precision.

Low noise, wide bandwidth, and high linearity make this amplifier suitable for a variety of RF and video applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1179B
BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

		OPA640H, P, U			OPA640HSQ, PB, UB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE								
Input Offset Voltage			±2.0	±5		1.0	±2.0	mV
Average Drift,			±10			±6		μV/°C
HSQ Grade Over Temperature						±3.0	±5	mV
Power Supply Rejection (+V_S)	V_S = ±4.5 to ±5.5V	60	75		*	*		dB
(−V_S)		53	60		*	*		dB
INPUT BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0V		15	25		*	*	μA
Over Specified Temperature			30	75		18	55	μA
HSQ Grade Over Temperature						20	75	μA
Input Offset Current	V_{CM} = 0V		0.3	2.0		*	1.0	μA
Over Specified Temperature			0.5	2.5		*	2.0	μA
HSQ Grade Over Temperature						0.5	3.0	μA
NOISE								
Input Voltage Noise Density								
f = 100Hz			7.0			*		nV/√Hz
f = 10kHz			2.8			*		nV/√Hz
f = 1MHz			2.8			*		nV/√Hz
f = 1MHz to 500MHz			2.9			*		nV/√Hz
Voltage Noise, BW = 100Hz to 500MHz			65			*		μVrms
Input Bias Current Noise Density								
f = 0.1Hz to 20kHz			2.0			*		pA/√Hz
Noise Figure (NF)								
R_S = 1kΩ			2.6			*		dB
R_S = 50Ω			10.9			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.5	±2.85		*	*		V
Over Temperature		±2.5	±2.75		*	*		V
Common-Mode Rejection	V_{CM} = ±0.5V	70	85		80	88		dB
INPUT IMPEDANCE								
Differential			15 || 1			*		kΩ || pF
Common-Mode			2 || 1			*		MΩ || pF
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	50	57		53	*		dB
Over Specified Temperature	V_O = ±2V, R_L = 100Ω	45	55		*	*		dB
FREQUENCY RESPONSE, R_{FB} = 402Ω	All Four Power Pins Used							
Closed-Loop Bandwidth	Gain = +1V/V		1.3			*		GHz
	Gain = +2V/V		280			*		MHz
	Gain = +5V/V		65			*		MHz
	Gain = +10V/V		31			*		MHz
Slew Rate[2]	G = +1, 2V Step		350			*		V/μs
At Minimum Specified Temperature	G = +1, 2V Step		285			*		V/μs
Settling Time 0.01%	G = +1, 2V Step		22			*		ns
0.1%	G = +1, 2V Step		18			*		ns
1%	G = +1, 2V Step		4.5			*		ns
Spurious Free Dynamic Range	G = +1, f = 5MHz, V_O = 2Vp-p		85			*		dBc
	G = +1, f = 10MHz, V_O = 2Vp-p		75			*		dBc
	G = +1, f = 20MHz, V_O = 2Vp-p		65			*		dBc
Gain Flatness to 0.1dB	G = +1 or +2		120			*		MHz
Differential Gain at 3.58MHz, G = +2V/V	V_O = 0V to 1.4V, R_L = 150Ω		0.07			*		%
Differential Phase at 3.58MHz, G = +2V/V	V_O = 0V to 1.4V, R_L = 150Ω		0.008			*		Degrees
OUTPUT								
Voltage Output	No Load							
Over Specified Temperature		±2.6	±3.0		*	*		V
HSQ Grade Over Temperature					±2.5	±2.8		V
Voltage Output	R_L = 100Ω							
Over Specified Temperature		±2.25	±2.5		*	*		V
HSQ Grade Over Temperature					±2.0	±2.25		V
Current Output, +25°C		±40	±52		*	*		mA
Over Specified Temperature		±25	±45		*	*		mA
HSQ Grade Over Temperature					±25	±35		mA
Short Circuit Current			75			*		mA
Output Resistance	1MHz, G = +1V/V		0.2			*		Ω

ELECTRICAL

$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

		OPA640H, P, U			OPA640HSQ, PB, UB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}		±5			*		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	*		*	V
Quiescent Current			±18	±22		*	*	mA
Over Specified Temperature			±19	±24		*	*	mA
TEMPERATURE RANGE								
Specification: H, P, PB, U, UB	Ambient	–40		+85	*		*	°C
HSQ	Ambient				–55		+125	°C
Thermal Resistance	θ_{JA}, Junction to Ambient							°C/W
P			120					°C/W
U			170			*		°C/W
H			120			*		°C/W

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

ORDERING INFORMATION

OPA640 ( ) ( ) (Q)

Basic Model Number

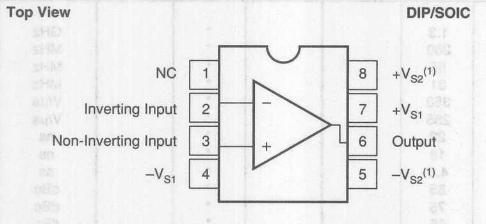
Package Code
- H = 8-pin Sidebraze DIP
- P = 8-pin Plastic DIP
- U = 8-pin Plastic SOIC

Performance Grade Code
- S = –55°C to +125°C
- B[1] or No Letter = –40°C to +85°C

Reliability Screening
- Q = Q-Screened (HSQ Model Only)

NOTE: (1) The "B" grade of the SOIC package will be designated with a dot. Refer to the mechanical section for the location.

PIN CONFIGURATION



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

ABSOLUTE MAXIMUM RATINGS

Supply .... ±5.5VDC
Internal Power Dissipation[1] .... See Applications Information
Differential Input Voltage .... Total V_{CC}
Input Voltage Range .... See Applications Information
Storage Temperature Range: H, HSQ .... –65°C to +150°C
P, PB, U, UB .... –40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
(soldering, SOIC 3s) .... +260°C
Junction Temperature (T_J) .... +175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA640H, HSQ	8-Pin Sidebraze DIP	157
OPA640P, PB	8-Pin DIP	006
OPA640U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

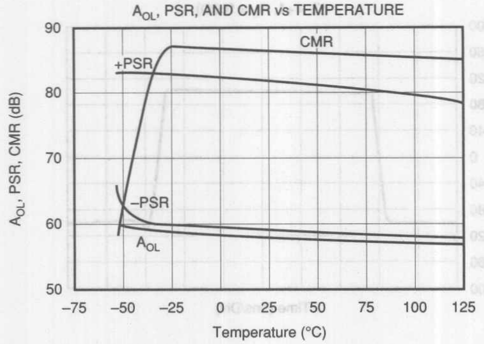
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

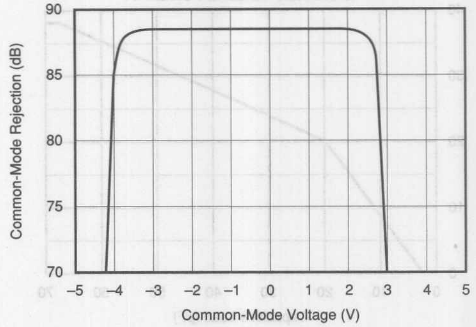
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

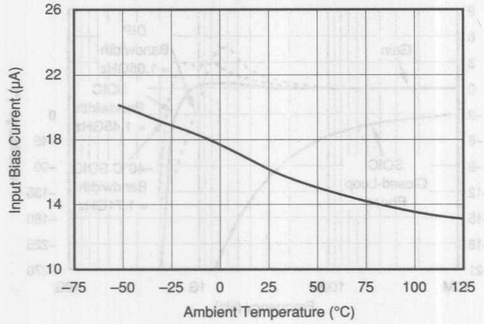
A_{OL}, PSR, AND CMR vs TEMPERATURE



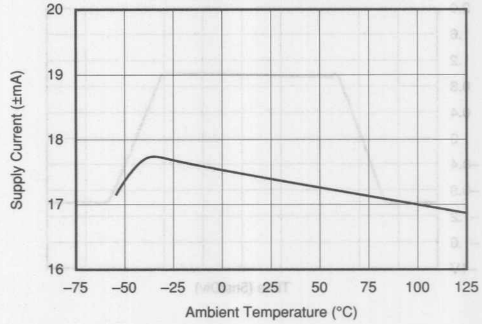
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



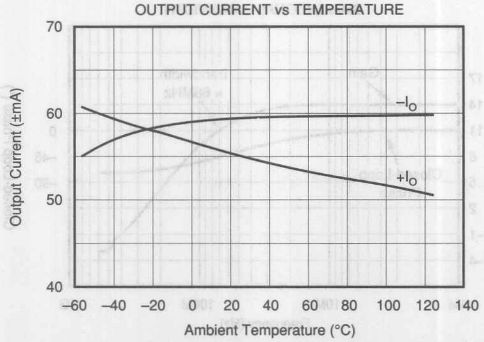
INPUT BIAS CURRENT vs TEMPERATURE



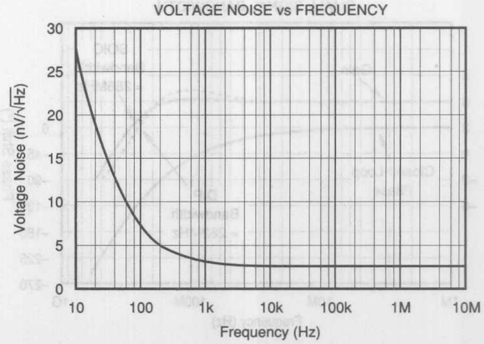
SUPPLY CURRENT vs TEMPERATURE



OUTPUT CURRENT vs TEMPERATURE



VOLTAGE NOISE vs FREQUENCY



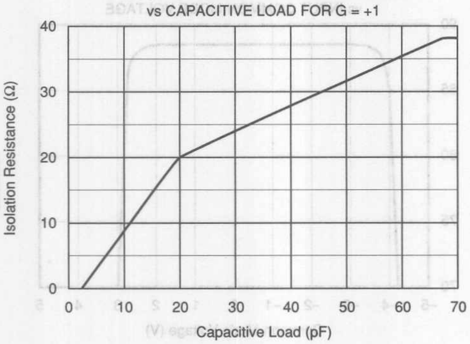
OPA640

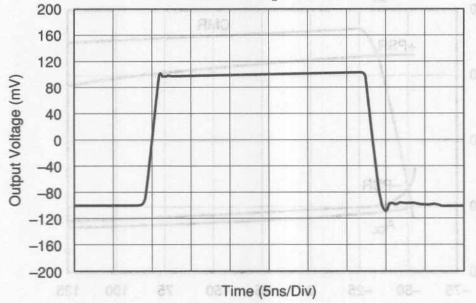
2

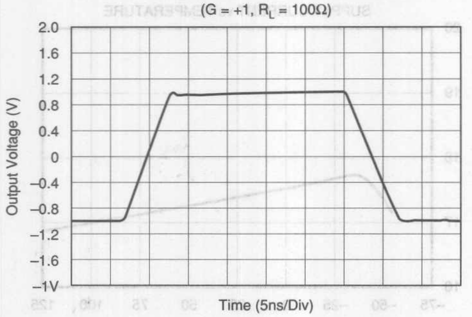
OPERATIONAL AMPLIFIERS

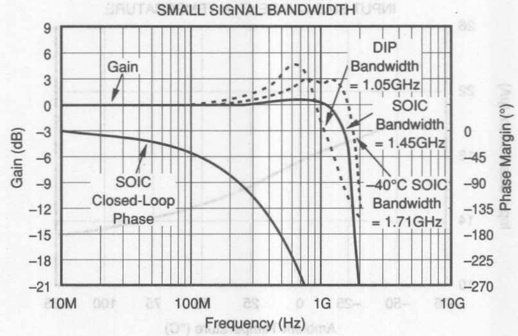
TYPICAL PERFORMANCE CURVES (CONT)

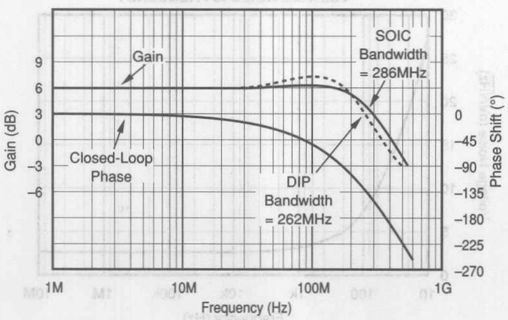
$T_A = +25°C$, $V_S = ±5V$, $R_L = 100Ω$, $C_L = 2pF$, $R_{FB} = 402Ω$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25Ω$ for a gain of +1.

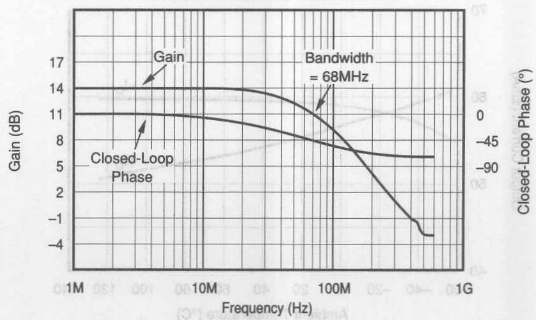








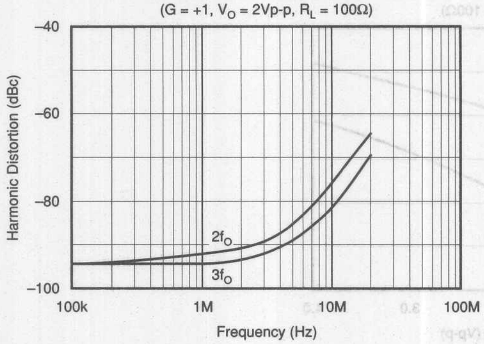




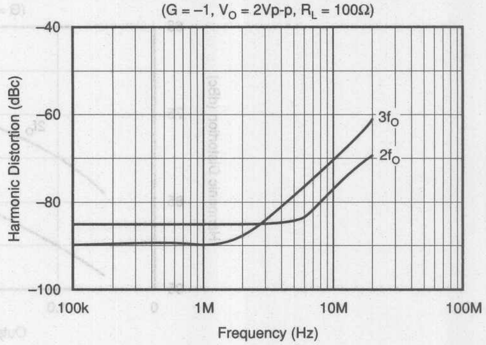
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

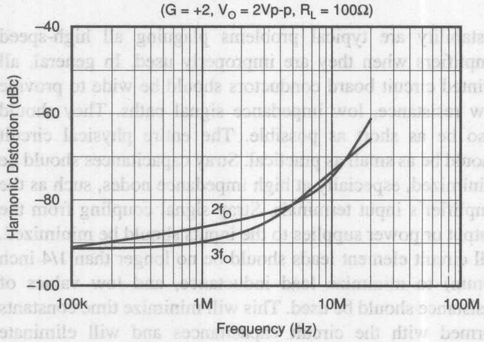
HARMONIC DISTORTION vs FREQUENCY
(G = +1, V_O = 2Vp-p, R_L = 100Ω)



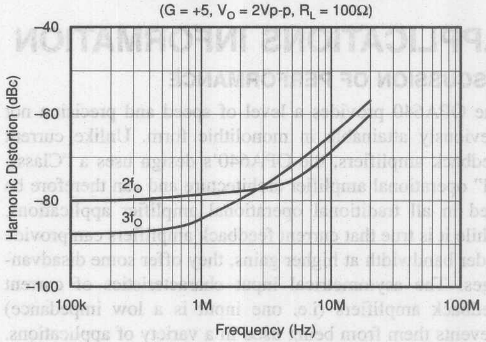
HARMONIC DISTORTION vs FREQUENCY
(G = –1, V_O = 2Vp-p, R_L = 100Ω)



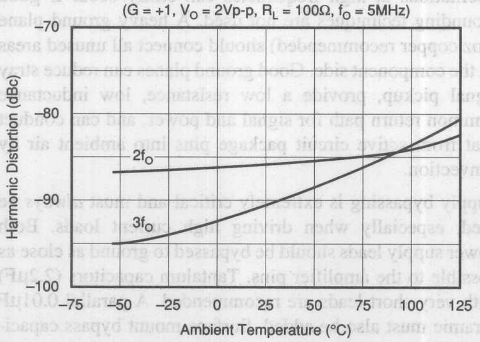
HARMONIC DISTORTION vs FREQUENCY
(G = +2, V_O = 2Vp-p, R_L = 100Ω)



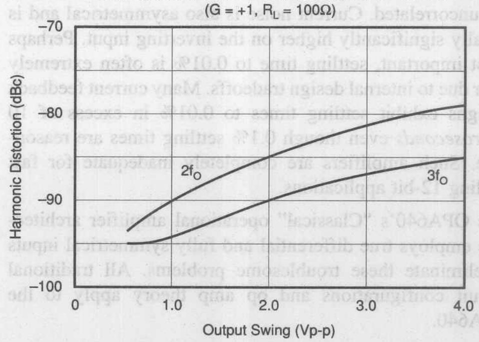
HARMONIC DISTORTION vs FREQUENCY
(G = +5, V_O = 2Vp-p, R_L = 100Ω)



HARMONIC DISTORTION vs TEMPERATURE
(G = +1, V_O = 2Vp-p, R_L = 100Ω, f_O = 5MHz)

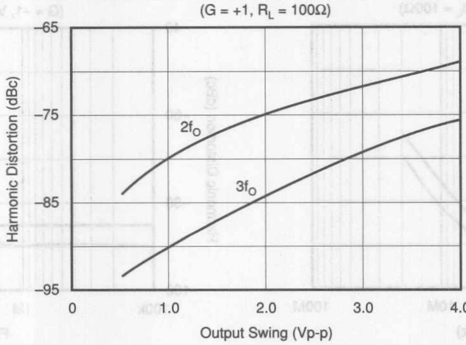


5MHz HARMONIC DISTORTION vs OUTPUT SWING
(G = +1, R_L = 100Ω)



T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

10MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = +1$, $R_L = 100\Omega$)



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA640 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA640's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Cancelling offset errors (due to input bias currents) through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA640's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA640.

WIRING PRECAUTIONS

Maximizing the OPA640's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA640, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2μF) with very short leads are recommended. A parallel 0.01μF ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages. This will improve the AC performance **including lower distortion**. The lowest distortion is achieved when running separate traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface mount capacitors on the topside of the PC board is recommended. It is essential to keep the 0.01µF capacitor very close to the power supply pins. Refer to the DEM-OPA64X data sheet for the recommended layout and component placements.

2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on backside of PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA640 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. Refer to the demonstration board layout at the end of the data sheet. **A longer feedback path than this will decrease the realized bandwidth substantially**.

6) Due to the extremely high bandwidth of the OPA640, the SOIC package is strongly recommended due its low parasitic impedance. The parasitic impedance in the PDIP and CERDIP packages causes the OPA640 to experience about 5dB of gain peaking in unity-gain configurations. This is compared with virtually no gain peaking in the SOIC package in unity-gain. The gain peaking in the PDIP and CERDIP packages is minimized in gains of 2 or greater, however. Surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are also strongly recommended.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

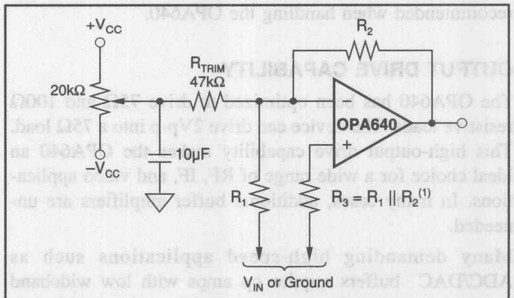
9) Standard commercial test equipment has not been designed to test devices in the OPA640's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current.



Output Trim Range $\cong +V_{CC}\frac{R_2}{R_{Trim}}$ to $-V_{CC}\frac{R_2}{R_{Trim}}$

NOTE: (1) R_3 is optional and can be used to cancel offset errors due to input bias currents.

FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA640 incor-

porates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

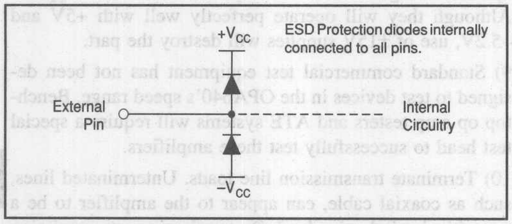


FIGURE 2. Internal ESD Protection.

All pins on the OPA640 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA640 utilizes a fine geometry high speed process that withstands 500V using Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA640.

OUTPUT DRIVE CAPABILITY

The OPA640 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA640 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA640 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

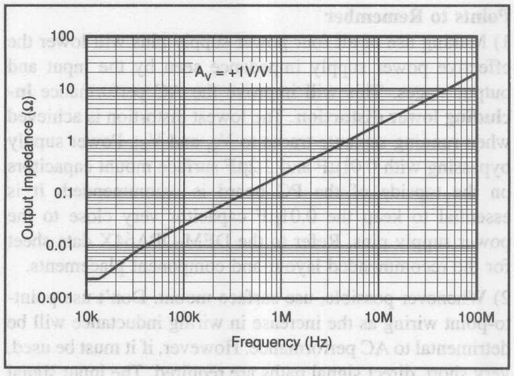


FIGURE 3. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA640 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 22mA = 220mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max $= (\pm V_{CC})^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

A short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in Figure 4.

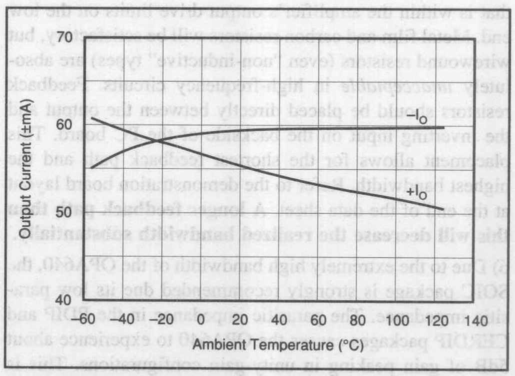


FIGURE 4. Output Current vs. Temperature.

CAPACITIVE LOADS

The OPA640's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 2pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

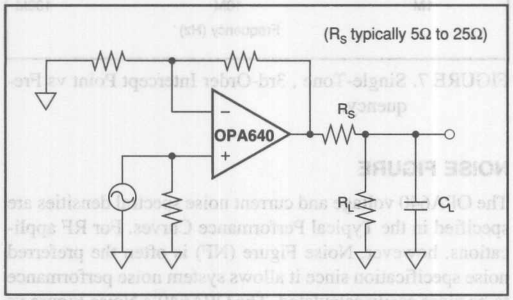


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA640 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA640 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200μV centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 15ns to 0.01% for a 2V step, making the OPA640 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 35ns.

In practice, settling time measurements on the OPA640 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA640's Harmonic Distortion characteristics vs frequency and power output are shown in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance. Refer to Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

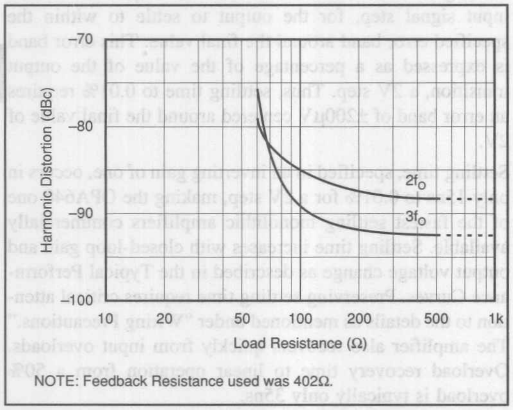


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept point is an important parameter for many RF amplifier applications. Figure 7 shows the OPA640's single tone, third-order intercept vs frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA640 to operate in a gain of +1V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 11 we find that the intercept point is +47dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OPI}^3\text{P} - \text{P}_O)$$

where OPI^3P = third-order intercept, dBm

P_O = output level, dBm

For this case OPI^3P = 47dBm, P_O = 47dBm, and the third Harmonic = 2(47 – 10) = 74dB below the fundamental tone. The OPA640's low distortion makes the device an excellent choice for a variety of RF signal processing applications. The value for the two-tone, third-order intercept is typically 8dB lower than the single tone value.

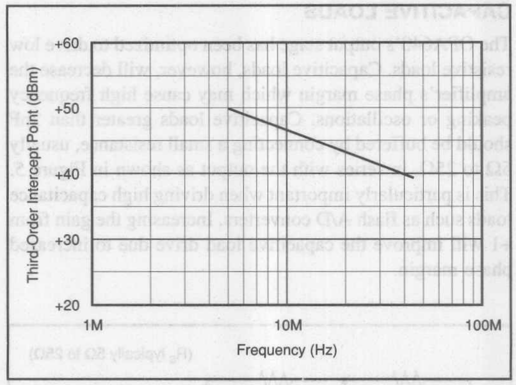


FIGURE 7. Single-Tone , 3rd-Order Intercept Point vs Frequency.

NOISE FIGURE

The OPA640 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA640's Noise Figure vs Source Resistance is shown in Figure 8.

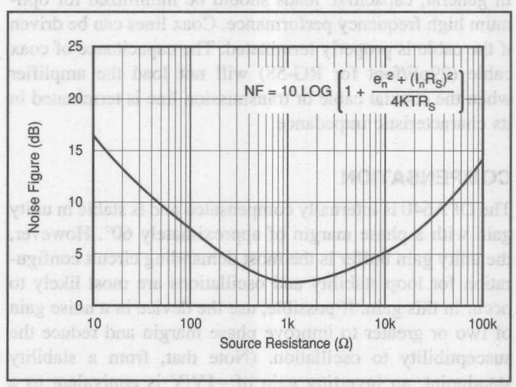


FIGURE 8. Noise Figure vs Source Resistance.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device —it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = –65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate < 5 x 10^{-8} atm cc/s, 30PSiG Gross: per Fluorocarbon bubble test, 60PSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on the HS package only.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA640. Contact Burr-Brown Applications Department to receive a spice diskette.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64x data sheet for details.

APPLICATIONS

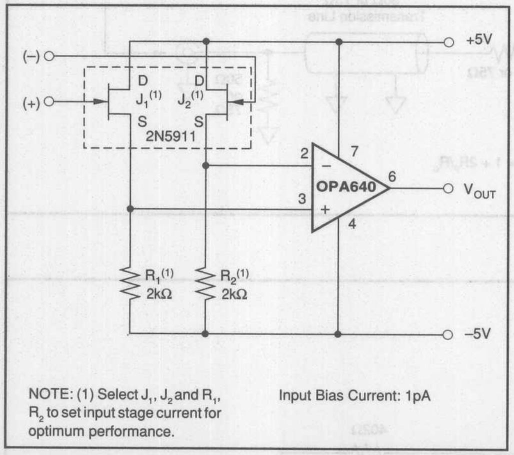


FIGURE 9. Low Noise, Wideband FET Input Op Amp.

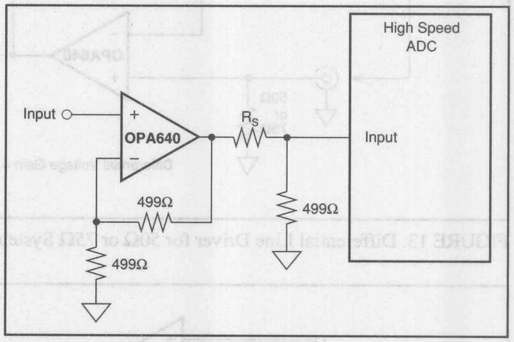


FIGURE 10. Differential Input Buffer Amplifier (G = +2V/V).

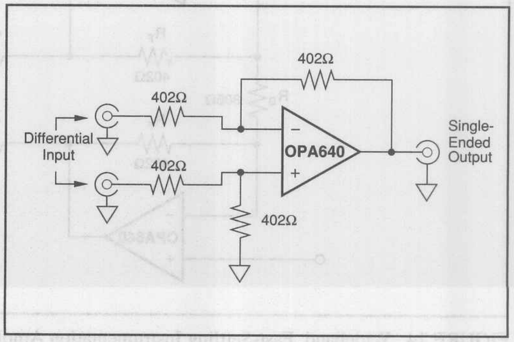


FIGURE 11. Unity Gain Difference Amplifier.

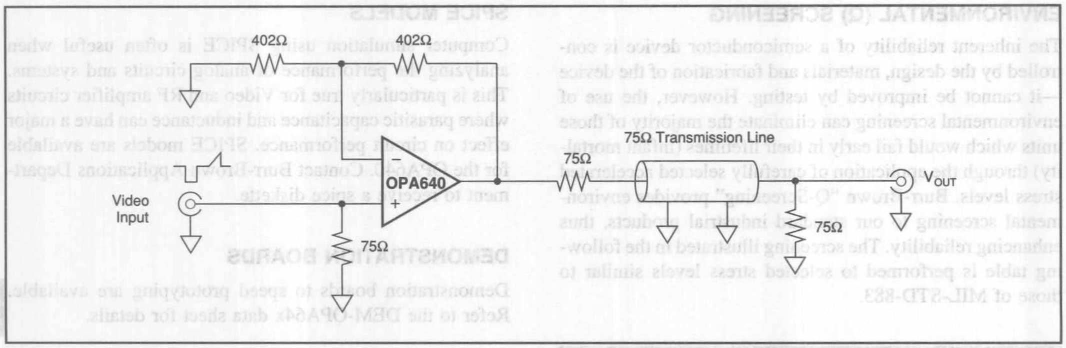


FIGURE 12. Video Gain Amplifier.

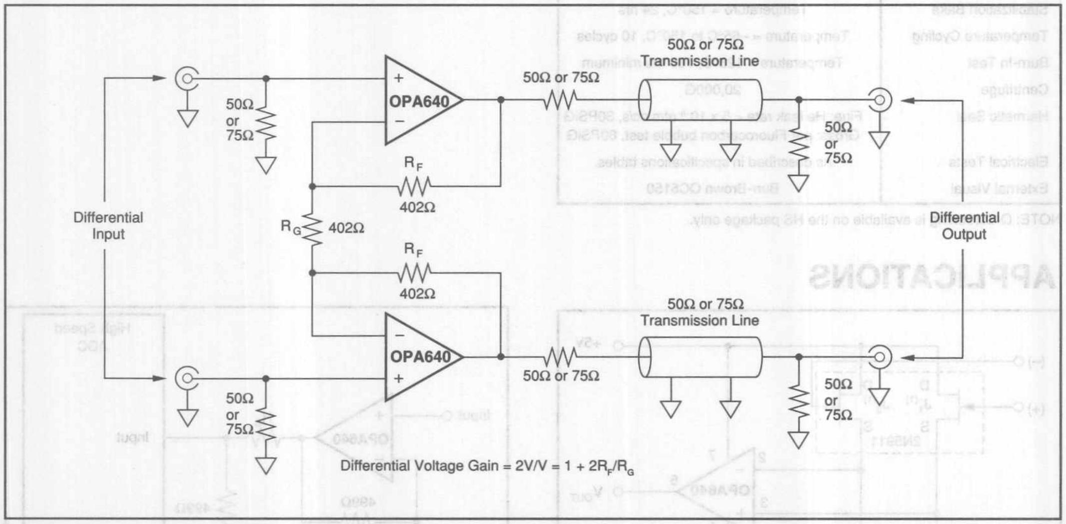


FIGURE 13. Differential Line Driver for 50Ω or 75Ω Systems.

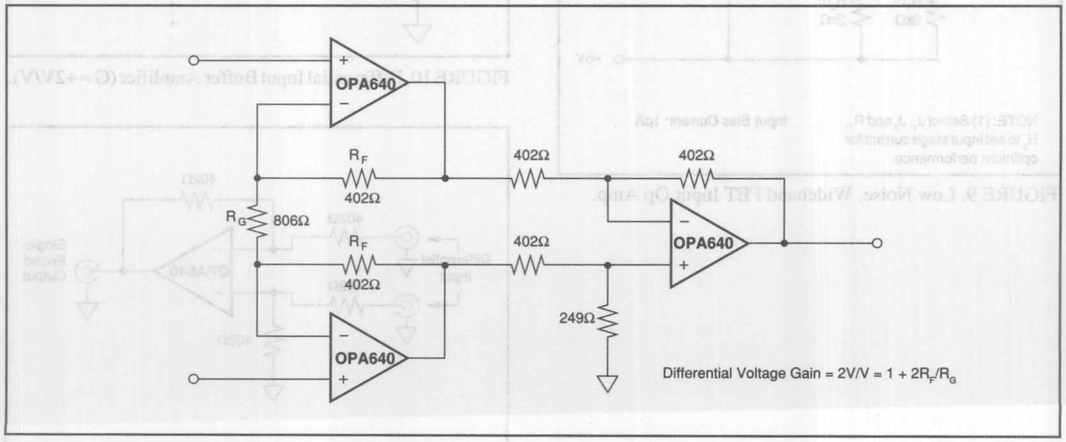
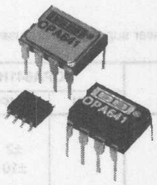


FIGURE 14. Wideband, Fast-Settling Instrumentation Amplifier.

BURR - BROWN®



OPA641

DEMO BOARD AVAILABLE
See Appendix A

Wideband Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- GAIN-BANDWIDTH: 1.6GHz
- STABLE IN GAINS ≥ 2
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.015%/0.006°
- HIGH SLEW RATE: 650V/µs
- FAST 12-BIT SETTLING: 18ns (0.01%)
- HIGH COMMON-MODE REJECTION: 80dB
- LOW HARMONICS: –72dBc at 10MHz

APPLICATIONS

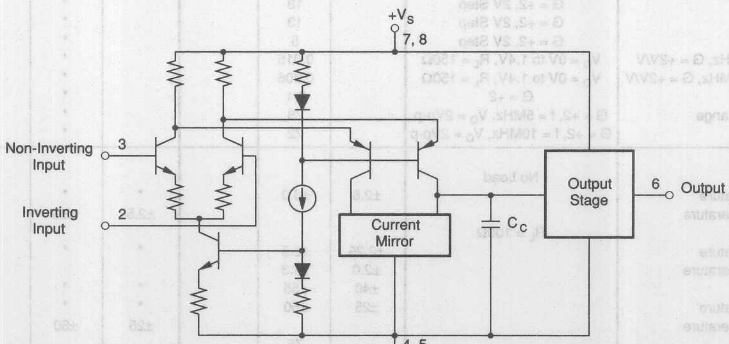
- COMMUNICATIONS
- MEDICAL IMAGING
- TEST EQUIPMENT
- CCD IMAGING
- ADC/DAC GAIN AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LOW NOISE PREAMPLIFIER
- ACTIVE FILTERS

DESCRIPTION

The OPA641 is an extremely wideband operational amplifier featuring low noise, high slew rate and high spurious free dynamic range.

The OPA641 is conservatively compensated for stability in gains of 2 or greater. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. This allows the OPA641 to be used in all op amp applications requiring high speed and precision.

Low noise, wide bandwidth, and high linearity make this amplifier suitable for a variety of RF, video, and imaging applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PARAMETER	CONDITIONS	OPA641H, P, U			OPA641HSQ, PB, UB			
		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE								
Input Offset Voltage			±2	±6		±1	±2	mV
Average Drift			±10			±6		µV/°C
HSQ Grade Over Temperature						±3	±6	mV
Power Supply Rejection (+V_S)	V_S = ±4.5 to ±5.5V	56	79		61	82		dB
(−V_S)		51	58		54	60		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		13	30		*	*	µA
Over Specified Temperature			20	90		*	*	µA
HSQ Grade Over Temperature						30	75	µA
Input Offset Current	V_{CM} = 0V		0.2	2		*	1.0	µA
Over Specified Temperature			0.5	2.5		*	2.0	µA
HSQ Grade Over Temperature						1.2	4.0	µA
NOISE								
Input Voltage Noise								
Noise Density, f = 100Hz			8.0			*		nV/√Hz
f = 10kHz			2.9			*		nV/√Hz
f = 1MHz			2.8			*		nV/√Hz
f = 1MHz to 500MHz			2.8			*		nV/√Hz
Voltage Noise, BW = 100Hz to 500MHz			63			*		µVrms
Input Bias Current Noise Density								
f = 0.1Hz to 20kHz			2.0			*		pA/√Hz
Noise Figure (NF)								
R_S = 1kΩ			4			*		dB
R_S = 50Ω			13			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.5	±2.85		*	*		V
Over Specified Temperature		±2.5	±2.75		*	*		V
Common-Mode Rejection	V_{CM} = ±0.5V	56	78		65	80		dB
INPUT IMPEDANCE								
Differential			15 || 1			*		kΩ || pF
Common-Mode			2 || 1			*		MΩ || pF
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	50	58		53	61		dB
Over Specified Temperature	V_O = ±2V, R_L = 100Ω	45	56		48			dB
FREQUENCY RESPONSE, R_{FB} = 402Ω	All Four Power Pins Used							
Closed-Loop Bandwidth								
	Gain = +2V/V		800			*		MHz
	Gain = +5V/V		78			*		MHz
	Gain = +10V/V		39			*		MHz
Slew Rate(1)	G = +2, 2V Step		650			*		V/µs
At Minimum Specified Temperature	G = +2, 2V Step		550			*		V/µs
Settling Time: 0.01%	G = +2, 2V Step		18			*		ns
0.1%	G = +2, 2V Step		13			*		ns
1%	G = +2, 2V Step		5			*		ns
Differential Gain at 3.58MHz, G = +2V/V	V_O = 0V to 1.4V, R_L = 150Ω		0.015			*		%
Differential Phase at 3.58MHz, G = +2V/V	V_O = 0V to 1.4V, R_L = 150Ω		0.006			*		degrees
Gain Flatness	G = +2		0.1			*		MHz
Spurious Free Dynamic Range	G = +2, f = 5MHz, V_O = 2Vp-p		78			*		dBc
	G = +2, f = 10MHz, V_O = 2Vp-p		72			*		dBc
OUTPUT								
Voltage Output	No Load							
Over Specified Temperature		±2.6	±3.0		*	*		V
HSQ Grade Over Temperature					±2.5	±2.8		V
Voltage Output	R_L = 100Ω							
Over Specified Temperature		±2.25	±2.5		*	*		V
HSQ Grade Over Temperature		±2.0	±2.3					
Current Output		±40	±55		*	*		mA
Over Specified Temperature		±25	±50		*	*		mA
HSQ Grade Over Temperature					±25	±50		mA
Short Circuit Current			75					mA
Output Resistance	1MHz, G = +2V/V		0.04			*		Ω

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = +25°C$, $V_S = ±5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$, and all four power supply pins are used unless otherwise noted.

PARAMETER	CONDITIONS	OPA641H, P, U			OPA641HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}		±5			*		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	*		*	V
Quiescent Current			±15	±22		*	*	mA
Over Specified Temperature			±19	±24		*	*	mA
TEMPERATURE RANGE								
Specification: H, P, PB, U, UB	Ambient	–40		+85	*		*	°C
HSQ	Ambient				–55		+125	°C
Thermal Resistance	θ_{JA}, Junction to Ambient							
P			120			*		°C/W
U			170			*		°C/W
H			120			*		°C/W

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

ORDERING INFORMATION

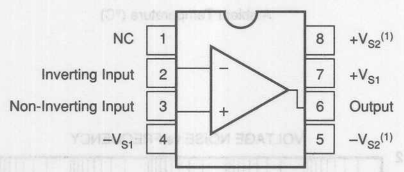
OPA641 ( ) ( ) (Q)

- Basic Model Number
- Package Code
  - H = 8-pin Sidebraze DIP
  - P = 8-pin Plastic DIP
  - U = 8-pin Plastic SOIC
- Performance Grade Code
  - S = –55°C to +125°C
  - B[1] or No Letter = –40°C to +85°C
- Reliability Screening
  - Q = Q-Screened (HSQ Model Only)

NOTE: (1) The "B" grade of the SOIC package will be designated with a "B". Refer to the mechanical section for the location.

PIN CONFIGURATION

Top View | DIP/SOIC



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

ABSOLUTE MAXIMUM RATINGS

Supply	±5.5VDC
Internal Power Dissipation[1]	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	–65°C to +150°C
P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA641H, HSQ	8-Pin Cerdip	157
OPA641P, PB	8-Pin DIP	006
OPA641U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

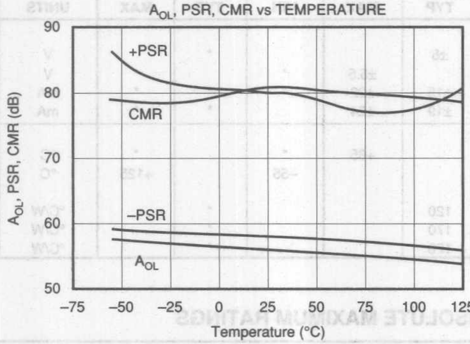
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

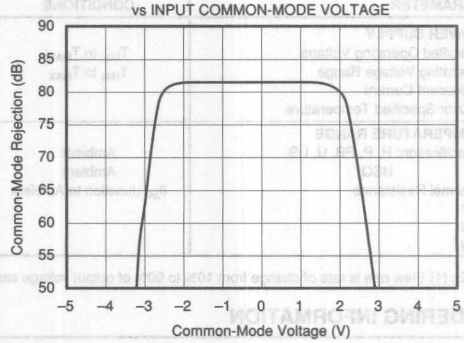
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$, and all four power supply pins are used unless otherwise noted.

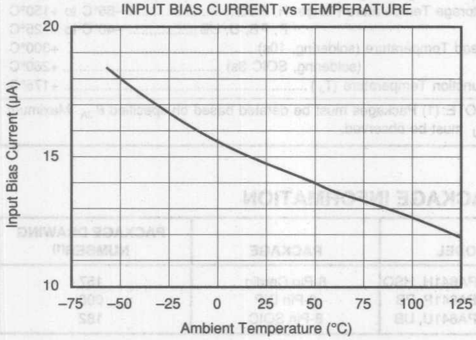
A_{OL}, PSR, CMR vs TEMPERATURE



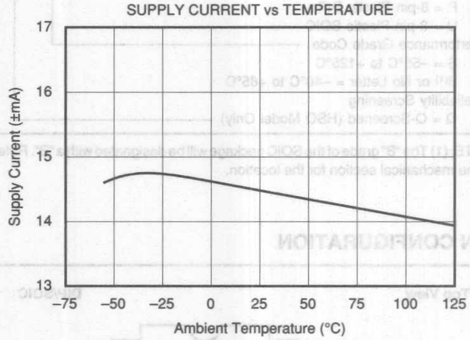
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



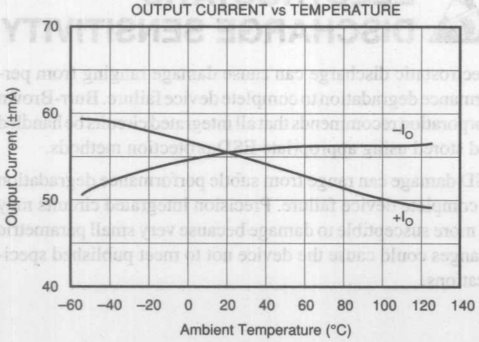
INPUT BIAS CURRENT vs TEMPERATURE



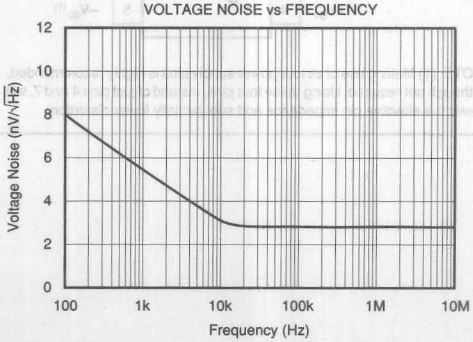
SUPPLY CURRENT vs TEMPERATURE



OUTPUT CURRENT vs TEMPERATURE

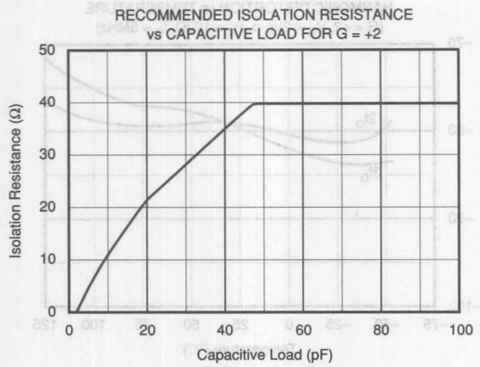


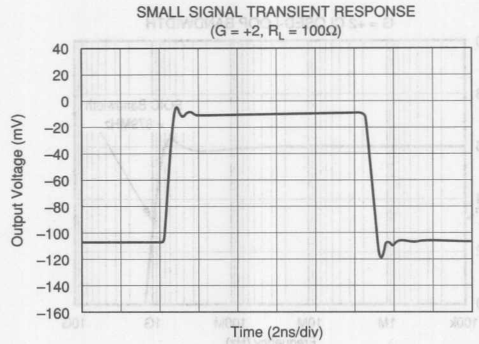
VOLTAGE NOISE vs FREQUENCY

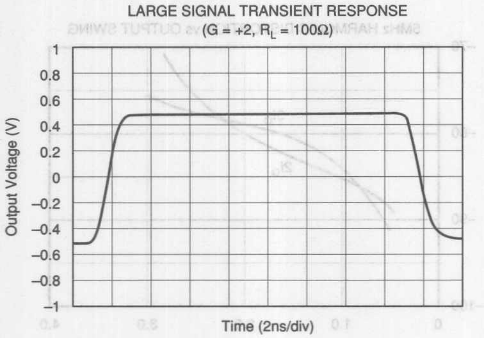


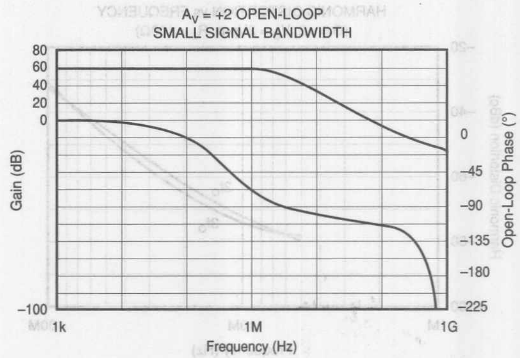
TYPICAL PERFORMANCE CURVES (CONT)

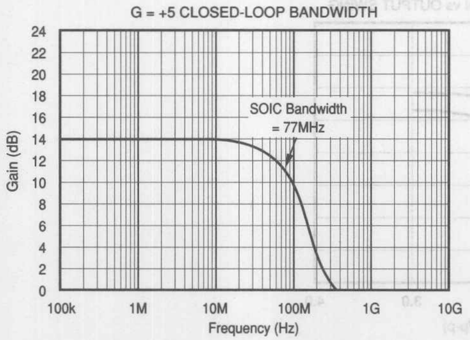
$T_A = +25°C$, $V_S = ±5V$, $R_L = 100Ω$, $C_L = 2pF$, $R_{FB} = 402Ω$, and all four power supply pins are used unless otherwise noted.

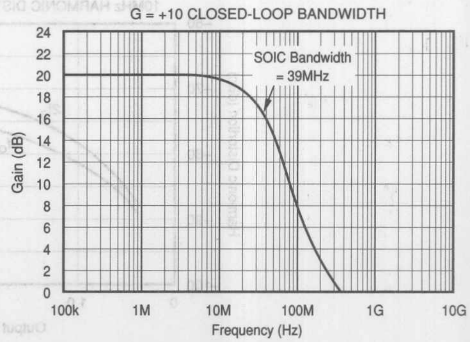












OPA641

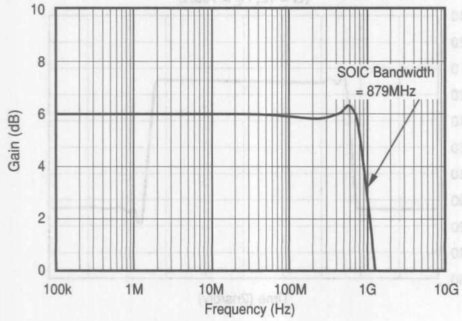
2

OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

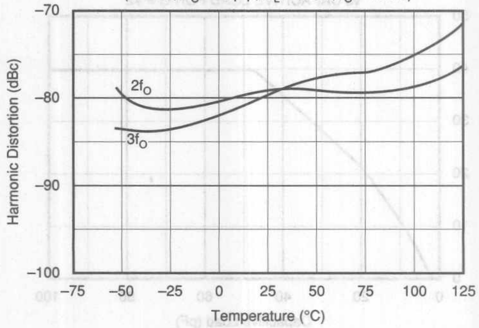
$T_A = +25°C$, $V_S = ±5V$, $R_L = 100Ω$, $C_L = 2pF$, $R_{FB} = 402Ω$, and all four power supply pins are used unless otherwise noted.

G = +2 CLOSED-LOOP BANDWIDTH

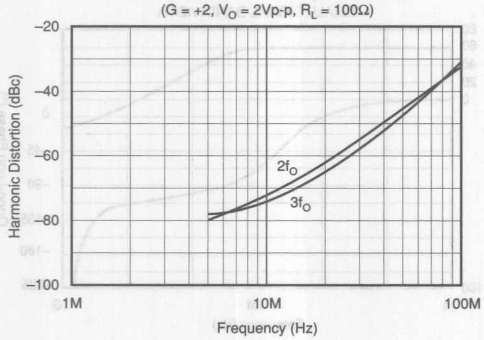


NOTE: Dip Bandwidth = 785MHz

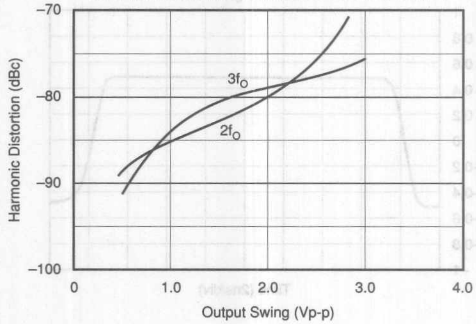
HARMONIC DISTORTION vs TEMPERATURE
($G = +2$, $V_O = 2Vp\text{-}p$, $R_L = 100Ω$, $f_O = 5MHz$)



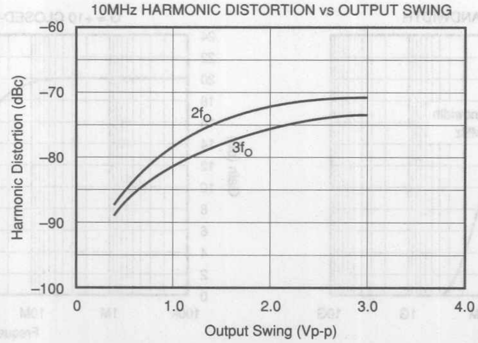
HARMONIC DISTORTION vs FREQUENCY
($G = +2$, $V_O = 2Vp\text{-}p$, $R_L = 100Ω$)



5MHz HARMONIC DISTORTION vs OUTPUT SWING



10MHz HARMONIC DISTORTION vs OUTPUT SWING



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA641 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA641's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e., one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA641's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA641.

WIRING PRECAUTIONS

Maximizing the OPA641's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA641, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2 oz. copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2µF) with very short leads are recommended. A parallel 0.01µF ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages. This will improve the AC performance **including lower distortion**. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface mount capacitors on the topside of the PC board is recommended. It is essential to keep the 0.01µF capacitor very close to the power supply pins. Refer to the DEM-OPA64x Datasheet for the recommended layout and component placement.

2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on the PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA641 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. See the demonstration board layout at

the end of the datasheet. **A longer feedback path than this will decrease the realized bandwidth substantially.**

6) Due to the extremely high bandwidth of the OPA641, the SOIC package is strongly recommended due its low parasitic impedance. The parasitic impedance in the PDIP and CERDIP packages causes the OPA641 to experience about 5dB of gain peaking in unity-gain configurations. This is compared with virtually no gain peaking in the SOIC package in unity-gain. The gain peaking in the PDIP and CERDIP packages is minimized in gains of 4 or greater, however. Surface mount components (chip resistors, capacitors, etc.) also have low lead inductance and are therefore strongly recommended.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

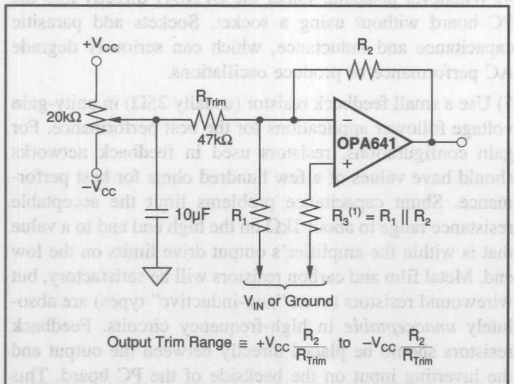
9) Standard commercial test equipment has not been designed to test devices in the OPA641's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current.



NOTE: (1) R_3 is optional and can be used to cancel offset errors due to input bias currents.

FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA641 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

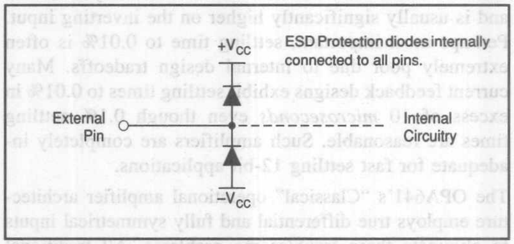


FIGURE 2. Internal ESD Protection.

All pins on the OPA641 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA641 utilizes a fine geometry high speed process that withstands 500V using Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA641.

OUTPUT DRIVE CAPABILITY

The OPA641 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA641 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA641 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

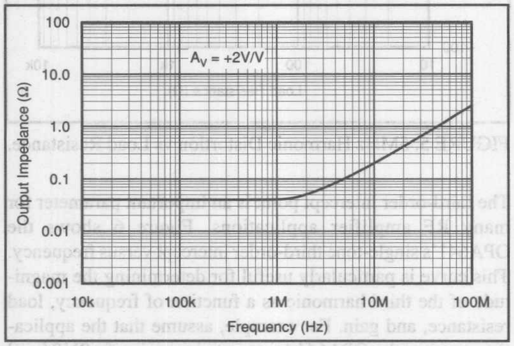


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA641 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, P_{DQ} = 10V x 24mA = 240mW, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max $= (\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA641's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax

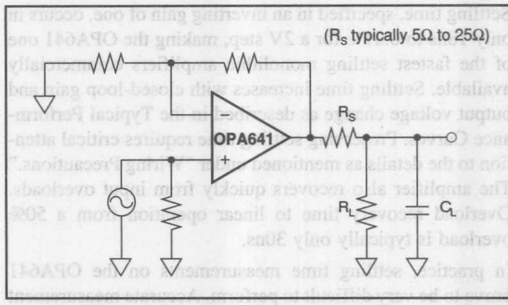


FIGURE 4. Driving Capacitive Loads.

cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA641 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA641 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200μV centered around the final value of 2V.

available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA641 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results, a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 6 shows the test circuit used to measure settling time for the OPA641. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION AND NOISE

The OPA641's harmonic distortion characteristics vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance (refer to Figure 5). Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Although harmonic distortion may decrease with higher load resistances (i.e., higher feedback resistors), the effective output noise will increase due to the higher resistance. Therefore, noise or harmonic distortion may be optimized by picking the appropriate feedback resistor.

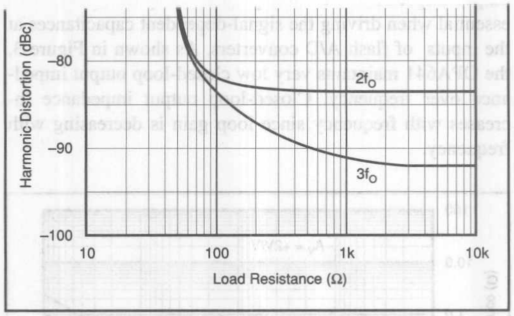


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept point is an important parameter for many RF amplifier applications. Figure 6 shows the OPA641's single-tone third-order intercept versus frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA641 to operate in a gain of +2V/V and drive 2Vp-p into 100Ω at a frequency of 5MHz. Referring to Figure 6 we find that the intercept point is +38dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm

P_O = output level/tone, dBm/tone

For this case OPI^3P = 38dBm, P_O = 7dBm, and the third harmonic = 2(38 – 7) = 62dB below the fundamental tone. The OPA641's low IMD makes the device an excellent choice for a variety of RF signal processing applications. The value for the two-tone third-order intercept is typically 6dB lower than the single-tone value.

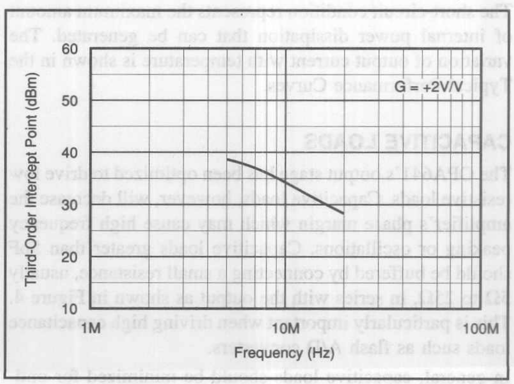


FIGURE 6. Single-Tone Third-Order Intercept Point vs Frequency.

NOISE FIGURE

The OPA641 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA641's Noise Figure vs Source Resistance is shown in Figure 7.

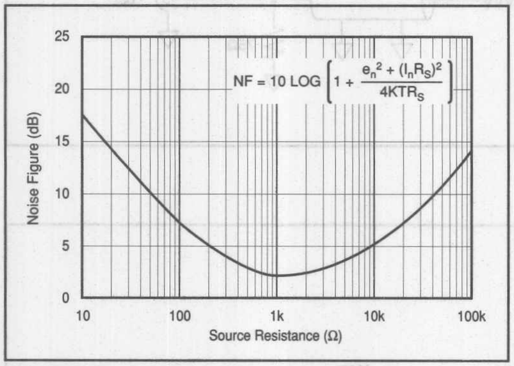


FIGURE 7. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA641. Contact Burr-Brown Applications Department to receive a spice diskette.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device —it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = –65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate < 5 x 1x0^{-8} atm cc/s, 30PSiG Gross: per Fluorocarbon bubble test, 60PSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on the HSQ package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64X Datasheet for details.

APPLICATIONS

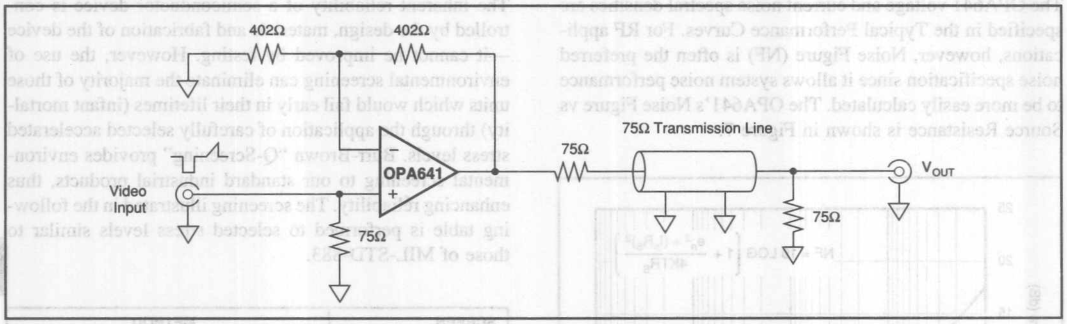


FIGURE 8. Video Gain Amplifier.

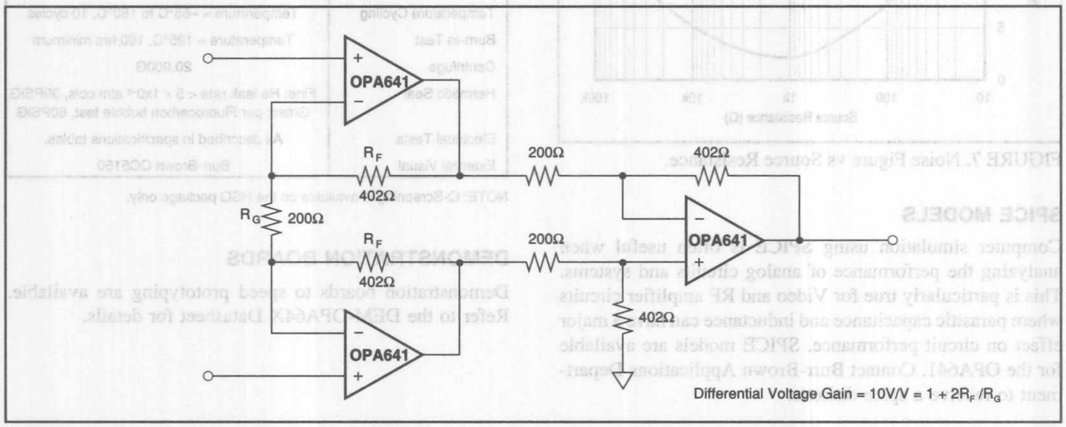


FIGURE 9. Wideband, Fast-Settling Instrumentation Amplifier.

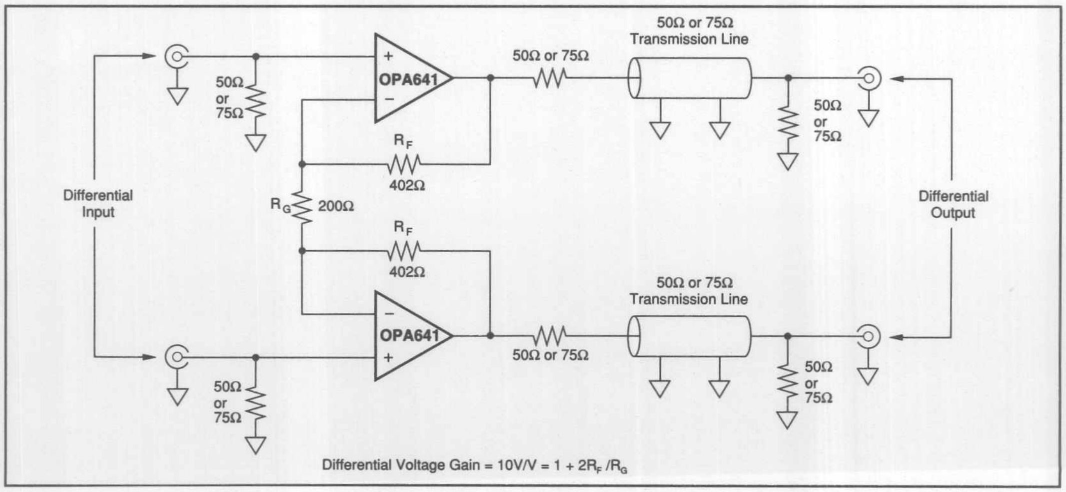


FIGURE 10. Differential Gain Amplifier and Driver for 50Ω or 75Ω Systems.

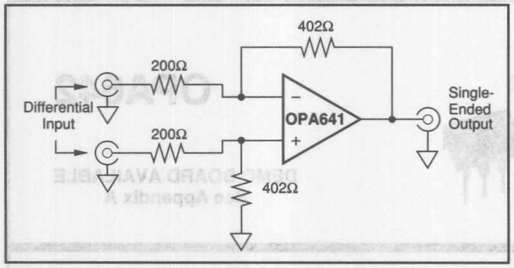


FIGURE 11. Difference Amplifier with Gain.

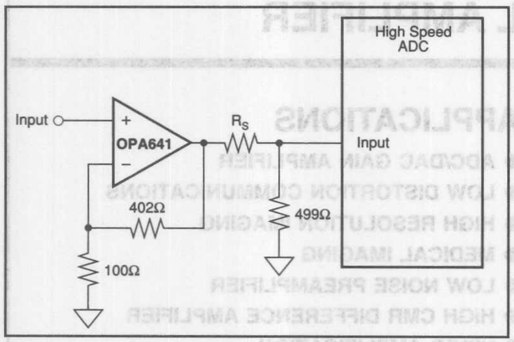


FIGURE 12. Gain Amplifier for ADCs (G = +5V/V).

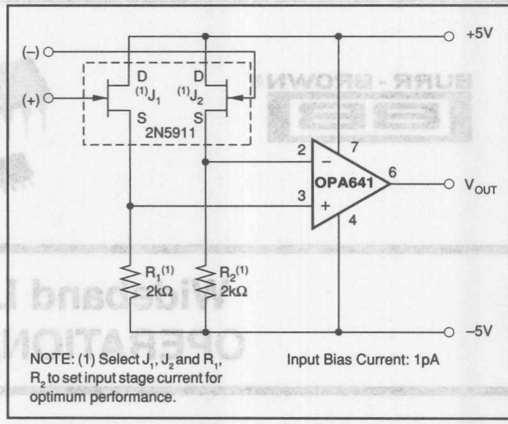
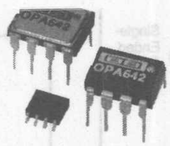


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

BURR - BROWN®



OPA642

DEMO BOARD AVAILABLE
See Appendix A

Wideband Low Distortion OPERATIONAL AMPLIFIER

FEATURES

- LOW DISTORTION: –95dBc at 5MHz
- UNITY-GAIN BANDWIDTH: 450MHz
- UNITY-GAIN STABLE
- HIGH OPEN LOOP GAIN: 95dB
- HIGH COMMON MODE REJECTION: 90dB
- FAST 12-BIT SETTLING: 13ns (0.01%)
- LOW NOISE: 2.3nV/$\sqrt{\text{Hz}}$
- HIGH OUTPUT CURRENT: ±60mA
- VERY LOW DIFF GAIN/PHASE ERROR: 0.007%/0.008°

APPLICATIONS

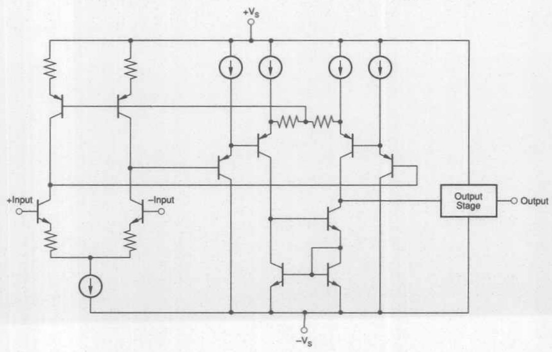
- ADC/DAC GAIN AMPLIFIER
- LOW DISTORTION COMMUNICATIONS
- HIGH RESOLUTION IMAGING
- MEDICAL IMAGING
- LOW NOISE PREAMPLIFIER
- HIGH CMR DIFFERENCE AMPLIFIER
- VIDEO AMPLIFICATION
- TEST INSTRUMENTATION
- AUDIO AMPLIFICATION

DESCRIPTION

The OPA642 is a voltage feedback operational amplifier featuring an unusual combination of high open loop gain and high bandwidth. The high open loop gain allows for minimal DC errors. The extra open loop gain at high bandwidths gives exceptionally low harmonic distortion. This makes the OPA642 compatible with high resolution and high dynamic range systems. It also offers fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA642 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. This allows the OPA642 to be used in all op amp applications requiring high speed and precision.

Low distortion, low noise and high bandwidth make this amplifier suitable for a variety of RF, video, imaging and audio applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

		OPA642H, P, U			OPA642HSQ, PB, UB			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE								
Input Offset Voltage			±1.5	±4		±0.5	±1.0	mV
Average Drift			4			2		µV/°C
HSQ Grade Over Temperature						±2.0	±4.0	mV
Power Supply Rejection	V_S = ±4.5 to ±5.5V	65	85		73	95		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		25	45		*	*	µA
Over Specified Temperature				70		*	*	µA
HSQ Grade Over Temperature							80	µA
Input Offset Current	V_{CM} = 0V		0.1	2.0		*	*	µA
Over Specified Temperature			0.5	3.0		*	*	µA
HSQ Grade Over Temperature						1.0	5.0	µA
NOISE								
Input Voltage Noise								
Noise Density: f = 100Hz			8.6			*		nV/√Hz
f = 10kHz			2.5			*		nV/√Hz
f = 1MHz			2.3			*		nV/√Hz
f_B = 1MHz to 100MHz			2.3			*		nV/√Hz
Voltage Noise, BW = 100Hz to 100MHz			23			*		µVrms
Input Bias Current Noise Density								
f = 0.1MHz to 100MHz			2.2			*		pA/√Hz
Noise Figure								
R_S = 1kΩ			2.2			*		dB
R_S = 50Ω			9.5			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.75	±3.0		*	*		V
Over Temperature		±2.5	±2.75		*	*		V
Common-Mode Rejection	V_{CM} = ±0.5V	65	85		80	92		dB
INPUT IMPEDANCE								
Differential			15 || 1			*		kΩ || pF
Common-Mode			1.3 || 1			*		MΩ || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	80	95		85	98		dB
Over Specified Temperature		80	90		*	*		dB
FREQUENCY RESPONSE	All Four Supply Pins Used							
Closed Loop Response	Gain = +1V/V		450			*		MHz
	Gain = +2V/V		150			*		MHz
	Gain = +5V/V		45			*		MHz
	Gain = +10V/V		21			*		MHz
Slew Rate(1)	G = +1, 2V Step		380			*		V/µs
At Minimum Specified Temperature	G = +1, 2V Step		340			*		V/µs
Settling Time: 0.003%	G = +1, 1V Step		20			*		ns
0.01%	G = +1, 1V Step		13			*		ns
0.1%	G = +1, 1V Step		11.5			*		ns
1%	G = +1, 1V Step		3.5			*		ns
Spurious Free Dynamic Range	G = +1, f = 5MHz V_O = 2Vp-p, R_L = 100Ω		92		80	95		dBc
Differ. Gain Error at 3.58MHz, G = +2V/V	V_O = 0V to 1.4V, R_L = 150Ω		0.007			*		%
Differ. Phase Error at 3.58MHz, G = +2V/V	V_O = 0V to 1.4V, R_L = 150Ω		0.008			*		degrees
OUTPUT								
Current Output, +25°C		±40	±60		±50	±65		mA
Over Specified Temperature		±35	±55		±40	±60		mA
Voltage Output	No Load							
Over Specified Temperature		±3.0	±3.5		*	*		V
Voltage Output	R_L = 100Ω							
Over Specified Temperature		±2.5	±2.75		*	*		V
Short Circuit Current			75			*		mA
Output Resistance	0.1MHz, G = +1V/V		0.04			*		Ω

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω fo a gain of +1.

		OPA642H, P, U			OPA642HSQ, PB, UB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}		±5			*		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	*		*	V
Quiescent Current	T_{MIN} to T_{MAX}		±22	±29		*	*	mA
TEMPERATURE RANGE								
Specification: H, P, U	Ambient	–40		+85	*			°C
HSQ	Ambient				–55		+125	°C
Storage	Ambient	–55		+150	–55		+150	°C
Thermal Resistance	θ_{JA}, Junction-to-Ambient					*		°C/W
P			100			*		°C/W
U			125			*		°C/W
H			100			*		°C/W

NOTES: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

ORDERING INFORMATION

OPA642 ( ) ( ) (Q)

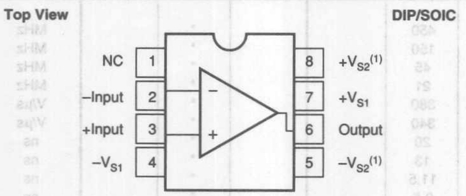
Basic Model Number
Package Code
- H = 8-pin Sidebraze DIP
- P = 8-pin Plastic DIP
- U = 8-pin Plastic SOIC

Performance Grade Code
- S = –55°C to +125°C
- B[1] or No Letter = –40°C to +85°C

Reliability Screening
- Q = Q-Screened (HSQ Model Only)

NOTE: (1) The "B" Grade of the SOIC package will be marked with a "B" by Pin 8. Refer to the mechanical section for the location.

PIN CONFIGURATION



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

ABSOLUTE MAXIMUM RATINGS

Supply	±5.5VDC
Internal Power Dissipation[1]	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	–65°C to +150°C
P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA642H, HSQ	8-Pin Sidebraze DIP	157
OPA642P, PB	8-Pin DIP	006
OPA642U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

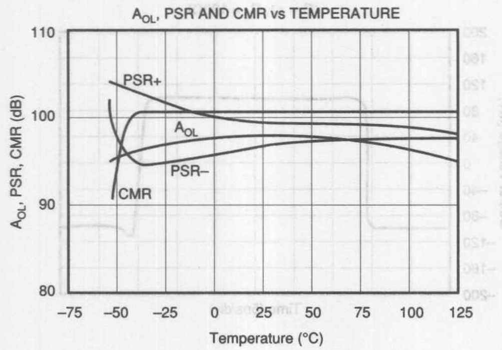
ELECTROSTATIC DISCHARGE SENSITIVITY

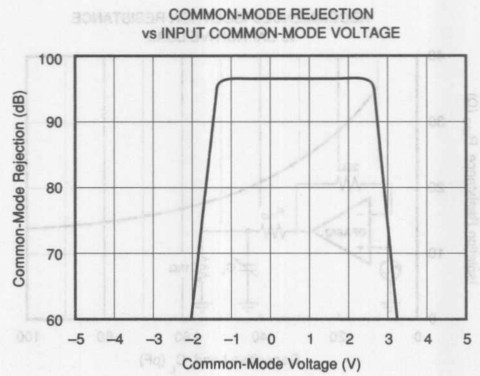
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

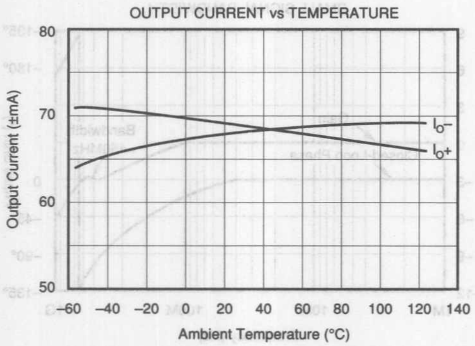
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

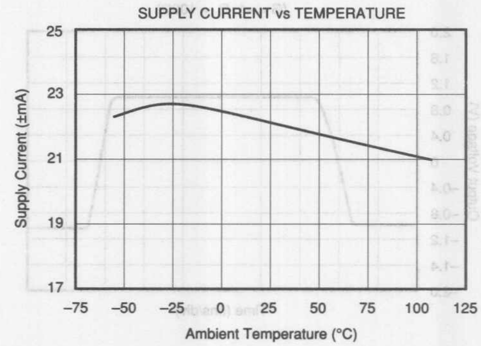
TYPICAL PERFORMANCE CURVES

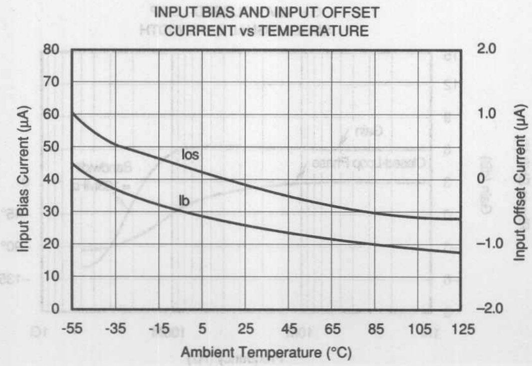
$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

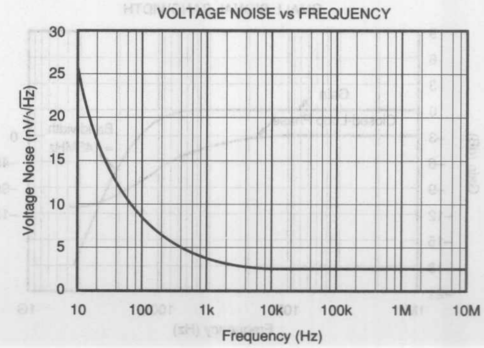




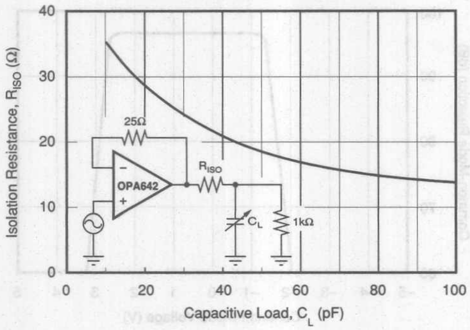




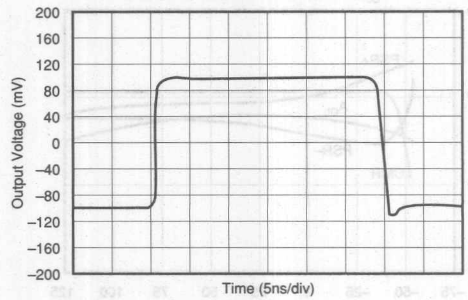




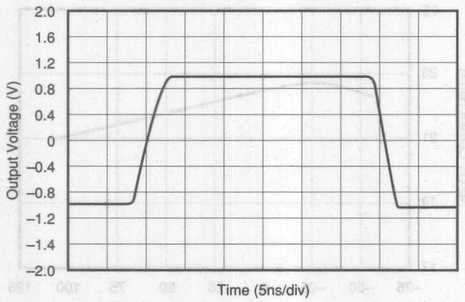
RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD



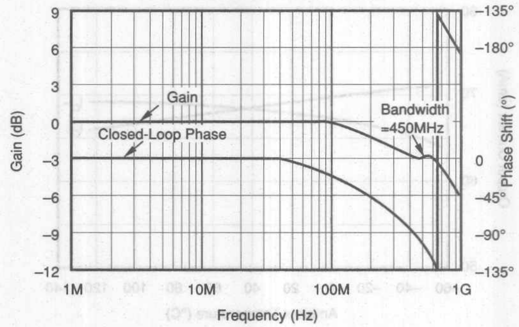
SMALL SIGNAL TRANSIENT RESPONSE ($G = +1$, $R_L = 100\Omega$)



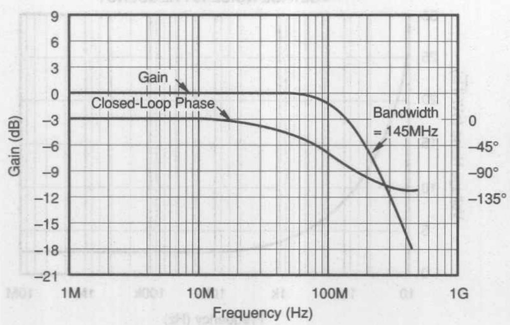
LARGE SIGNAL TRANSIENT RESPONSE ($G = +1$, $R_L = 100\Omega$)



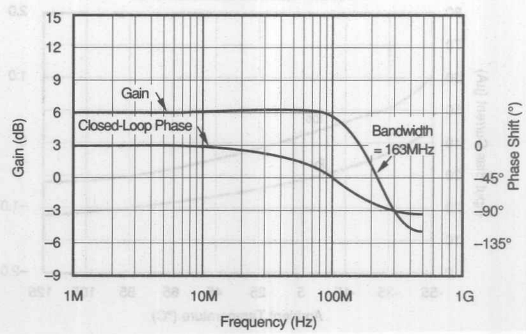
G = +1V/V CLOSED-LOOP SMALL SIGNAL BANDWIDTH



G = –1V/V CLOSED-LOOP SMALL SIGNAL BANDWIDTH



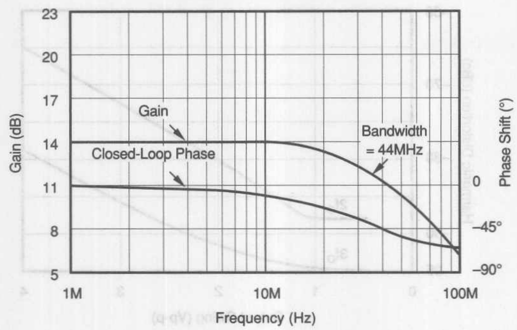
G = +2V/V CLOSED-LOOP SMALL SIGNAL BANDWIDTH



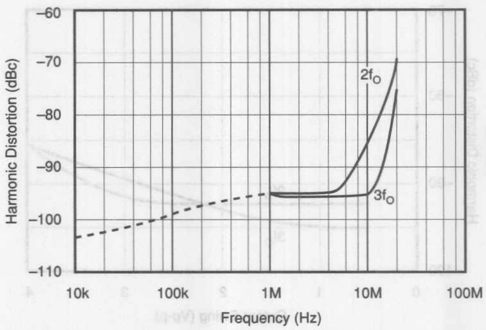
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

G = +5V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

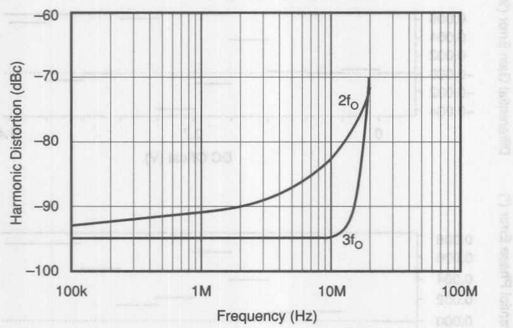


HARMONIC DISTORTION vs FREQUENCY
(G = +1, V_O = 2Vp-p, R_L = 100Ω)

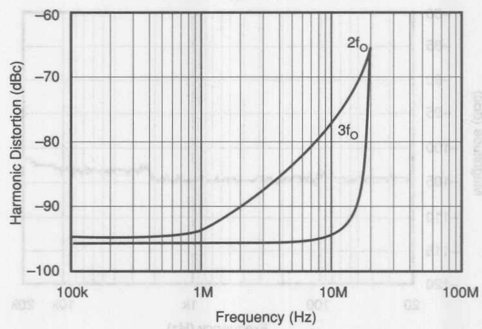


NOTE: The Dashed Line Represents THD + N
The Actual Harmonics will be Lower.

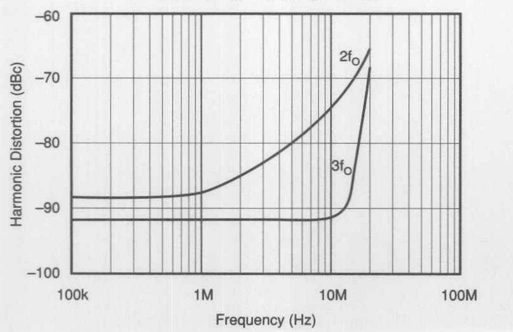
HARMONIC DISTORTION vs FREQUENCY
(G = –1, V_O = 2Vp-p, R_L = 100Ω)



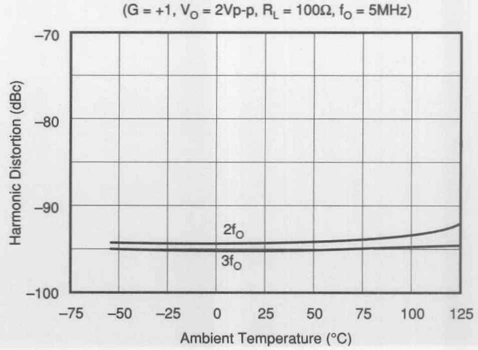
HARMONIC DISTORTION vs FREQUENCY
(G = +2, V_O = 2Vp-p, R_L = 100Ω)



HARMONIC DISTORTION vs FREQUENCY
(G = +5, V_O = 2Vp-p, R_L = 100Ω)

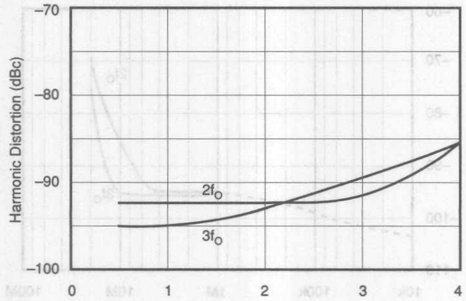


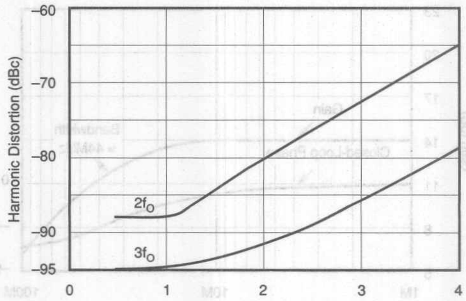
HARMONIC DISTORTION vs TEMPERATURE
(G = +1, V_O = 2Vp-p, R_L = 100Ω, f_O = 5MHz)

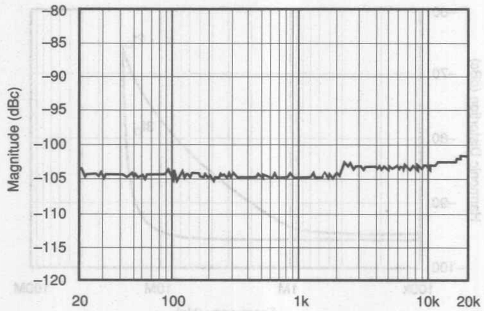


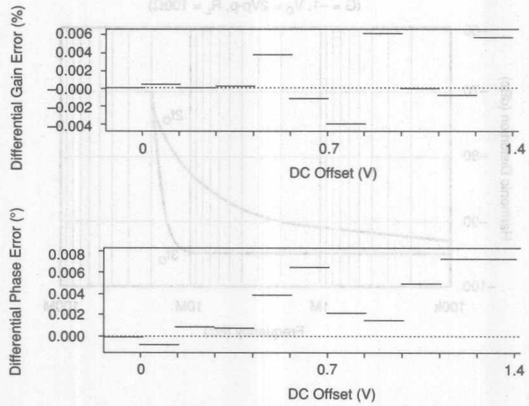
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = ±5V$, $R_L = 100Ω$, $C_L = 2pF$, $R_{FB} = 402Ω$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25Ω$ for a gain of +1.









APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA642 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA642's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Cancelling offset errors due to input bias currents through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA642's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA642.

WIRING PRECAUTIONS

Maximizing the OPA642's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA642, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2µF) with very short leads are recommended. A parallel 0.01µF ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages and improve the AC performance **including lower distortion.** The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface mount capacitors is recommended. It is essential to keep the 0.01µF capacitor very close to the power supply pins. Refer to the DEM-OPA64X Data Sheet for the recommended layout and component placements.

2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on backside of PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA642 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. Refer to the demonstration board layout at the end of the data sheet. **A longer feedback path than this will decrease the realized bandwidth substantially.**

recommended. Circuits using all surface mount components with the OPA642U (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

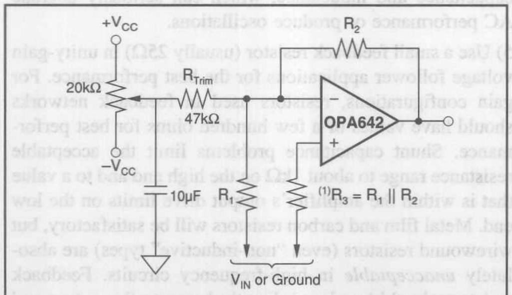
9) Standard commercial test equipment has not been designed to test devices in the OPA642's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current.



$$\text{Output Trim Range} \cong +V_{CC}\frac{R_2}{R_{Trim}} \text{ to } -V_{CC}\frac{R_2}{R_{Trim}}$$

NOTE: (1) R_3 is optional and can be used to cancel offset errors due to input bias currents.

FIGURE 1. Offset Voltage Trim.

vices, but any semiconductor device deserves protection from this potentially damaging source. The OPA642 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

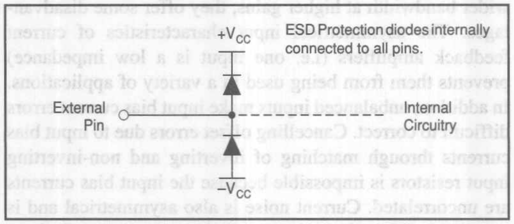


FIGURE 2. Internal ESD Protection.

All pins on the OPA642 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA642 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA642.

OUTPUT DRIVE CAPABILITY

The OPA642 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA642 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA642 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

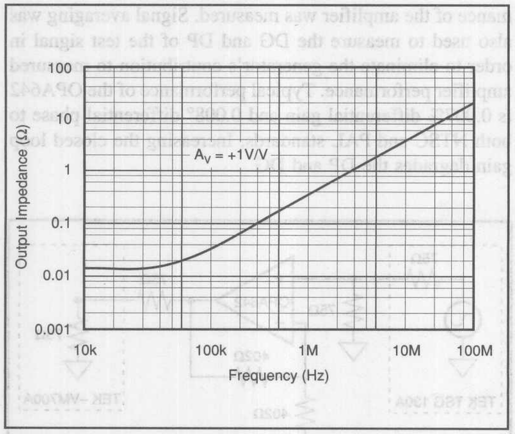


FIGURE 3. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA642 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, P_{DQ} = 10V x 27mA = 270mW, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max $= (\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

A short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in Figure 4.

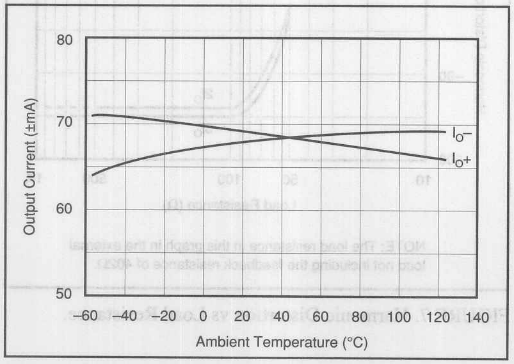


FIGURE 4. Output Current vs Temperature.

CAPACITIVE LOADS

The OPA642's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 2pF should be buffered by connecting a small resistance, usually 10Ω to 35Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the Gain from +1 will improve the capacitive load drive due to increased phase margin.

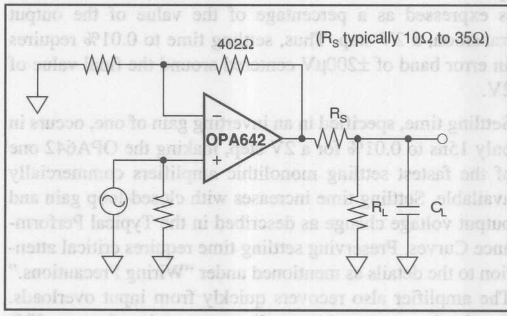


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA642 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA642 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break

frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200μV centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 15ns to 0.01% for a 2V step, making the OPA642 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 90ns.

In practice, settling time measurements on the OPA642 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

DG and DP of the OPA642 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with a sync pulse.

With these conditions the test circuit shown in Figure 6 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA642 is 0.007% differential gain and 0.008° differential phase to both NTSC and PAL standards. Increasing the closed loop gain degrades the DP and DG.

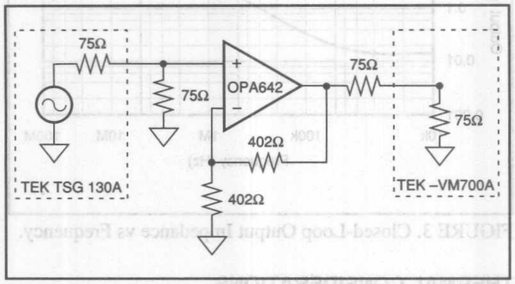


FIGURE 6. Differential Gain and Differential Phase Test Circuit.

DISTORTION

The OPA642's Harmonic Distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 7. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

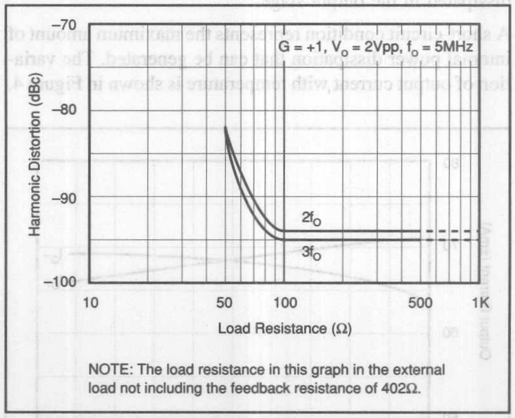


FIGURE 7. Harmonic Distortion vs Load Resistance.

The third-order intercept point is an important parameter for many RF amplifier applications. Figure 8 shows the OPA642's single tone, third-order IM Intercept vs Frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency and load resistance. For example, assume that the application requires the OPA642 to operate in a gain of +1V/V and drive 2Vp-p into 50Ω at a frequency of 5MHz. Referring to Figure 8, we find that the intercept point is +58dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level, dBm

For this case OPI^3P = 58dBm, P_O = 10dBm, and the third harmonic = 2(58 – 10) = 96dB below the fundamental. The OPA642's low distortion makes the device an excellent choice for a variety of RF signal processing applications. The two-tone third-order intercept point is approximately 8dB lower than the single tone intercept.

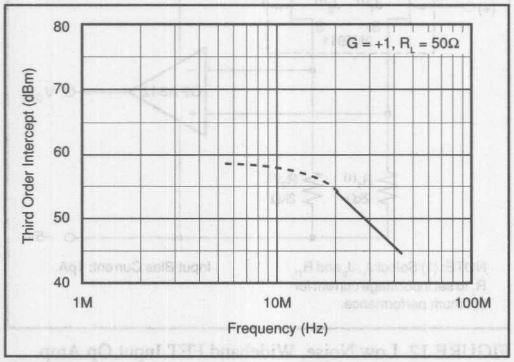


FIGURE 8. Single Tone, 3rd-Order Intercept vs Frequency.

NOISE FIGURE

The OPA642 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA642's Noise Figure vs Source Resistance is shown in Figure 9.

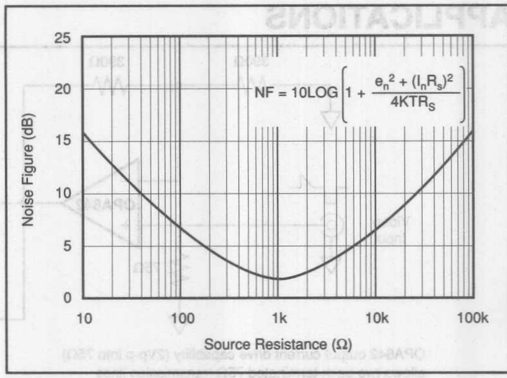


FIGURE 9. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA642. Contact Burr-Brown Applications Department to receive a spice diskette.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device —it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = –65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate < 5 x 10^{-8} atm cc/s, 30PSiG Gross: per Fluorocarbon bubble test, 60PSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on the HS package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64x Datasheet for details.

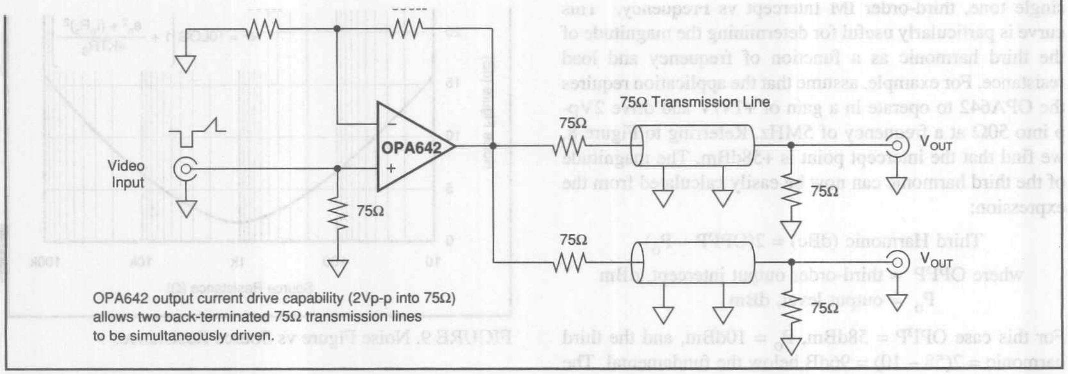


FIGURE 10. Video Distribution Amplifier.

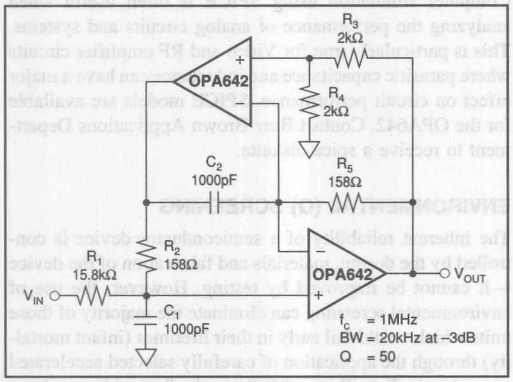


FIGURE 11. High-Q 1MHz Bandpass Filter.

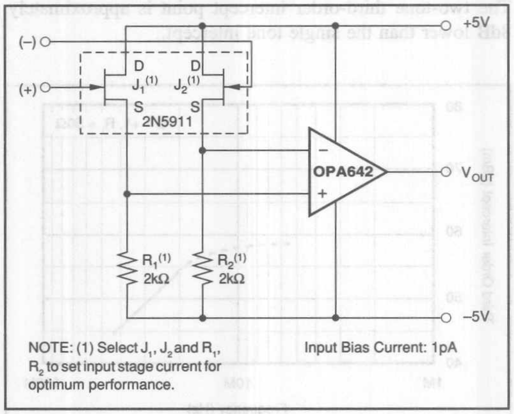


FIGURE 12. Low Noise, Wideband FET Input Op Amp.

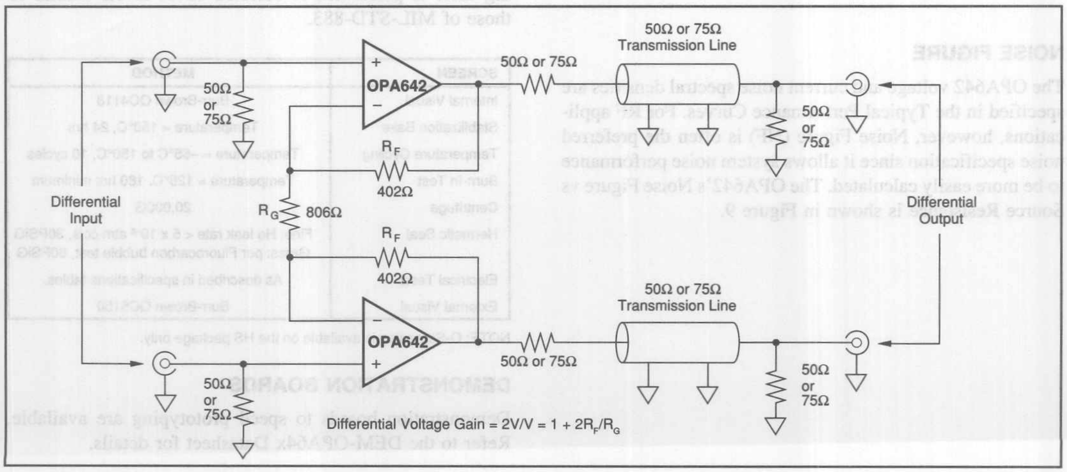


FIGURE 13. Differential Line Driver for 50Ω or 75Ω Systems.

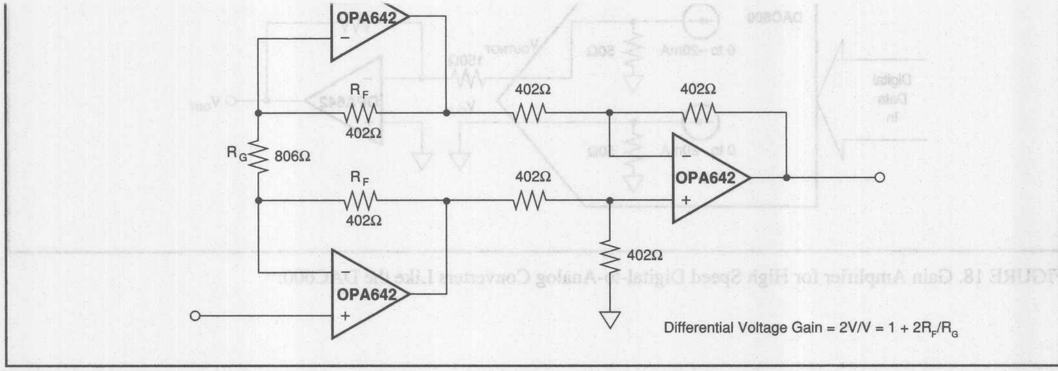


FIGURE 14. Wideband, Fast-Settling Instrumentation Amplifier.

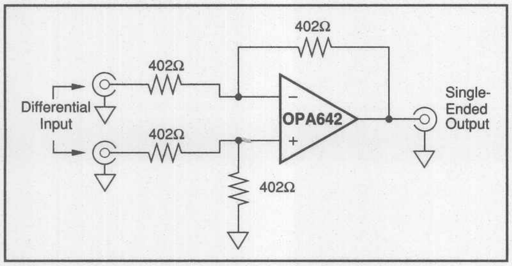


FIGURE 15. Unity Gain Difference Amplifier.

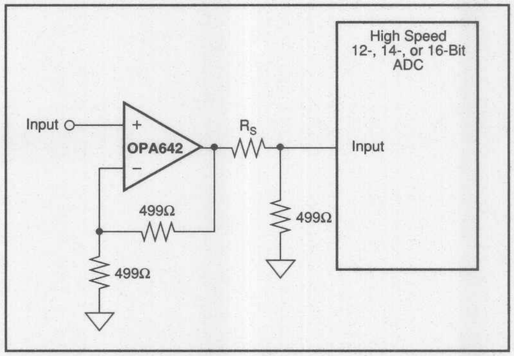


FIGURE 16. Low Distortion Gain Amplifier for ADCs (G = –2V/V).

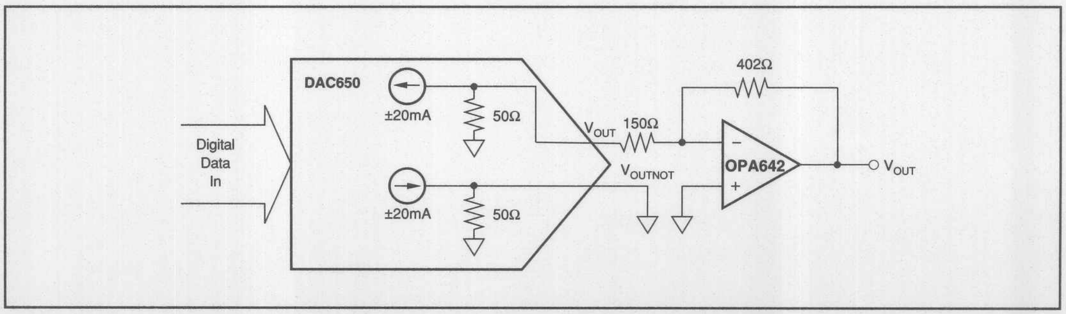


FIGURE 17. Gain Amplifier for High Speed Digital-to-Analog Converters Like the DAC650.

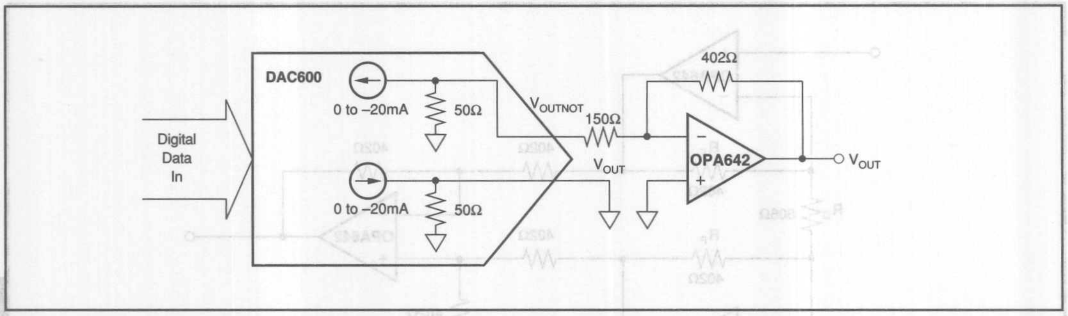


FIGURE 18. Gain Amplifier for High Speed Digital-to-Analog Converters Like the DAC600.

BURR - BROWN®

OPA643

DEMO BOARD AVAILABLE
See Appendix A

Wideband Low Distortion OPERATIONAL AMPLIFIER

FEATURES

- LOW DISTORTION: –90dBc at 5MHz
- LOW NOISE: 1.8nV/√Hz
- GAIN-BANDWIDTH: 1.5GHz
- STABLE IN GAINS ≥ 5
- HIGH SLEW RATE: 1000V/µs
- HIGH OPEN LOOP GAIN: 95dB
- HIGH COMMON-MODE REJECTION: 90dB
- FAST 12-BIT SETTLING: 21ns (0.01%)
- LOW DIFFERENTIAL GAIN/PHASE ERROR: 0.005%/0.015°

APPLICATIONS

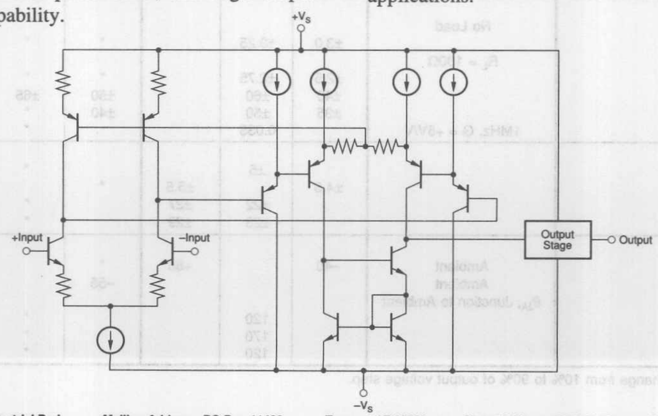
- ADC/DAC GAIN AMPLIFIER
- LOW DISTORTION COMMUNICATIONS
- HIGH RESOLUTION IMAGING
- MEDICAL IMAGING
- LOW NOISE PREAMPLIFIER
- VIDEO AMPLIFICATION
- TEST INSTRUMENTATION
- AUDIO AMPLIFICATION

DESCRIPTION

The OPA643 is a voltage feedback operational amplifier featuring an unusual combination of high open-loop gain and high bandwidth. The high open loop gain allows for minimal DC errors. The extra open-loop gain at high bandwidths gives exceptionally low harmonic distortion. This makes the OPA643 compatible with high resolution and high dynamic range systems. It also offers fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA643 is internally compensated for stability in gains of 5 or greater. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. This allows the OPA643 to be used in all op amp applications requiring high speed and precision.

Low distortion, low noise, and high linearity make this amplifier suitable for RF, video, imaging, and audio applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

$T_A = +25°C$, $V_S = ±5V$, $R_L = 100Ω$, $C_L = 2pF$, $R_{FB} = 402Ω$ and all four power supply pins are used unless otherwise noted.

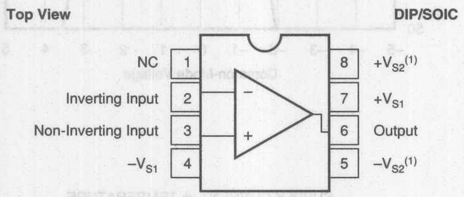
		OPA643H, P, U			OPA643HSQ, PB, UB			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE								
Input Offset Voltage			±2.5	±4		±0.5	±1.5	mV
Average Drift			5			3		μV/°C
HSQ Grade Over Temperature						±2.5	±5	mV
Power Supply Rejection (+V_S)	V_S = ±4.5 to ±5.5V	65	85		70	*		dB
INPUT BIAS CURRENT(1)								
Input Bias Current	V_{CM} = 0V		19	30		*	*	μA
Over Specified Temperature			24	40		*	*	μA
HSQ Grade Over Temperature						2.5	40	μA
Input Offset Current	V_{CM} = 0V		0.1	2.0		*	*	μA
Over Specified Temperature			0.5	3.0		*	*	μA
HSQ Grade Over Temperature						1.0	5.0	μA
NOISE								
Input Voltage Noise								
Noise Density: f = 100Hz			10.3			*		nV/√Hz
f = 10kHz			1.9			*		nV/√Hz
f = 1MHz			1.8			*		nV/√Hz
f_B = 1MHz to 100MHz			1.8			*		nV/√Hz
Voltage Noise, BW = 100Hz to 100MHz			18			*		μVrms
Input Bias Current Noise								
Current Noise Density, f = 0.1Hz to 20kHz			2.4			*		pA/√Hz
Noise Figure								
R_S = 1kΩ			1.6			*		dB
R_S = 50Ω			7.0			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.75	±3.0		*	*		V
Over Specified Temperature		±2.5	±3.0		*	*		V
Common-Mode Rejection	V_{CM} = ±0.5V	65	85		80	92		dB
INPUT IMPEDANCE								
Differential			15 || 1			*		kΩ || pF
Common-Mode			8 || 1			*		MΩ || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	82	95		87	*		dB
Over Specified Temperature	V_O = ±2V, R_L = 100Ω	80	90		82	*		dB
FREQUENCY RESPONSE, R_{FB} = 402Ω	All Four Power Pins Used							
Closed-Loop Bandwidth	Gain = +5V/V		300			*		MHz
	Gain = +10V/V		112			*		MHz
	Gain = +20V/V		47			*		MHz
Slew Rate(1)	G = +5, 2V Step		1000			*		V/μs
At Minimum Specified Temperature	G = +5, 2V Step		920			*		V/μs
Settling Time: 0.003%	G = +5, 2V Step		60			*		ns
0.01%	G = +5, 2V Step		21			*		ns
0.1%	G = +5, 2V Step		16.5			*		ns
1%	G = +5, 2V Step		7.5			*		ns
Spurious Free Dynamic Range	G = +5, f = 5MHz, V_O = ±2Vp-p, R_L = 100Ω		90		80	90		dBc
Differential Gain Error at 3.58MHz	G = +5V/V, V_O = 0V to 1.4V, R_L = 150Ω		0.005			*		%
Differential Phase Error at 3.58MHz	G = +5V/V, V_O = 0V to 1.4V, R_L = 150Ω		0.015			*		degrees
OUTPUT								
Voltage Output	No Load							
Over Specified Temperature		±3.0	±3.25		*	*		V
Voltage Output, +25°C	R_L = 100Ω							
Over Specified Temperature		±2.5	±2.75		*	*		V
Current Output, +25°C		±40	±60		±50	±65		mA
Over Specified Temperature		±35	±50		±40	*		mA
Output Resistance	1MHz, G = +5V/V		0.035			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Operating Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current			±22	±27		*	*	mA
Over Specified Temperature			±23	±29		*	*	mA
TEMPERATURE RANGE								
Specification: H, P, U	Ambient	–40		+85	*		*	°C
HSQ	Ambient				–55		+125	°C
Thermal Resistance	θ_{JA}, Junction to Ambient							
P			120			*		°C/W
U			170			*		°C/W
H			120			*		°C/W

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

Basic Model Number
Package Code
H = 8-pin Sidebraze DIP
P = 8-pin Plastic DIP
U = 8-pin Plastic SOIC
Performance Grade Code
S = –55°C to +125°C
B(1) or No Letter = –40°C to +85°C
Reliability Screening
Q = Q-Screened (HSQ Model Only)

NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by Pin 8. Refer to the mechanical section for the location.

PIN CONFIGURATION



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

Internal Power Dissipation(1) .... See Applications Information
Differential Input Voltage .... Total V_{CC}
Input Voltage Range .... See Applications Information
Storage Temperature Range: H, HSQ .... –65°C to +150°C
P, PB, U, UB .... –40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
(soldering, SOIC 3s) .... +260°C
Junction Temperature (T_J) .... +175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA643H, HSQ	8-Pin Cerdip	157
OPA643P, PB	8-Pin DIP	006
OPA643U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

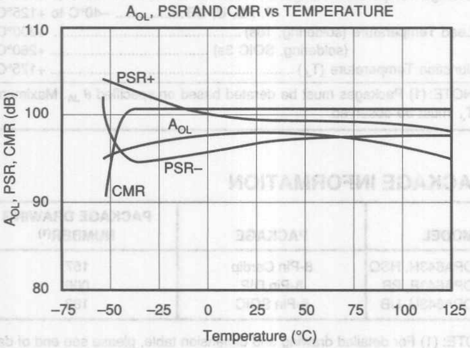
ELECTROSTATIC DISCHARGE SENSITIVITY

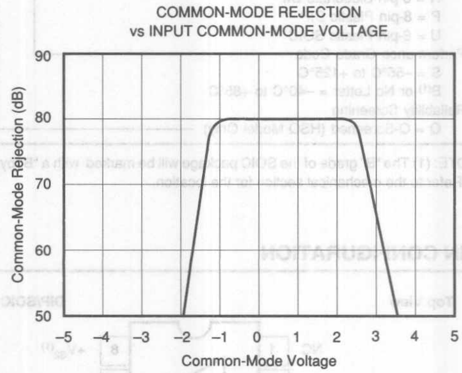
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

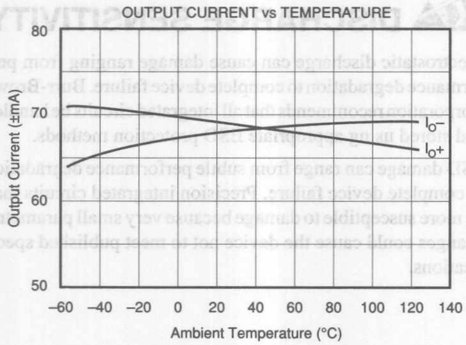
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

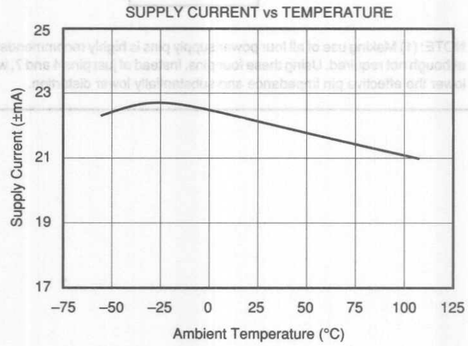
TYPICAL PERFORMANCE CURVES

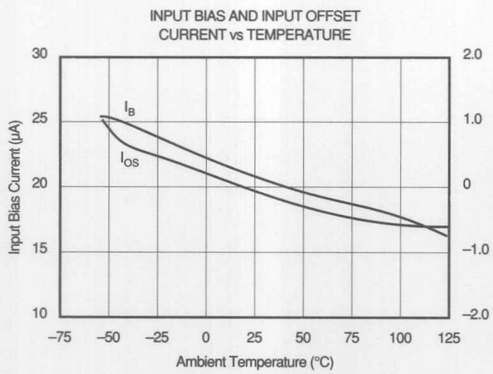
$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted

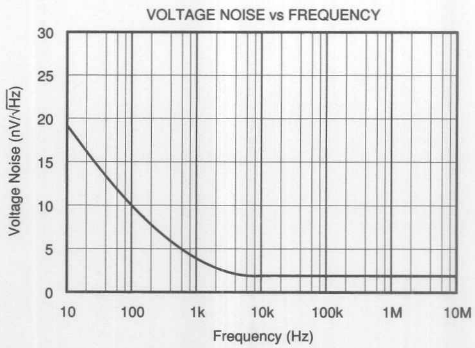








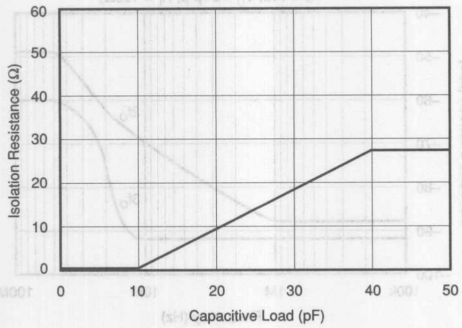




TYPICAL PERFORMANCE CURVES (CONT)

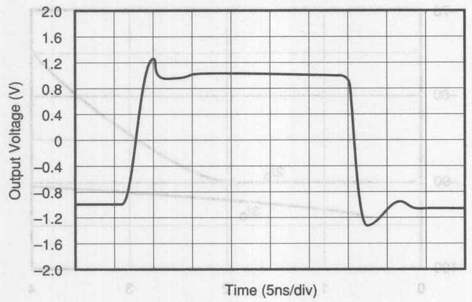
$T_A = +25°C$, $V_S = \pm 5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted.

RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD FOR G = +5

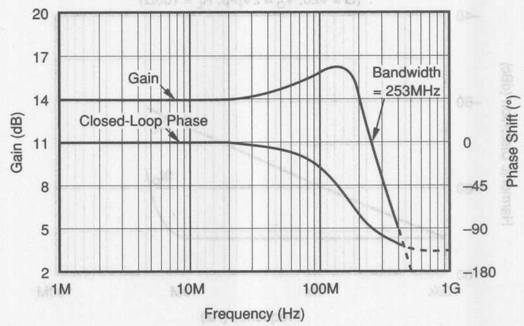


SMALL SIGNAL TRANSIENT RESPONSE (G = +5, R_L = 100Ω)

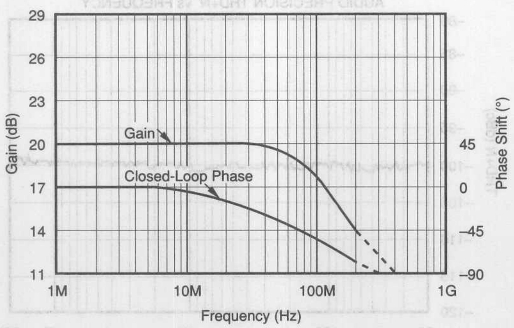
LARGE SIGNAL TRANSIENT RESPONSE (G = +5, R_L = 100Ω)



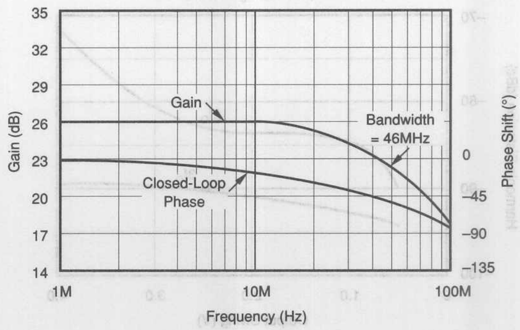
G = CLOSED-LOOP SMALL SIGNAL BANDWIDTH



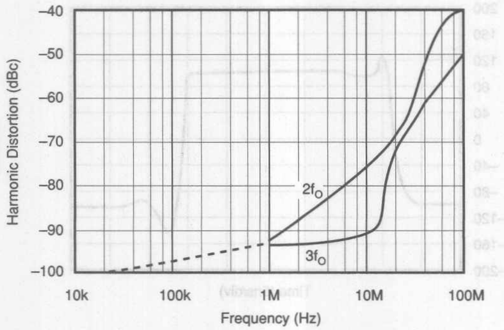
G = +10 CLOSED-LOOP SMALL SIGNAL BANDWIDTH



G = +20 CLOSED-LOOP SMALL SIGNAL BANDWIDTH

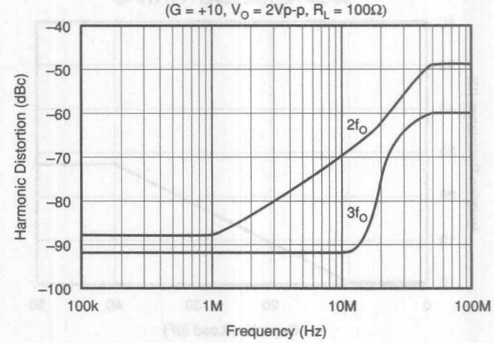


HARMONIC DISTORTION vs FREQUENCY
($G = +5$, $V_O = 2Vp\text{-}p$, $R_L = 100\Omega$)

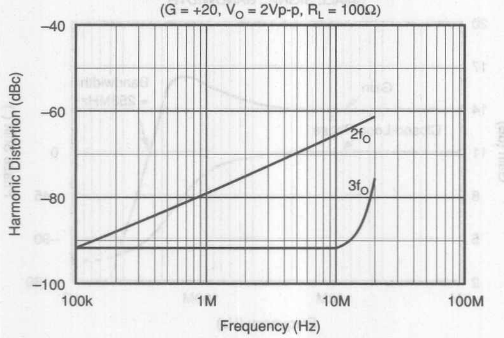


NOTE: The Dashed Line Represents THD + N.
The Actual Harmonics will be lower.

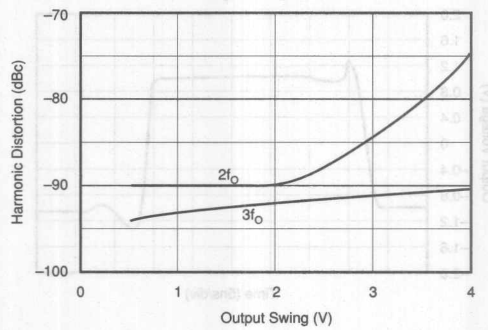
HARMONIC DISTORTION vs FREQUENCY
($G = +10$, $V_O = 2Vp\text{-}p$, $R_L = 100\Omega$)



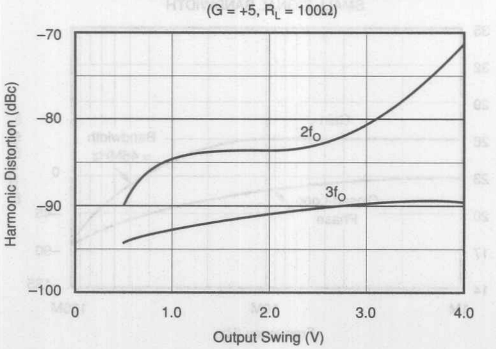
HARMONIC DISTORTION vs FREQUENCY
($G = +20$, $V_O = 2Vp\text{-}p$, $R_L = 100\Omega$)



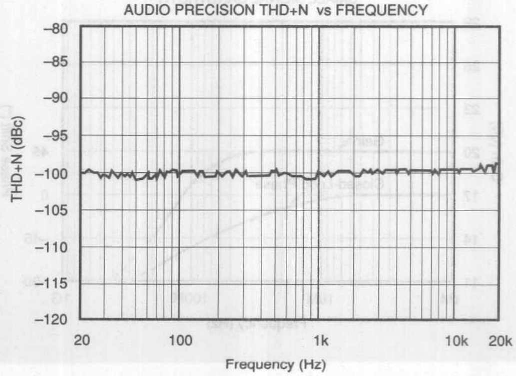
5MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = +5$, $R_L = 100\Omega$)



10MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = +5$, $R_L = 100\Omega$)

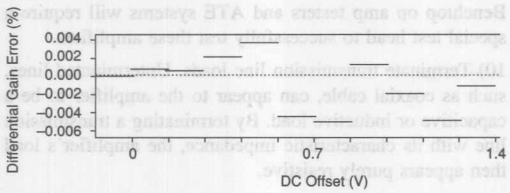


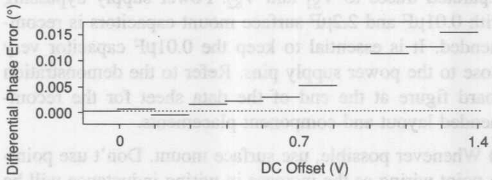
AUDIO PRECISION THD+N vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted.





APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA643 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA643's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e., one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Cancelling offset errors (due to input bias currents) through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA643's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA643.

WIRING PRECAUTIONS

Maximizing the OPA643's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA643, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2 oz. copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2µF) with very short leads are recommended. A parallel 0.01µF ceramic must also be added. Surface-mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective pin impedance seen by the input and output stages. This will improve the AC performance **including lower distortion**. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface mount capacitors is recommended. It is essential to keep the 0.01µF capacitor very close to the power supply pins. Refer to the demonstration board figure at the end of the data sheet for the recommended layout and component placements.

2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on backside of PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA643 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. **A longer feedback path than this will decrease the realized bandwidth substantially**. Refer to the demonstration board layout at the end of the data sheet.

6) Surface-mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface-mount components with the OPA643U (SOIC package) will offer the best AC performance. The parasitic package impedance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

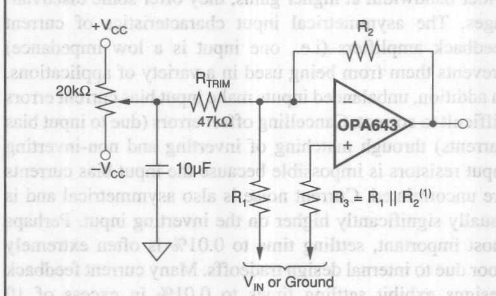
9) Standard commercial test equipment has not been designed to test devices in the OPA643's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current, which is typically only 0.2µA.



$$\text{Output Trim Range} \cong +V_{CC}\frac{R_2}{R_{Trim}} \text{ to } -V_{CC}\frac{R_2}{R_{Trim}}$$

NOTE: (1) R_3 is optional and can be used to cancel offset errors due to input bias currents.

FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA643 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

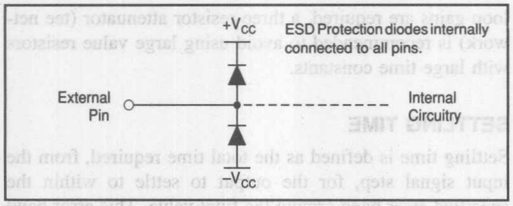


FIGURE 2. Internal ESD Protection.

All pins on the OPA643 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA643 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA643.

OUTPUT DRIVE CAPABILITY

The OPA643 has been optimized to drive 30Ω, 75Ω, and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA643 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA643 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

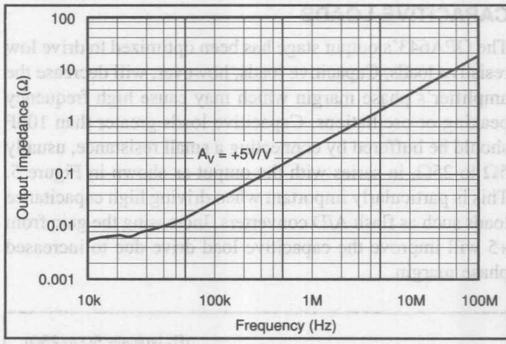


FIGURE 3. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA643 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 29mA = 290mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max $= (\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of short-circuit output current with temperature is shown in the Figure 4.

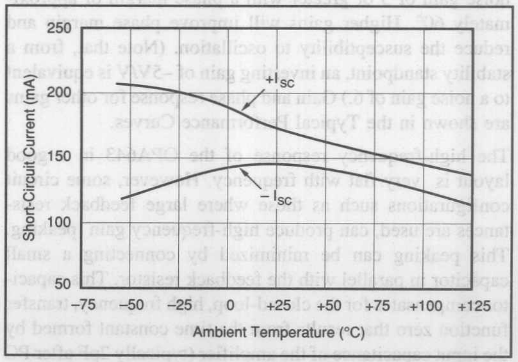


FIGURE 4. Short-Circuit Output Current vs Temperature.

OPA643

2

OPERATIONAL AMPLIFIERS

resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +5 will improve the capacitive load drive due to increased phase margin.

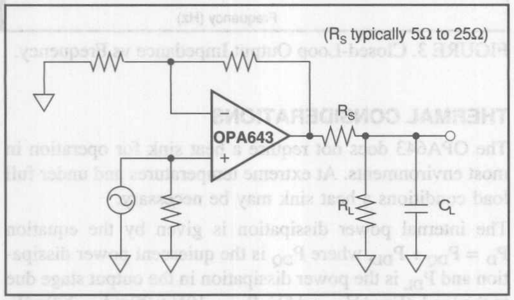


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA643 is internally compensated and is stable in a noise gain of 5 or greater with a phase margin of approximately 60°. Higher gains will improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –5V/V is equivalent to a noise gain of 6.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA643 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200μV centered around the final value of 2V.

Settling time, specified in a non-inverting gain of 5, occurs in only 15ns to 0.01% for a 2V output step, making the OPA643 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 90ns.

In practice, settling time measurements on the OPA643 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results, a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DB) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set. All PAL measurements were performed using a Rohde & Schwarz Video Analyzer UAF.

DG and DP of the OPA643 were measured with the amplifier in a gain of +5V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse.

With these conditions the test circuit shown in Figure 1 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer

was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA643 is 0.005% differential gain and 0.015° differential phase to both NTSC and PAL standards. Increasing the closed-loop gain degrades the DP and DG.

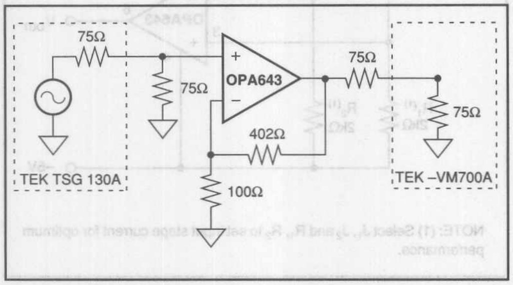


FIGURE 6. Configuration for Testing Differential Gain/Phase.

DISTORTION

The OPA643's Harmonic Distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 7. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

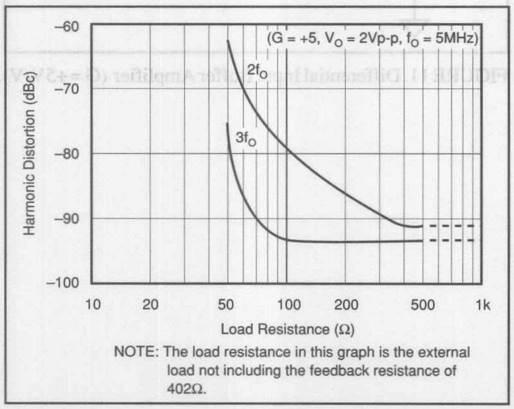


FIGURE 7. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept point is an important parameter for many RF amplifier applications. Figure 8 shows the OPA643's single-tone third-order intercept vs frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA643 to operate in a gain of +5V/V and drive 2Vp-p into 50Ω at a frequency of 5MHz. Referring to Figure 8 we find that the intercept point is +47dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level, dBm

For this case OPI^3P = 47dBm, P_O = 10dBm, and the third-order IMD = 2(47 – 10) = 74dB below the fundamental. The OPA643's low distortion makes the device an excellent choice for a variety of RF signal processing applications.

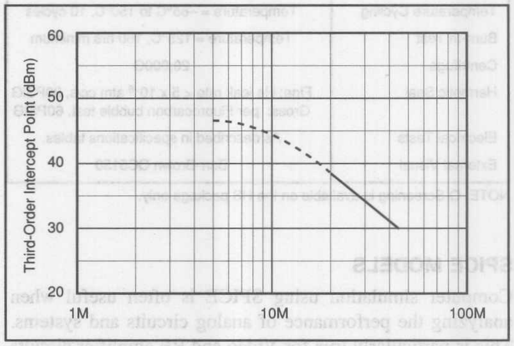


FIGURE 8. Single-Tone 3rd-Order Intermodulation Intercept vs Frequency.

NOISE FIGURE

The OPA643 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA643's Noise Figure vs Source Resistance is shown in Figure 9.

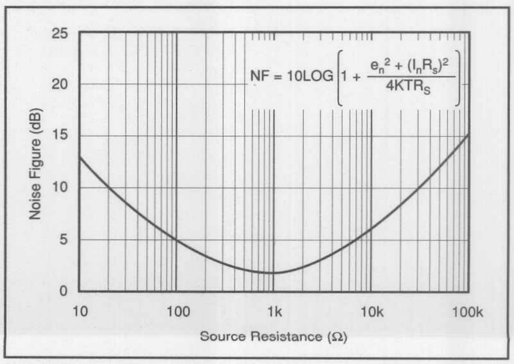


FIGURE 9. Noise Figure vs Source Resistance.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device —it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = –65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate < 5 x 10^{-8} atm cc/s, 30PSiG Gross: per Fluorocarbon bubble test, 60PSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on the HS package only.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA643. Contact Burr-Brown Applications Department to receive a spice diskette.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64X Datasheet for details.

APPLICATIONS

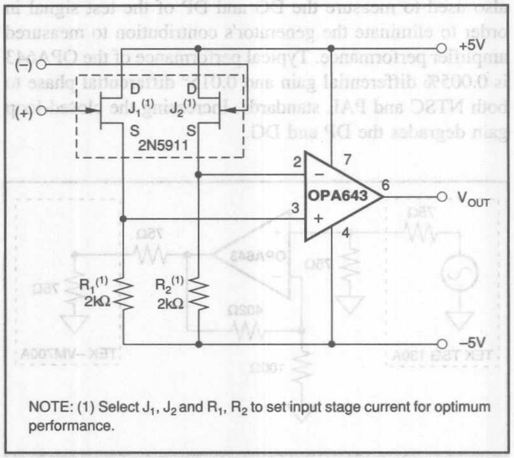


FIGURE 10. Low Noise, Wideband FET Input Op Amp.

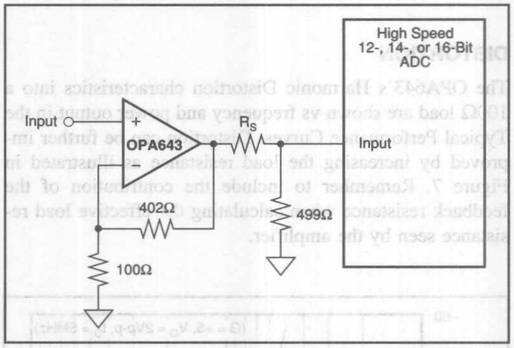


FIGURE 11. Differential Input Buffer Amplifier (G = +5V/V).

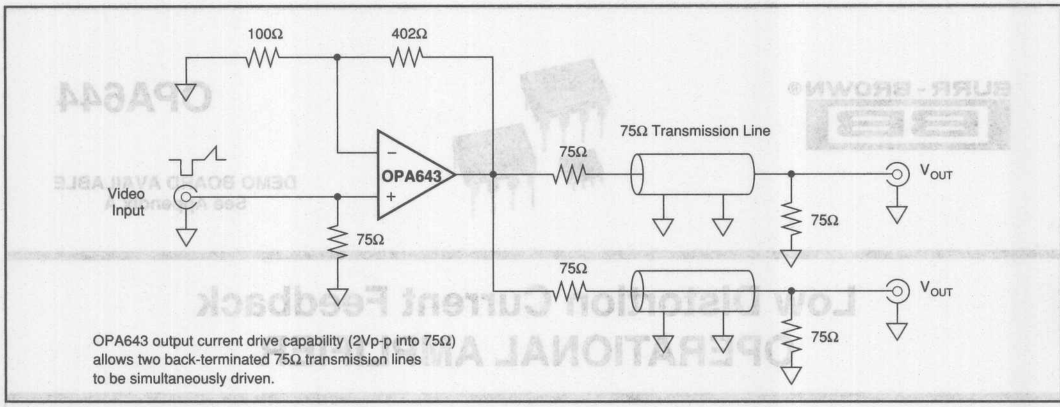


FIGURE 12. Video Distribution Amplifier.

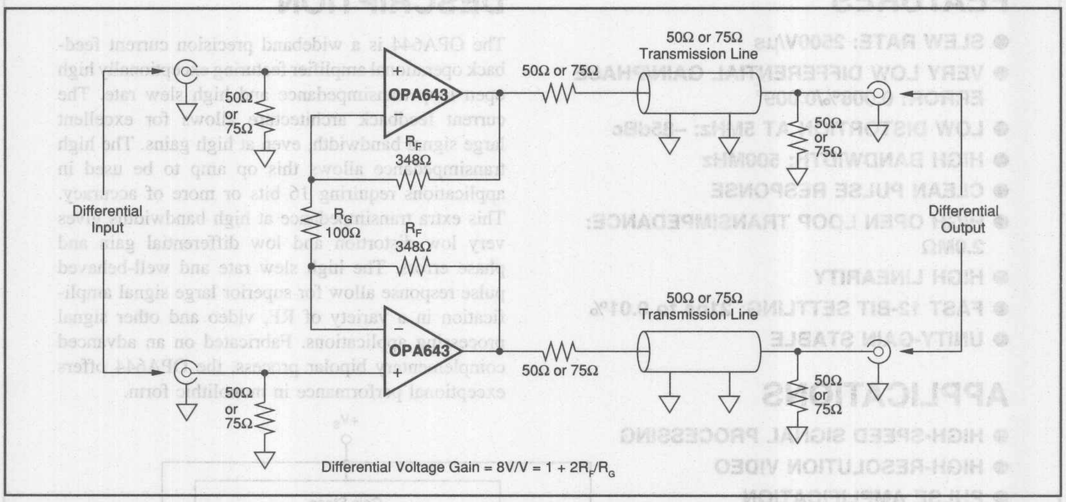


FIGURE 13. Differential Gain Amplifier and Driver for 50Ω and 75Ω Systems.

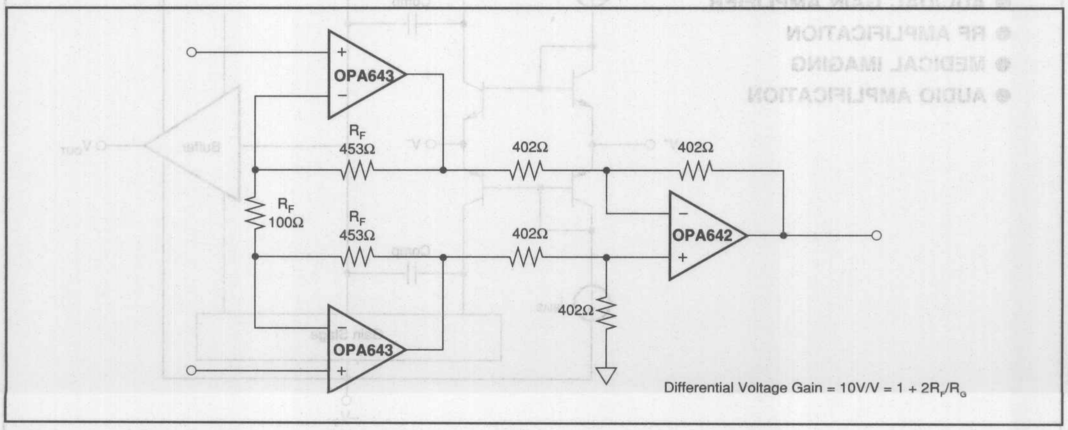


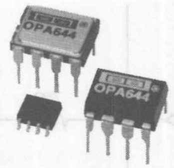
FIGURE 14. Wideband, Fast-Settling Instrumentation Amplifier with Two High Impedance Inputs.

OPA643

2

OPERATIONAL AMPLIFIERS

BURR - BROWN®



OPA644

DEMO BOARD AVAILABLE
See Appendix A

Low Distortion Current Feedback OPERATIONAL AMPLIFIER

FEATURES

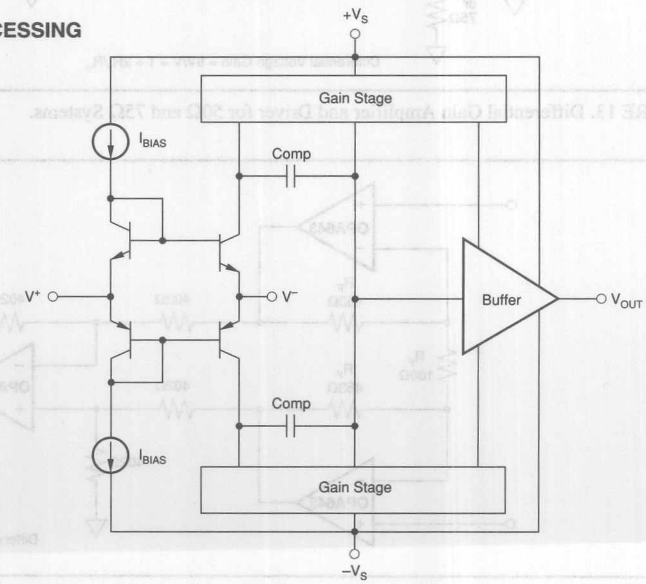
- SLEW RATE: 2500V/µs
- VERY LOW DIFFERENTIAL GAIN/PHASE ERROR: 0.008%/0.009°
- LOW DISTORTION AT 5MHz: –85dBc
- HIGH BANDWIDTH: 500MHz
- CLEAN PULSE RESPONSE
- HIGH OPEN LOOP TRANSIMPEDANCE: 2.0MΩ
- HIGH LINEARITY
- FAST 12-BIT SETTLING: 21ns to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- HIGH-RESOLUTION VIDEO
- PULSE AMPLIFICATION
- COMMUNICATIONS
- ADC/DAC GAIN AMPLIFIER
- RF AMPLIFICATION
- MEDICAL IMAGING
- AUDIO AMPLIFICATION

DESCRIPTION

The OPA644 is a wideband precision current feedback operational amplifier featuring exceptionally high open loop transimpedance and high slew rate. The current feedback architecture allows for excellent large signal bandwidth, even at high gains. The high transimpedance allows this op amp to be used in applications requiring 16 bits or more of accuracy. This extra transimpedance at high bandwidths gives very low distortion and low differential gain and phase errors. The high slew rate and well-behaved pulse response allow for superior large signal amplification in a variety of RF, video and other signal processing applications. Fabricated on an advanced complementary bipolar process, the OPA644 offers exceptional performance in monolithic form.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted.

		OPA644H, P, U			OPA644HSQ, PB, UB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE								
Input Offset Voltage	G = +10		±2.5	±6		±2	±3	mV
Average Drift			20			10		µV/°C
HSQ Grade Average Drift						20	35	µV/°C
Power Supply Rejection	V_S = ±4.5 to ±5.5V	40	65		60	75		dB
INPUT BIAS CURRENT(1)								
Non-Inverting			±20	±40		±15	±20	µA
Over Specified Temperature			±24	±90		±20	±50	µA
HSQ Grade Over Temperature						35	60	µA
Inverting			±2	±25		*	±10	µA
Over Specified Temperature			±4	±35		±3	±25	µA
HSQ Grade Over Temperature						±5	±25	µA
NOISE								
Input Voltage Noise Density	G = +10							
f = 100Hz			10.3			*		$nV/\sqrt{Hz}$
f = 1kHz			2.9			*		$nV/\sqrt{Hz}$
f = 10kHz			1.9			*		$nV/\sqrt{Hz}$
f = 1MHz			1.9			*		$nV/\sqrt{Hz}$
f_B = 100Hz to 200MHz			33.6			*		µVrms
Inverting Input Bias Current								
Noise Density: f = 10MHz			15			*		$pA/\sqrt{Hz}$
Non-Inverting Input Current								
Noise Density: f = 10MHz			15			*		$pA/\sqrt{Hz}$
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.0	±2.25		*	*		V
Over Specified Temperature		±1.8	±2.1		*	*		V
Common-Mode Rejection	V_{CM} = ±2V	35	55		45	65		dB
INPUT IMPEDANCE								
Non-Inverting			500 || 1.0			*		kΩ || pF
Inverting			20			46		Ω
Open-Loop Transimpedance	V_O = ±2V, R_L = 1kΩ	1.4	2.0		*	*		MΩ
FREQUENCY RESPONSE, R_{FB} = 402Ω	All Four Power Pins Used							
Closed-Loop Bandwidth	G = +1V/V		500			*		MHz
	G = +2V/V		300			*		MHz
	G = +5V/V		180			*		MHz
	G = +10V/V		125			*		MHz
	G = +20V/V		80			*		MHz
Slew Rate(1)	G = +2, 2V Step		2500			*		V/µs
Settling Time: 0.01%	G = +2, 2V Step		21			*		ns
0.1%	G = +2, 2V Step		16.5			*		ns
1%	G = +2, 2V Step		5.5			*		ns
Overload Recovery Time(2)			60			*		ns
Spurious Free Dynamic Range	G = −1, f = 5.0MHz		84			86		dBc
	V_O = 2Vp-p							
	G = −1, f = 20MHz							dBc
Differential Gain Error at 3.58MHz	G = +2V/V, V_O = 0V to 1.4V, R_L = 150Ω		0.008			*		%
Differential Phase Error at 3.58MHz	G = +2V/V, V_O = 0V to 1.4V, R_L = 150Ω		0.009			*		Degrees
Gain Flatness to 1dB	G = +1		250			*		MHz
OUTPUT								
Current Output		±40	±60		±50	±66		mA
Over Specified Temperature		±30	±45		±40	±50		mA
Voltage Output	No Load							
Over Specified Temperature		±3.0	±3.5		*	*		V
Voltage Output	R_L = 100Ω							
Over Specified Temperature		±2.75	±3.25		*	*		V
Short Circuit Current			75				*	mA
Output Resistance	1MHz, G = +2V/V		0.2				*	Ω
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}		±5			*		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	*		*	V
Quiescent Current	T_{MIN} to T_{MAX}		±18	±26		*	*	mA

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = +25°C$, $V_S = ±5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

PARAMETER	CONDITIONS	OPA644H, P, U MIN	OPA644H, P, U TYP	OPA644H, P, U MAX	OPA644HSQ, PB UB MIN	OPA644HSQ, PB UB TYP	OPA644HSQ, PB UB MAX	UNITS
TEMPERATURE RANGE								
Specification: H, P, U		–40		+85	*			°C
HSQ					–55		+125	°C
Thermal Resistance, θ_{JA}								
P			120			*		°C/W
U			170			*		°C/W
H			120			*		°C/W

NOTES: (1) Slew rate is rate of change from 10% to 90% of the output voltage step. (2) Time for the output to resume linear operation after saturation.

ORDERING INFORMATION

OPA644 ( ) ( )

Basic Model Number

Package Code
- H = 8-pin Sidebraze DIP
- P = 8-pin Plastic DIP
- U = 8-pin Plastic SOIC

Performance Grade Code
- SQ = –55°C to +125°C, Reliability Screened
- B(1) or No Letter = –40°C to +85°C

NOTE: (1) The "B" Grade of the SOIC package will be marked with a "B" by pin 8. Refer to the mechanical section for the location.

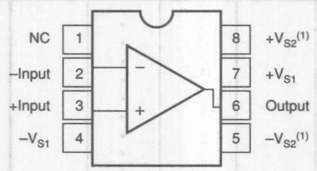
ABSOLUTE MAXIMUM RATINGS

Supply .... ±5.5VDC
Internal Power Dissipation(1) .... See Applications Information
Differential Input Voltage .... Total V_{CC}
Input Voltage Range .... See Applications Information
Storage Temperature Range: H, HSQ .... –65°C to +150°C
P, PB, U, UB .... –40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
(soldering, SOIC 3s) .... +260°C
Junction Temperature (T_J) .... +175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PIN CONFIGURATION (All Packages)

Top View — Cerdip/DIP/SOIC



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA644H, HSQ	8-Pin Cerdip	157
OPA644P, PB	8-Pin DIP	006
OPA644U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

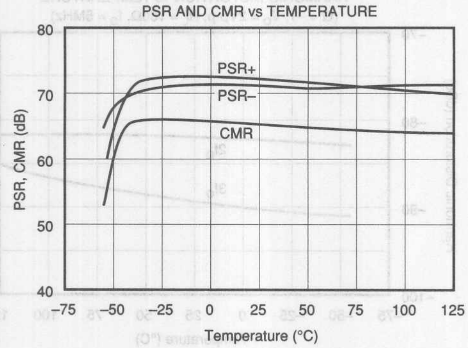
ELECTROSTATIC DISCHARGE SENSITIVITY

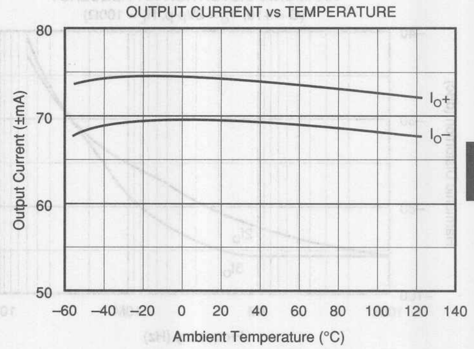
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

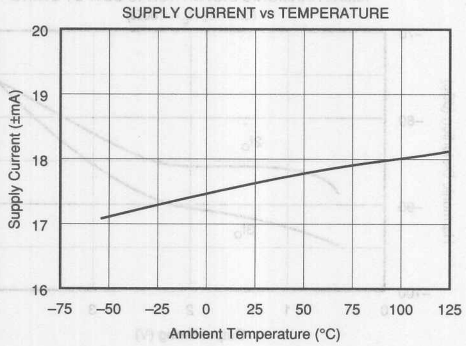
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

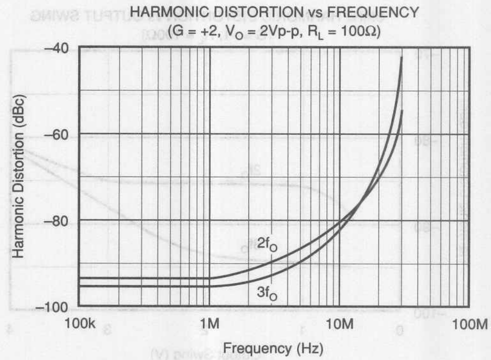
TYPICAL PERFORMANCE CURVES

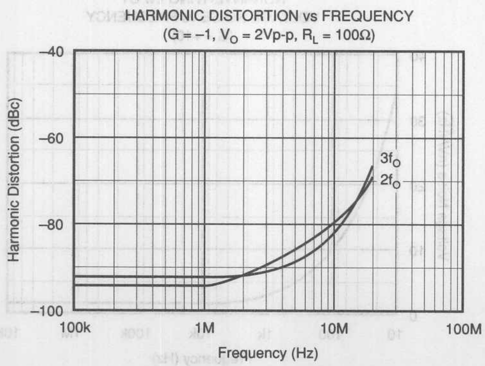
$T_A = +25°C$, $V_S = \pm 5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

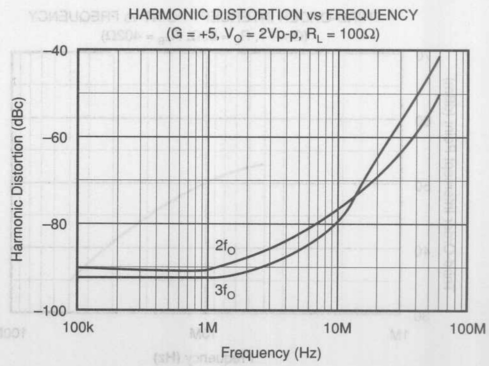






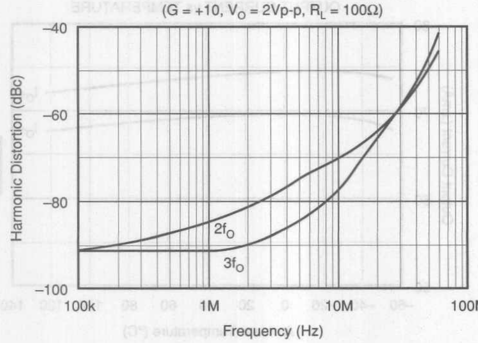




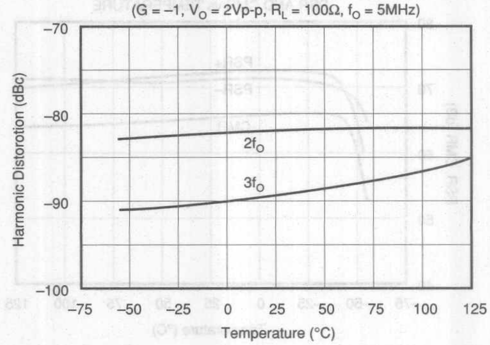


...and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

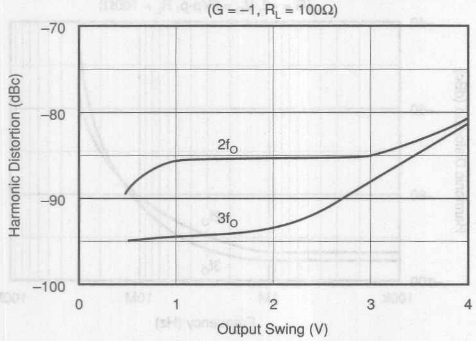
HARMONIC DISTORTION vs FREQUENCY
($G = +10$, $V_O = 2Vp\text{-}p$, $R_L = 100\Omega$)



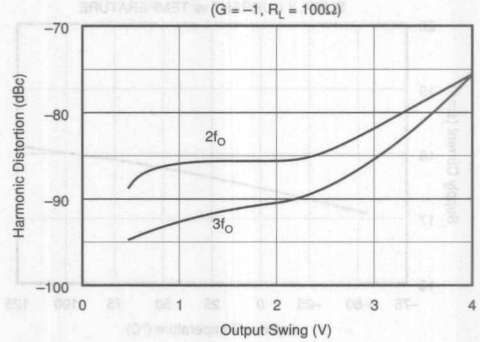
HARMONIC DISTORTION vs TEMPERATURE
($G = -1$, $V_O = 2Vp\text{-}p$, $R_L = 100\Omega$, $f_O = 5MHz$)



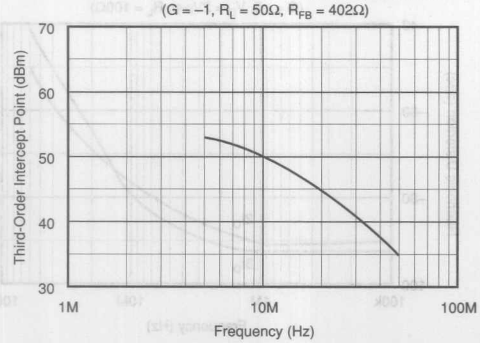
5MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = -1$, $R_L = 100\Omega$)



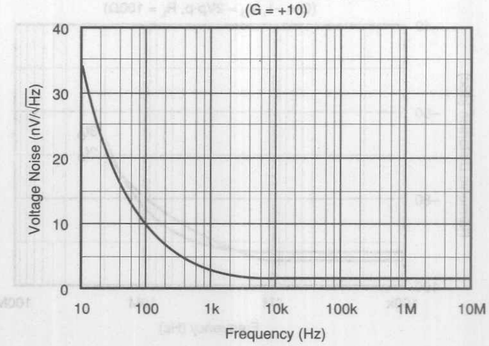
10MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = -1$, $R_L = 100\Omega$)



THIRD-ORDER INTERCEPT POINT vs FREQUENCY
($G = -1$, $R_L = 50\Omega$, $R_{FB} = 402\Omega$)

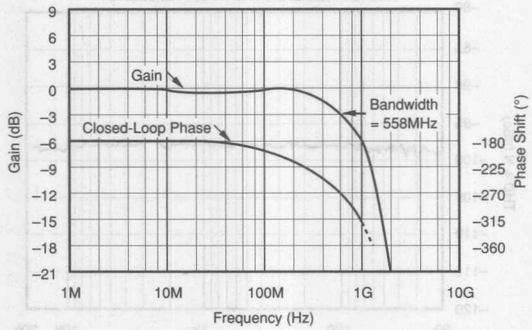


NON-INVERTING INPUT
VOLTAGE NOISE vs FREQUENCY
($G = +10$)

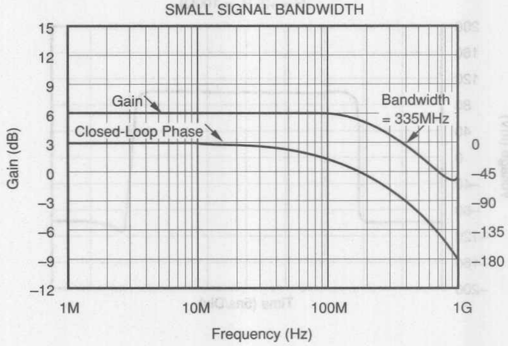


$T_A = +25°C$, $V_S = \pm 5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

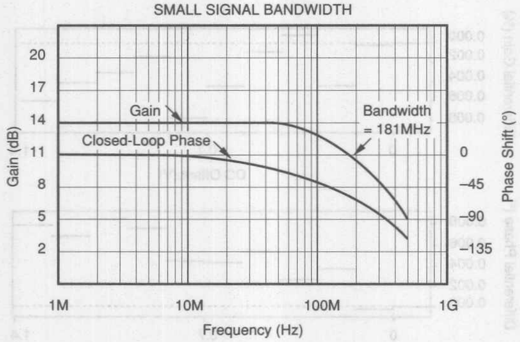
G = +1V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



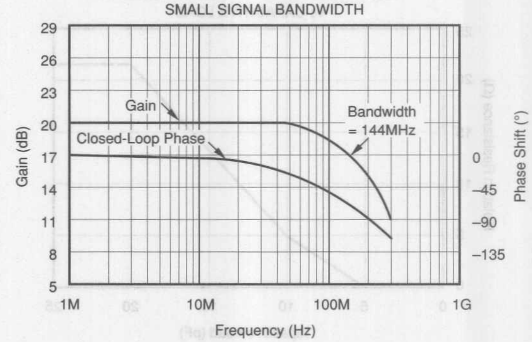
G = +2V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



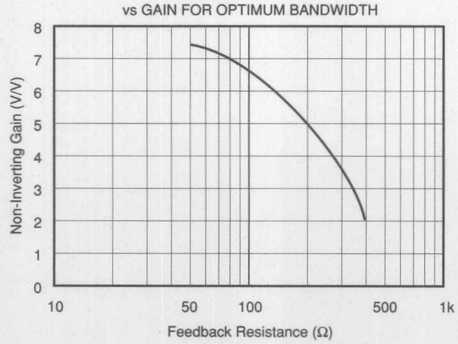
G = +5V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



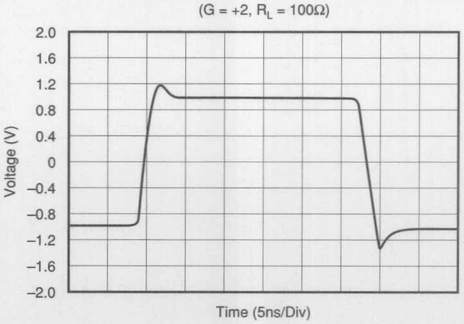
G = +10V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



FEEDBACK RESISTOR
vs GAIN FOR OPTIMUM BANDWIDTH



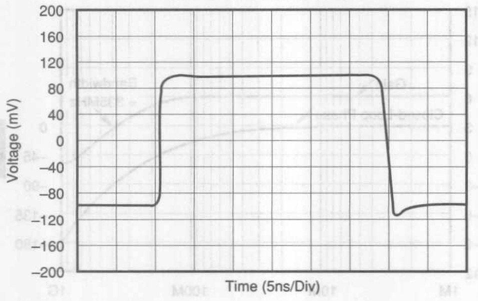
LARGE SIGNAL TRANSIENT RESPONSE
(G = +2, $R_L = 100\Omega$)



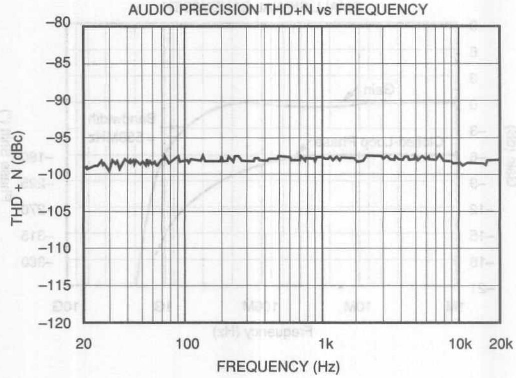
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

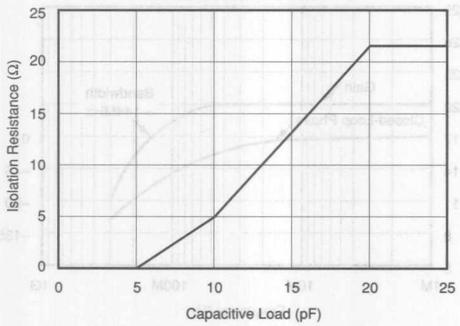
SMALL SIGNAL TRANSIENT RESPONSE
($G = +2$, $R_L = 100\Omega$)

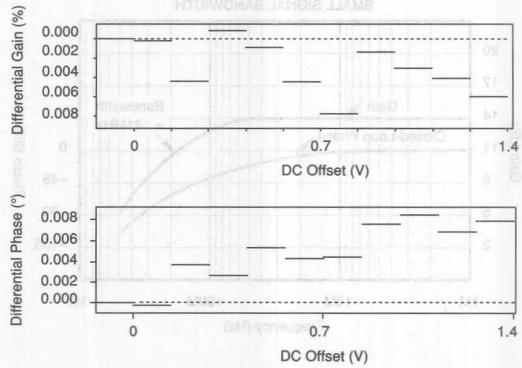


AUDIO PRECISION THD+N vs FREQUENCY



RECOMMENDED ISOLATION RESISTANCE
vs CAPACITIVE LOAD





APPLICATIONS INFORMATION

THEORY OF OPERATION

This current feedback architecture offers the following important advantages over voltage feedback architectures: (1) the high slew rate allows the large signal performance to approach the small signal performance, and: (2) there is very little bandwidth degradation at higher gain settings.

The current feedback architecture of the OPA644 provides the traditional strength of excellent large signal response with the unusual addition of very high open-loop transimpedance. This high open-loop transimpedance allows the OPA644 to be used in applications requiring 16 bits or more of accuracy and dynamic linearity.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open-loop transimpedance gain (T_O). The output signal generated is equal to $T_O \times I_E$. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

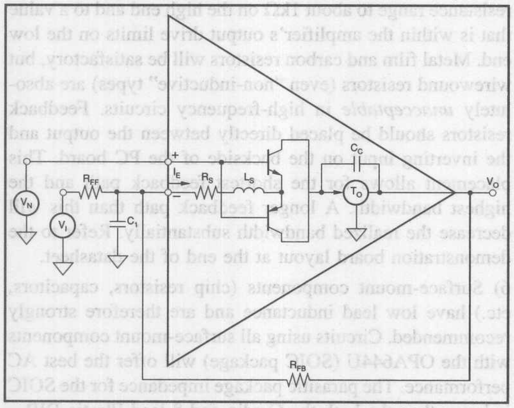


FIGURE 1. Equivalent Circuit.

For non-inverting operation, the input signal is applied to the non-inverting (high impedance buffer) input. The output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the overall gain is $(1 + R_{FF}/R_I)$.

Where a voltage-feedback amplifier has two symmetrical high impedance inputs, a current feedback amplifier has a low inverting (buffer output) impedance and a high non-inverting (buffer input) impedance.

The closed-loop gain for the OPA644 can be calculated using the following equations:

$$\text{Inverting Gain} = (-R_{FB}/R_{FF})/(1+1/\text{Loop Gain}) \quad (1)$$

$$\text{Non-inverting Gain} = (1 + R_{FB}/R_{FF})/(1 + 1/\text{Loop Gain}) \quad (2)$$

$$\text{where: Loop Gain} = T(o)/(R_{FB}) \times (1/(1+T(o)/(R_{FB}/R_{FF}))$$

At higher gains the small value inverting input impedance (R_{INV}) causes an apparent loss in bandwidth. This can be seen from the equation:

$$F_{actual} = F_{IDEAL}/(1 + (R_{INV}/R_{FB})\ (1 + R_{FB}/R_{FF})) \quad (3)$$

This loss in bandwidth at high gains can be corrected without affecting stability by lowering the value of the feedback resistor from the specified value of 402Ω.

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the input voltage and current sources that influence DC operation. The output offset is calculated by the following equation:

$$\text{Output Offset Voltage} = \pm Ib_N \times R_N\ (1 + R_{FB}/R_G) \pm V_{IO}\ (1 + R_{FB}/R_G) \pm Ib_I \times R_{FB} \quad (4)$$

If all terms are divided by the gain $(1 + R_F/R_G)$ it can be observed that input referred offsets improve as gain increases.

The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of equation 4 and applying the spectral noise values found in the Typical Performance Curve graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltages improve as the closed-loop gain increases (by keeping R_F fixed and reducing R_I with $R_N = 0\Omega$).

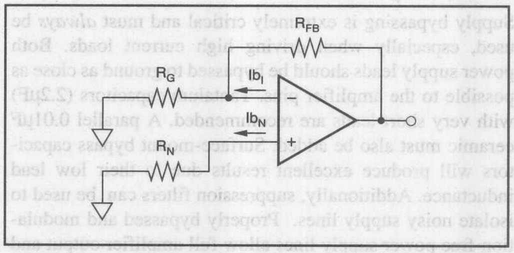


FIGURE 2. Output Offset Voltage Equivalent Circuit.

INCREASING BANDWIDTH AT HIGH GAINS

The closed-loop bandwidth can be extended at high gains by reducing the value of the feedback resistor R_{FB} (refer to Figure 1). This bandwidth reduction is caused by the feedback current being split between R_S and R_{FF}. As the gain increases (for a fixed R_{FB}), more feedback current is shunted through R_{FF}, which reduces closed-loop bandwidth. To maintain specified bandwidth, the following equations can be used to approximate R_F and R_I for any gain from ±1 to ±15:

$R_I = (424 + 8G)/G$ (inverting)

G = Closed-loop gain

WIRING PRECAUTIONS

Maximizing the OPA644's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA644, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2 oz. copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2µF) with very short leads are recommended. A parallel 0.01µF ceramic must also be added. Surface-mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply inductance seen by the input and output stages. This will improve the AC performance including lower distortion. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface-mount capacitors is recommended. It is essential to keep the 0.01µF capacitor very close to the power supply pins. Refer to the demonstration board figure in the DEM-OPA64X datasheet for the recommended layout and component placements.

detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on the backside of the PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA644 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. A longer feedback path than this will decrease the realized bandwidth substantially. Refer to the demonstration board layout at the end of the datasheet.

6) Surface-mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface-mount components with the OPA644U (SOIC package) will offer the best AC performance. The parasitic package impedance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA644's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA644 incorporates on-chip ESD protection diodes as shown in Figure 3. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

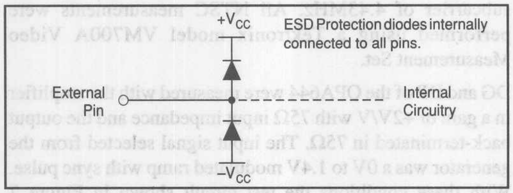


FIGURE 3. Internal ESD Protection.

All pins on the OPA644 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA644 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the machine model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA644.

OUTPUT DRIVE CAPABILITY

The OPA644 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA644 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 4, the OPA644 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

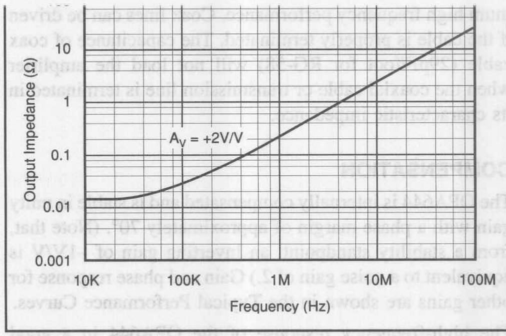


FIGURE 4. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA644 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 26mA = 260mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max $= (\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA644's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters.

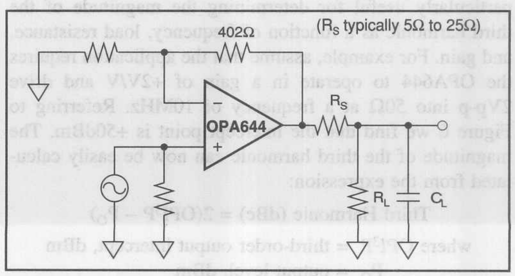


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA644 is internally compensated and is stable in unity gain with a phase margin of approximately 70°. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA644 in a good layout is very flat with frequency.

DISTORTION

The OPA644's harmonic distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

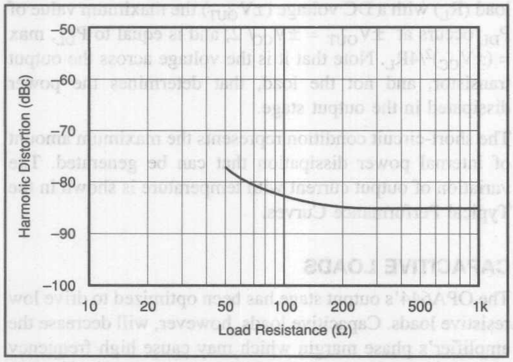


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept is an important parameter for many RF amplifier applications. Figure 6 shows the OPA644's single tone third-order intercept vs frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA644 to operate in a gain of +2V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 6 we find that the intercept point is +50dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level, dBm

For this case OPI^3P = 60dBm, P_O = 10dBm, and the third harmonic = 2(50 – 10) = 80dB below the fundamental. The OPA644's low distortion makes the device an excellent choice for a variety of RF signal processing applications.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

DG and DP of the OPA644 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 7 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA644 is 0.008% differential gain and 0.009° differential phase to both NTSC and PAL standards.

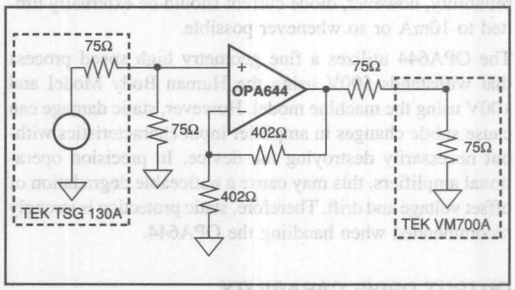


FIGURE 7. Configuration for Testing Differential Gain/Phase.

NOISE FIGURE

The OPA644's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA644's Noise Figure vs Source Resistance is shown in Figure 8.

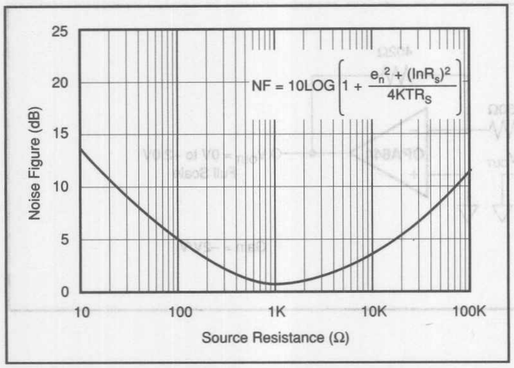


FIGURE 8. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA644. Contract Burr-Brown applications departments to receive a SPICE Diskette.

APPLICATIONS

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device —it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = –55°C to 125°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate < 5 X 10⁻⁸ atm cc/s, 30pPSiG Gross: per Fluorocarbon bubble test, 30pPSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on HS package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64X datasheet for details.

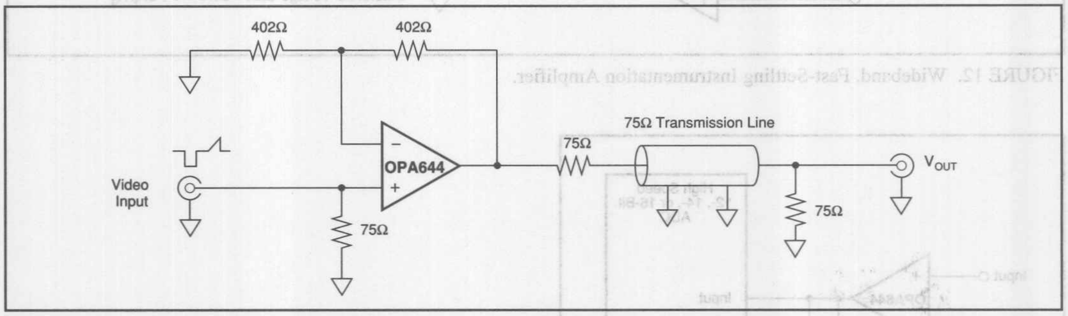


FIGURE 9. Low Distortion Video Amplifier.

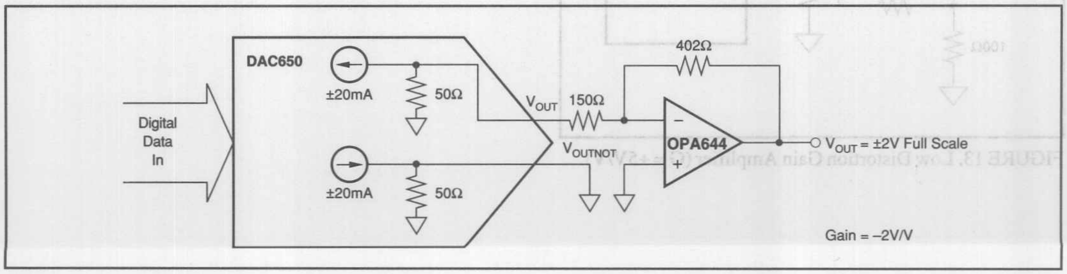


FIGURE 10. Output Amplification for the DAC650.

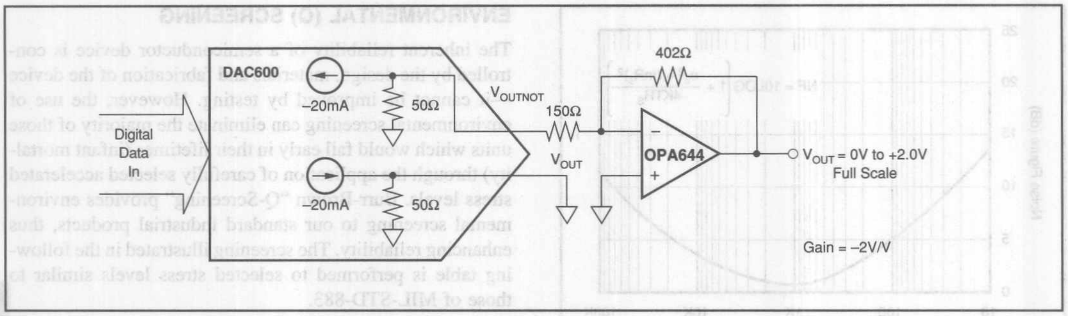


FIGURE 11. Output Amplification for the DAC600.

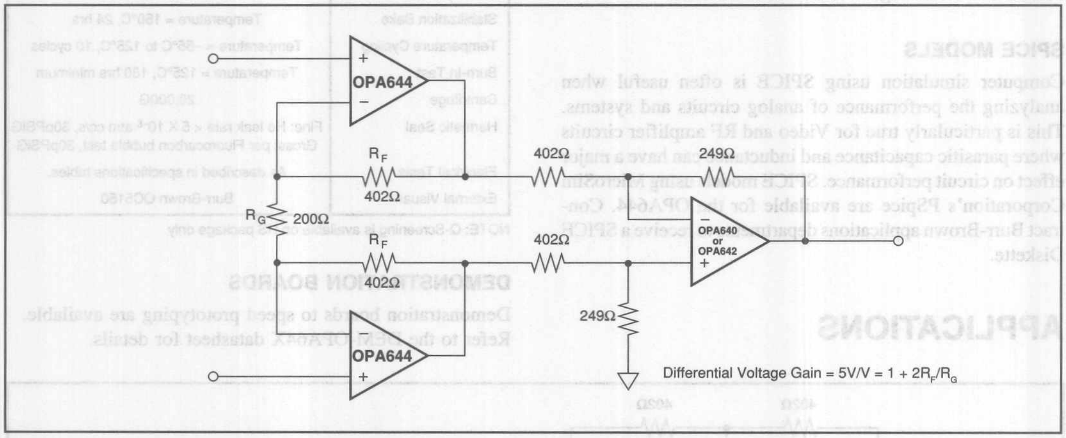


FIGURE 12. Wideband, Fast-Settling Instrumentation Amplifier.

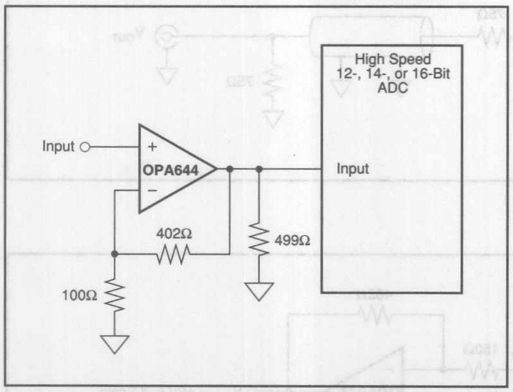
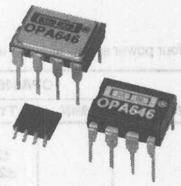


FIGURE 13. Low Distortion Gain Amplifier (G = +5V/V).

BURR - BROWN®



OPA646

DEMO BOARD AVAILABLE
See Appendix A

Low Power, Wide Bandwidth OPERATIONAL AMPLIFIER

FEATURES

- LOW POWER: 55mW
- UNITY-GAIN BANDWIDTH: 650MHz
- UNITY-GAIN STABLE
- FAST 12-BIT SETTLING: 15ns (0.01%)
- LOW INPUT BIAS CURRENT: 2µA
- LOW HARMONICS: –82dBc at 5MHz
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.025%/0.08°

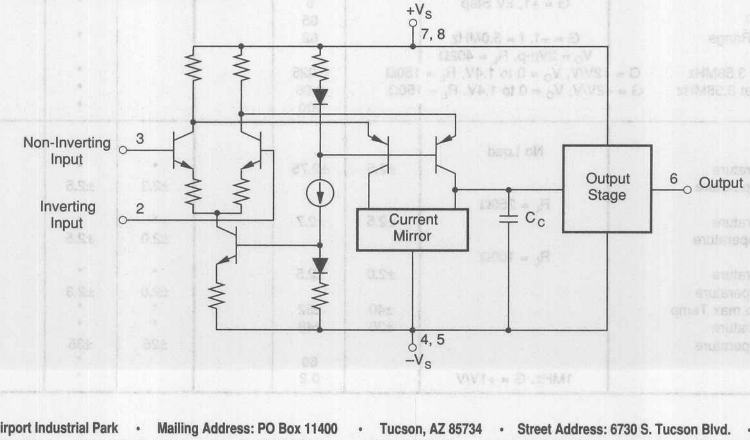
APPLICATIONS

- TELECOMMUNICATIONS
- MEDICAL IMAGING
- CCD IMAGING
- PORTABLE EQUIPMENT
- ACTIVE FILTERS
- VIDEO AMPLIFICATION
- ADC/DAC GAIN AMPLIFIER
- HIGH SPEED INTEGRATORS

DESCRIPTION

The OPA646 is a low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 650MHz as well as a 12-bit settling time of only 15ns. Its low input bias current and wide bandwidth allows it to be used for high speed integrator and active filter designs. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA646 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an ideal choice for many portable, multichannel and other high speed applications where power is at a premium.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

PARAMETER	CONDITIONS	OPA646H, P, U			OPA646HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			±3	±8		±1	±2.5	mV
Average Drift			±20			±12		µV/°C
HSQ Grade Over Temperature						±5	±8	mV
Power Supply Rejection (+V_S)	V_S = ±4.5 to ±5.5V	50	70		60	*		dB
(–V_S)		45	55		48	*		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		2	5		*	3.5	µA
Over Specified Temperature			3	7		*	*	µA
HSQ Grade Over Temperature						4	10	µA
Input Offset Current	V_{CM} = 0V		0.4	1.5		*	*	µA
Over Specified Temperature			0.9	3.0		*	*	µA
HSQ Grade Over Temperature						1.5	5.0	µA
NOISE								
Input Voltage Noise								
Noise Density: f = 100Hz			23.2			*		nV/√Hz
f = 10kHz			7.5			*		nV/√Hz
f = 1MHz			7.1			*		nV/√Hz
f = 1MHz to 100MHz			7.2			*		nV/√Hz
Voltage Noise, BW = 100Hz to 100MHz			141			*		µVrms
Input Bias Current Noise								
Current Noise Density, f = 0.1Hz to 20kHz			1.1			*		pA/√Hz
Noise Figure (NF)								
R_S = 10kΩ			3.0			*		dB
R_S = 50Ω			19.1			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.5	±3.0		*	*		V
Over Specified Temperature		±2.5	±3.0		*	*		V
Common-Mode Rejection	V_{CM} = ±0.5V	60	80		75	90		dB
INPUT IMPEDANCE								
Differential			15 || 1			*		kΩ || pF
Common-Mode			1.6 || 1			*		MΩ || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	45	51		47	55		dB
Over Specified Temperature		43	49		45	53		dB
FREQUENCY RESPONSE, R_{FB} = 402Ω	All Four Power Pins Used							
Closed-Loop Bandwidth	G = +1V/V		650			*		MHz
	G = +2V/V		160			*		MHz
	G = +5V/V		45			*		MHz
	G = +10V/V		22			*		MHz
Slew Rate(1)	G = +1, 2V Step		180			*		V/µs
At Minimum Specified Temperature			155			*		V/µs
Rise Time	1V Step		5.3			*		ns
Fall Time	1V Step		5.9			*		ns
Settling Time: 0.01%	G = +1, 2V Step		15			*		ns
0.1%	G = +1, 2V Step		11.5			*		ns
1%	G = +1, 2V Step		6			*		ns
Over-Voltage Recovery(2)			65					ns
Spurious Free Dynamic Range	G = +1, f = 5.0MHz V_O = 2Vp-p, R_L = 402Ω		82			*		dBc
Differential Gain Error at 3.58MHz	G = +2V/V, V_O = 0 to 1.4V, R_L = 150Ω		0.025			*		%
Differential Phase Error at 3.58MHz	G = +2V/V, V_O = 0 to 1.4V, R_L = 150Ω		0.08			*		degrees
Gain Flatness to 0.1dB			100			*		MHz
OUTPUT								
Voltage Output	No Load							
Over Specified Temperature		±2.5	±2.75		*	*		V
HSQ Grade Over Temperature					±2.3	±2.5		V
Voltage Output	R_L = 250Ω							V
Over Specified Temperature		±2.5	±2.7		*	*		V
HSQ Grade Over Temperature					±2.0	±2.5		V
Voltage Output	R_L = 100Ω							
Over Specified Temperature		±2.0	±2.5		*	*		V
HSQ Grade Over Temperature					±2.0	±2.3		V
Current Output, +25°C to max Temp		±40	±52		*	*		mA
Over Specified Temperature		±30	±48		*	*		mA
HSQ Grade Over Temperature					±25	±35		mA
Short Circuit Current			60			*		mA
Output Resistance	1MHz, G = +1V/V		0.2			*		Ω

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = +25°C$, $V_S = ±5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

PARAMETER	CONDITIONS	OPA646H, P, U			OPA646HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}		±5			*		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	*		*	V
Quiescent Current			±5.25	±6.5		*	*	mA
Over Specified Temperature			±6.5	±7.5		*	*	mA
HSQ Grade Over Temperature						±7.5	±8.5	mA
TEMPERATURE RANGE								
Specification: H, P, PB, U, UB	Ambient	–40		+85	*		*	°C
HSQ	Ambient				–55		+125	°C
Thermal Resistance	θ_{JA}, Junction to Ambient							
P			120			*		°C/W
U			170			*		°C/W
H			120			*		°C/W

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step. (2) Recovery time to linear operation after a 50% overload recovery.

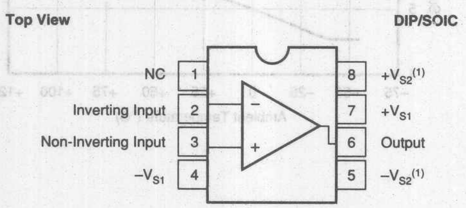
ORDERING INFORMATION

OPA646 ( ) ( )

- Basic Model Number
- Package Code
  - H = 8-pin Sidebraze DIP
  - P = 8-pin Plastic DIP
  - U = 8-pin Plastic SOIC
- Performance Grade Code
  - SQ = –55°C to +125°C, Reliability Screened
  - B(1) or No Letter = –40°C to +85°C

NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by Pin 8. Refer to the mechanical section for the location.

PIN CONFIGURATION



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

ABSOLUTE MAXIMUM RATINGS

Supply	±5.5VDC
Internal Power Dissipation(1)	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	–65°C to +150°C
P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA646H, HSQ	8-Pin Cerdip	157
OPA646P, PB	8-Pin DIP	006
OPA646U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

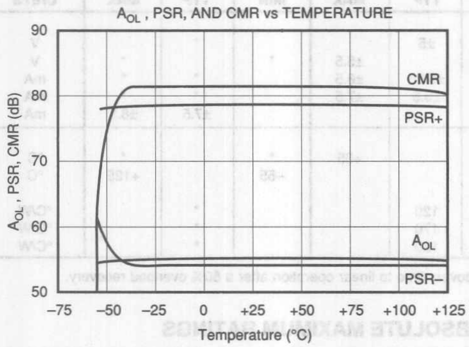
ELECTROSTATIC DISCHARGE SENSITIVITY

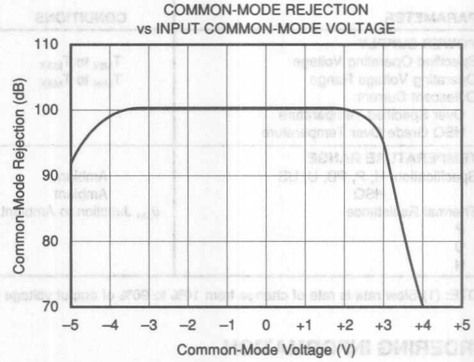
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

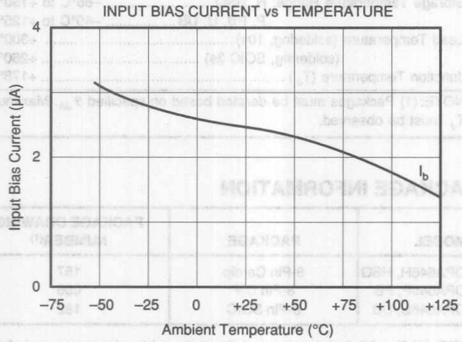
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

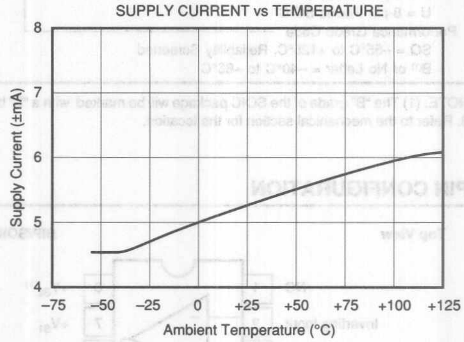
OPA646
2
OPERATIONAL AMPLIFIERS

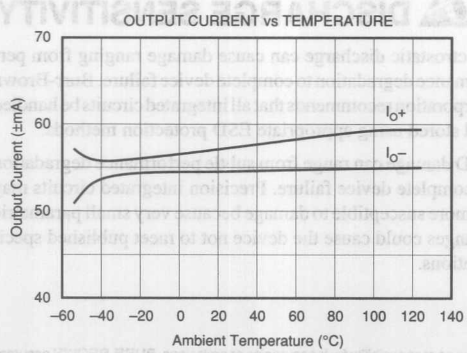
At $T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

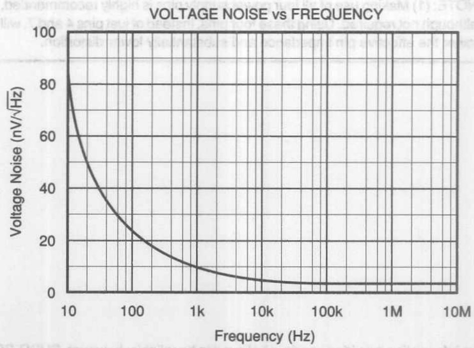






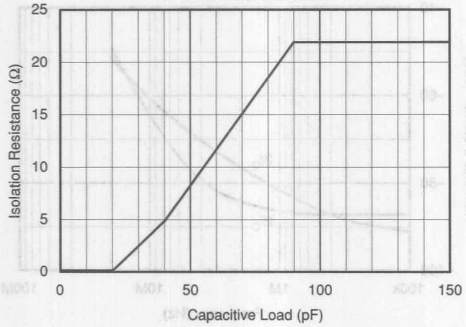




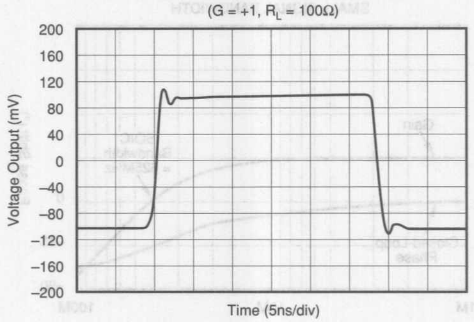


At $T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

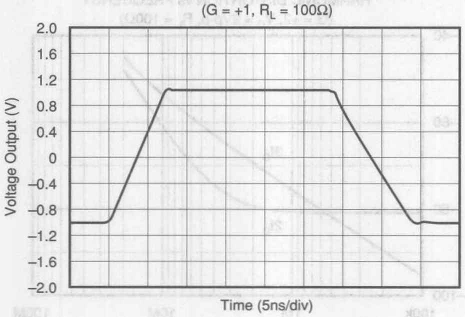
RECOMMENDED ISOLATION RESISTANCE
vs CAPACITIVE LOAD



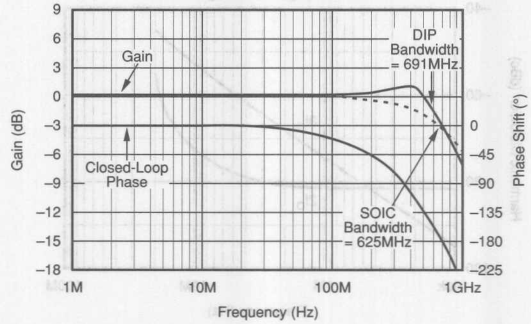
SMALL SIGNAL TRANSIENT RESPONSE
($G = +1$, $R_L = 100\Omega$)



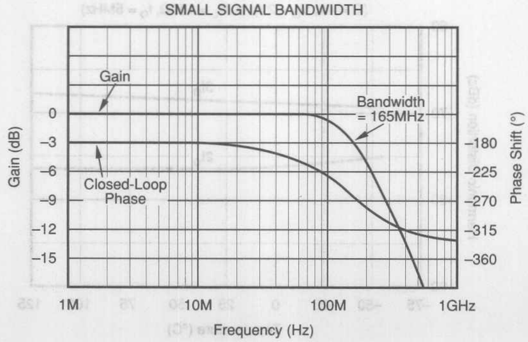
LARGE SIGNAL TRANSIENT RESPONSE
($G = +1$, $R_L = 100\Omega$)



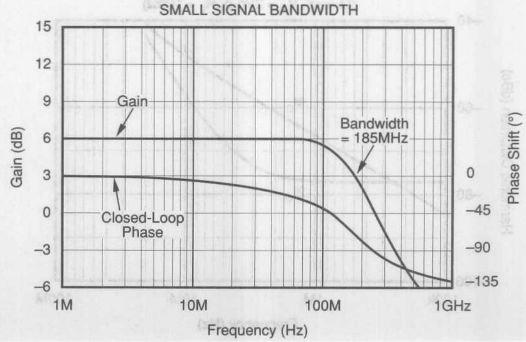
G = +1 CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



G = –1V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

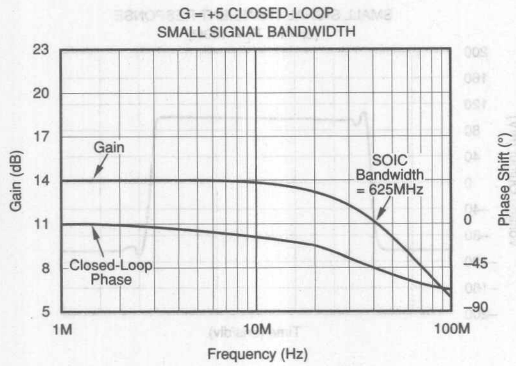


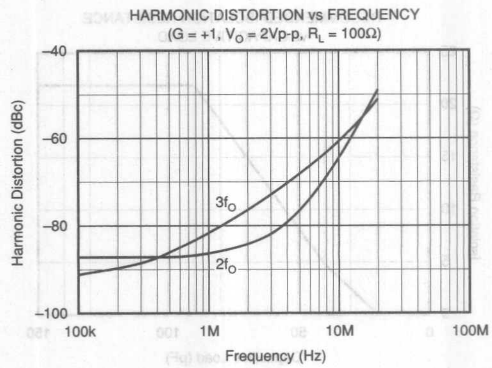
G = +2 CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

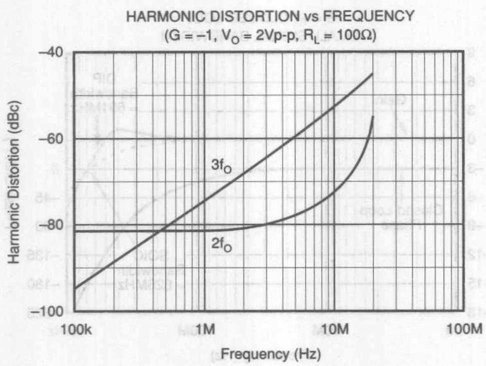


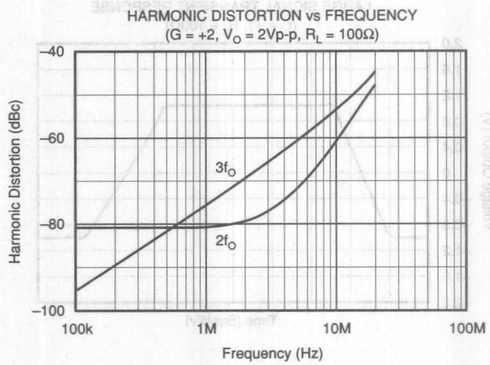
TYPICAL PERFORMANCE CURVES (CONT)

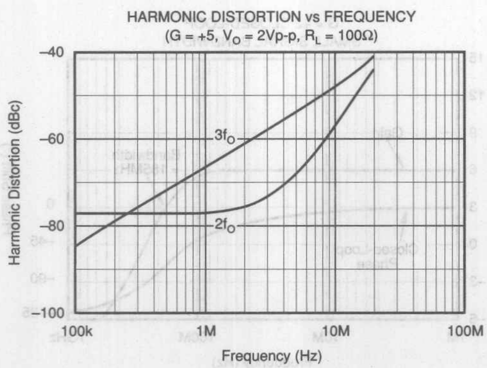
At $T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

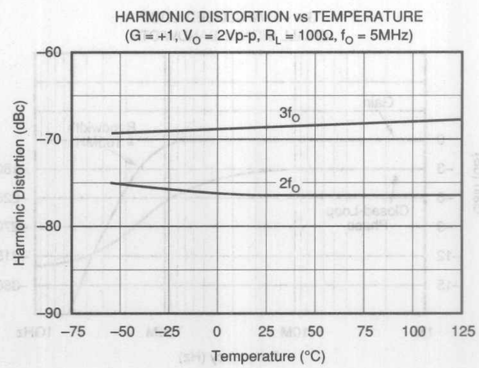






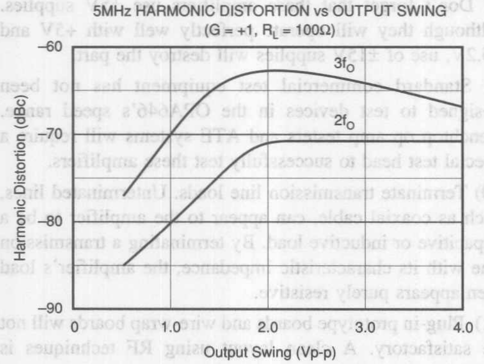


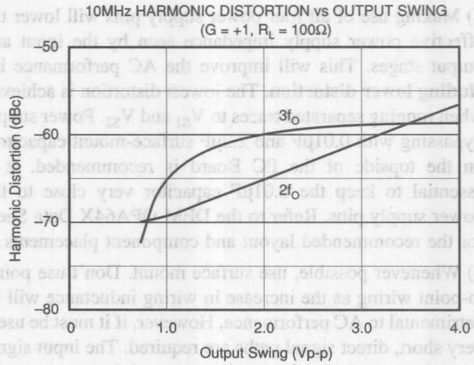




TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = ±5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.





APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA646 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA646's design uses a "classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e., one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Cancelling offset errors (due to input bias currents) through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA646's "classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA646.

WIRING PRECAUTIONS

Maximizing the OPA646's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA646, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2 oz. copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2µF) with very short leads are recommended. A parallel 0.01µF ceramic must also be added. Surface-mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to

tion-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages. This will improve the AC performance **including lower distortion.** The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface-mount capacitors on the topside of the PC Board is recommended. It is essential to keep the 0.01µF capacitor very close to the power supply pins. Refer to the DEM-OPA64X Data Sheet for the recommended layout and component placements.

2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on backside of PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA646 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. Refer to the demonstration board layout at the end of the datasheet. **A longer feedback path than this will decrease the realized bandwidth substantially.**

6) Surface-mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface-mount components with the OPA646U (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

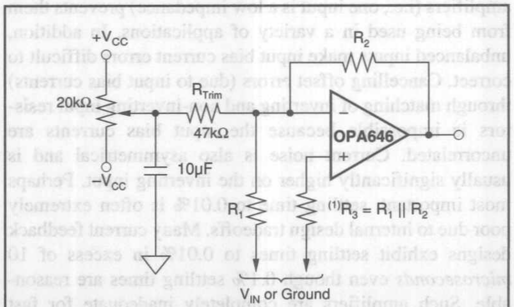
9) Standard commercial test equipment has not been designed to test devices in the OPA646's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current.



$$\text{Output Trim Range} \equiv +V_{CC}\frac{R_2}{R_{Trim}} \text{ to } -V_{CC}\frac{R_2}{R_{Trim}}$$

NOTE: (1) R_3 is optional and can be used to cancel offset errors due to input bias currents.

FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection

This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA646 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

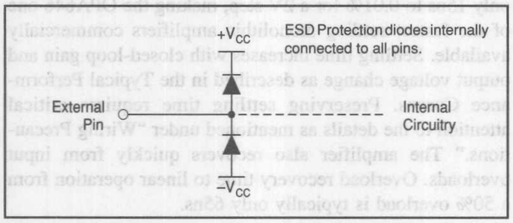


FIGURE 2. Internal ESD Protection.

The OPA646 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA646.

OUTPUT DRIVE CAPABILITY

The OPA646 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA646 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA646 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

THERMAL CONSIDERATIONS

The OPA646 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 7.5mA = 75mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max $= (\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

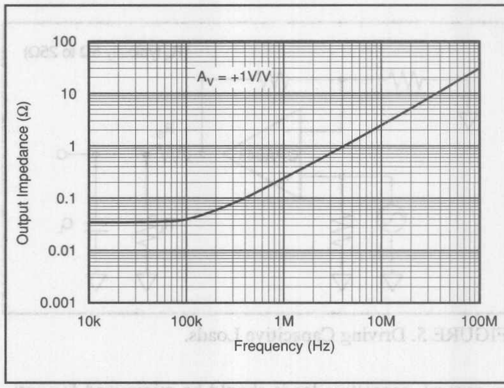


FIGURE 3. Small-Signal Output Impedance vs Frequency.

A short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in Figure 4.

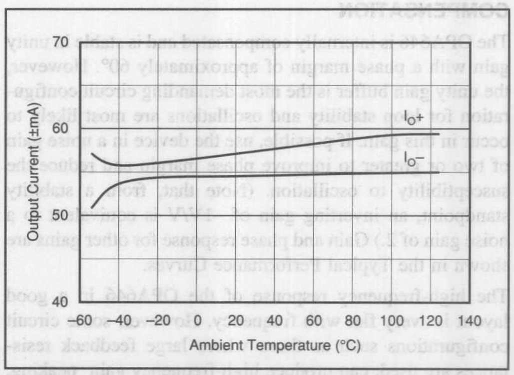


FIGURE 4. Output Current vs Temperature.

CAPACITIVE LOADS

The OPA646's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

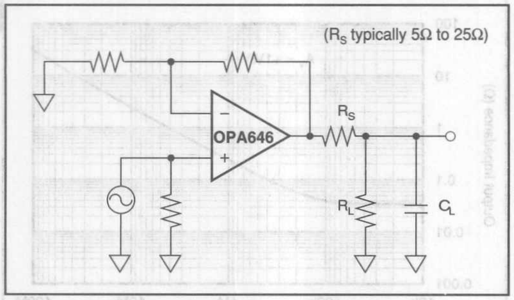


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA646 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA646 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 15ns to 0.01% for a 2V step, making the OPA646 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 65ns.

In practice, settling time measurements on the OPA646 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA646's harmonic distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be significantly improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

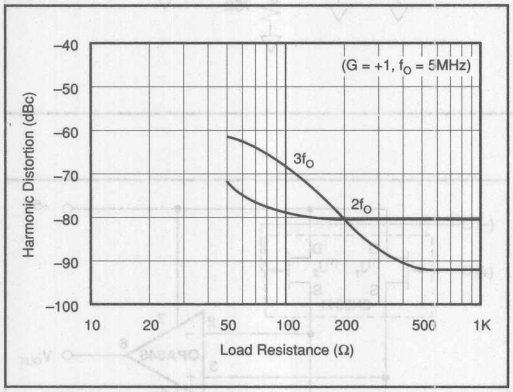


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance with R_F = 402Ω.

NOISE FIGURE

The OPA646 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA646's Noise Figure vs Source Resistance is shown in Figure 7.

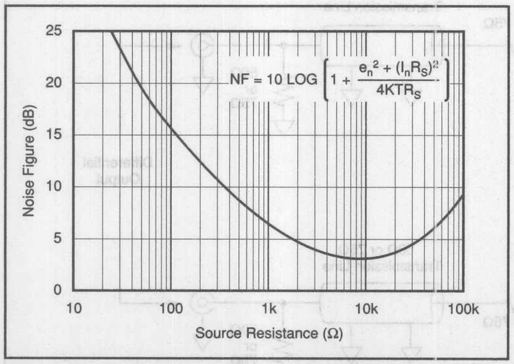


FIGURE 7. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA646. Contact Burr-Brown Applications Department to receive a spice diskette.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device —it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" on the HSQ grade provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = –65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20000G
Hermetic Seal	Fine: He leak rate < 5 x 10^{-8} atm cc/s, 30PSiG Gross: per Fluorocarbon bubble test, 60PSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on the HS package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64X Data Sheet for details.

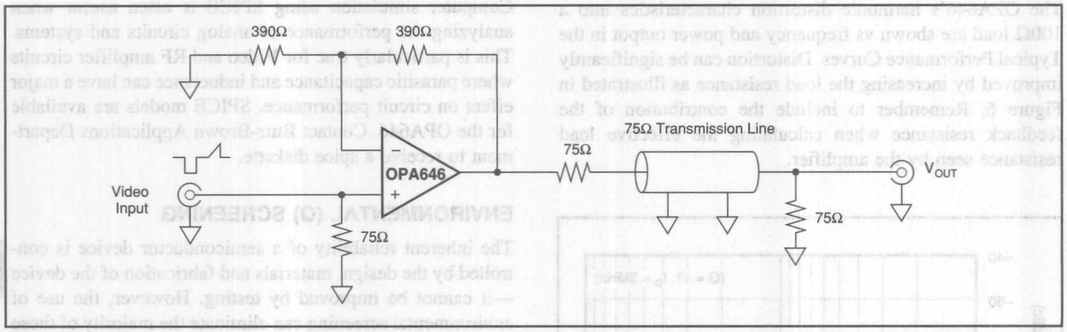


FIGURE 8. Low Power Video Amplifier.

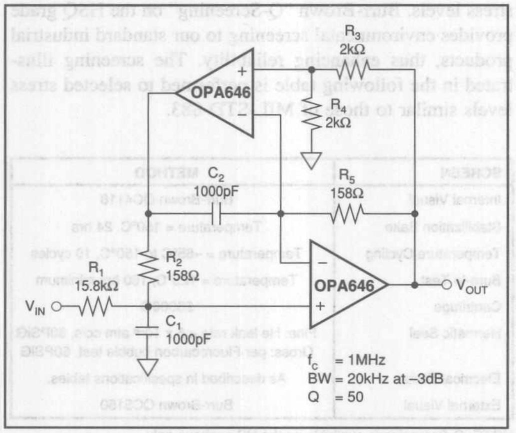


FIGURE 9. High-Q 1MHz Bandpass Filter.

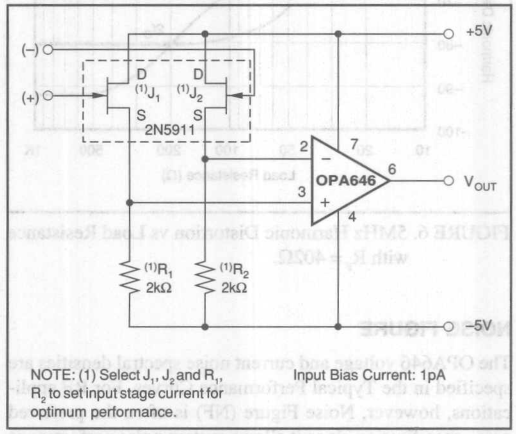


FIGURE 10. Low Power, Wideband FET Input Op Amp.

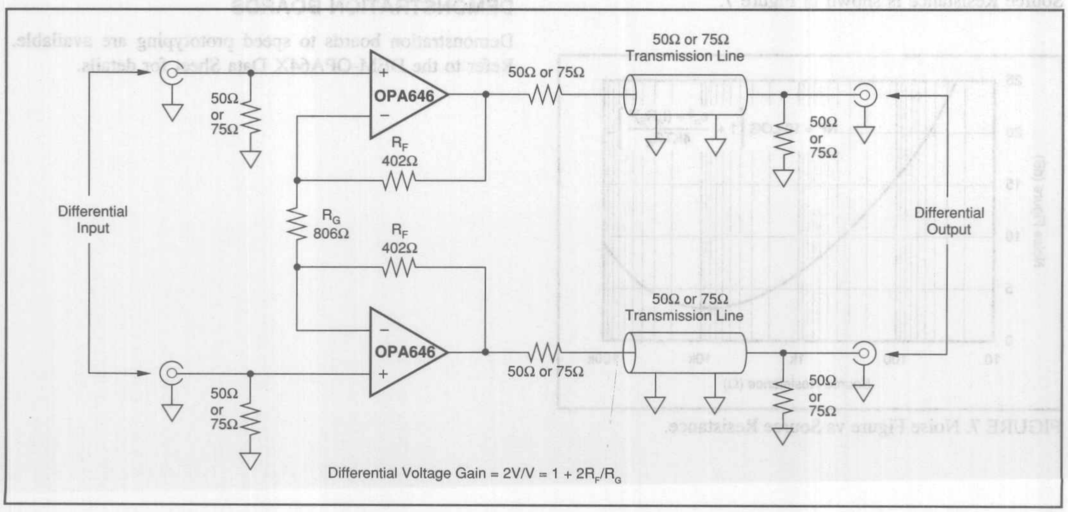


FIGURE 11. Differential Line Driver for 50Ω or 75Ω Systems.

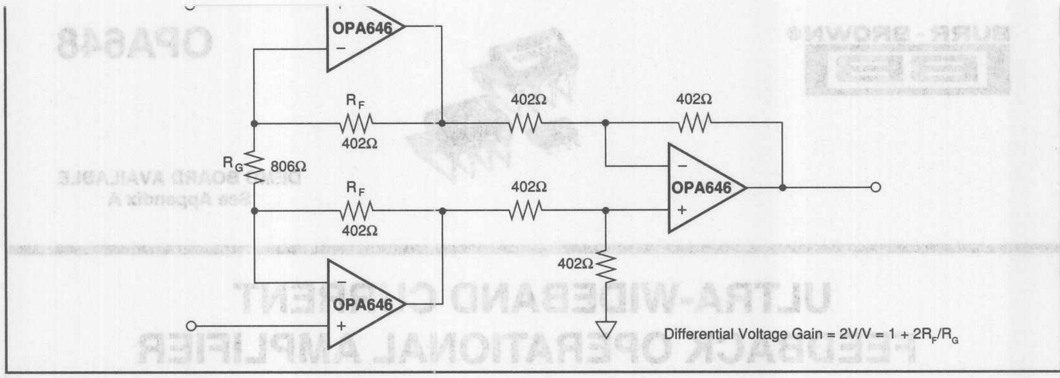


FIGURE 12. Wideband, Fast-Settling Instrumentation Amplifier.

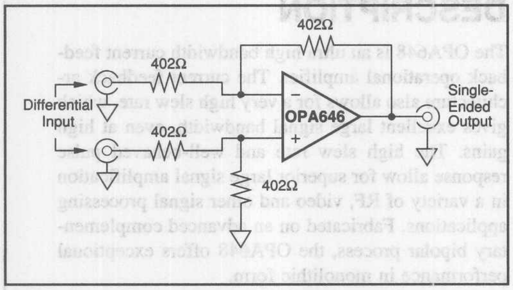


FIGURE 13. Unity Gain Difference Amplifier.

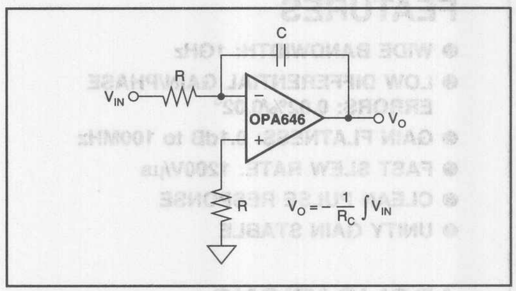


FIGURE 15. A High Speed Integrator.

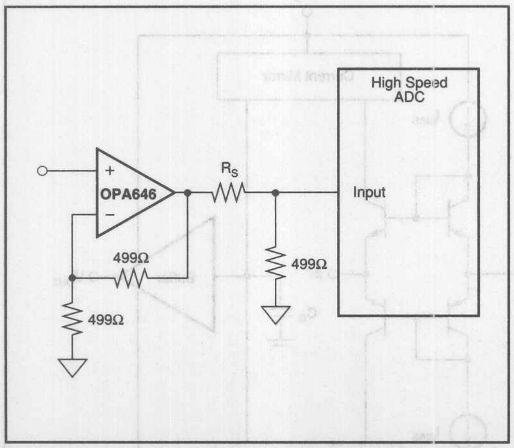


FIGURE 14. Differential Input Buffer Amplifier (G = +2V/V).

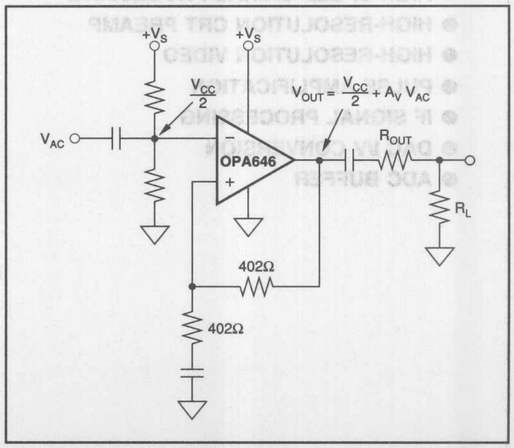
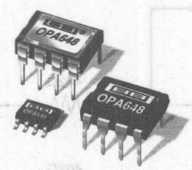


FIGURE 16. Single Supply Operation.

BURR - BROWN®



OPA648

DEMO BOARD AVAILABLE
See Appendix A

ULTRA-WIDEBAND CURRENT FEEDBACK OPERATIONAL AMPLIFIER

FEATURES

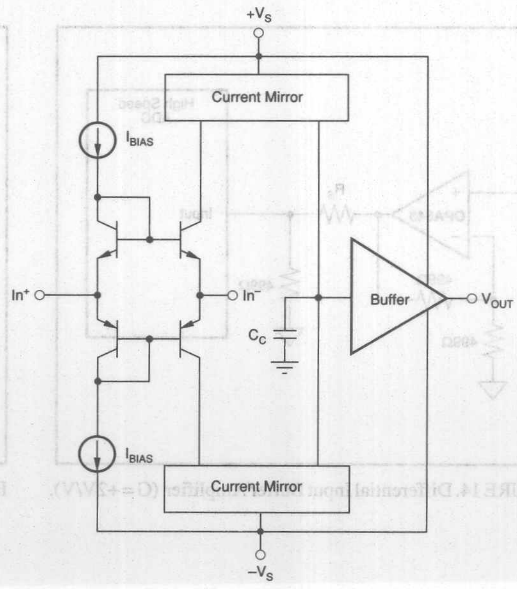
- WIDE BANDWIDTH: 1GHz
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.02%/0.02°
- GAIN FLATNESS: 0.1dB to 100MHz
- FAST SLEW RATE: 1200V/µs
- CLEAN PULSE RESPONSE
- UNITY GAIN STABLE

APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- HIGH-RESOLUTION CRT PREAMP
- HIGH-RESOLUTION VIDEO
- PULSE AMPLIFICATION
- IF SIGNAL PROCESSING
- DAC I/V CONVERSION
- ADC BUFFER

DESCRIPTION

The OPA648 is an ultra high bandwidth current feedback operational amplifier. The current feedback architecture also allows for a very high slew rate, which gives excellent large signal bandwidth, even at high gains. The high slew rate and well-behaved pulse response allow for superior large signal amplification in a variety of RF, video and other signal processing applications. Fabricated on an advanced complementary bipolar process, the OPA648 offers exceptional performance in monolithic form.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1253A

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

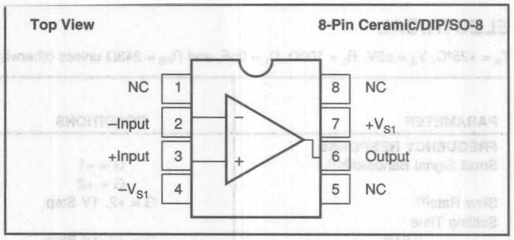
$T_A = +25°C$, $V_S = ±5V$, $R_L = 100Ω$, $C_L = 2pF$, and $R_{FB} = 243Ω$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA648H, P, U MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE					
Small Signal Bandwidth(1)	G = +1		1.0		GHz
	G = +2		600		MHz
Slew Rate(2)	G = +2, 1V Step		1200		V/μs
Settling Time					
0.01%	G = +2, 1V Step		20		ns
0.1%	G = +2, 1V Step		9		ns
1%	G = +2, 1V Step		3		ns
Spurious Free Dynamic Range	G = +2, f = 5.0MHz, V_O = 2Vp-p		60		dBc
	G = +2, f = 20.0MHz, V_O = 2Vp-p		51		dBc
Differential Gain, G = +2	3.58MHz, V_O = 1.4Vp-p, R_L = 150Ω		0.02		%
Differential Phase, G = +2	3.58MHz, V_O = 1.4Vp-p, R_L = 150Ω		0.02		degrees
Gain Flatness	DC to 100MHz		0.1		dB
OFFSET VOLTAGE					
Input Offset Voltage			±2	±6	mV
Average Drift			±10		μV/°C
Power Supply Rejection Ratio	V_S = ±4.5 to ±5.5V	45	58		dB
INPUT BIAS CURRENT					
Non-Inverting			±12	±65	μA
Over Specified Temperature			±30	±95	μA
Inverting			±20	±65	μA
Over Specified Temperature			±50	±95	μA
NOISE					
Input Voltage Noise					
Noise Density, f = 100Hz			10.4		nV/√Hz
f = 1kHz			2.3		nV/√Hz
f = 10kHz			2.3		nV/√Hz
f = 1MHz			2.3		nV/√Hz
Voltage Noise, BW = 10Hz to 200MHz			32.5		μVrms
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			15		pA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±2	±2.25		V
Common-Mode Rejection	V_{CM} = ±0.5V	35	55		dB
INPUT IMPEDANCE					
Non-inverting			22 || 0.75		kΩ || pF
Inverting			20		Ω
OPEN-LOOP TRANSIMPEDANCE					
Open-Loop Transimpedance	V_O = ±2V, R_L = 1kΩ	100	165		kΩ
OUTPUT					
Current Output		33	45		mA
Over Specified Temperature		25	40		mA
Voltage Output	No Load				
Over Specified Temperature		±2.75	±3.0		V
Voltage Output	R_L = 150Ω	±2.2	±2.5		V
Over Specified Temperature		±2.0	±2.3		V
Short-Circuit Current			75		mA
Output Resistance	1MHz, G = +2V/V		0.08		Ω
POWER SUPPLY					
Specified Operating Voltage	T_{MIN} to T_{MAX}		±5		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	V
Quiescent Current			±13	±20	mA
Over Specified Temperature			±15	±23	mA
TEMPERATURE RANGE					
Specification	Ambient	–40		+85	°C
Storage	Ambient	–55		+150	°C
Thermal Resistance, θ_{JA}					
P			120		°C/W
U			170		°C/W
H			120		°C/W

NOTES: (1) Bandwidth can be degraded by a non-optimal PC board layout. Refer to the DEM-OPA64X datasheet for layout recommendations. (2) Slew rate is the *rate of change from 10% to 90% of the output voltage step.*

Supply	±5.5VDC
Internal Power Dissipation[1]	See Thermal Considerations
Differential Input Voltage	Total V_S
Input Voltage Range	±5V
Storage Temperature Range: H	–65°C to +150°C
P	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SO-8 3s)	+260°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA648H	8-Pin Ceramic Sidebraze DIP	157
OPA648P	8-Pin Plastic Single-Wide DIP	006
OPA648U	8-Pin Surface Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA648H	8-Pin Ceramic Sidebraze DIP	–40°C to +85°C
OPA648P	8-Pin Plastic Single-Wide DIP	–40°C to +85°C
OPA648U	8-Pin Surface Mount	–40°C to +85°C

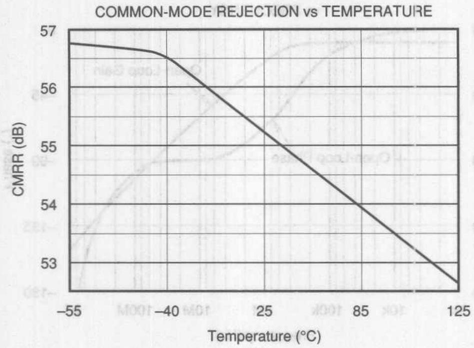
ELECTROSTATIC DISCHARGE SENSITIVITY

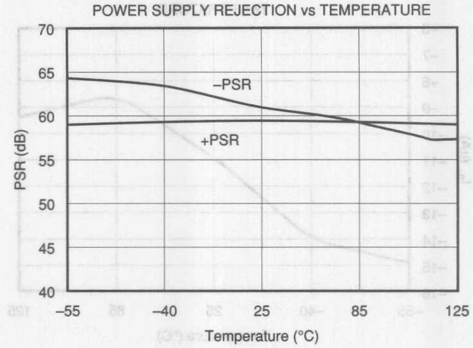
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

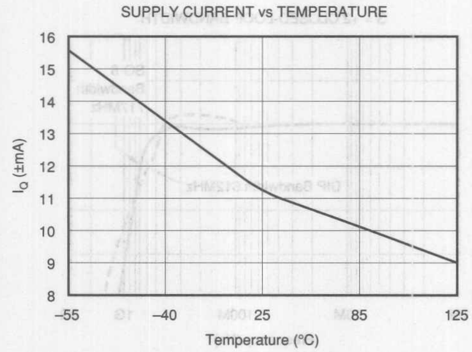
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

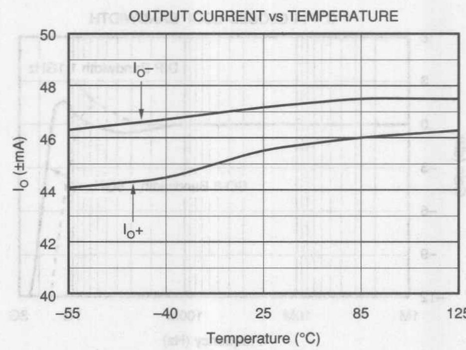
TYPICAL PERFORMANCE CURVES

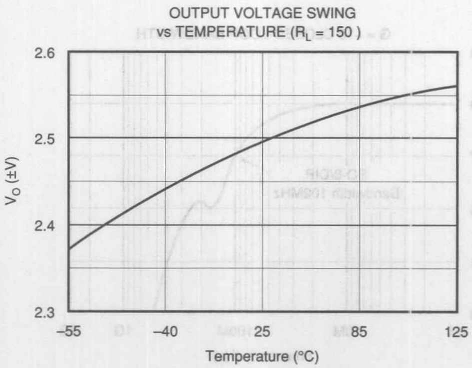
$T_A = +25°C$, $V_S = \pm 5V$, $R_L = 100\Omega$, $C_L = 2pF$, and $R_{FB} = 243\Omega$ unless otherwise noted.

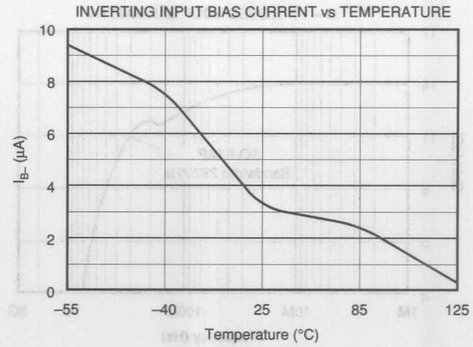












OPA648

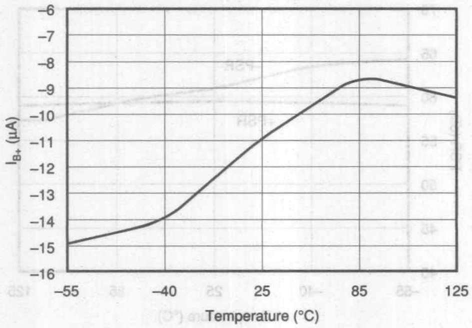
2

OPERATIONAL AMPLIFIERS

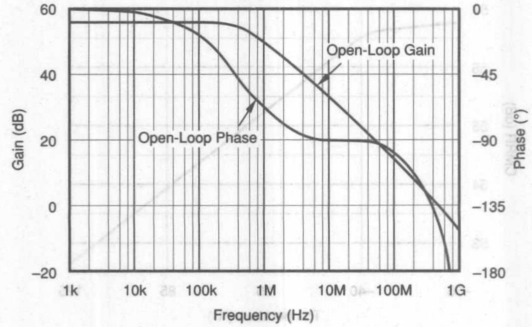
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, and $R_{FB} = 243\Omega$ unless otherwise noted.

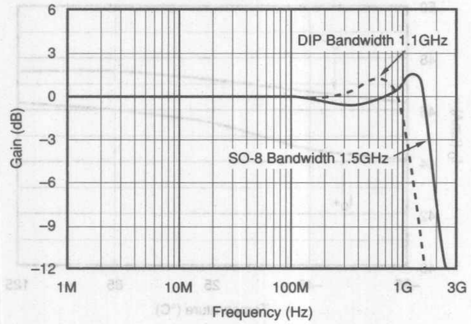
NON-INVERTING INPUT BIAS CURRENT vs TEMPERATURE



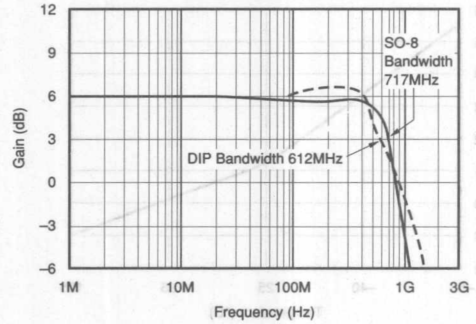
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



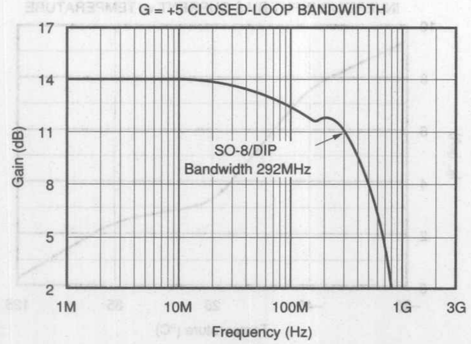
G = +1 CLOSED-LOOP BANDWIDTH



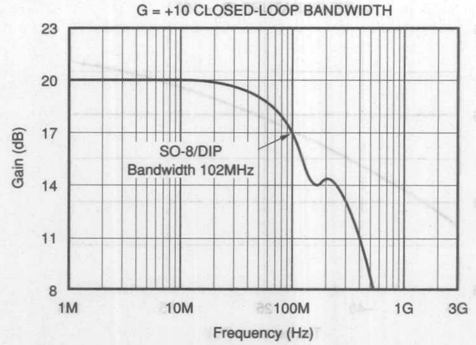
G = +2 CLOSED-LOOP BANDWIDTH



G = +5 CLOSED-LOOP BANDWIDTH



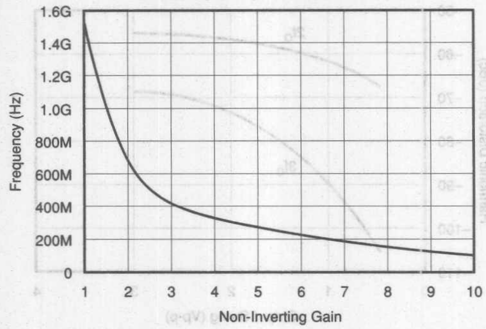
G = +10 CLOSED-LOOP BANDWIDTH



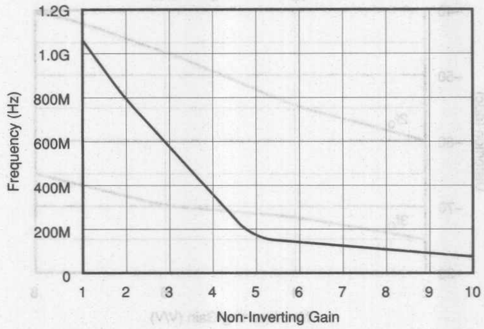
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = ±5V$, $R_L = 100\Omega$, $C_L = 2pF$, and $R_{FB} = 243\Omega$ unless otherwise noted.

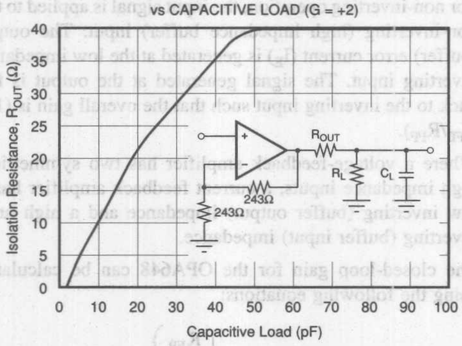
SO-8 CLOSED-LOOP BANDWIDTH vs GAIN



DIP CLOSED-LOOP BANDWIDTH vs GAIN

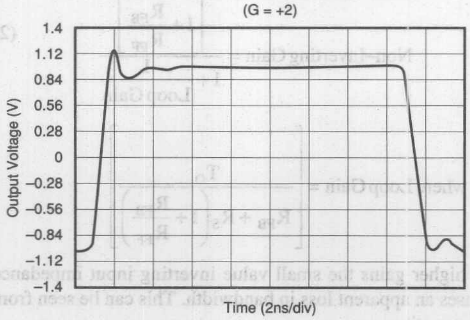


RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD (G = +2)

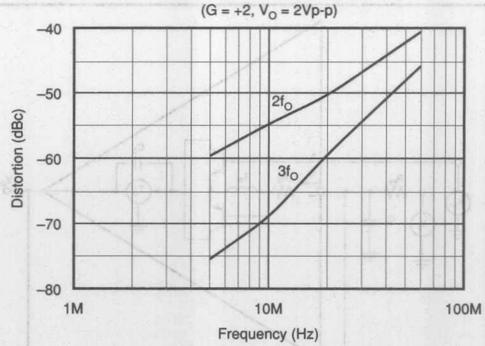


SMALL SIGNAL TRANSIENT RESPONSE (G = +2)

LARGE SIGNAL TRANSIENT RESPONSE (G = +2)



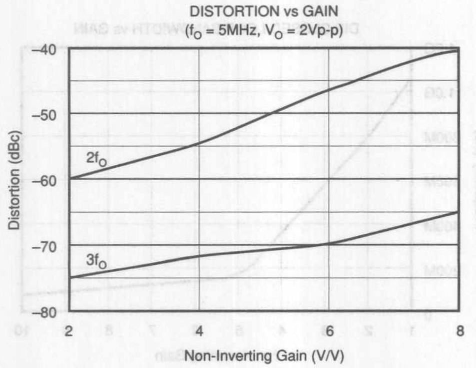
DISTORTION vs FREQUENCY (G = +2, V_O = 2Vp-p)

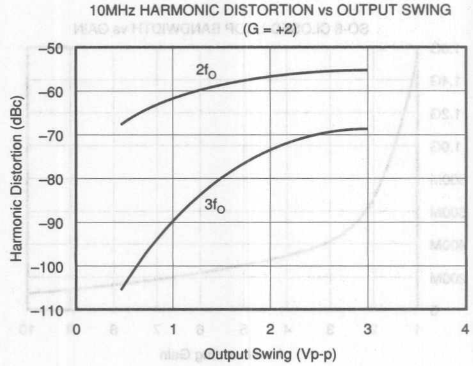


OPA648

2

OPERATIONAL AMPLIFIERS





APPLICATIONS INFORMATION

THEORY OF OPERATION

This current feedback architecture offers the following important advantages over voltage feedback architectures: (1) the high slew rate allows the large signal performance to approach the small signal performance, and: (2) there is less bandwidth degradation at higher gain settings.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open-loop transimpedance gain (T_O). The output signal generated is equal to T_O X I_E. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

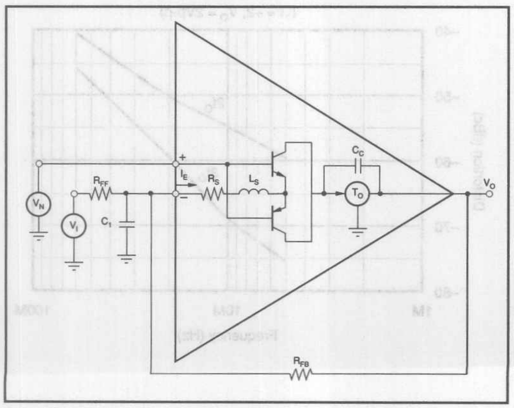


FIGURE 1. Equivalent Circuit.

For non-inverting operation, the input signal is applied to the non-inverting (high impedance buffer) input. The output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the overall gain is $(1 + R_{FB}/R_{FF})$.

Where a voltage-feedback amplifier has two symmetrical high impedance inputs, a current feedback amplifier has a low inverting (buffer output) impedance and a high non-inverting (buffer input) impedance.

The closed-loop gain for the OPA648 can be calculated using the following equations:

$$\text{Inverting Gain} = \frac{-\left(\dfrac{R_{FB}}{R_{FF}}\right)}{1+\dfrac{1}{\text{Loop Gain}}} \tag{1}$$

$$\text{Non–Inverting Gain} = \frac{\left[1+\dfrac{R_{FB}}{R_{FF}}\right]}{1+\dfrac{1}{\text{Loop Gain}}} \tag{2}$$

$$\text{where Loop Gain} = \left[\frac{T_O}{R_{FB} + R_S\left(1+\dfrac{R_{FB}}{R_{FF}}\right)}\right]$$

At higher gains the small value inverting input impedance causes an apparent loss in bandwidth. This can be seen from the equation:

$$f_{\text{ACTUAL}}\ \text{BW} = \frac{f_{\text{IDEAL}}\ \text{BW}}{\left[1+\left(\dfrac{R_S}{R_{FB}}\right)\times\left(1+\dfrac{R_{FB}}{R_{FF}}\right)\right]} \tag{3}$$

feedback resistor from the specified value of 243Ω.

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the input voltage and current sources that influence DC operation. The output offset is calculated by the following equation:

$$\text{Output Offset Voltage} = \pm Ib_N \times R_N (1 + R_{FB}/R_G) \pm V_{IO} (1 + R_{FB}/R_G) \pm Ib_I \times R_{FB} \quad (4)$$

If all terms are divided by the gain $(1 + R_F/R_G)$, it can be observed that input referred offsets improve as gain increases.

The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of equation 4 and applying the spectral noise values found in the Typical Performance Curve–graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltages improve as the closed-loop gain increases (by keeping R_F fixed and reducing R_I with $R_N = 0\Omega$).

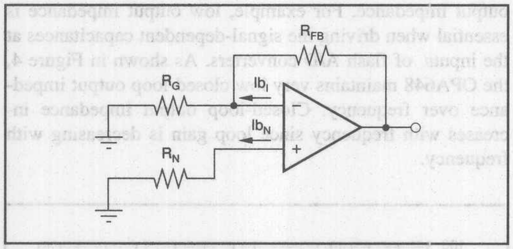


FIGURE 2. Output Offset Voltage Equivalent Circuit.

WIRING PRECAUTIONS

Maximizing the OPA648's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA648, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2µF) with very short leads are recommended. A parallel 0.1µF ceramic must also be added. Surface-mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply inductance seen by the input and output stages. This will improve the AC performance including lower distortion. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface mount capacitors is recommended. It is essential to keep the 0.1µF capacitor very close to the power supply pins. Refer to the demonstration board figure in the DEM-OPA64X datasheet for the recommended layout and component placements.

(2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on the backside of the PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA648 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 243Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are abso-

lutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. A longer feedback path than this will decrease the realized bandwidth substantially. Refer to the demonstration board layout at the end of the datasheet.

6) Surface-mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface-mount components with the OPA648U (SO-8 package) will offer the best AC performance. The parasitic package impedance for the SO-8 is lower than the both the 8-pin Ceramic and 8-pin Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA648's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA648 incorporates on-chip ESD protection diodes as shown in Figure 3. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

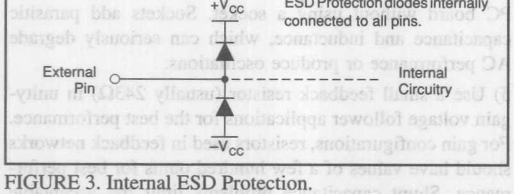


FIGURE 3. Internal ESD Protection.

All pins on the OPA648 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA648 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the machine model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA648.

OUTPUT DRIVE CAPABILITY

The OPA648 has been optimized to drive 75Ω and 100Ω resistive loads. This high-output drive capability makes the OPA648 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 4, the OPA648 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

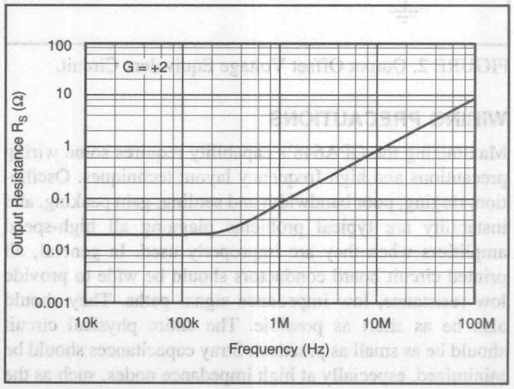


FIGURE 4. Output Resistance vs Frequency.

THERMAL CONSIDERATIONS

The OPA648 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_S = \pm 5V$, $P_{DQ} = 10V \times 23mA = 230mW$,

max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$), the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_S/2$, and is equal to P_{DL}, max = $(\pm V_S)^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA648's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 40Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters.

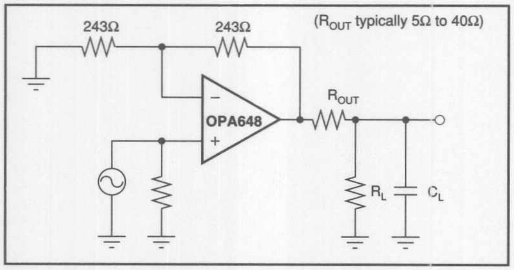


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA648 is internally compensated and is stable in unity gain with a phase margin of approximately 68°. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves. The high-frequency response of the OPA648 in a good layout is very flat with frequency.

DISTORTION

The OPA648's harmonic distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

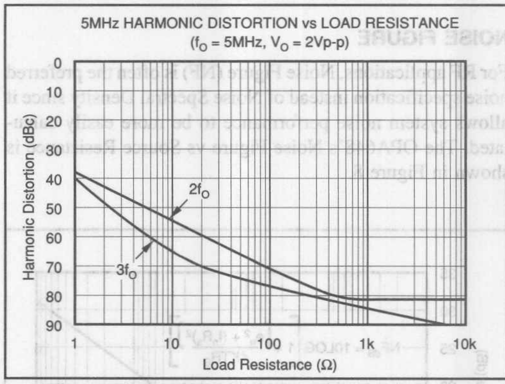


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

DG and DP of the OPA648 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 7 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to

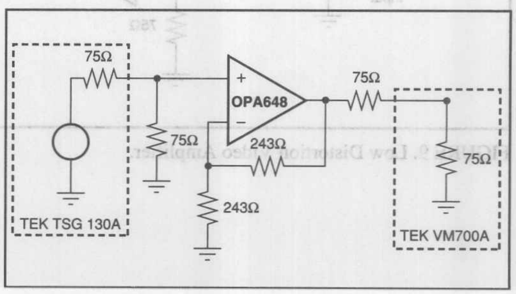


FIGURE 7. Configuration for Testing Differential Gain/Phase.

performance. Typical performance of the OPA648 is 0.02% differential gain and 0.02° differential phase to both NTSC and PAL standards.

NOISE FIGURE

For RF applications, Noise Figure (NF) is often the preferred noise specification instead of Noise Spectral Density since it allows system noise performance to be more easily calculated. The OPA648's Noise Figure vs Source Resistance is shown in Figure 8.

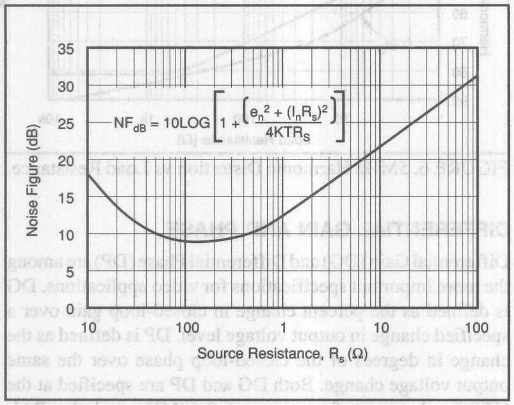


FIGURE 8. Noise Figure vs Source Resistance.

APPLICATIONS

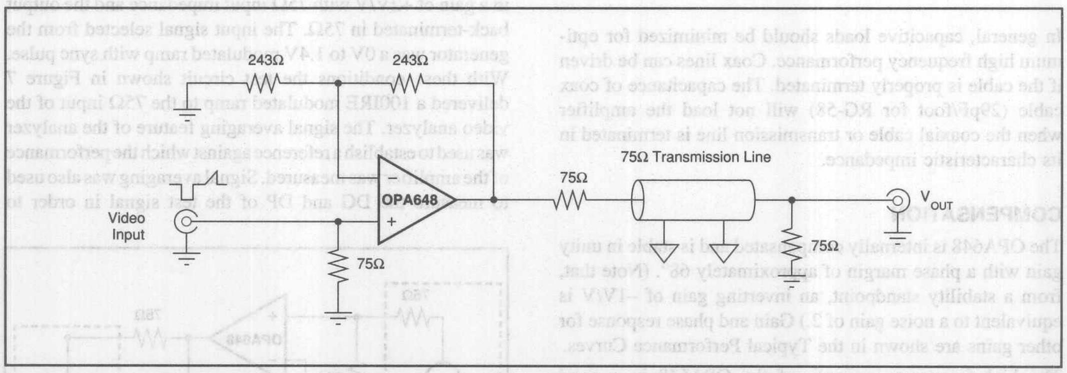


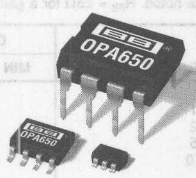
FIGURE 9. Low Distortion Video Amplifier.

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE Macromodels using PSpice are available for the OPA648. Contract Burr-Brown applications departments to receive a SPICE Diskette.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64X (LI-445) data sheet for details.

BURR-BROWN®



OPA650

Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- LOW POWER: 50mW
- UNITY GAIN STABLE BANDWIDTH: 560MHz
- LOW HARMONICS: –77dBc at 5MHz
- FAST SETTLING TIME: 20ns to 0.01%
- LOW INPUT BIAS CURRENT: 5µA
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.03°
- HIGH OUTPUT CURRENT: 85mA

APPLICATIONS

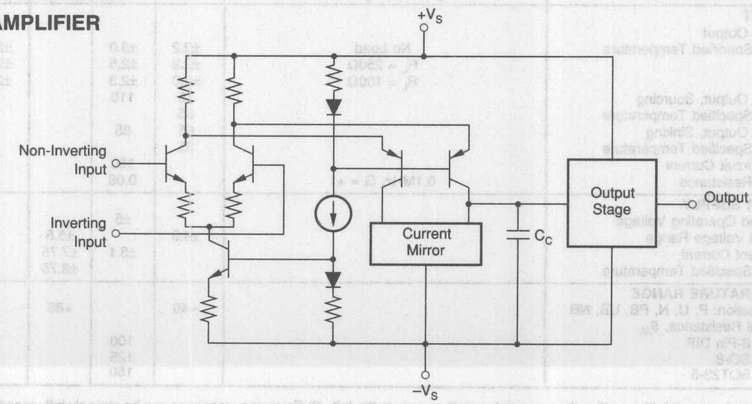
- HIGH RESOLUTION VIDEO
- BASEBAND AMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- ACTIVE FILTERS
- HIGH SPEED INTEGRATORS
- DIFFERENTIAL AMPLIFIER

DESCRIPTION

The OPA650 is a low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 560MHz as well as a 12-bit settling time of only 20ns. The low distortion allows its use in communications applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA650 is also available in dual (OPA2650) and quad (OPA4650) configurations.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

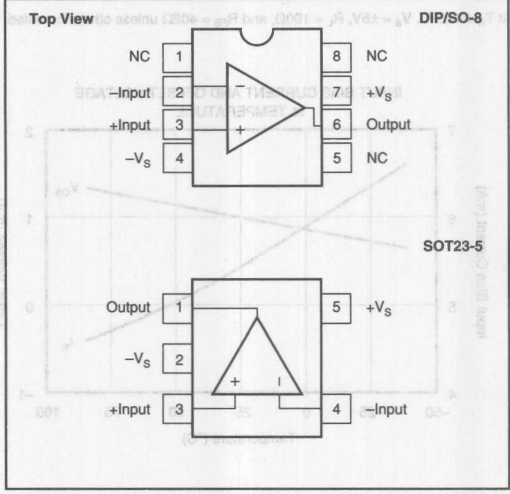
		OPA650P, U, N			OPA650PB, UB, NB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE								
Closed-Loop Bandwidth[2]	G = +1		560			*[1]		MHz
	G = +2		140			*		MHz
	G = +5		37			*		MHz
	G = +10		18			*		MHz
Gain Bandwidth Product			180			*		MHz
Slew Rate	G = +1, 2V Step		240			*		V/µs
Over Specified Temperature			220			*		V/µs
Rise Time	0.2V Step		1			*		ns
Fall Time	0.2V Step		1			*		ns
Settling Time 0.01%	G = +1, 2V Step		19.6			*		ns
0.1%	G = +1, 2V Step		10.2			*		ns
1%	G = +1, 2V Step		6.3			*		ns
Spurious Free Dynamic Range	G = +1, f = 5.0 MHz, V_O = 2Vp-p							
	R_L = 100Ω		73			*		dBc
	R_L = 200Ω		77			*		dBc
Differential Gain	G = +1, NTSC, V_O = 1.4Vp, R_L = 150Ω		0.01			*		%
Differential Phase	G = +1, NTSC, V_O = 1.4Vp, R_L = 150Ω		0.03			*		Degrees
Bandwidth for 0.1dB Gain Flatness	G = +2		25			*		MHz
INPUT OFFSET VOLTAGE								
Input Offset Voltage			±1	±5		0.6	±2.5	mV
Average Drift			±3			*		µV/°C
Power Supply Rejection (+V_S)	$\lvert V_S \rvert$ = 4.5V to 5.5V	60	76		70	*		dB
(−V_S)		47	53		50	*		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		5	20		*	10	µA
Over Temperature				30			20	µA
Input Offset Current	V_{CM} = 0V		0.5	1		0.2	0.5	µA
Over Temperature				3			2	µA
NOISE								
Input Voltage Noise								
Noise Density, f = 100Hz			43			*		nV/√Hz
f = 10kHz			9.4			*		nV/√Hz
f = 1MHz			8.4			*		nV/√Hz
f = 1MHz to 100MHz			8.4			*		nV/√Hz
Integrated Noise, BW = 10Hz to 100MHz			84			*		µVrms
Input Bias Current Noise								
Current Noise Density, f = 0.1MHz to 100MHz			1.2			*		pA/√Hz
Noise Figure (NF)								
	R_S = 10kΩ		4			*		dB
	R_S = 50Ω		19.5			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range			±2.8			*		V
Over Specified Temperature		±2.2			*			V
Common-Mode Rejection	V_{CM} = ±0.5V	65	90		70	*		dB
INPUT IMPEDANCE								
Differential			15 ∥ 1			*		kΩ ∥ pF
Common-Mode			16 ∥ 1			*		MΩ ∥ pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	45	51		46	*		dB
Over Specified Temperature	V_O = ±2V, R_L = 100Ω	43			44			dB
OUTPUT								
Voltage Output								
Over Specified Temperature	No Load	±2.2	±3.0		±2.4	*		V
	R_L = 250Ω	±2.2	±2.5		±2.4	*		V
	R_L = 100Ω	±2.0	±2.3		±2.2	*		V
Current Output, Sourcing		75	110		*	*		mA
Over Specified Temperature		65			*			mA
Current Output, Sinking		65	85		*	*		mA
Over Specified Temperature		35			*			mA
Short Circuit Current			150			*		mA
Output Resistance	0.1MHz, G = +1		0.08			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Derated Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current			±5.1	±7.75		±5.1	±6.5	mA
Over Specified Temperature				±8.75			±7.5	mA
TEMPERATURE RANGE								
Specification: P, U, N, PB, UB, NB		−40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
P 8-Pin DIP			100			*		°C/W
U SO-8			125			*		°C/W
N SOT23-5			150			*		°C/W

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The OPA650 is nominally compensated assuming 2pF parasitic load. The demonstration board, DEM-OPA65xP, shows a low parasitic layout for this device.

ABSOLUTE MAXIMUM RATINGS

Supply	±5.5V
Internal Power Dissipation	See Thermal Conditions
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE	PACKAGE MARKING(2)	ORDERING NUMBER
OPA650U	SO-8 Surface Mount	182	–40°C to +85°C	OPA650U	OPA650U
OPA650UB	SO-8 Surface Mount	182	–40°C to +85°C	OPA650UB	OPA650UB
OPA650P	8-Pin Plastic DIP	006	–40°C to +85°C	OPA650P	OPA650P
OPA650PB	8-Pin Plastic DIP	006	–40°C to +85°C	OPA650PB	OPA650PB

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 and DIP packages will be marked with a "B" by pin 8.

ADVANCE PACKAGE INFORMATION(2)

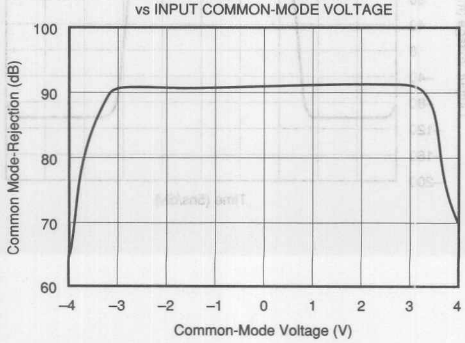
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER
OPA650N	5-Pin SOT23-5	331	–40°C to +85°C	—	—
OPA650NB	5-Pin SOT23-5	331	–40°C to +85°C	—	—

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The SOT23-5 will be available in tape and reel only by August, 1996.

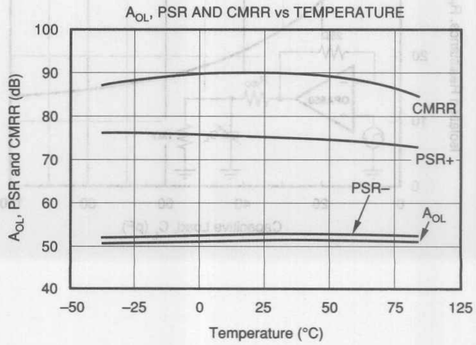
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for Gain of +1.

COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



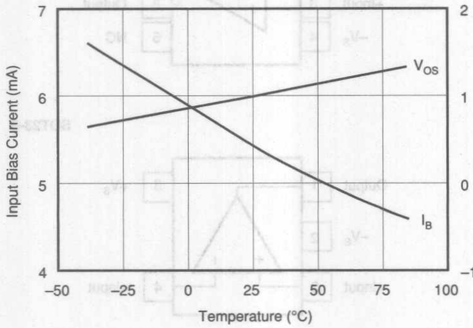
A_{OL}, PSR AND CMRR vs TEMPERATURE



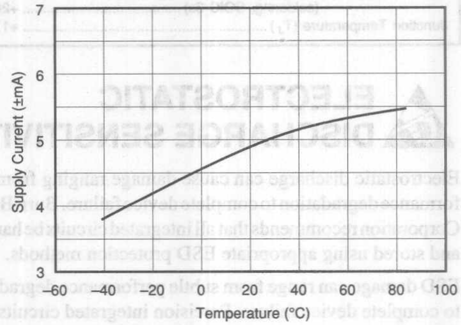
OPERATIONAL AMPLIFIERS 2 OPA650

At $T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted. $R_{FB} = 25\Omega$ for Gain of +1.

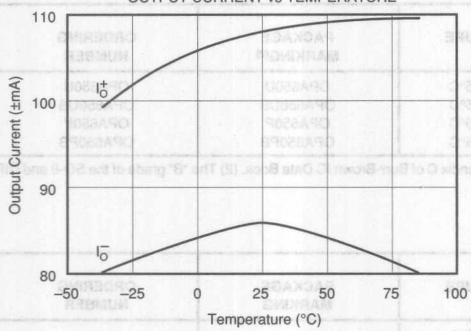
INPUT BIAS CURRENT AND OFFSET VOLTAGE
vs TEMPERATURE



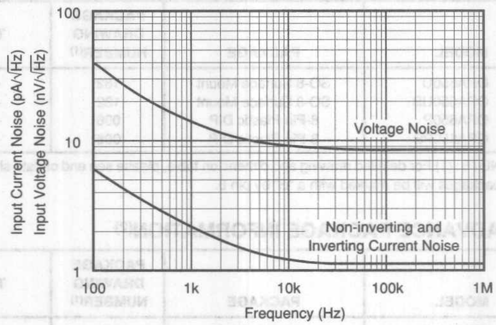
SUPPLY CURRENT vs TEMPERATURE



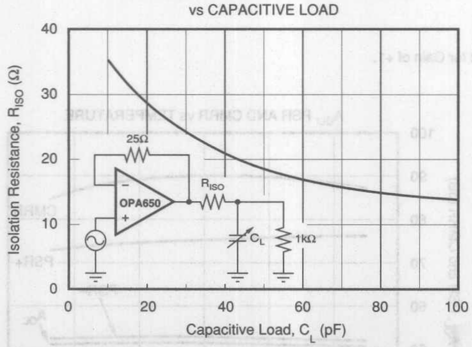
OUTPUT CURRENT vs TEMPERATURE



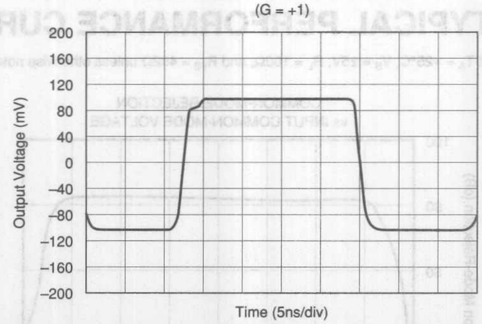
INPUT VOLTAGE AND CURRENT NOISE
vs FREQUENCY



RECOMMENDED ISOLATION RESISTANCE
vs CAPACITIVE LOAD

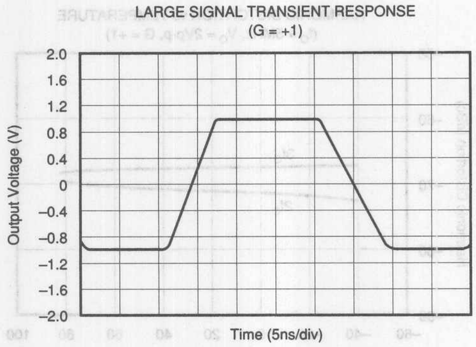


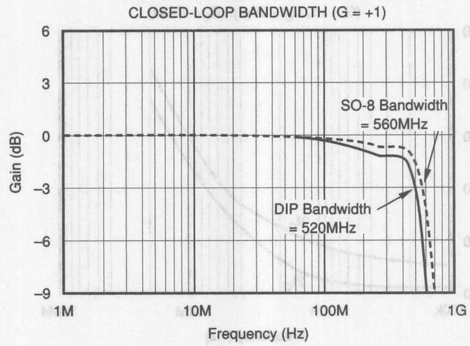
SMALL SIGNAL TRANSIENT RESPONSE
(G = +1)

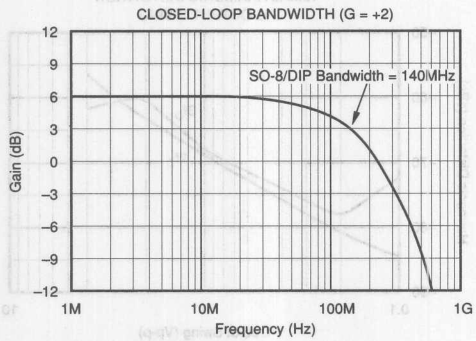


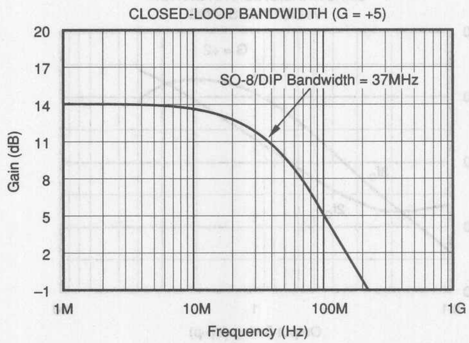
TYPICAL PERFORMANCE CURVES (CONT)

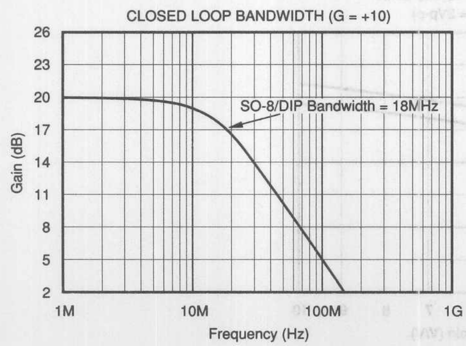
At $T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted. $R_{FB} = 25\Omega$ for Gain of +1.

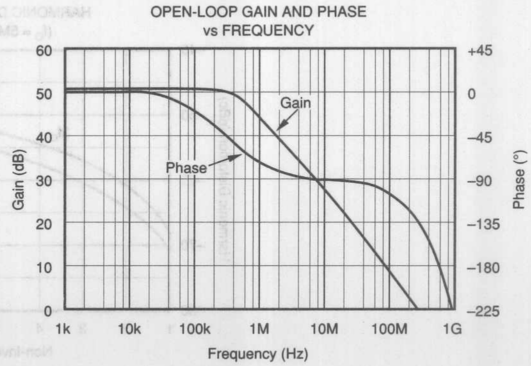






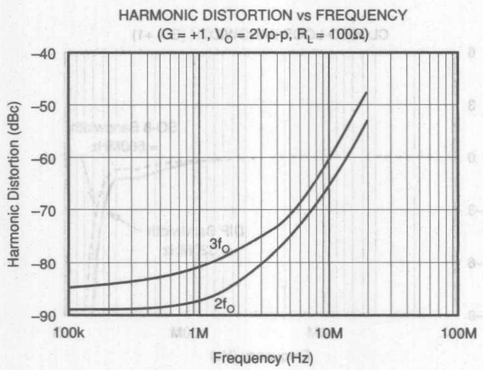


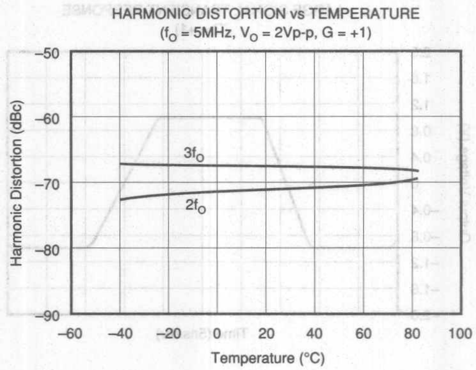


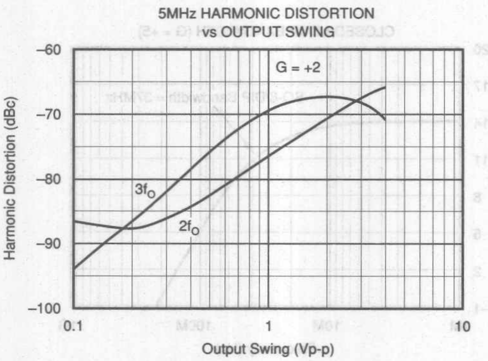


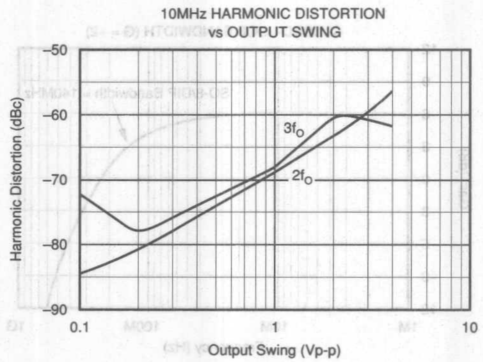
TYPICAL PERFORMANCE CURVES (CONT)

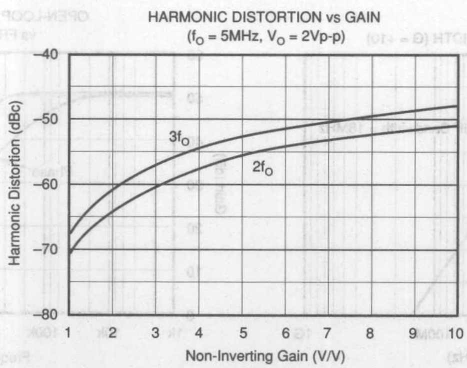
At $T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted. $R_{FB} = 25\Omega$ for Gain of +1.











DISCUSSION OF PERFORMANCE

The OPA650 is a low power, wideband voltage feedback operational amplifier. Each channel is internally compensated to provide unity gain stability. The OPA650's voltage feedback architecture features true differential and fully symmetrical inputs. This minimizes offset errors, making the OPA650 well suited for implementing filter and instrumentation designs. The OPA650's AC performance is optimized to provide a gain bandwidth product of 180MHz and a fast 0.1% settling time of 10.2ns, which is an important consideration in high speed data conversion applications. Along with its excellent settling characteristics, the low DC input offset of ±1mV and drift of ±3µV/°C support high accuracy requirements. In applications requiring a higher slew rate and wider bandwidth, such as video and high bit rate digital communications, consider the current feedback OPA658.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA650 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the two power pins to high frequency 0.1µF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA650. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Other network components, such as non-inverting input termination resistors, should also be placed close to the package.

Even with a low parasitic capacitance shunting external resistors, excessively high resistor values can create significant time constants and degrade performance. Good metal film or surface mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this adds a pole and/or zero below 500MHz that can affect circuit operation. Keep resistor values as low as possible consistent with output loading considerations. The 402Ω feedback used for the Typical Performance Plots is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for a unity gain follower. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA650 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) Socketing a high speed part like the OPA650 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

power supplies. A 10% tolerance on the supplies, or an ECL –5.2V for the negative supply, is within the maximum specified total supply voltage of 11V. Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single supply operation. Figure 1 shows one approach to single-supply operation.

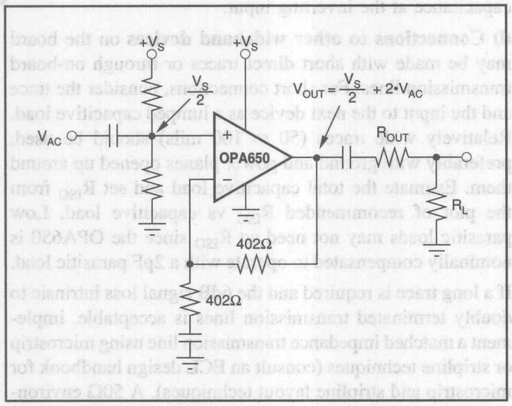


FIGURE 1. Single Supply Operation.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 2 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current.

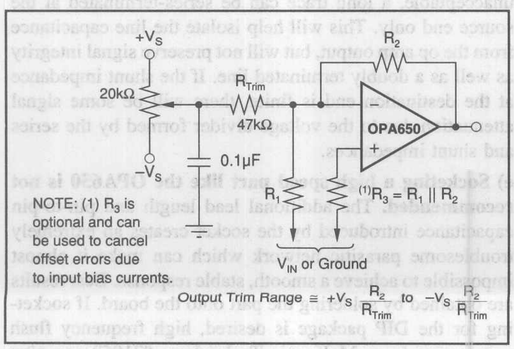


FIGURE 2. Offset Voltage Trim.

ESD damage has been well recognized for MOSFET devices, but any semiconductor device is vulnerable to this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are strongly recommended when handling the OPA650.

OUTPUT DRIVE CAPABILITY

The OPA650 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive a 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA650 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as driving A/D converters require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA650 maintains very low-closed loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing.

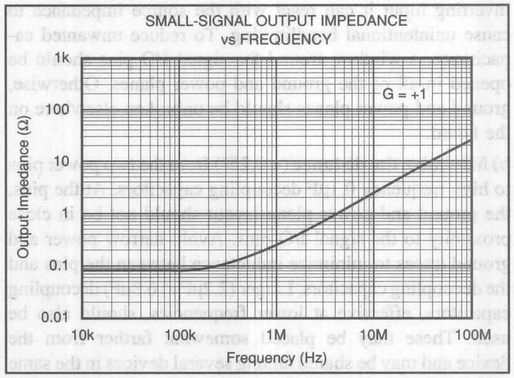


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA650 will not require heatsinking under most operating conditions. Maximum desired junction temperature will limit the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D\theta_{JA}$. The total internal power dissipation (P_D) is a combination of the total quiescent power (P_{DQ}) and the power dissipated in of the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load

when the output is a fixed DC voltage equal to 1/2 of either supply voltage (assuming equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading. Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation. As an example, compute the maximum T_J for an OPA650N at $A_V = +2$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, $\pm V_S = \pm 5V$, with the output at $|V_S/2|$, and the specified maximum $T_A = +85°C$. $P_D = 10V \bullet 8.75mA + (5^2)/(4 \bullet (100\Omega \| 804\Omega)) = 158mW$. Maximum $T_J = +85°C + 0.158W \bullet 150°C/W = 109°C$.

DRIVING CAPACITIVE LOADS

The OPA650's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be isolated by connecting a small resistance, usually 15Ω to 30Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

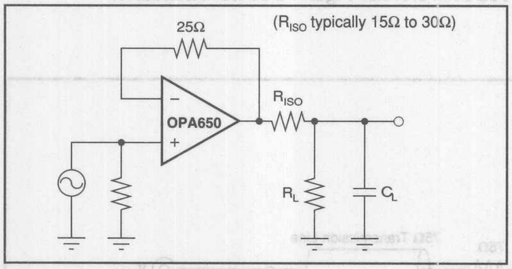


FIGURE 4. Driving Capacitive Loads.

FREQUENCY RESPONSE COMPENSATION

The OPA650 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain greater than one to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Frequency response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA650 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high-frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee-network) is recommended to avoid using large value resistors with large time constants.

PULSE SETTLING TIME

High speed amplifiers like the OPA650 are capable of extremely fast settling time with a pulse input. Excellent frequency response flatness and phase linearity are required to get the best settling times. As shown in the specifications table, settling time for a ±1V step at a gain of +1 for the OPA650 is extremely fast. The specification is defined as the time required, after the input transition, for the output to settle within a specified error band around its final value. For a 2V step, 1% settling corresponds to an error band of ±20mV, 0.1% to an error band of ±2mV, and 0.01% to an error band of ±0.2mV. For the best settling times, particularly into an ADC capacitive load, little or no peaking in the frequency response can be allowed. Using the recommended R_{ISO} for capacitive loads will limit this peaking and reduce the settling times. Fast, extremely fine scale settling (0.01%) requires close attention to ground return currents in the supply decoupling capacitors. For highest performance, consider the OPA642 which isolates the output stage decoupling from the rest of the amplifier.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. The percentage change in closed-loop gain over a specified change in output voltage level is defined as DG. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. DG and DP are both specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA650's harmonic distortion characteristics into a 100Ω load are shown versus frequency and power output in the typical performance curves. Distortion can be significantly improved by increasing the load resistance as illustrated in Figure 5. Remember to include the contribution of the feedback network when calculating the effective load resistance seen by the amplifier.

NOISE FIGURE

The OPA650 voltage noise spectral density is specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA650's Noise Figure vs Source Resistance is shown in Figure 6.

SPICE MODELS AND EVALUATION BOARD

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models and evaluation PC boards (DEM-OPA65xP) are available for the OPA650. Contact the Burr-Brown Applications Department to receive a SPICE diskette.

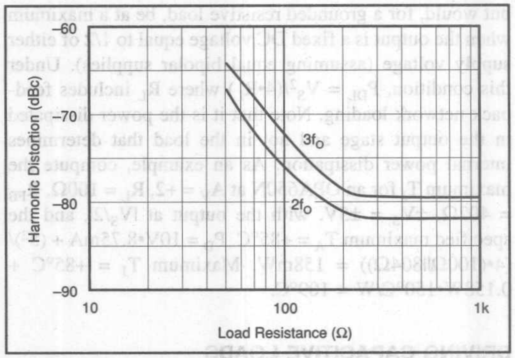


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

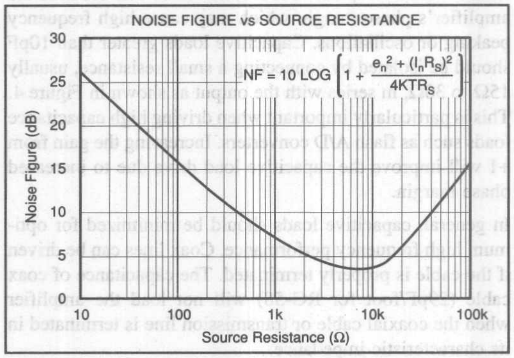


FIGURE 6. Noise Figure vs Source Resistance.

TYPICAL APPLICATION

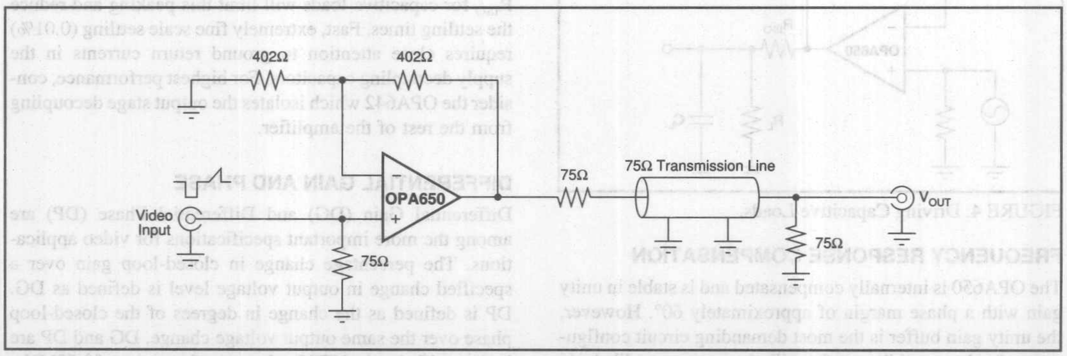


FIGURE 7. Low Distortion Video Amplifier.

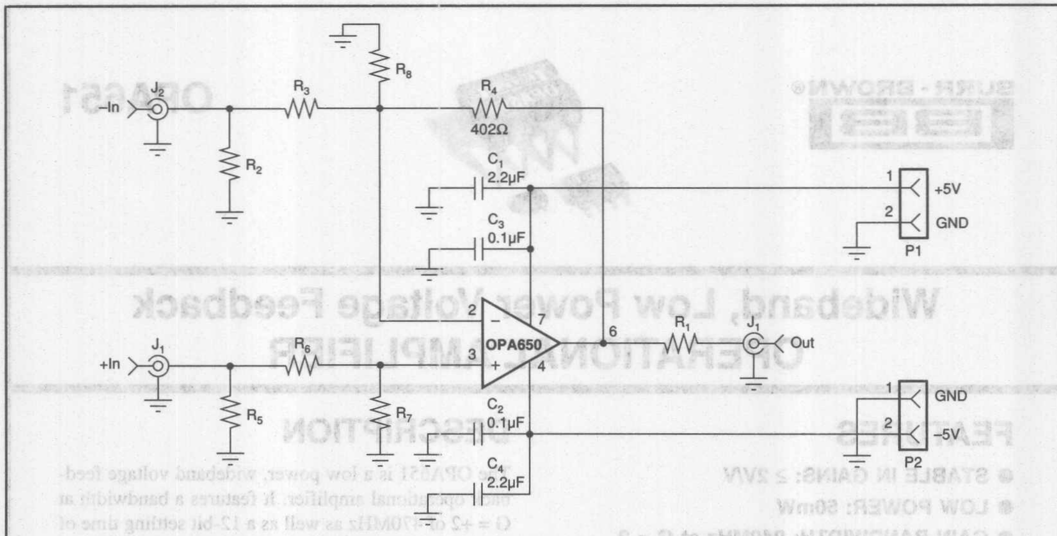


FIGURE 8. Layout Detail For DEM-OPA65X Demonstration Board.

DEM-OPA65XP Demonstration Board Layout

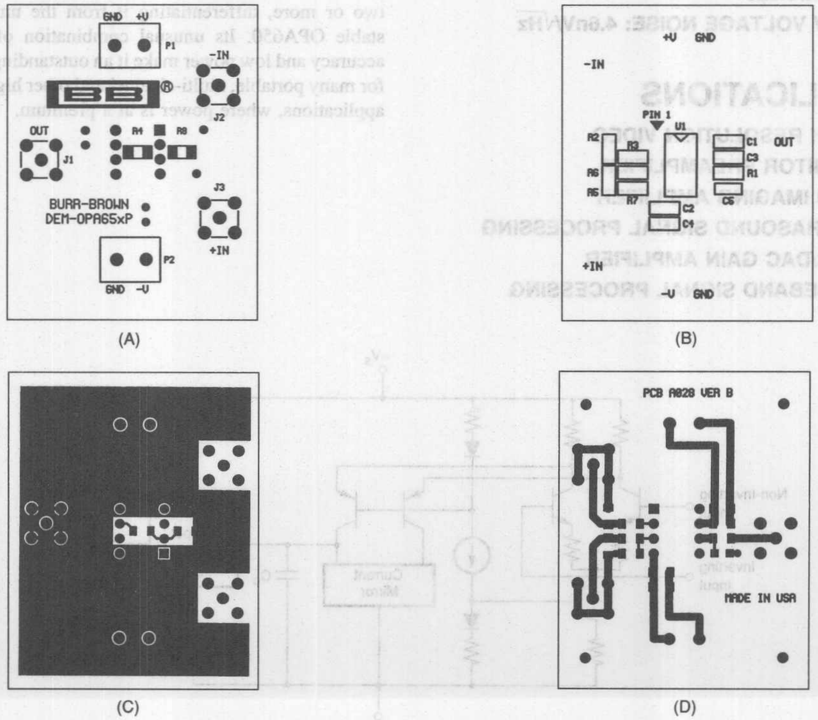
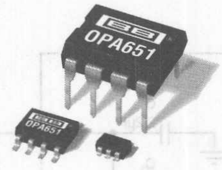


FIGURE 9a. Evaluation Board Silkscreen (Bottom). 9b. Evaluation Board Silkscreen (Top). 9c. Evaluation Board Layout (Solder Side). 9d. Evaluation Board Layout (Layout Side).

BURR - BROWN®

OPA651



Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- STABLE IN GAINS: ≥ 2V/V
- LOW POWER: 50mW
- GAIN-BANDWIDTH: 940MHz at G = 2
- FAST SETTLING TIME: 16ns to 0.01%
- LOW HARMONICS: –78dB at 5MHz
- LOW INPUT BIAS CURRENT: 4μA
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.025°
- LOW VOLTAGE NOISE: 4.6nV/$\sqrt{Hz}$

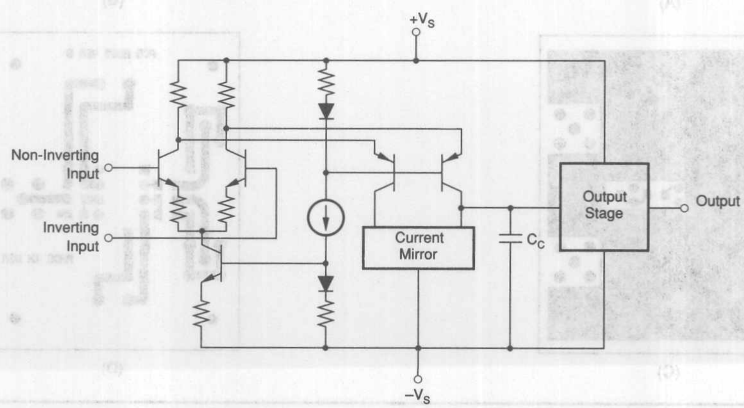
APPLICATIONS

- HIGH RESOLUTION VIDEO
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- BASEBAND SIGNAL PROCESSING

DESCRIPTION

The OPA651 is a low power, wideband voltage feedback operational amplifier. It features a bandwidth at G = +2 of 470MHz as well as a 12-bit settling time of only 16ns. The wide bandwidth and true differential input stage make it suitable for use in a variety of applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA651 is compensated for stability in gains of two or more, differentiating it from the unity gain stable OPA650. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

$T_A = +25°C$, $V_S = ±5V$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, G = +2, unless otherwise noted.

		OPA651P, U			OPA651PB, UB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE								
Closed-Loop Bandwidth(2)	G = +2		470			*(1)		MHz
	G = +5		70			*		MHz
	G = +10		34			*		MHz
Gain Bandwidth Product			340			*		MHz
Slew Rate	G = +2, V_O = 2V step		300			*		V/µs
Over Specified Temperature			275			*		V/µs
Rise Time	0.2V Step		0.8			*		ns
Fall Time	0.2V Step		0.8			*		ns
Settling Time 0.01%	G = +2, V_O = 2V step		16.2			*		ns
0.1%	G = +2, V_O = 2V step		11.5			*		ns
1%	G = +2, V_O = 2V step		7.2			*		ns
Spurious Free Dynamic Range	G = +2, f = 5.0 MHz, V_O = 2Vp-p,							
	$R_L = 100\Omega$		67			*		dBc
	$R_L = 400\Omega$		78			*		dBc
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$		0.01			*		%
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$		0.025			*		Degrees
Bandwidth For 0.1dB Flatness	G = +2		43			*		MHz
INPUT OFFSET VOLTAGE								
Input Offset Voltage			±1	±5.0		*	±2.0	mV
Average Drift			±3			*		µV/°C
Power Supply Rejection ($+V_S$)	V_S = ±4.5V to ±5.5V	65	85		70	*		dB
($-V_S$)		52	60		55	*		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		4	20		*	10	µA
Over Temperature			6	30		*	20	µA
Input Offset Current	V_{CM} = 0V		0.4	1.5		*	*	µA
Over Temperature			0.9	3.0		*	*	µA
INPUT NOISE								
Input Voltage Noise								
Noise Density, f = 100Hz			13			*		nV/√Hz
f = 10kHz			4.6			*		nV/√Hz
f = 1MHz			4.6			*		nV/√Hz
Voltage Noise, BW = 10Hz to 100MHz			46			*		µVrms
Input Bias Current Noise								
Current Noise Density, f = 0.1Hz to 20kHz			1.1			*		pA/√Hz
Noise Figure (NF)	$R_S = 10k\Omega$		3.2			*		dB
	$R_S = 50\Omega$		14			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range			±3.5			*		V
Over Specified Temperature		±3.0			*			V
Common-Mode Rejection	V_{CM} = ±0.5V	75	90		80	*		dB
INPUT IMPEDANCE								
Differential			60 || 1			*		kΩ || pF
Common-Mode			2.6 || 1			*		MΩ || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±2V, $R_L = 100\Omega$	42	50		45	*		dB
Over Specified Temperature	V_O = ±2V, $R_L = 100\Omega$	40			42			dB
OUTPUT								
Voltage Output								
Over Specified Temperature	No Load	±2.2	±3.0		±2.4	*		V
	$R_L = 250\Omega$	±2.2	±2.5		±2.4	*		V
	$R_L = 100\Omega$	±2.0	±2.3		±2.1	*		V
Current Output, Sourcing		75	110		*	*		mA
Over Specified Temperature		65			*			mA
Current Output, Sinking		65	85		*	*		mA
Over Specified Temperature		35			*			mA
Short Circuit Current			150			*		mA
Output Resistance	0.1MHz, G = +2		0.05			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Operating Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current			±5.1	±7.75		*	±6.5	mA
Over Specified Temperature				±8.75			±7.5	mA
TEMPERATURE RANGE								
Specification: P, U, PB, UB		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
P 8-Pin DIP			100			*		°C/W
U SO-8			125			*		°C/W
N SOT23-5			150			*		°C/W

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The OPA651 is nominally compensated assuming 2pF parasitic load. The demonstration board, DEM-OPA65xP, shows a low parasitic layout for this device.

ABSOLUTE MAXIMUM RATINGS

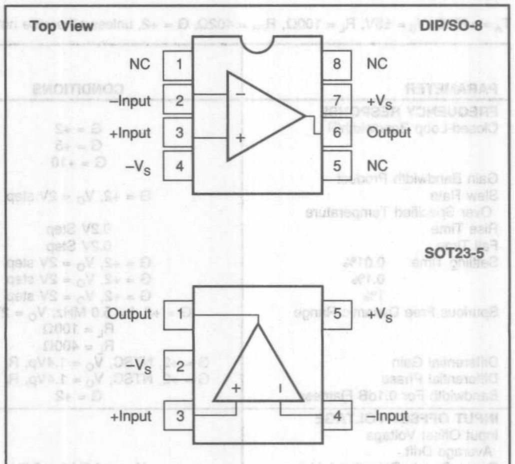
Supply .... ±5.5V
Internal Power Dissipation(1): .... See Thermal Conditions
Differential Input Voltage .... ±1.2V
Input Voltage Range .... $\pm V_S$
Storage Temperature Range: P, PB, U, UB, N, NB..... –40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
(soldering, SO-8 3s) .... +260°C
Junction Temperature (T_J) .... +175°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION



PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE	PACKAGE MARKING(2)	ORDERING NUMBER
OPA651U	SO-8 Surface Mount	182	–40°C to +85°C	OPA651U	OPA651U
OPA651UB	SO-8 Surface Mount	182	–40°C to +85°C	OPA651UB	OPA651UB
OPA651P	8-Pin Plastic DIP	006	–40°C to +85°C	OPA651P	OPA651P
OPA651PB	8-Pin Plastic DIP	006	–40°C to +85°C	OPA651PB	OPA651PB

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 and DIP packages will be marked with a "B" by pin 8.

ADVANCE PACKAGE INFORMATION(2)

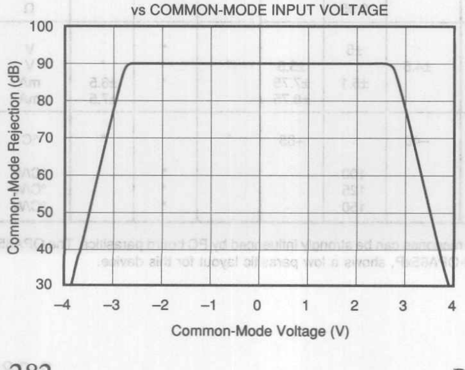
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER
OPA651N	5-Pin SOT23-5	331	–40°C to +85°C	—	—
OPA651NB	5-Pin SOT23-5	331	–40°C to +85°C	—	—

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The SOT23-5 will be available in tape and reel only by August, 1996.

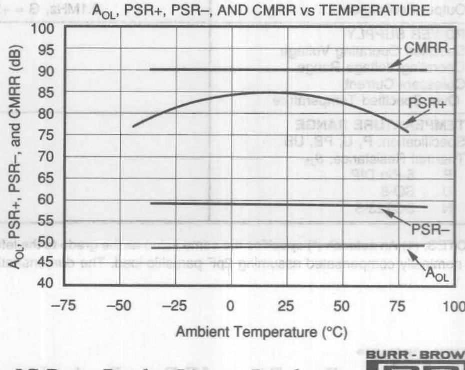
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, and $G = +2$, unless otherwise noted.

COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE

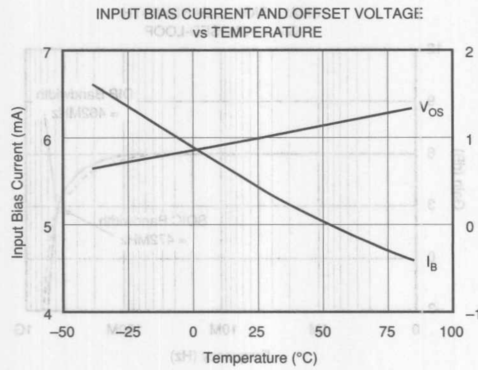


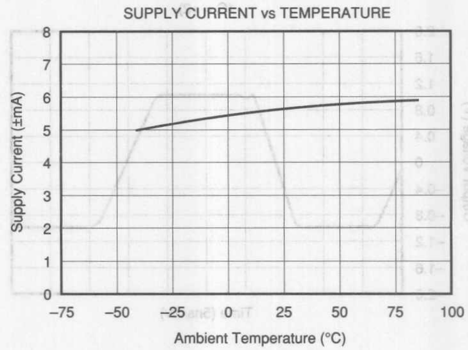
A_{OL}, PSR+, PSR–, AND CMRR vs TEMPERATURE

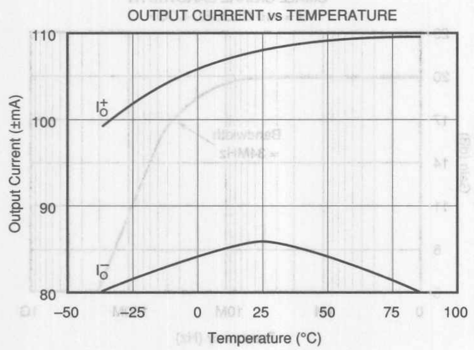


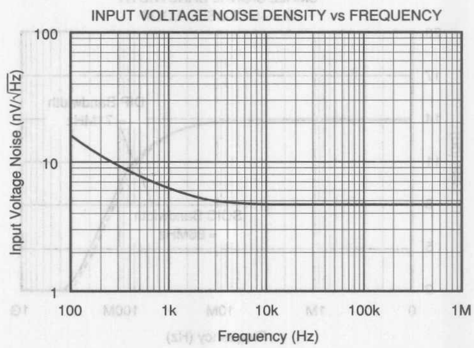
TYPICAL PERFORMANCE CURVES (CONT)

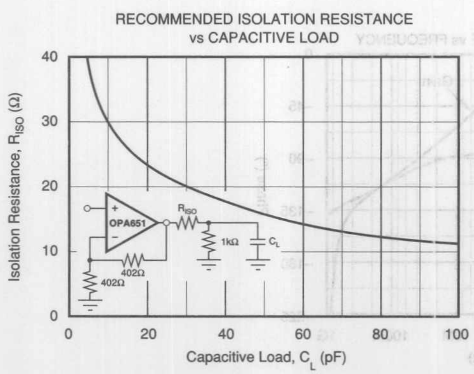
T_A = +25°C, V_S = ±5V, R_L = 100Ω, R_{FB} = 402Ω, and G = +2, unless otherwise noted.

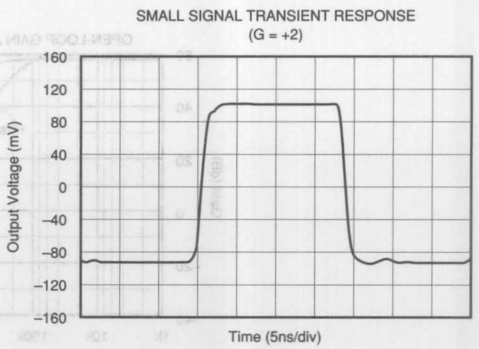






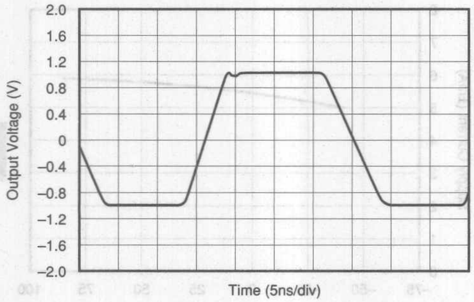




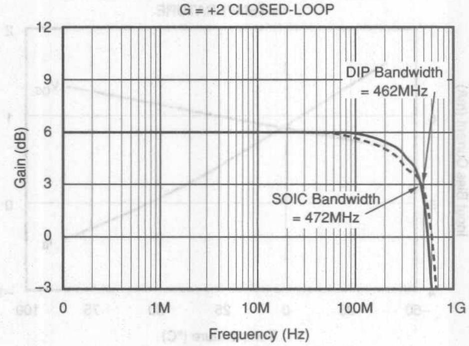


$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, and $G = +2$, unless otherwise noted.

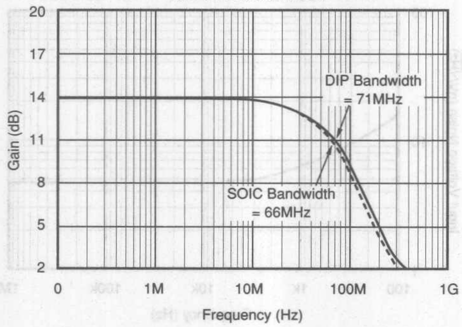
LARGE SIGNAL TRANSIENT RESPONSE
(G = +2)



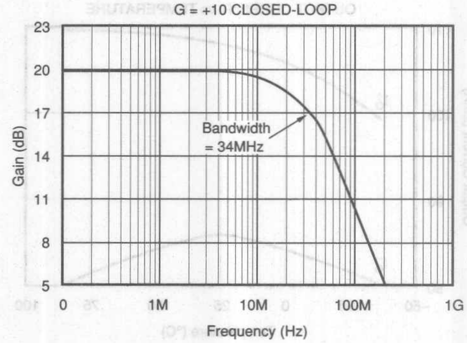
SMALL SIGNAL BANDWIDTH
G = +2 CLOSED-LOOP



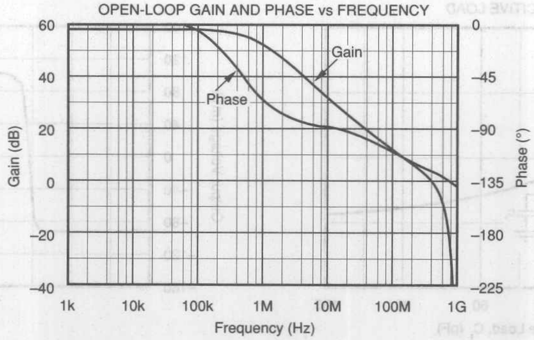
SMALL SIGNAL BANDWIDTH
G = +5 CLOSED-LOOP



SMALL SIGNAL BANDWIDTH
G = +10 CLOSED-LOOP

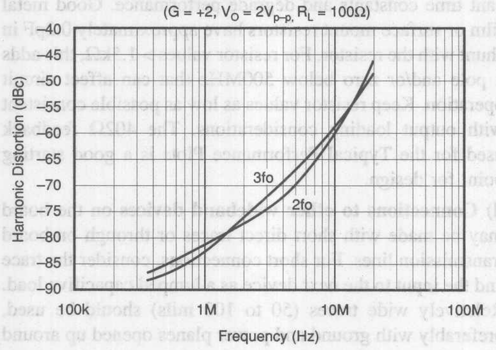


OPEN-LOOP GAIN AND PHASE vs FREQUENCY

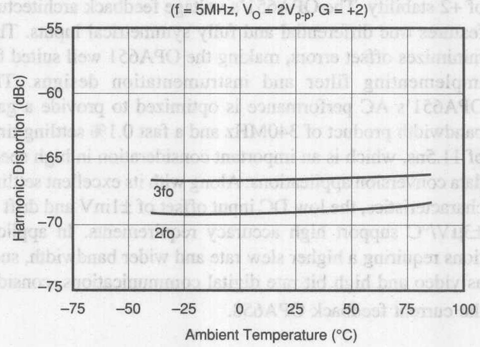


$T_A = +25°C$, $V_S = ±5V$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, and $G = +2$, unless otherwise noted.

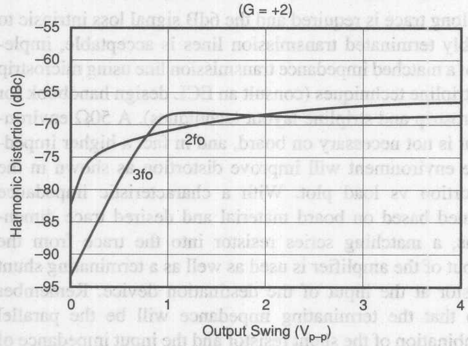
HARMONIC DISTORTION vs FREQUENCY
($G = +2$, $V_O = 2V_{p-p}$, $R_L = 100\Omega$)



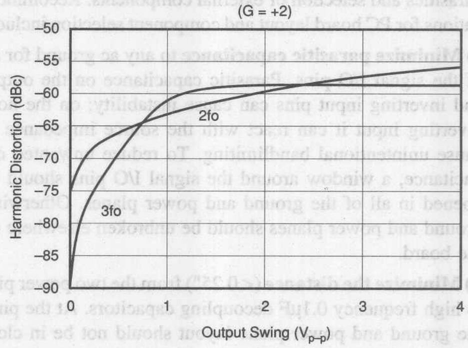
HARMONIC DISTORTION vs TEMPERATURE
($f = 5MHz$, $V_O = 2V_{p-p}$, $G = +2$)



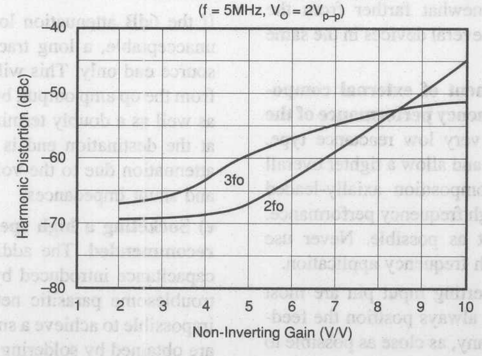
5MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = +2$)



10MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = +2$)



HARMONIC DISTORTION vs GAIN
($f = 5MHz$, $V_O = 2V_{p-p}$)



DISCUSSION OF PERFORMANCE

The OPA651 is a low power, wideband voltage feedback operational amplifier, internally compensated to provide gain of +2 stability. The OPA651's voltage feedback architecture features true differential and fully symmetrical inputs. This minimizes offset errors, making the OPA651 well suited for implementing filter and instrumentation designs. The OPA651's AC performance is optimized to provide a gain bandwidth product of 340MHz and a fast 0.1% settling time of 11.5ns, which is an important consideration in high speed data conversion applications. Along with its excellent settling characteristics, the low DC input offset of ±1mV and drift of ±3µV/°C support high accuracy requirements. In applications requiring a higher slew rate and wider bandwidth, such as video and high bit rate digital communications, consider the current feedback OPA658.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA651 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) **Minimize parasitic capacitance** to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) **Minimize the distance** (< 0.25") from the two power pins to high frequency 0.1µF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) **Careful selection and placement of external components will preserve the high frequency performance of the OPA651**. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Other network components, such as non-inverting input termination resistors, should also be placed close to the package.

Even with a low parasitic capacitance shunting external resistors, excessively high resistor values can create significant time constants and degrade performance. Good metal film or surface mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this adds a pole and/or zero below 500MHz that can affect circuit operation. Keep resistor values as low as possible consistent with output loading considerations. The 402Ω feedback used for the Typical Performance Plots is a good starting point for design.

d) **Connections to other wideband devices** on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA651 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) **Socketing a high speed part like the OPA651 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

The OPA651 is nominally specified for operation using ±5V power supplies. A 10% tolerance on the supplies, or an ECL –5.2V for the negative supply, is within the maximum specified total supply voltage of 11V. Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single supply operation. Figure 1 shows one approach to single-supply operation.

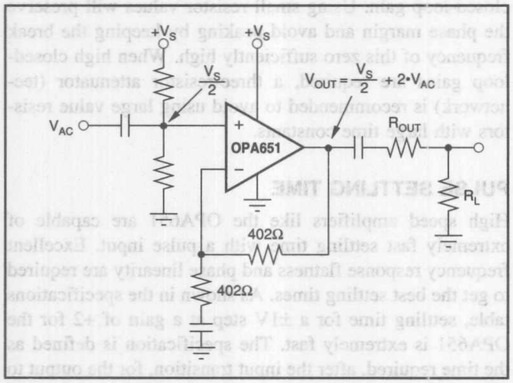


FIGURE 1. Single Supply Operation.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 2 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current.

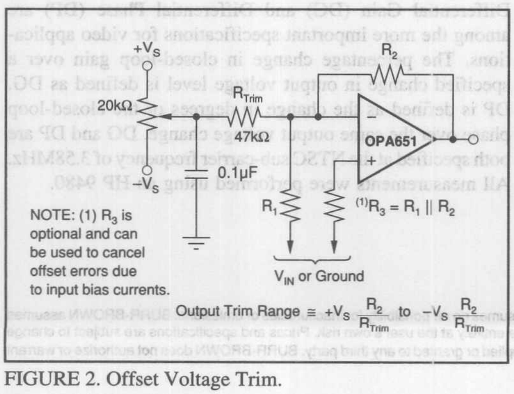


FIGURE 2. Offset Voltage Trim.

ESD PROTECTION

ESD damage has been well recognized for MOSFET devices, but any semiconductor device is vulnerable to this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are strongly recommended when handling the OPA651.

OUTPUT DRIVE CAPABILITY

The OPA651 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive a 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA651 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as driving A/D converters require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA651 maintains very low-closed loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing.

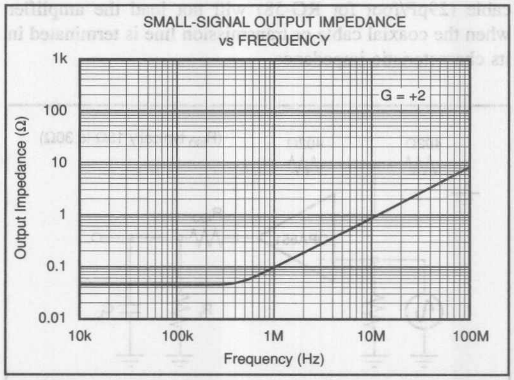


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA651 will not require heatsinking under most operating conditions. Maximum desired junction temperature will limit the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D\theta_{JA}$. The total internal power dissipation (P_D) is a combination of the total quiescent power (P_{DQ}) and the power dissipated in of the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load

but would, for a grounded resistive load, be at a maximum when the output is a fixed DC voltage equal to 1/2 of either supply voltage (assuming equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading. Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation. As an example, compute the maximum T_J for an OPA651N at $A_V = +2$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, $\pm V_S = \pm 5V$, with the output at $|V_S/2|$, and the specified maximum $T_A = +85°C$. $P_D = 10V \bullet 8.75mA + (5^2)/(4 \bullet (100\Omega \| 804\Omega)) = 158mW$. Maximum $T_J = +85°C + 0.158W \bullet 150°C/W = 109°C$.

DRIVING CAPACITIVE LOADS

The OPA651's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be isolated by connecting a small resistance, usually 15Ω to 30Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +2 will improve the capacitive load drive due to increased phase margin.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

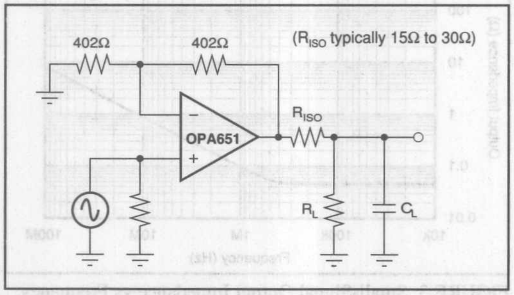


FIGURE 4. Driving Capacitive Loads.

FREQUENCY RESPONSE COMPENSATION

The OPA651 is internally compensated and is stable at a gain of 2 with a phase margin of approximately 60°. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Frequency response for other gains are shown in the Typical Performance Curves.

The high frequency response of the OPA651 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high-frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee-network) is recommended to avoid using large value resistors with large time constants.

PULSE SETTLING TIME

High speed amplifiers like the OPA651 are capable of extremely fast settling time with a pulse input. Excellent frequency response flatness and phase linearity are required to get the best settling times. As shown in the specifications table, settling time for a ±1V step at a gain of +2 for the OPA651 is extremely fast. The specification is defined as the time required, after the input transition, for the output to settle within a specified error band around its final value. For a 2V step, 1% settling corresponds to an error band of ±20mV, 0.1% to an error band of ±2mV, and 0.01% to an error band of ±0.2mV. For the best settling times, particularly into an ADC capacitive load, little or no peaking in the frequency response can be allowed. Using the recommended R_{ISO} for capacitive loads will limit this peaking and reduce the settling times. Fast, extremely fine scale settling (0.01%) requires close attention to ground return currents in the supply decoupling capacitors. For highest performance, consider the OPA642 which isolates the output stage decoupling from the rest of the amplifier.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. The percentage change in closed-loop gain over a specified change in output voltage level is defined as DG. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. DG and DP are both specified at the NTSC sub-carrier frequency of 3.58MHz. All measurements were performed using an HP 9480.

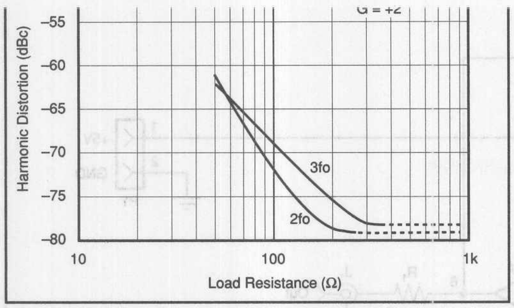


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

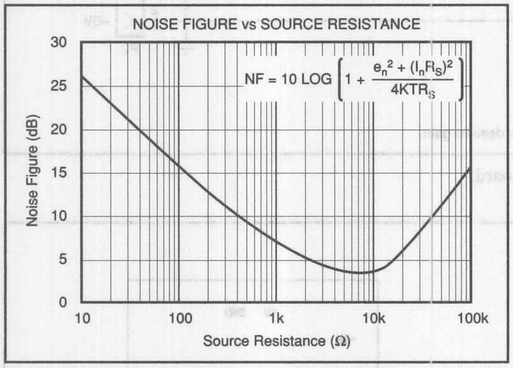


FIGURE 6. Noise Figure vs Source Resistance.

The OPA651's harmonic distortion characteristics into a 100Ω load are shown versus frequency and power output in the typical performance curves. Distortion can be significantly improved by increasing the load resistance as illustrated in Figure 5. Remember to include the contribution of the feedback network when calculating the effective load resistance seen by the amplifier.

NOISE FIGURE

The OPA651 voltage noise spectral density is specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA651's Noise Figure vs Source Resistance is shown in Figure 6.

SPICE MODELS AND EVALUATION BOARD

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models and evaluation PC boards (DEM-OPA65xP) are available for the OPA651. Contact the Burr-Brown Applications Department to receive a SPICE diskette.

TYPICAL APPLICATION

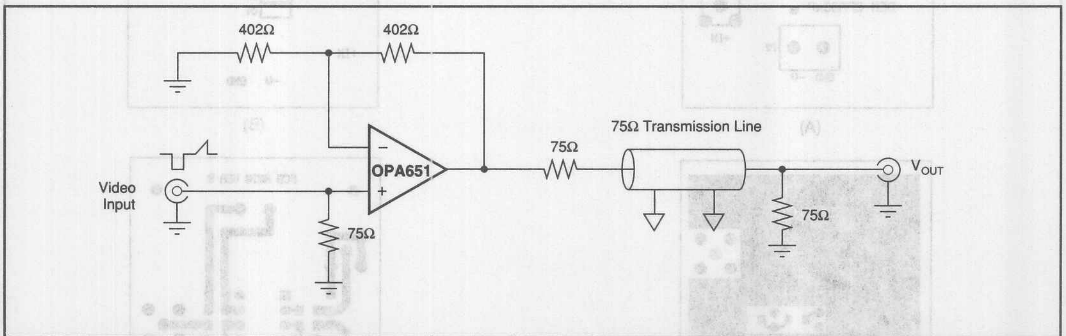
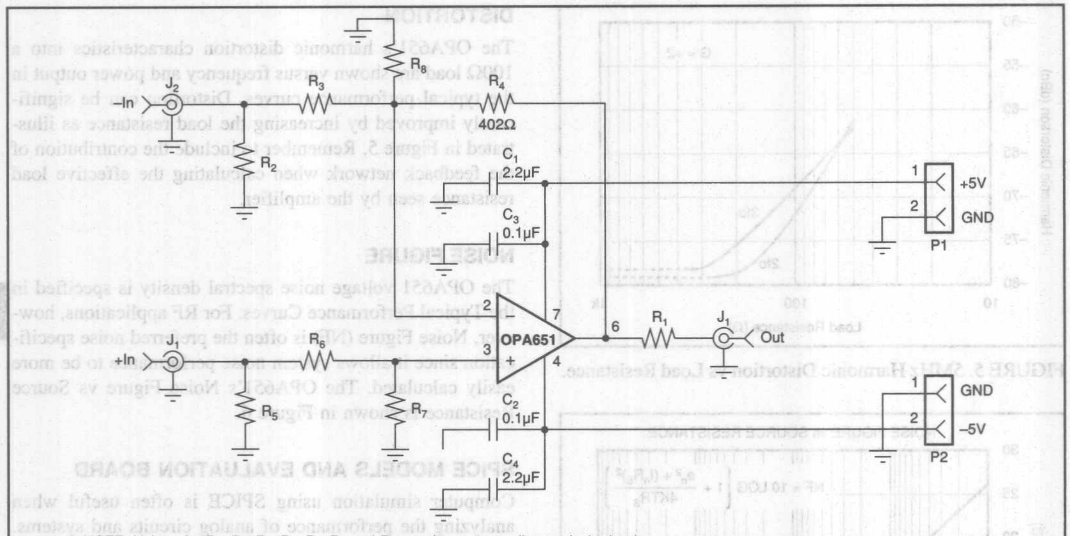


FIGURE 7. Low Distortion Video Amplifier.



NOTE: Values for R_1, R_2, R_3, R_5, R_6, R_7 and R_8 are chosen according to desired gain.

FIGURE 8. Layout Detail For DEM-OPA65X Demonstration Board.

DEM-OPA65XP Demonstration Board Layout

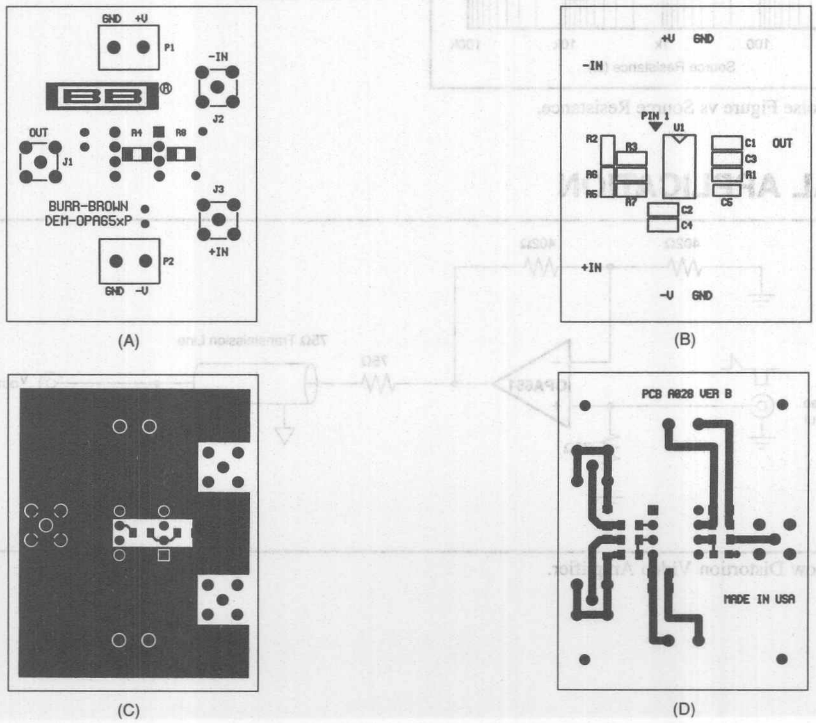
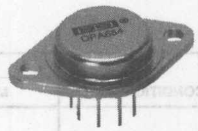


FIGURE 9a. Evaluation Board Silkscreen (Solder Side). 9b. Evaluation Board Silkscreen (Component Side). 9 c. Evaluation Board Layout (Solder Side). 9d. Evaluation Board Layout (Component Side).

BURR - BROWN®

OPA654



Wide Bandwidth, High Output Current *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- HIGH SLEW RATE: 750V/µs
- HIGH OUTPUT CURRENT: 200mA
- WIDE GAIN-BANDWIDTH: 700MHz
- FAST SETTLING: 150ns to 0.1%
- FET INPUT: I_B = 50pA max

APPLICATIONS

- LINE DRIVERS
- PIN DRIVERS
- HIGH-SPEED DATA ACQUISITION
- WAVEFORM GENERATORS

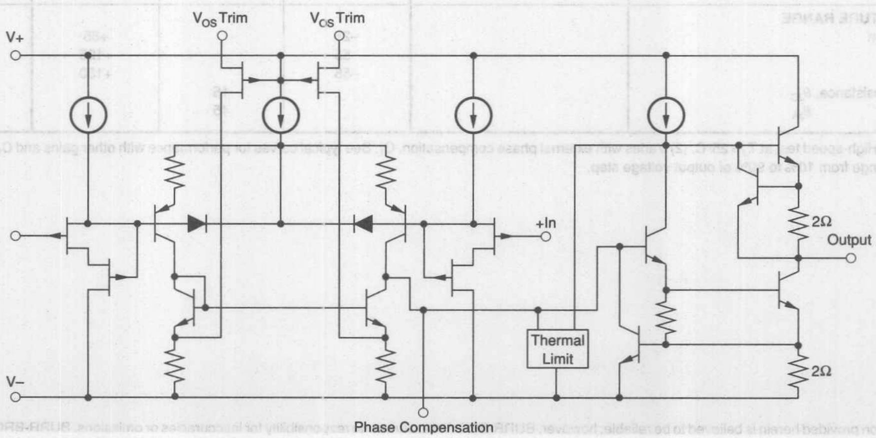
DESCRIPTION

The OPA654 is a high-speed monolithic operational amplifier featuring 200mA output current. Fabricated using Burr-Brown's Complementary-Bipolar, ***Difet*** process, it provides an excellent combination of high speed and high output current.

The OPA654 is versatile, operating from power supplies ranging from ±5V to ±18V. It can deliver up to ±10V signals into a 50Ω load at slew rates of 750V/µs. Its speed and output current make it useful for line driver and automatic test applications.

The OPA654 is externally compensated, allowing open-loop gain and phase characteristics to be optimized for the desired closed-loop gain, load and dynamic characteristics.

The OPA654 is available in an 8-pin metal TO-3 package that provides excellent thermal characteristics and is specified for the industrial temperature range.



Difet®, Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V unless otherwise noted.

		OPA654AM			
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE					
Gain-Bandwidth Product (2)			See Typical Curve		
Slew Rate (2,3)	G = –1, 20V Step		750		V/µs
Settling Time (2) 0.01%	G = –1, 10V Step		240		ns
0.1%	G = –1, 10V Step		150		ns
1%	G = –1, 10V Step		85		ns
OFFSET VOLTAGE					
Input Offset Voltage			±0.1	±3	mV
Average Drift			±40		µV/°C
Power Supply Rejection	V_S = ±5 to ±15V	72	82		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		3	50	pA
Input Offset Current	V_{CM} = 0V		2	25	pA
NOISE					
Input Voltage Noise					
Noise Density,	f = 10Hz		115		nV/√Hz
	f = 100Hz		37		nV/√Hz
	f = 1kHz		19		nV/√Hz
	f = 10kHz		14		nV/√Hz
Voltage Noise,	f_B = 10Hz to 1MHz		85		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			1		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±12	±13		V
Common-Mode Rejection	V_{CM} = ±10V	70	76		dB
INPUT IMPEDANCE					
Differential			10^{12} ‖ 2.5		Ω ‖ pF
Common-Mode			10^{12} ‖ 3.2		Ω ‖ pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ		94		dB
	V_O = ±10V, R_L = 50Ω	80	82		dB
OUTPUT					
Voltage Output	R_L = 50Ω	±11	±12.3		V
Current Output	V_O = ±10V		200		mA
Short Circuit Current			325		mA
Output Resistance, Open-Loop	DC		800		Ω
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±5		±18	V
Quiescent Current			±38	±43	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–55		+125	°C
Storage		–55		+150	°C
Thermal Resistance, θ_{JC}			15		°C/W
θ_{JA}			45		°C/W

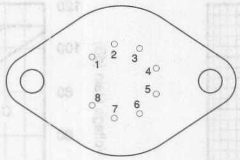
NOTES: (1) High-speed test at T_J = 25°C. (2) Varies with external phase compensation, C_1. See typical curves for performance with other gains and C_1. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

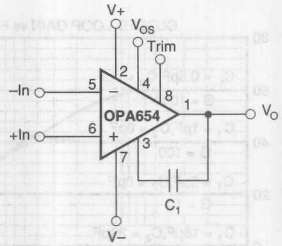
PIN CONFIGURATION

"M" TO-3 Metal Package

PIN LIST
1. V_O
2. V+
3. Compensation
4. V_{OS} Trim
5. –In
6. +In
7. V–
8. V_{OS} Trim

BOTTOM VIEW





Case is connected to IC substrate. Connect case to ground—see text.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	$\pm V_S \pm 1V$
Output Short Circuit (to ground)	10s
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +150°C
Junction Temperature	+165°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA654AM	8-Pin Metal TO-3	030

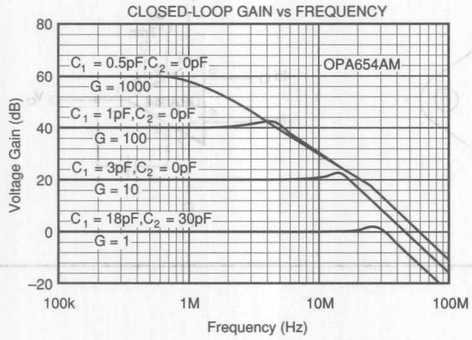
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

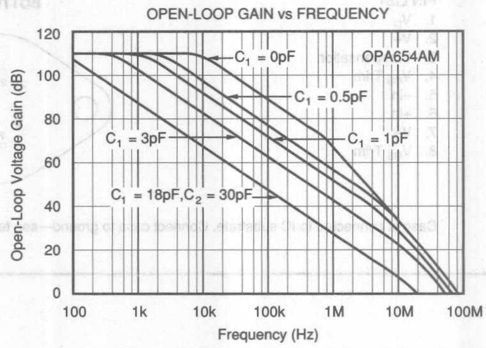
ORDERING INFORMATION

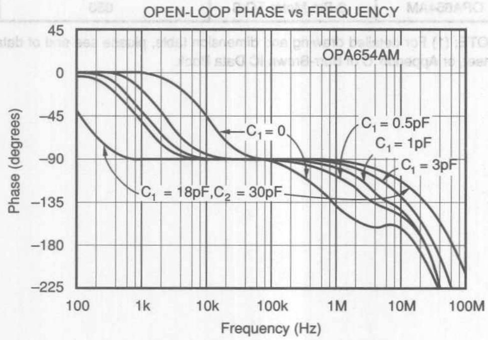
MODEL	PACKAGE	TEMPERATURE RANGE
OPA654AM	8-Pin Metal TO-3	–25°C to +85°C

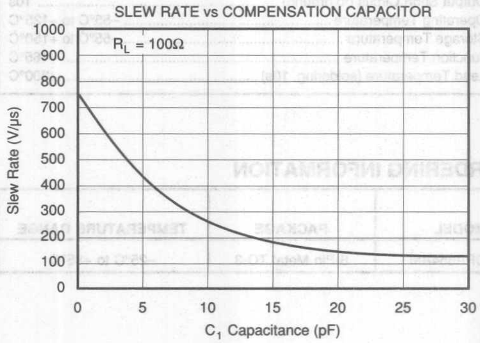
TYPICAL PERFORMANCE CURVES

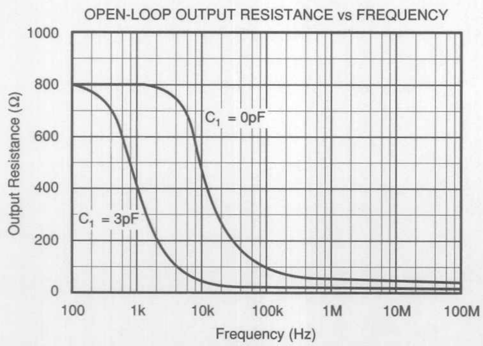
$T_A = +25°C$, $V_S = \pm15V$ unless otherwise noted.

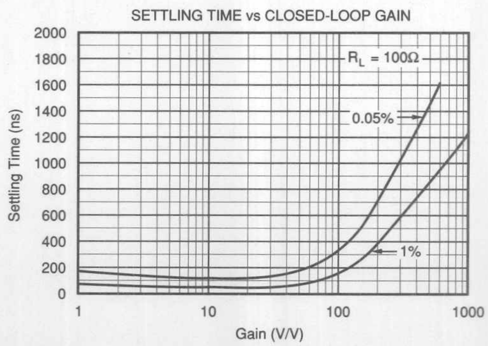






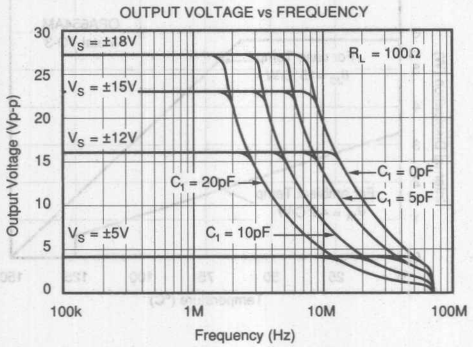


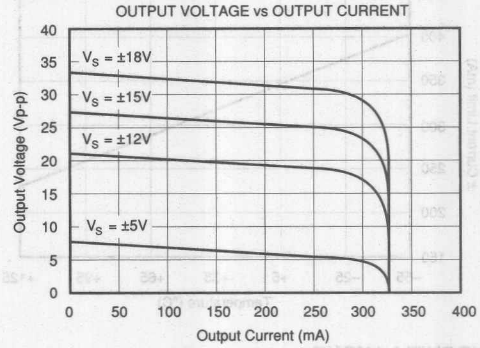


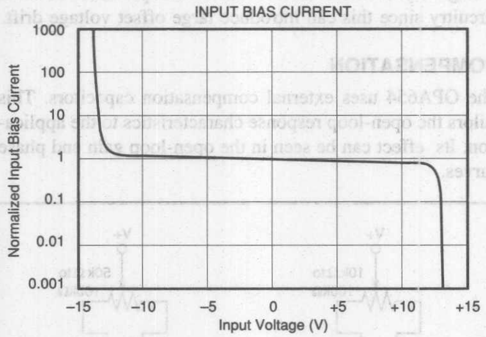


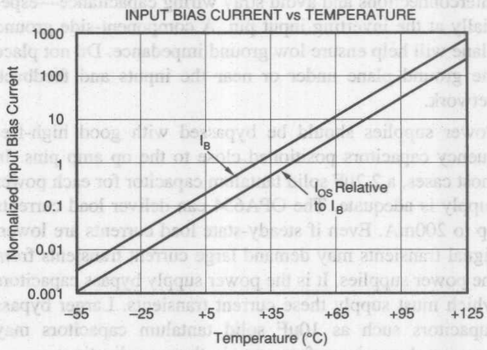
TYPICAL PERFORMANCE CURVES (CONT)

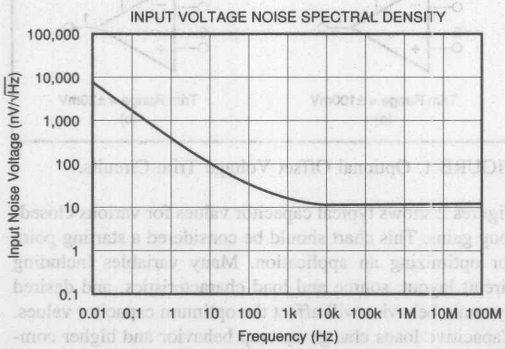
$T_A = +25°C$, $V_S = ±15V$ unless otherwise noted.

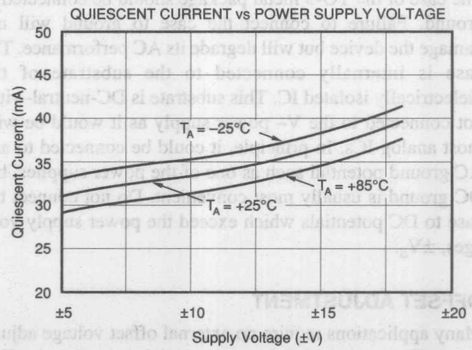






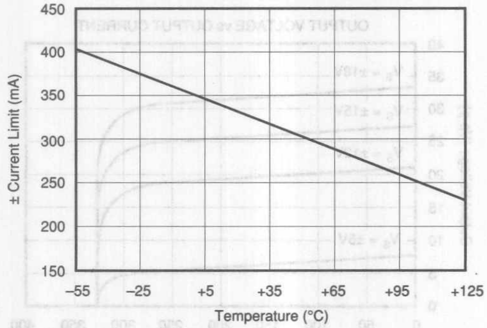




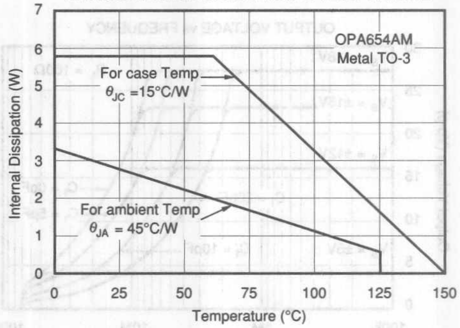


$T_A = +25°C$, $V_S = ±15V$ unless otherwise noted.

OUTPUT CURRENT LIMIT vs TEMPERATURE



MAXIMUM POWER DISSIPATION vs TEMPERATURE



CIRCUIT LAYOUT

With any wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

Power supplies should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, a 2.2µF solid tantalum capacitor for each power supply is adequate. The OPA654 can deliver load currents up to 200mA. Even if steady-state load currents are lower, signal transients may demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as 10µF solid tantalum capacitors may improve dynamic performance in these applications.

CASE CONNECTION

The case of the TO-3 metal package should be connected to ground. Failure to connect the case to ground will not damage the device but will degrade its AC performance. The case is internally connected to the substrate of the dielectrically isolated IC. This substrate is DC-neutral—it is not connected to the V– power supply as it would be with most analog ICs. In principle, it could be connected to any AC ground potential such as one of the power supplies, but DC ground is usually most convenient. Do not connect the case to DC potentials which exceed the power supply voltages, $±V_S$.

OFFSET ADJUSTMENT

Many applications require no external offset voltage adjustment. Figure 1a shows connection of an optional offset voltage trimming potentiometer. Use a small, non-inductive potentiometer with short connections to the trim pins. Avoid stray capacitance from the input or output nodes. The added resistors in Figure 1b help decouple the potentiometer from these sensitive nodes, making the type and location of the potentiometer less critical. This also reduces the trim range, providing more adjustment resolution. Do not use an offset voltage adjustment to correct for offsets produced in other circuitry since this can introduce large offset voltage drift.

COMPENSATION

The OPA654 uses external compensation capacitors. This tailors the open-loop response characteristics to the application. Its effect can be seen in the open-loop gain and phase curves.

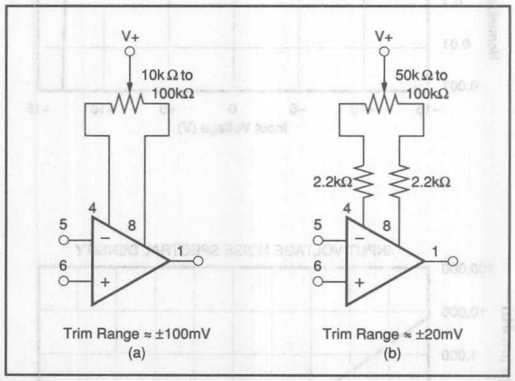
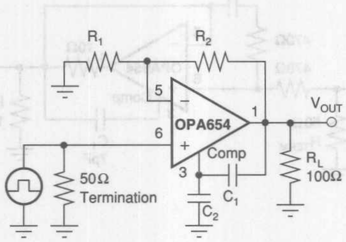
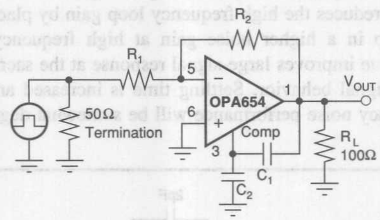


FIGURE 1. Optional Offset Voltage Trim Circuits.

Figures 2 shows typical capacitor values for various closed-loop gains. This chart should be considered a starting point for optimizing an application. Many variables including circuit layout, source and load characteristics, and desired dynamic behavior will affect the optimum capacitor values. Capacitive loads change op amp behavior and higher compensation capacitor values are generally required. Resistor R_S, shown in Figure 3, can improve the ability to drive a capacitive load. Typical values for R_S range from 5Ω to 50Ω, depending on the load and how much voltage drop can be tolerated.

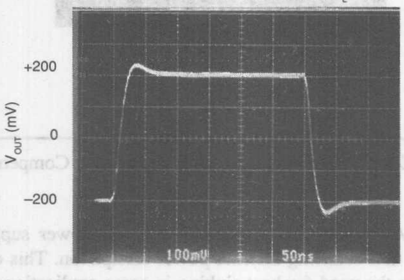


CLOSED-LOOP GAIN	C_1	C_2	R_1	R_2
+1000	0.5pF	0	10Ω	10kΩ
+100	1pF	0	100Ω	10kΩ
+10	3pF	0	100Ω	900Ω
+1	18pF	30pF	—	0

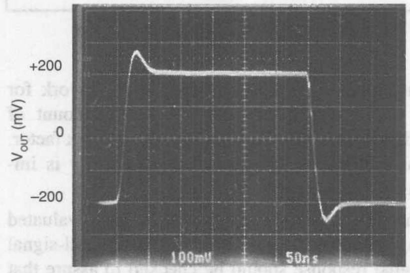


CLOSED-LOOP GAIN	C_1	C_2	R_1	R_2
−1000	0.5pF	0	10Ω	10kΩ
−100	1pF	0	100Ω	10kΩ
−10	3pF	0	100Ω	1kΩ
−1	18pF	20pF	1kΩ	1kΩ

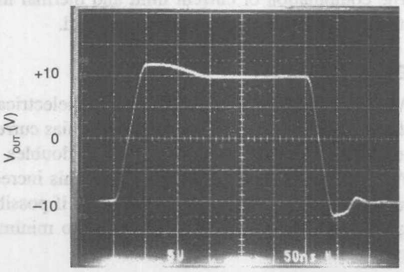
G = +10 SMALL-SIGNAL RESPONSE, R_L =100Ω



G = −10 SMALL-SIGNAL RESPONSE, R_L =100Ω



G = +10 LARGE-SIGNAL RESPONSE, R_L =100Ω



G = −10 LARGE-SIGNAL RESPONSE, R_L =100Ω

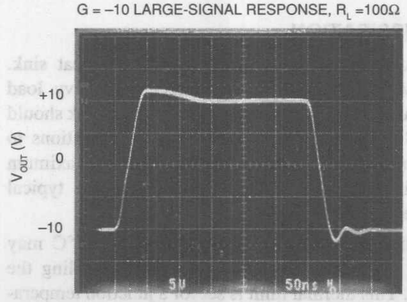


FIGURE 2. Basic Amplifier Circuits.

Figure 3 also demonstrates a compensation technique using an additional network, R_3-C_3. This allows use of a smaller value for C_1, producing a corresponding increase in slew rate. It reduces the high frequency loop gain by placing the op amp in a higher noise gain at high frequency. This technique improves large-signal response at the sacrifice of small-signal behavior. Settling time is increased and high frequency noise performance will be somewhat degraded.

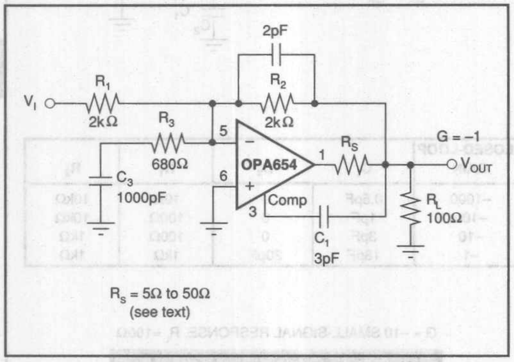


FIGURE 3. High Slew Rate Compensation Circuit.

Figure 4 shows an alternative compensation network for unity gain. This technique provides a small amount of positive feedback, reducing the net negative feedback factor. Large signal response and load driving capability is improved with this approach.

The compensation for a given application can be evaluated by observing amplifier pulse response. Both small-signal and large-signal response should be checked to assure that both are acceptable. Large overshoot or many cycles of ringing in the small-signal response is a sign of instability and the circuit may require further optimization. Good practice dictates a somewhat conservative approach to allow for device-to-device variation.

POWER DISSIPATION

Many applications do not require an external heat sink. However, with high ambient temperature or heavy load conditions, a heat sink may be required. The heat sink should be electrically connected to ground—see "Connections to Case". Operate within the power derating curve (Maximum Power Dissipation vs Temperature) shown in the typical performance curve section.

Exceeding the maximum die temperature of 165°C may activate the internal thermal limit circuitry, disabling the output stage. This thermal limit is set for a junction temperature of approximately 185°C.

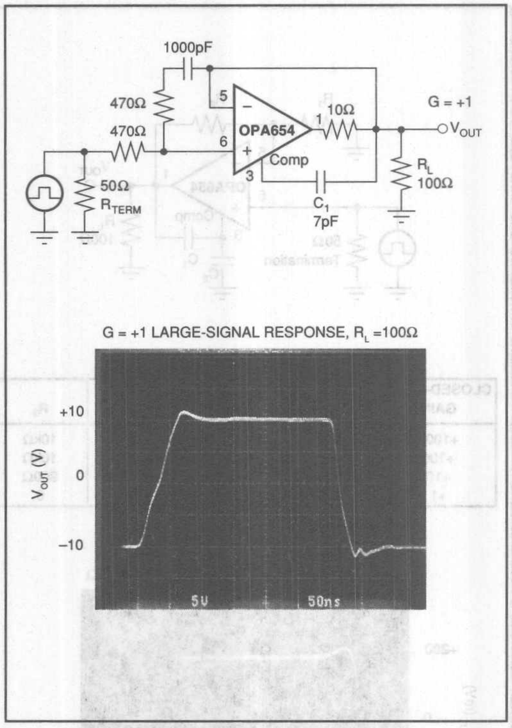


FIGURE 4. G = +1 Amplifier with Alternative Compensation.

The OPA654 may be operated at reduced power supply voltage, thus reducing internal power dissipation. This can eliminate the need for heat sinking in some applications.

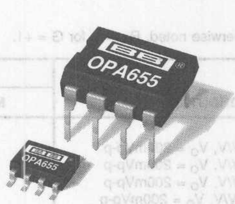
OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately 325mA at 25°C. The limit current decreases with increasing junction temperature as shown in the typical curves. The combination of current limit and thermal limit protects the device from short circuits to ground.

INPUT BIAS CURRENT

The OPA654 is fabricated with Burr-Brown's dielectrically isolated ***Difet*** process, giving it very low input bias current. Like other FET amplifiers, input bias current doubles for every 10°C increase in junction temperature. This increase can be minimized by providing a heat sink and, if possible, operating with reduced power supply voltage to minimize power dissipation.

BURR - BROWN®



OPA655

Wideband FET-Input OPERATIONAL AMPLIFIER

FEATURES

- 400MHz UNITY GAIN BANDWIDTH
- LOW INPUT BIAS CURRENT: 5pA
- HIGH INPUT IMPEDANCE: $10^{12}\Omega$ ‖ 1.0pF
- ULTRA-LOW dG/dP: 0.006%/0.009°
- LOW DISTORTION: 90dB SFDR at 5MHz
- FAST SETTLING: 17ns (0.01%)
- HIGH OUTPUT CURRENT: 60mA
- FAST OVERDRIVE RECOVERY

APPLICATIONS

- WIDEBAND PHOTODIODE AMPLIFIER
- PEAK DETECTOR
- CCD OUTPUT BUFFER
- ADC INPUT BUFFER
- HIGH SPEED INTEGRATOR
- TEST AND MEASUREMENT FRONT END

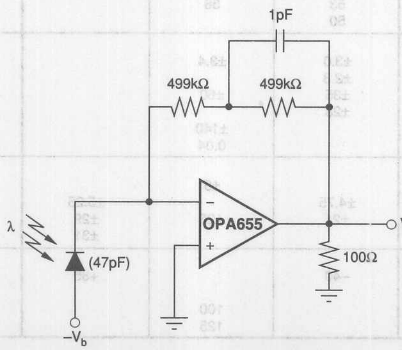
DESCRIPTION

The OPA655 combines a very wideband, unity gain stable, voltage feedback op amp with a FET input stage to offer an ultra high dynamic range amplifier for ADC buffering and transimpedance applications. Extremely low harmonic distortion along with excellent pulse settling characteristics will support even the most demanding ADC input buffer requirements.

The broad unity gain stable bandwidth and FET input allows exceptional performance in high speed, low noise integrators.

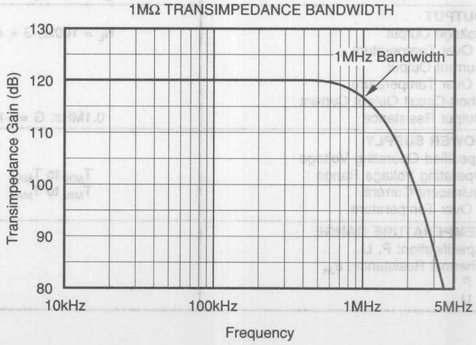
The high input impedance and low bias current provided by the FET input is further supported by the ultra-low $6nV/\sqrt{Hz}$ input voltage noise to achieve a very low integrated noise in wideband photodiode transimpedance applications.

Broad transimpedance bandwidths are achievable given the OPA655's high 240MHz gain bandwidth product. As shown below, a –3dB bandwidth of 1MHz is provided even for a high 1MΩ transimpedance gain from a 47pF source capacitance.



Wideband Photodiode Transimpedance Amplifier

1MΩ TRANSIMPEDANCE BANDWIDTH



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

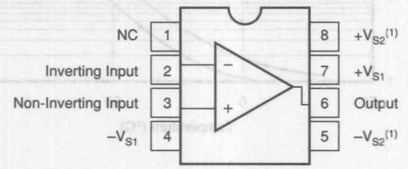
PARAMETER	CONDITIONS	OPA655P, U MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE					
Closed-Loop Response	Gain = +1V/V, V_O = 200mVp-p		400		MHz
	Gain = +2V/V, V_O = 200mVp-p		185		MHz
	Gain = +5V/V, V_O = 200mVp-p		57		MHz
	Gain = +10V/V, V_O = 200mVp-p		24		MHz
Gain-Bandwidth Product			240		MHz
Slew Rate	G = +1, 1V Step	210	290		V/µs
Over Temperature		200			V/µs
Rise Time	0.2V Step		1		ns
Fall Time	0.2V Step		1		ns
Settling Time: 0.01%	G = +1, 1V Step		17		ns
0.1%	G = +1, 1V Step		8		ns
1%	G = +1, 1V Step		6		ns
Spurious-Free Dynamic Range	G = +1, f = 5MHz V_O = ±1V, R_L = 100Ω	75	90		dBc
Differential Gain	3.58MHz, 0 to 1.4V, R_L = 150Ω		0.006		%
Differential Phase	3.58MHz, 0 to 1.4V, R_L = 150Ω		0.009		degrees
Bandwidth for 0.1dB flatness	G = +2, 2Vp-p		30		MHz
OFFSET VOLTAGE					
Input Offset Voltage			±1	±2	mV
Over Temperature			±10		µV/°C
Power Supply Rejection (+V_S)	$\vert V_S \vert$ = 4.50V to 5.50V	55	70		dB
(−V_S)		50	65		dB
INPUT BIAS CURRENT					
Input Bias Current	V_{CM} = 0V		−5	−125	pA
Over Temperature	V_{CM} = 0V			−8.0	nA
Input Offset Current	V_{CM} = 0V		±2	±125	pA
Over Temperature	V_{CM} = 0V			±8	nA
NOISE					
Input Voltage Noise					
Noise Density: f = 100Hz			20		nV/√Hz
f = 1kHz			8		nV/√Hz
f = 10kHz			6		nV/√Hz
f = 0.1MHz to 100MHz			6		nV/√Hz
Integrated Voltage Noise, BW = 1MHz to 100MHz			60		µVrms
Input Bias Current Noise					
Current Noise Density, f = 10Hz to 10kHz			1.3	4	fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range			±2.75		V
Over Temperature		±2.5			V
Common-Mode Rejection	V_{CM} = ±0.5V	55	70		dB
INPUT IMPEDANCE					
Differential			10^{12} || 1.2		Ω || pF
Common-Mode			10^{12} || 1.0		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	53	58		dB
Over Temperature	V_O = ±2V, R_L = 100Ω	50			dB
OUTPUT					
Voltage Output	R_L = 100Ω, G = +1	±3.0	±3.4		V
Over Temperature		±2.8			V
Current Output		±35	±60		mA
Over Temperature		±28			mA
Short-Circuit Output Current			±140		mA
Output Resistance	0.1MHz, G = +1		0.04		Ω
POWER SUPPLY					
Specified Operating Voltage			±5		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.75		±5.25	V
Quiescent Current	T_{MIN} to T_{MAX}	±21	±25	±29	mA
Over Temperature				±31	mA
TEMPERATURE RANGE					
Specification: P, U		−40		+85	°C
Thermal Resistance, θ_{JA}					
P			100		°C/W
U			125		°C/W

Total Supply Voltage Across Device ($V_{S\,(TOTAL)}$) ....

Internal Power Dissipation .... See Thermal Considerations
Differential Input Voltage .... $V_{S\,(TOTAL)}$
Common-Mode Input Voltage Range .... $\pm V_S$
Storage Temperature Range: P, U .... –40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
(soldering, SOIC 3s) .... +260°C
Junction Temperature (T_J) .... +175°C

PIN CONFIGURATION

Top View DIP/SOIC



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of pins 4 and 7 only, will reduce the effective pin impedance and substantially improve distortion.

MODEL	PACKAGE	NUMBER(1)
OPA655P	8-Pin Plastic DIP	006
OPA655U	8-Pin SO-8 Surface Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA655P	8-Pin Plastic DIP	–40°C to +85°C
OPA655U	8-Pin SO-8 Surface Mount	–40°C to +85°C

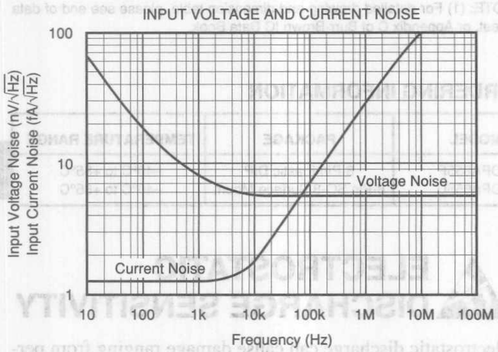
ELECTROSTATIC DISCHARGE SENSITIVITY

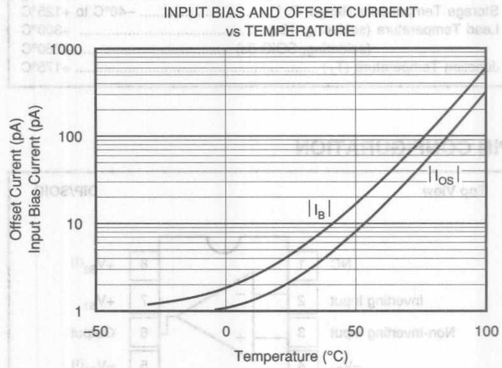
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

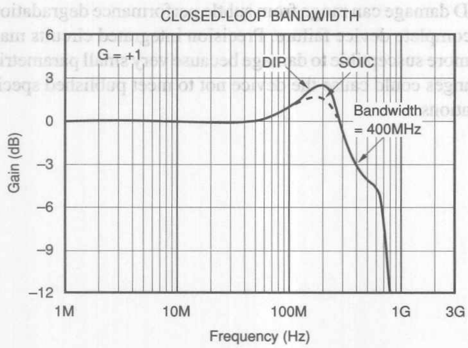
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

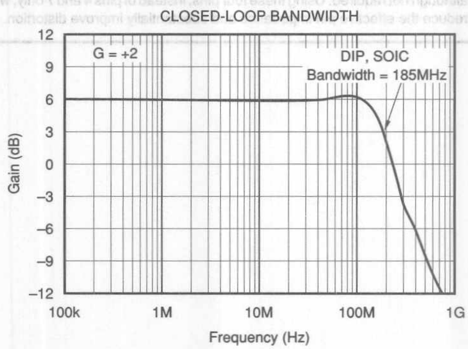
TYPICAL PERFORMANCE CURVES

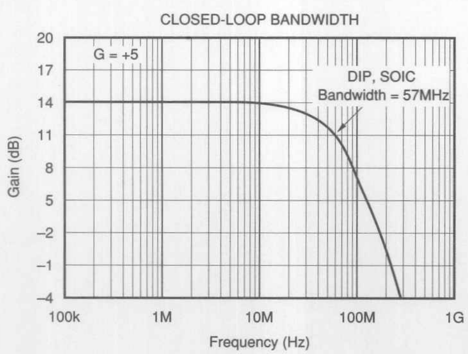
$T_A = +25°C$, $V_S = \pm5V$, $R_{FB} = 100\Omega$, and $R_L = 100\Omega$, unless otherwise noted. $R_{FB} = 0$ for G = +1.

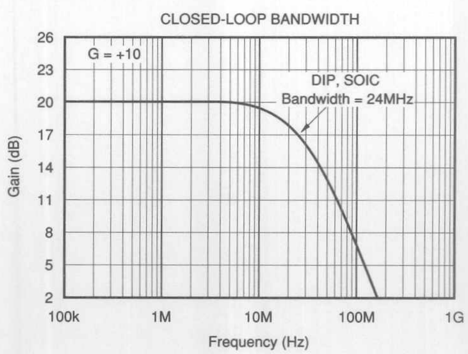








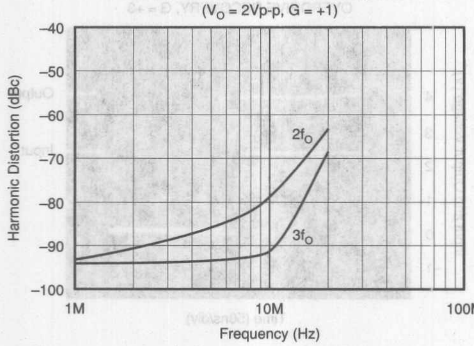




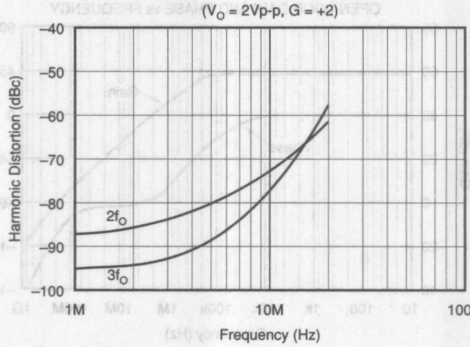
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = ±5V$, $R_{FB} = 100Ω$, and $R_L = 100Ω$, unless otherwise noted. $R_{FB} = 0$ for G = +1.

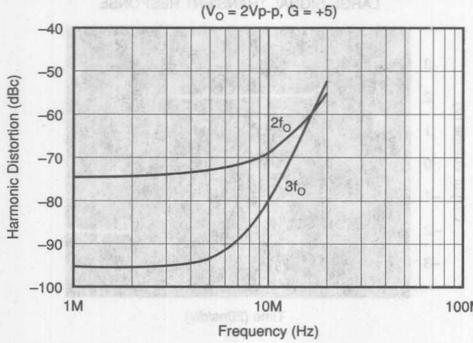
HARMONIC DISTORTION vs FREQUENCY (V_O = 2Vp-p, G = +1)



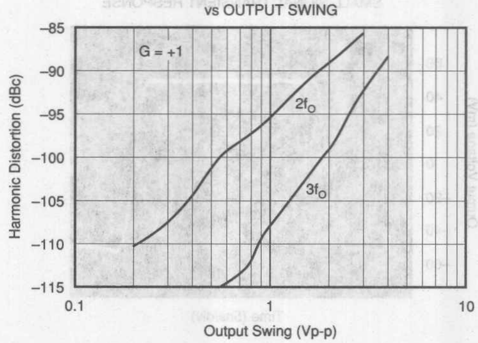
HARMONIC DISTORTION vs FREQUENCY (V_O = 2Vp-p, G = +2)



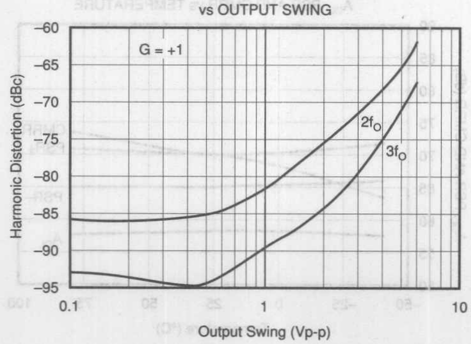
HARMONIC DISTORTION vs FREQUENCY (V_O = 2Vp-p, G = +5)



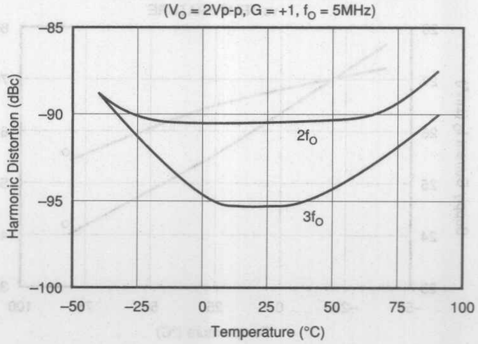
5MHz HARMONIC DISTORTION vs OUTPUT SWING

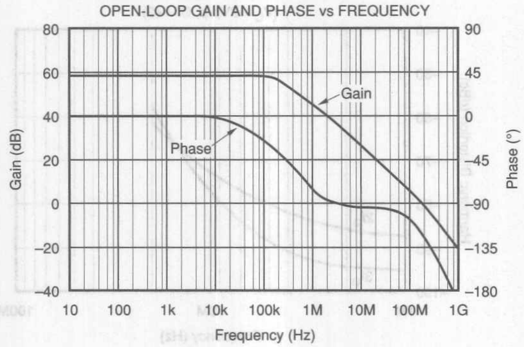


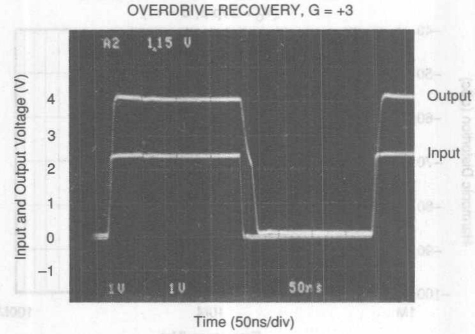
10MHz HARMONIC DISTORTION vs OUTPUT SWING

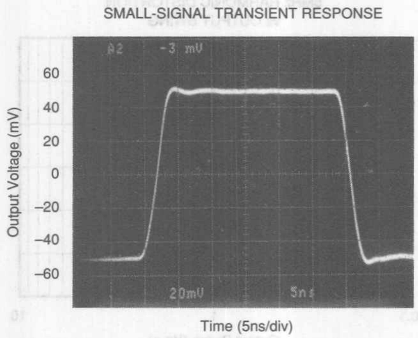


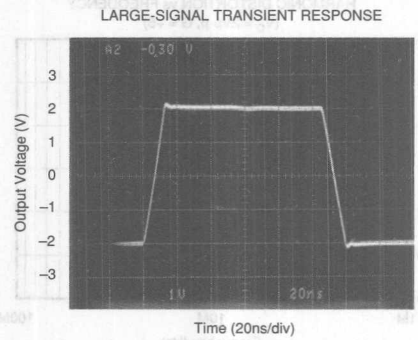
HARMONIC DISTORTION vs TEMPERATURE (V_O = 2Vp-p, G = +1, f_O = 5MHz)

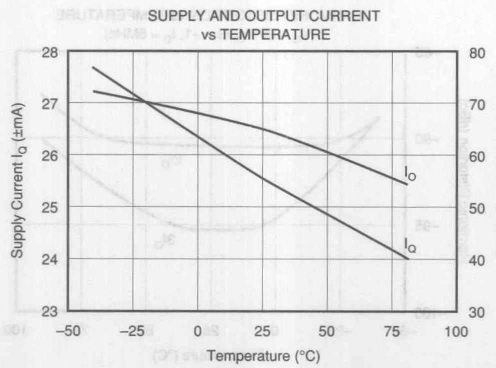


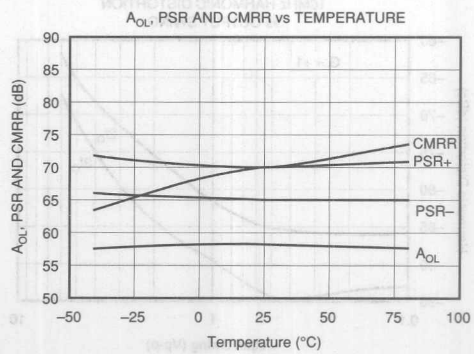

OPEN-LOOP GAIN AND PHASE vs FREQUENCY
Gain
Phase
Gain (dB)
Phase (°)
Frequency (Hz)


OVERDRIVE RECOVERY, G = +3
Output
Input
Input and Output Voltage (V)
Time (50ns/div)

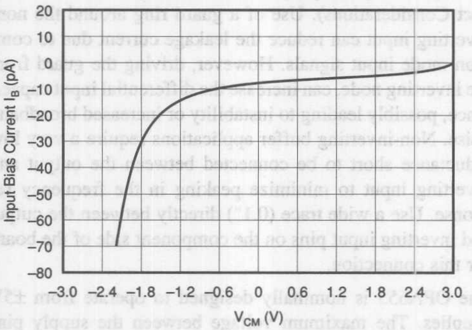

SMALL-SIGNAL TRANSIENT RESPONSE
Output Voltage (mV)
Time (5ns/div)


LARGE-SIGNAL TRANSIENT RESPONSE
Output Voltage (V)
Time (20ns/div)

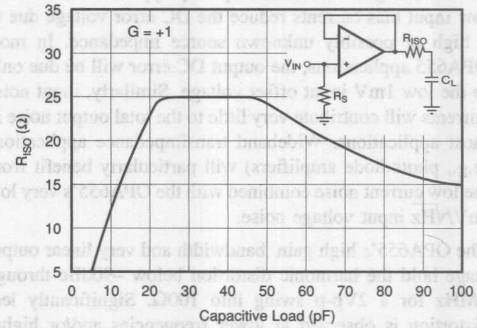

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE
Supply Current I_Q (±mA)
Output Current I_O (±mA)
I_O
I_Q
Temperature (°C)


A_{OL}, PSR AND CMRR vs TEMPERATURE
A_{OL}, PSR AND CMRR (dB)
CMRR
PSR+
PSR–
A_{OL}
Temperature (°C)

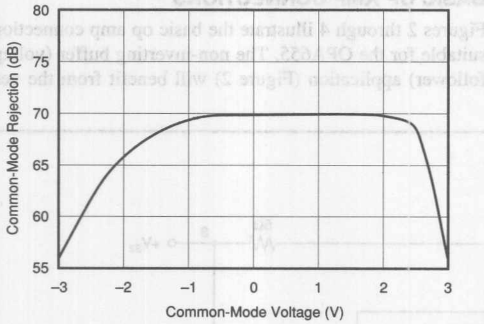
INPUT BIAS CURRENT
vs INPUT COMMON-MODE VOLTAGE



RECOMMENDED RESISTANCE
vs CAPACITIVE LOAD



COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



DISCUSSION OF PERFORMANCE

Amplifiers using FET input transistors operate in a similar manner to those using bipolar transistors, with some important advantages. In standard op amp applications, the very low input bias currents reduce the DC error voltage due to a high or possibly unknown source impedance. In most OPA655 applications, the output DC error will be due only to the low 1mV input offset voltage. Similarly, input noise currents will contribute very little to the total output noise in most applications. Wideband transimpedance applications (e.g., photodiode amplifiers) will particularly benefit from the low current noise combined with the OPA655's very low $6nV/\sqrt{Hz}$ input voltage noise.

The OPA655's high gain bandwidth and very linear output stage hold the harmonic distortion below –90dBc through 5MHz for a 2Vp-p swing into 100Ω. Significantly less distortion is observed at lower frequencies and/or higher load impedance. The voltage feedback architecture supports this level of accuracy with greater than 65dB power supply and common mode rejection ratios. This very high dynamic range, along with the low DC errors and noise of the FET input stage, can provide an exceptional buffering capability for ADC's, PMT's and other applications requiring high impedance sensing of a high speed signal. For similar distortion performance with a bipolar input stage, refer to the OPA642.

OPERATING CONSIDERATIONS

Careful attention to PC board layout will deliver the exceptional performance shown in the Typical Performance Curves. Generally, very low impedance paths to the power supplies, along with low parasitic connections to the signal I/O pins are required for best performance (See Layout and Interconnect Considerations). Use of a guard ring around the non-inverting input can reduce the leakage current due to common mode input signals. However, driving the guard from the inverting node, can increase the differential input capacitance, possibly leading to instability or increased broadband noise. Non-inverting buffer applications require a very low inductance short to be connected between the output and inverting input to minimize peaking in the frequency response. Use a wide trace (0.1") directly between the output and inverting input pins on the component side of the board for this connection.

The OPA655 is nominally designed to operate from ±5V supplies. The maximum voltage between the supply pins should be limited to less than 11V. Since a supply independent bias is used, very little change in AC performance is observed as the supply voltage is changed.

BASIC OP AMP CONNECTIONS

Figures 2 through 4 illustrate the basic op amp connections suitable for the OPA655. The non-inverting buffer (voltage follower) application (Figure 2) will benefit from the very

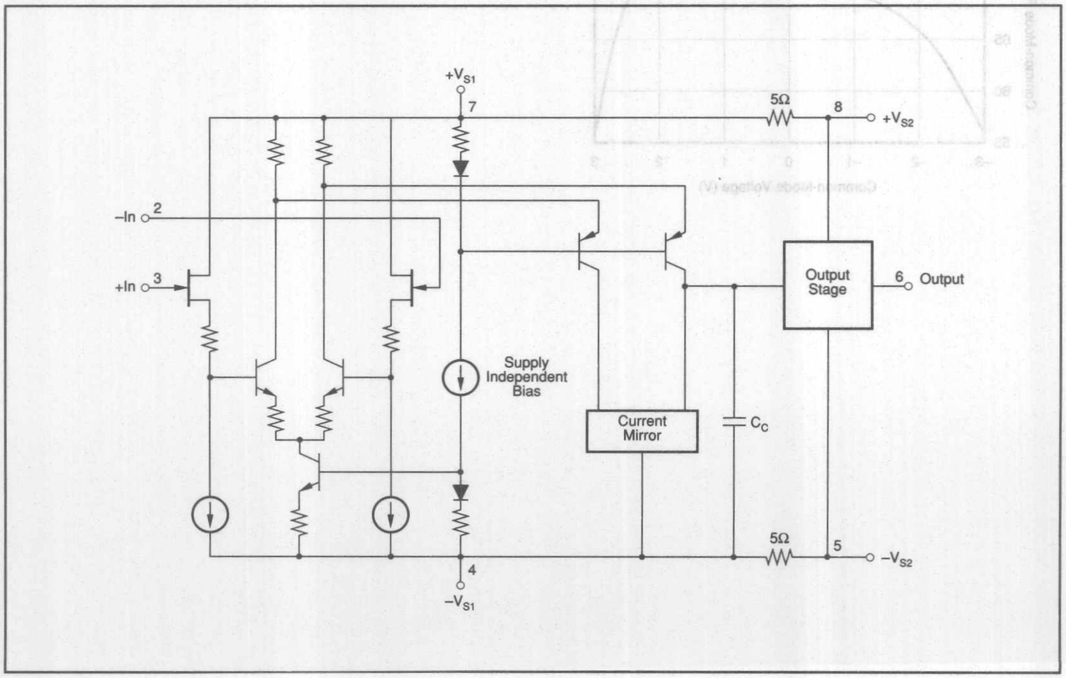


FIGURE 1. Simplified Internal Schematic.

high FET input impedance and low closed loop output impedance. Remember that a DC path to the input is still necessary; even with the ultra low FET input bias current (5pA), open or capacitively coupled sources will cause the input to saturate. For best frequency response, a direct short between the output and inverting inputs is suggested. Since the input bias currents are not necessarily correlated, matching the non-inverting source resistance with a resistor in the feedback network is not recommended.

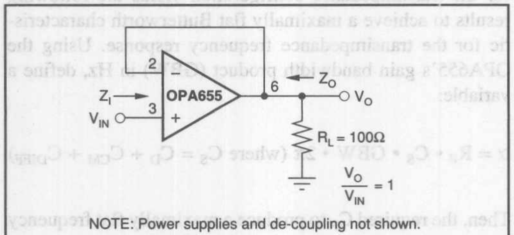


FIGURE 2. Non-Inverting Unity Gain Buffer.

The non-inverting amplifier configuration (Figure 3) will again present a very high input impedance to the input signal and a low output impedance drive with signal gain. The 100Ω shown for R_F will give the frequency response shown in the Typical Performance Curves. Higher values for R_F and R_1 are possible but for high frequency non-inverting op amp applications, should be limited to less than 1.0kΩ. The amplifier will be loaded by ($R_F + R_1$) in parallel with the load impedance.

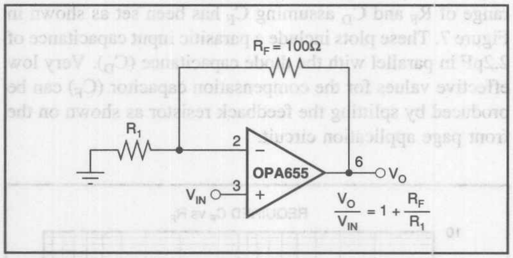


FIGURE 3. Non-Inverting Op Amp.

The inverting amplifier configuration (Figure 4) offers a broadband, low DC error amplifier with a controlled input impedance. The input impedance may be set by adjusting R_1 to the desired value and then adjusting R_F to the desired gain, or by setting R_F and R_1 to the desired values then controlling the input impedance independently as the parallel combination of R_1 and an optional R_T resistor to ground. To estimate the bandwidth in any configuration, first calculate the gain as a non-inverting amplifier. This is often referred to as "noise gain" or NG, and is simply the inverse of the feedback factor β.

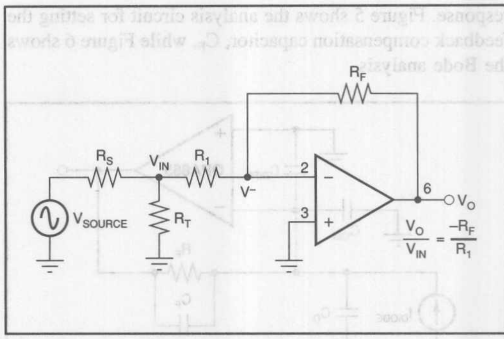


FIGURE 4. Inverting Op Amp.

$\beta = V^-/V_O$

Non-Inverting Gain = Noise Gain = NG = 1/β

Taking the inverting amplifier as an example, β is found by setting V_{SOURCE} to zero and calculating the voltage divider ratio from V_O to V^-:

$R_1 + R_T \parallel R_S$ = total resistance to ground on the inverting input

$$\beta = \frac{V^-}{V_O} = \frac{R_1 + R_T \| R_S}{R_F + R_1 + R_T \| R_S}$$

$$NG = \frac{1}{\beta} = 1 + \frac{R_F}{R_1 + R_T \| R_S}$$

The resulting bandwidth is approximately the amplifier's gain bandwidth product divided by the calculated noise gain:

$$BW \approx GBW/NG$$

In practice, low noise gains (< 5) will produce a wider bandwidth than predicted due to the peaking effect of second order poles. For example, at an inverting gain of –1 from a zero ohm source impedance, this yields a non-inverting gain of 2 and an approximate signal bandwidth of 185MHz.

TYPICAL APPLICATIONS

WIDEBAND TRANSIMPEDANCE AMPLIFIER

The high gain bandwidth product and low noise of the OPA655 make it particularly suitable for wideband transimpedance applications. The front page of the data sheet shows measured results for a 1MΩ transimpedance gain from a relatively large diode having 47pF parasitic capacitance. The key to broadband transimpedance applications is to set the compensation capacitance across the feedback resistor to achieve a flat, or bandlimited, frequency

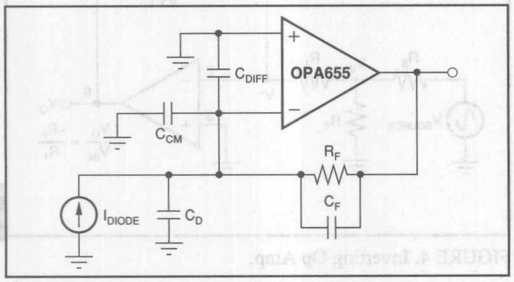


FIGURE 5. Transimpedance Analysis Circuit.

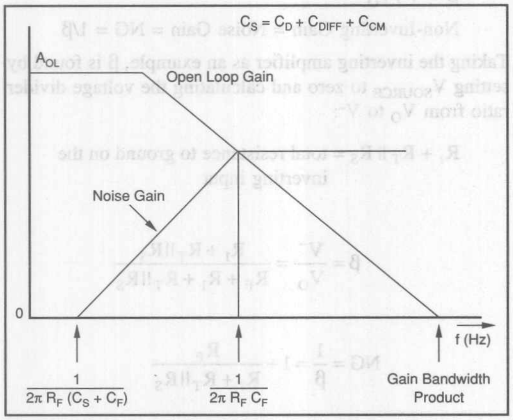


FIGURE 6. Bode Analysis for Transimpedance Circuit.

The total capacitance to ground on the inverting input of the OPA655 will set the source capacitance (C_S) for analysis purposes. C_S is the sum of the diode capacitance (C_D), the common mode input capacitance C_{CM} and the differential input capacitance (C_{DIFF}). Looking at the Bode analysis for the transimpedance configuration, at low frequencies the noise gain is 1 (0dB) but will increase for frequencies above $1/2\pi(R_F \bullet (C_S + C_F))$ due to the zero formed by the capacitance on the inverting node. It is important to note that the gain for the op amp input noise voltage will increase similarly. To get maximum bandwidth, C_F is often set to form a high frequency pole at the intersection of this increasing noise gain and the open loop gain rolloff. This is accomplished by setting $1/2\pi(R_F \bullet C_F)$ equal to the geometric mean of the zero frequency and the gain bandwidth product of the op amp. If the gain bandwidth product is in Hz, and assuming that $C_F << C_S$, C_F may be calculated as:

$$C_F = \frac{1}{\left[R_F \bullet \sqrt{\dfrac{(2\pi \bullet GBWP)}{(R_F \bullet C_S)}}\right]}$$

If the $1/2\pi R_F C_F$ pole for the noise gain were set exactly at the intersection with the amplifier's open loop gain rolloff, the circuit would be operating with a 45° phase margin yielding a highly peaked frequency response. To reduce broadband noise and pulse response ringing, it is preferable to set this pole at a slightly lower frequency than the simplified analysis shown above. A second order analysis for the transimpedance configuration yields the following results to achieve a maximally flat Butterworth characteristic for the transimpedance frequency response. Using the OPA655's gain bandwidth product (GBW) in Hz, define a variable:

$$\alpha = R_F \bullet C_S \bullet GBW \bullet 2\pi \text{ (where } C_S = C_D + C_{CM} + C_{DIFF})$$

Then, the required C_F to produce a maximally flat frequency response is:

$$C_F = C_S \bullet \frac{\sqrt{2\alpha - 1}}{\alpha} \approx C_S \sqrt{\frac{2}{\alpha}}$$

and the resulting –3dB bandwidth for the transimpedance gain will be:

$$F_{-3dB} = GBW \bullet \sqrt{\frac{2}{\alpha + \sqrt{2\alpha - 1}}}$$

Figure 7 plots the required C_F vs R_F (given different values for the diode capacitance) to achieve the maximally flat response. Figure 8 plots the resulting bandwidth for the same range of R_F and C_D assuming C_F has been set as shown in Figure 7. These plots include a parasitic input capacitance of 2.2pF in parallel with the diode capacitance (C_D). Very low effective values for the compensation capacitor (C_F) can be produced by splitting the feedback resistor as shown on the front page application circuit.

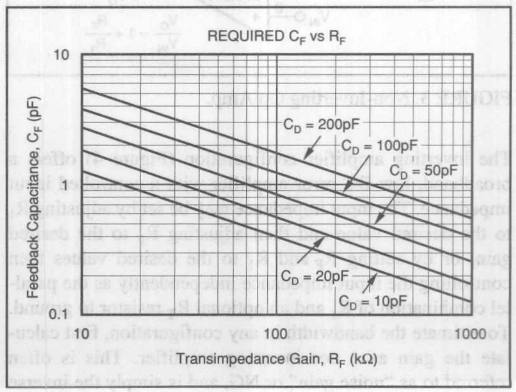


FIGURE 7. Compensation Capacitance vs Feedback Resistance.

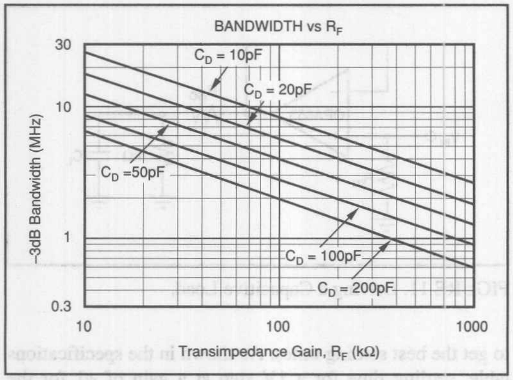


FIGURE 8. Maximally Flat Bandwidth.

HIGH SPEED INSTRUMENTATION DIFFERENTIAL AMPLIFIER

Very high speed differential amplifiers can be implemented using the OPA655. The very low input bias currents allow relatively high resistor values to be used in a standard single op amp differential configuration. Alternatively, a very high input impedance differential amplifier can be implemented using a three op amp instrumentation amplifier topology as shown in Figure 9.

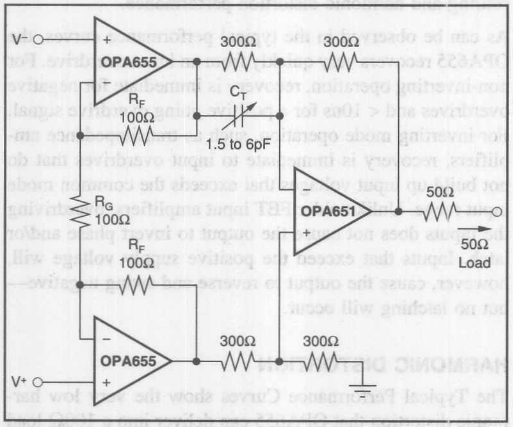


FIGURE 9. High Input Impedance, Broadband INA.

In this example, the OPA655's provide a differential gain of:

$$\left(1+\frac{2R_F}{R_G}\right)=3$$

and a common mode gain of 1 to the input of the OPA651 differential stage. The OPA651, a gain of 2 stable, broadband voltage feedback op amp, rejects the common mode signal and provides a differential gain of 1/2 the matched 50Ω load. This circuit delivers a 136MHz bandwidth at a differential gain of 1.5V/V (3.5dB) to the matched load as shown in Figure 10. The C_T tuning capacitor is used to match the high frequency gains for the two signal paths to improve the high frequency CMRR. Using this adjustment, a CMRR > 40dB through 100MHz was achieved.

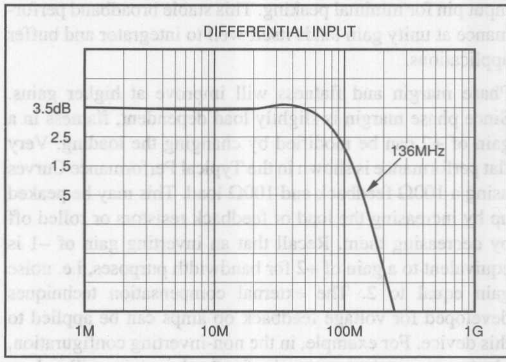


FIGURE 10. Measured Frequency Response for INA.

OPTIMIZING PERFORMANCE

DC ACCURACY

The OPA655 is laser trimmed for low input offset voltage, limiting the need for external trim circuits. In most cases, the low bias current of the FET input will not contribute significantly to the output DC error. For example, at minimum gain (G = +1) and maximum temperature (85°C), the error contribution due to the inverting input bias current would only exceed the input offset voltage for feedback resistors > (1mV/3.2nA) = 312kΩ. Only for relatively high source and/or feedback resistor values will the input bias current contribute significantly to the output DC error. Similarly, since the two input bias currents are very low, but not tightly matched, input bias current cancellation through source impedance matching is not recommended.

Changes in the power supply voltages contribute to shifts in the input offset voltage. This can be calculated using the PSR specifications. For example, a 0.5V change in the negative power supply will show up typically as a $0.5V \cdot 10^{(-65/20)} = 0.28mV$ change in the input offset voltage. Negative common mode voltage inputs can cause an increase in the input bias currents as shown in the Typical Performance Curves. This can have an effect on DC accuracy when the source and/or feedback resistors are large and the common mode input voltage approaches the negative limit of –2.5V. Positive input biases are therefore preferred for diode transimpedance applications requiring a bias voltage on the non-inverting op amp input.

FREQUENCY RESPONSE COMPENSATION

The OPA655 is internally compensated to be stable at unity gain into a 100Ω load with a nominal phase margin of 58°. This unity gain phase margin shows a slight peaking in the frequency response and requires a very low inductance shorting connection from the output pin to the inverting input pin for minimal peaking. This stable broadband performance at unity gain lends itself well to integrator and buffer applications.

Phase margin and flatness will improve at higher gains. Since phase margin is slightly load dependent, flatness in a gain of +2 can be modified by changing the loading. Very flat performance is shown in the Typical Performance Curves using a 100Ω feedback and 100Ω load. This may be peaked up by increasing the load or feedback resistors or rolled off by decreasing them. Recall that an inverting gain of –1 is equivalent to a gain of +2 for bandwidth purposes, i.e. noise gain equal to 2. The external compensation techniques developed for voltage feedback op amps can be applied to this device. For example, in the non-inverting configuration, placing a capacitor across the feedback resistor will reduce the gain to +1 starting at $f = 1/(2\pi R_F C_F)$ Hz. Alternatively, in the inverting configuration, the bandwidth may be limited without modifying the low frequency inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at higher frequencies, thereby limiting the bandwidth for the inverting input signal through the gain-bandwidth product.

At higher gains, the gain-bandwidth product (240MHz) of this voltage feedback topology will limit the achievable signal bandwidth. If FET input is not required and higher bandwidths at higher gains are needed, consider the broad bandwidth available from a current feedback op amp such as the OPA658.

DRIVING CAPACITIVE LOADS

The high open loop gain and Class AB output stage of the OPA655 are optimized for driving the low impedance of doubly terminated cables. Capacitive loads directly on the output pin can decrease phase margin leading to frequency response peaking and possibly sustained oscillations. This effect is particularly pronounced at unity gain and becomes less significant at higher gains. Frequency response flatness can be maintained into a capacitive load by isolating it with a resistor as shown in Figure 11. The Typical Performance Curves show a plot of the minimum value for R_{ISO} to hold a flat frequency response as C_L is increased. The 1kΩ shunt load across C_L shown in Figure 11 was the probe load for this measurement and should be considered optional.

PULSE AND OVERDRIVE PERFORMANCE

High speed amplifiers like the OPA655 can provide an extremely fast settling time for a pulse input. Excellent frequency response flatness and phase linearity are required

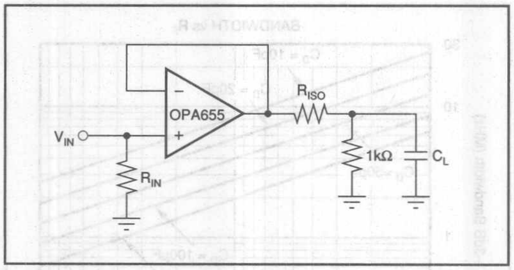


FIGURE 11. Driving a Capacitive Load.

to get the best settling times. As shown in the specifications table, settling time for a 1V step at a gain of +1 for the OPA655 is an extremely fast 8ns to 0.1%. This specification is defined as the time required, after the input transition, for the output to settle within a specified error band around its final value. For a 1V step, 0.1% settling corresponds to an error band of ±1mV. For the best settling times, little or no peaking in the frequency response can be allowed. Using the recommended R_{ISO} for capacitive loads will limit this peaking and reduce the settling times. Fast, extremely fine scale settling (0.01%) requires close attention to the ground return currents in the supply de-coupling capacitors. De-coupling the output stage power supply connections ($+V_{S2}$ + ($-V_{S2}$)) separately from the main supply inputs will improve both settling and harmonic distortion performance.

As can be observed in the typical performance curves, the OPA655 recovers very quickly from an input overdrive. For non-inverting operation, recovery is immediate for negative overdrives and < 10ns for a positive going overdrive signal. For inverting mode operation, such as transimpedance amplifiers, recovery is immediate to input overdrives that do not build up input voltages that exceeds the common mode input range. Unlike older FET input amplifiers, overdriving the inputs does not cause the output to invert phase and/or latch. Inputs that exceed the positive supply voltage will, however, cause the output to reverse and swing negative—but no latching will occur.

HARMONIC DISTORTION

The Typical Performance Curves show the very low harmonic distortion that OPA655 can deliver into a 100Ω load over a wide range of operating conditions. Generally, distortion improves at lower gains, lower signal swings, lower frequencies, and higher loads. Figure 12 shows significant improvement in second harmonic distortion as the load is increased, and relative insensitivity of the third harmonic to load conditions. For measurement purposes, these distortion levels were increased from those listed in the specification table by increasing the gain to +5. Narrowband communications systems will benefit from the very low third order distortion vs load which will provide very low intermodulation spurs.

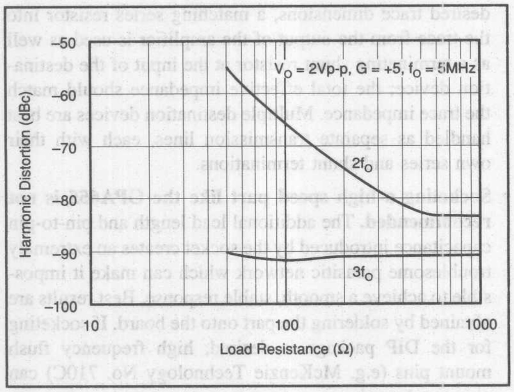


FIGURE 12. 5MHz Harmonic Distortion vs Load Resistance.

DIFFERENTIAL GAIN AND DIFFERENTIAL PHASE

The OPA655 provides one of the lowest dG/dP errors of any op amp. This specification is the change in the small signal gain and phase for a composite video color carrier frequency when the output voltage is slowly ramped over the luminance range. The specifications show less than 0.01%/0.01° for positive NTSC into a single video load. This level of performance challenges the accuracy of commercially available video test equipment. Measurements were taken using an HP9480 IC parametric test system.

OUTPUT DRIVE CAPABILITY

The guaranteed output current of ±28mA will drive a 100Ω load over the full guaranteed output voltage range of ±2.8V. These minimum performance levels are only applicable at cold temperatures, with higher output voltage and current available in most applications. Many demanding high speed applications, such as driving ADC's, require amplifiers with low, broadband, output impedance. As shown in Figure 13, the OPA655 maintains a very low closed loop output impedance over frequency. Closed loop output impedance increases with frequency as the loop gain rolls off.

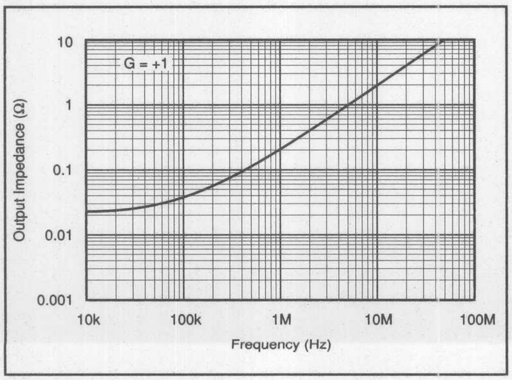


FIGURE 13. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA655 will not require heatsinking under most operating conditions. Maximum desired junction temperature will limit the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is a combination of the quiescent power plus the power dissipated in the output stage to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is a fixed DC voltage equal to 1/2 of either supply voltage (assuming equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading. Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation. As an example, compute the maximum T_J for the OPA655U at G = +2, R_L = 100Ω, R_F = 100Ω, $\pm V_S$ = ±5V, and at the specified maximum T_A = 85°C. P_D = 10V • 31mA + (5²)/[4 • (100 ∥ 200)] = 404mW. Maximum T_J = 85°C + 0.404W • 125°C/W = 136°C.

LAYOUT AND INTERCONNECT CONSIDERATIONS

Achieving optimum performance with a high frequency amplifier like the OPA655 requires careful attention to layout parasitics and selection of external components. Suggestions include:

- **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- **Minimize the distance** (< 0.25") from the four power pins to high frequency 0.1µF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. The OPA655 may be operated with only pins 4 and 7 connected as supply pins allowing a direct replacement into existing 8 pin op amp pinouts. Connecting the output stage power pins separately, and decoupling them, will give the best distortion and settling performance. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

OPA655

2

OPERATIONAL AMPLIFIERS

type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in the signal path for a high frequency application. For the lowest parasitic capacitance, consider the PR8351 style resistor from Precision Resistive Products (Phone No. 319-394-9131). These precision buffed resistors typically have less than 0.02pF shunt parasitic capacitance.

Since the output pin and inverting input pin are most sensitive to parasitic capacitance, always place the feedback, gain setting, and series output resistor (if any) as close as possible to the package pins. For a voltage follower buffer application, a wide trace (0.1") on the component side of the board between pins 6 and 2 will reduce frequency response peaking. Be sure to open up ground and power planes around this trace to limit parasitic capacitance to an AC ground on the output pin.

- **Connections to other wideband devices** on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA655 is nominally compensated to operate with a 5pF parasitic load.

  If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and tion device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

- **Socketing a high speed part like the OPA655 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g. McKenzie Technology No. 710C) can give good results.

SPICE MODEL AND EVALUATION BOARDS

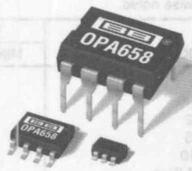
Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available on a disk from the Burr-Brown Applications Department.

The OPA655 is similar in distortion performance and identical in pinout to the OPA642. The demonstration boards developed for the OPA642 are recommended for the OPA655. The six boards available are:

Contact your local Burr-Brown sales office or distributor to order demonstration boards.

DEM-OPA64XP-F	8-pin DIP, unity gain follower configuration
DEM-OPA64XP-N	8-pin DIP, non-inverting gain configuration
DEM-OPA64XP-I	8-pin DIP, inverting gain configuration
DEM-OPA64XU-F	SO-8 Surface Mount, unity gain follower configuration
DEM-OPA64XU-N	SO-8 Surface Mount, non-inverting gain configuration
DEM-OPA64XU-I	SO-8 Surface Mount, inverting gain configuration

BURR - BROWN®



OPA658

Wideband, Low Power Current Feedback OPERATIONAL AMPLIFIER

FEATURES

- UNITY GAIN STABLE BANDWIDTH: 900MHz
- LOW POWER: 50mW
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.025%/0.02°
- HIGH SLEW RATE: 1700V/µs
- GAIN FLATNESS: 0.1dB to 135MHz
- HIGH OUTPUT CURRENT (80mA)

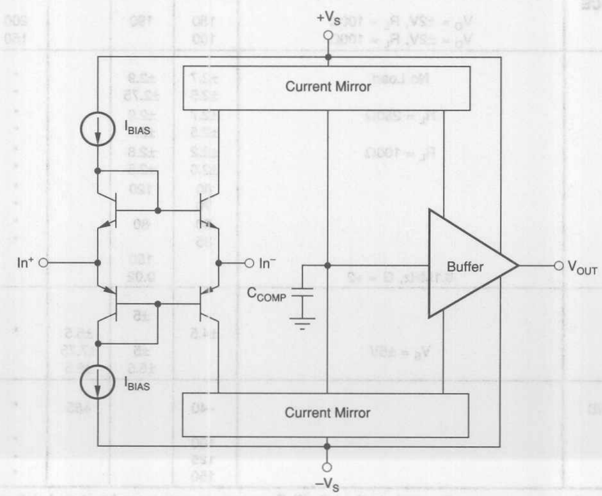
APPLICATIONS

- MEDICAL IMAGING
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- COMMUNICATIONS
- PULSE AMPLIFIERS
- ADC/DAC GAIN AMPLIFIER
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER

DESCRIPTION

The OPA658 is an ultra-wideband, low power current feedback video operational amplifier featuring high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low quiescent current make the OPA658 a perfect choice for numerous video, imaging and communications applications.

The OPA658 is optimized for low gain operation and is also available in dual (OPA2658) and quad (OPA4658) configurations.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted.

PARAMETER	CONDITION	OPA658P, U, N MIN	OPA658P, U, N TYP	OPA658P, U, N MAX	OPA658PB, UB, NB MIN	OPA658PB, UB, NB TYP	OPA658PB, UB, NB MAX	UNITS
FREQUENCY RESPONSE								
Closed-Loop Bandwidth(2)	G = +1(4)		900			*(1)		MHz
	G = +2		680		400	*		MHz
	G = +5		370			*		MHz
	G = +10		200			*		MHz
Slew Rate(3)	G = +2, 2V Step		1700		1000	*		V/µs
At Minimum Specified Temperature			1500		900	*		V/µs
Settling Time: 0.01%	G = +2, 2V Step		15			*		ns
0.1%	G = +2, 2V Step		11.5			*		ns
1%	G = +2, 2V Step		6			*		ns
Spurious Free Dynamic Range	f = 5MHz, G = +2, V_O = 2Vp-p		68			*		dBc
	f = 20MHz, G= +2, V_O = 2Vp-p		56			*		dBc
Third Order Intercept Point	f = 10MHz, 4dBm Each Tone		40			*		dBm
Differential Gain	G = +2, NTSC, V_O = 1.4Vp-p, R_L = 150Ω		0.025			*		%
Differential Phase	G = +2, NTSC, V_O = 1.4Vp-p, R_L = 150Ω		0.02			*		degrees
Bandwidth for 0.1dB Flatness	G = +2		135(5)			*		MHz
OFFSET VOLTAGE								
Input Offset Voltage	V_{CM} = 0V		±3	±5.5		±2	±4.5	mV
Over Temperature Range			±5	±8		±4	±7	mV
Power Supply Rejection Ratio	V_S = ±4.7 to ±5.5V	55	64		58	67		dB
INPUT BIAS CURRENT								
Non-Inverting	V_{CM} = 0V		±5.7	±30		*	±18	µA
Over Temperature Range			±10	±80		*	±35	µA
Inverting	V_{CM} = 0V		±1.1	±35		*	*	µA
Over Temperature Range			±30	±75		*	*	µA
NOISE								
Input Voltage Noise Density								
f = 100Hz			11			*		nV/√Hz
f = 2kHz			3.3			*		nV/√Hz
f = 10kHz			2.7			*		nV/√Hz
f = 1MHz			2.7			*		nV/√Hz
f_B = 100Hz to 200MHz			38.2			*		µVrms
Input Bias Current Noise Density								
Inverting: f = 10MHz			12.6			*		pA/√Hz
Non-Inverting: f = 10MHz			12.6			*		pA/√Hz
Noise Figure (NF)	R_S = 50Ω		10			*		dB
	R_S = 100Ω		8			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range								
Over Temperature Range		±2.5	±2.9		*	*		V
Common-Mode Rejection	V_{CM} = ±1V	45	50		*	*		dB
INPUT IMPEDANCE								
Non-Inverting			500 || 1			*		kΩ || pF
Inverting			50			*		Ω
OPEN-LOOP TRANSRESISTANCE								
Open-Loop Transresistance	V_O = ±2V, R_L = 100Ω	150	190		200	250		kΩ
Over Temperature Range	V_O = ±2V, R_L = 100Ω	100			150			kΩ
OUTPUT								
Voltage Output	No Load	±2.7	±2.9		*	*		V
Over Temperature Range		±2.5	±2.75		*	*		V
Voltage Output	R_L = 250Ω	±2.7	±2.9		*	*		V
Over Temperature Range		±2.5	±2.7		*	*		V
Voltage Output	R_L = 100Ω	±2.2	±2.8		*	*		V
Over Temperature Range		±2.0	±2.5		*	*		V
Output Current, Sourcing		80	120		*	*		mA
Over Temperature		70			*			mA
Output Current, Sinking		60	80		*	*		mA
Over Temperature		35			*			mA
Short Circuit Current			150			*		mA
Output Resistance	0.1MHz, G = +2		0.02			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Operating Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current	V_S = ±5V		±5	±7.75		±4.5	±5.75	mA
Over Temperature Range			±5.5	±8.5		±4.7	±6.5	mA
TEMPERATURE RANGE								
Specification: P, U, N, PB, UB, NB		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
P 8-Pin DIP		100			*		°C/W	
U SO-8		125			*		°C/W	
N SOT23-5		150			*		°C/W	

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The demonstration board, DEM-OPA65X shows a low parasitic layout for this part. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step. (4) At G = +1, R_{FB} = 560Ω for PDIP and 402Ω for SO-8. (5) This specification is PC board layout dependent.

ABSOLUTE MAXIMUM RATINGS

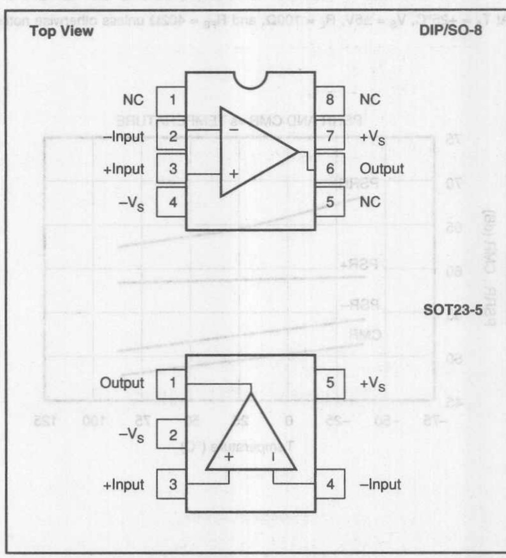
Supply	±5.5V
Internal Power Dissipation	See Thermal Considerations
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION



PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE	PACKAGE MARKING(2)	ORDERING NUMBER
OPA658U	SO-8 Surface Mount	182	–40°C to +85°C	OPA658U	OPA658U
OPA658UB	SO-8 Surface Mount	182	–40°C to +85°C	OPA658UB	OPA658UB
OPA658P	8-Pin Plastic DIP	006	–40°C to +85°C	OPA658P	OPA658P
OPA658PB	8-Pin Plastic DIP	006	–40°C to +85°C	OPA658PB	OPA658PB

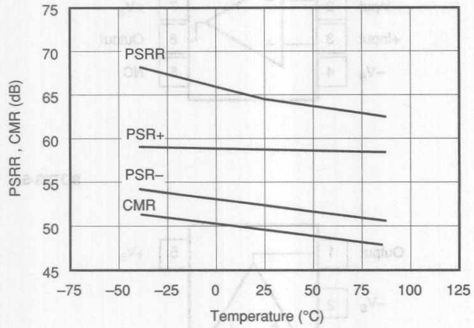
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 and DIP packages will be marked with a "B" by pin 8.

ADVANCE PACKAGE INFORMATION(2)

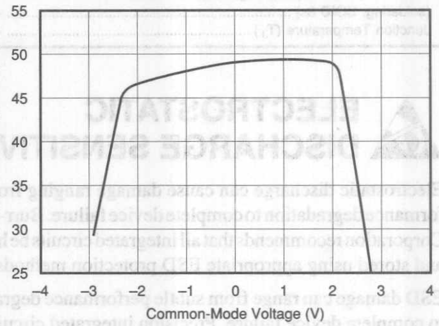
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER
OPA658N	5-Pin SOT23-5	331	–40°C to +85°C	—	—
OPA658NB	5-Pin SOT23-5	331	–40°C to +85°C	—	—

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The SOT23-5 will be available in tape and reel only by August, 1996.

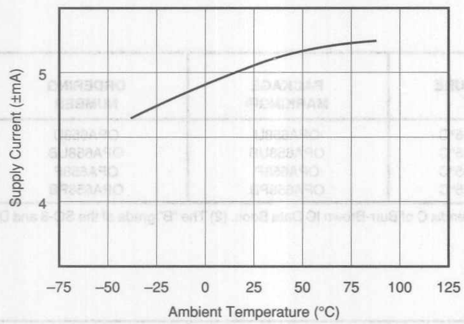
PSRR AND CMR vs TEMPERATURE



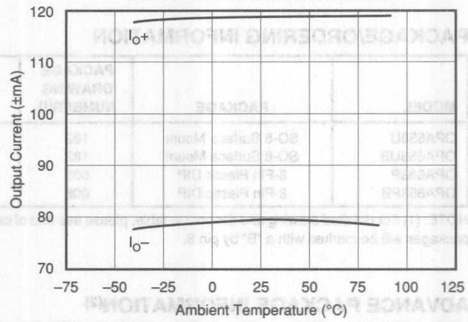
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



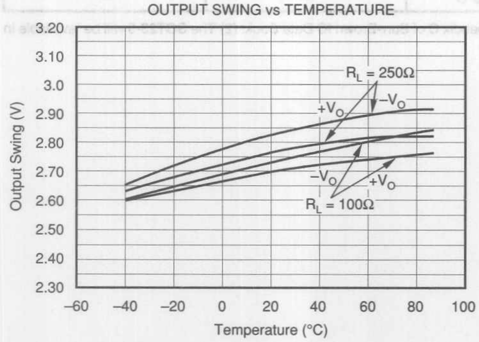
SUPPLY CURRENT vs TEMPERATURE



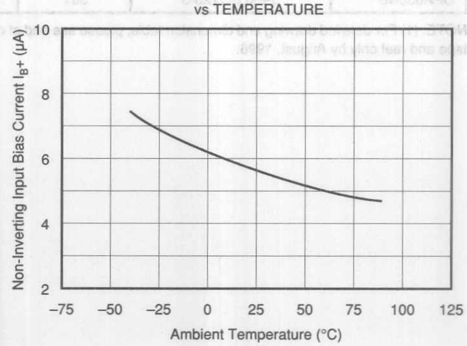
OUTPUT CURRENT vs TEMPERATURE



OUTPUT SWING vs TEMPERATURE



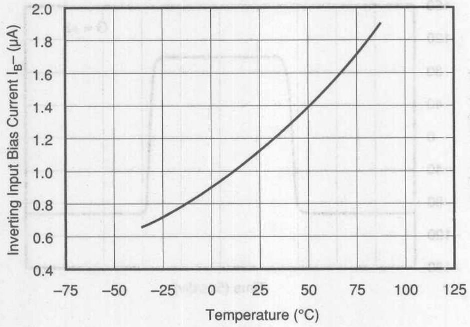
NON-INVERTING INPUT BIAS CURRENT vs TEMPERATURE



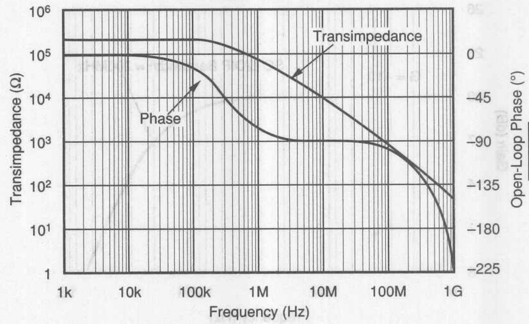
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted.

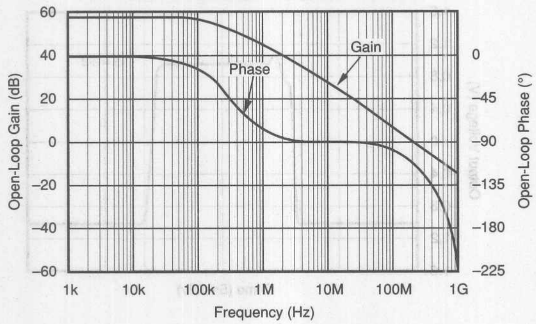
INVERTING INPUT BIAS CURRENT vs TEMPERATURE



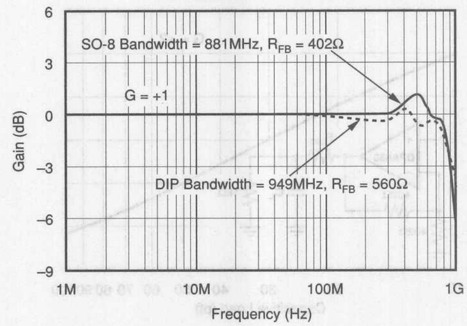
OPEN-LOOP TRANSIMPEDANCE AND PHASE vs FREQUENCY



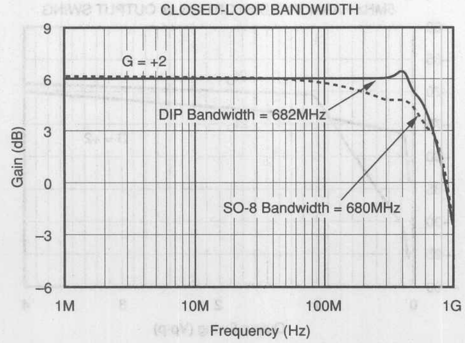
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



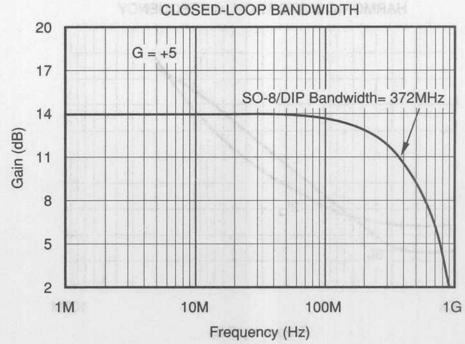
CLOSED-LOOP BANDWIDTH



CLOSED-LOOP BANDWIDTH



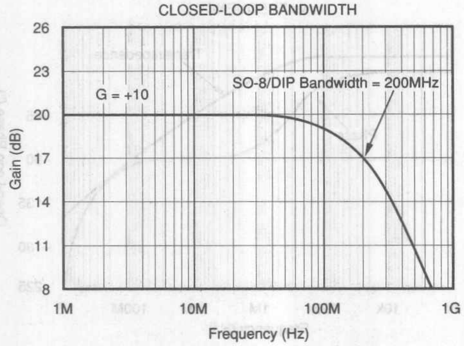
CLOSED-LOOP BANDWIDTH



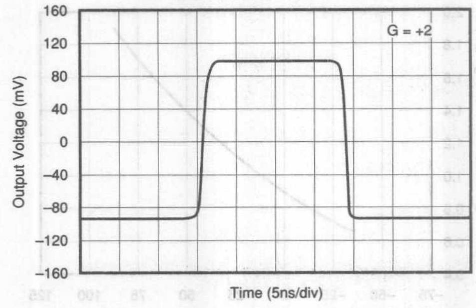
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted.

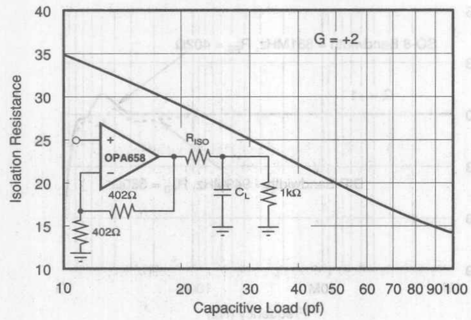
CLOSED-LOOP BANDWIDTH



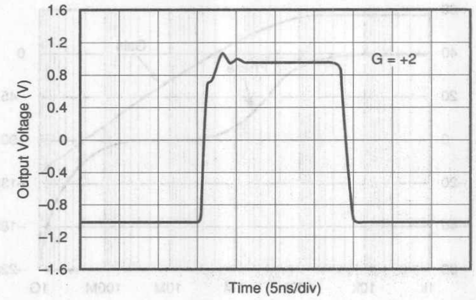
SMALL SIGNAL TRANSIENT RESPONSE



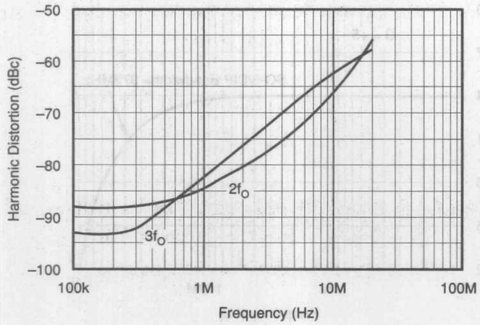
RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD



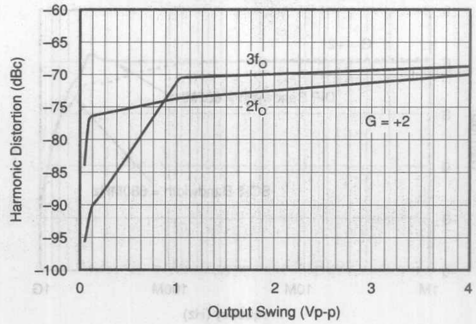
LARGE SIGNAL TRANSIENT RESPONSE



HARMONIC DISTORTION vs FREQUENCY



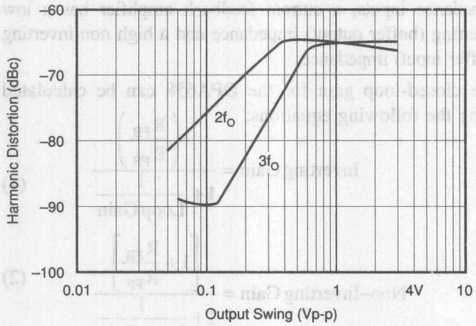
5MHz HARMONIC DISTORTION vs OUTPUT SWING



TYPICAL PERFORMANCE CURVES (CONT)

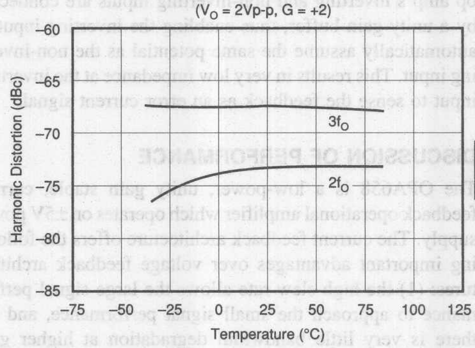
At $T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted.

10MHz HARMONIC DISTORTION vs OUTPUT SWING



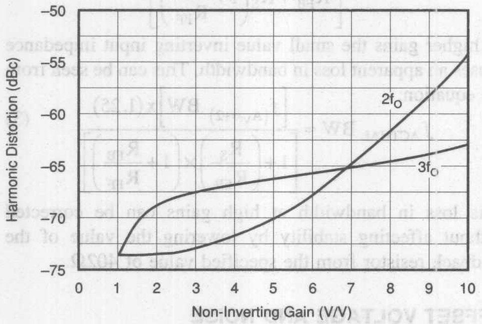
HARMONIC DISTORTION vs TEMPERATURE

(V_O = 2Vp-p, G = +2)



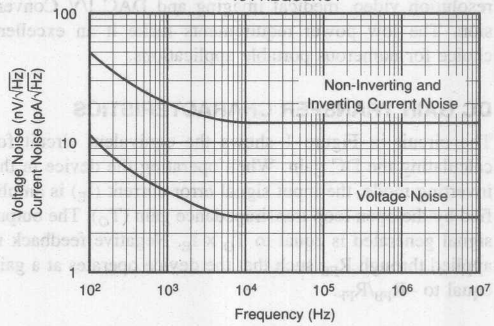
HARMONIC DISTORTION vs GAIN

(f_O = 5MHz, V_O = 2Vp-p)



INPUT VOLTAGE AND CURRENT NOISE

vs FREQUENCY



Conventional op amps depend on feedback to drive their inputs to the same potential, however the current feedback op amp's inverting and non-inverting inputs are connected by a unity gain buffer, thus enabling the inverting input to automatically assume the same potential as the non-inverting input. This results in very low impedance at the inverting input to sense the feedback as an error current signal.

DISCUSSION OF PERFORMANCE

The OPA658 is a low-power, unity gain stable, current feedback operational amplifier which operates on ±5V power supply. The current feedback architecture offers the following important advantages over voltage feedback architectures: (1) the high slew rate allows the large signal performance to approach the small signal performance, and (2) there is very little bandwidth degradation at higher gain settings.

The current feedback architecture of the OPA658 provides the traditional strength of excellent large signal response plus wide bandwidth, making it a good choice for use in high resolution video, medical imaging and DAC I/V Conversion. The low power requirements make it an excellent choice for numerous portable applications.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output signal generated is equal to T_O X I_E. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

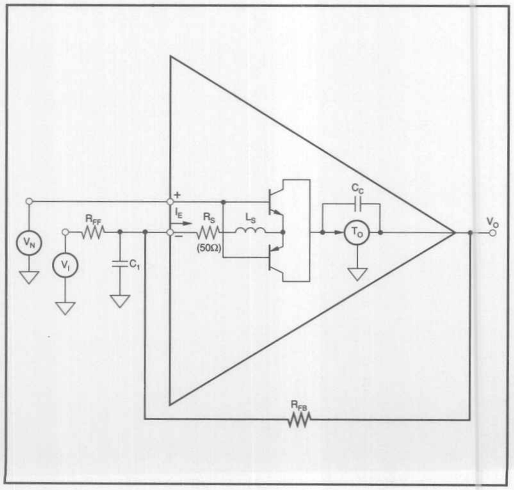


FIGURE 1. Equivalent Circuit.

(buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the overall gain is $(1 + R_{FB}/R_{FF})$. Where a voltage-feedback amplifier has two symmetrical high impedance inputs, a current feedback amplifier has a low inverting (buffer output) impedance and a high non-inverting (buffer input) impedance.

The closed-loop gain for the OPA658 can be calculated using the following equations:

$$\text{Inverting Gain} = \frac{-\left(\dfrac{R_{FB}}{R_{FF}}\right)}{1+\dfrac{1}{\text{Loop Gain}}} \quad (1)$$

$$\text{Non–Inverting Gain} = \frac{\left[1+\dfrac{R_{FB}}{R_{FF}}\right]}{1+\dfrac{1}{\text{Loop Gain}}} \quad (2)$$

$$\text{where Loop Gain} = \left[\frac{T_O}{R_{FB}+R_S\left(1+\dfrac{R_{FB}}{R_{FF}}\right)}\right]$$

At higher gains the small value inverting input impedance causes an apparent loss in bandwidth. This can be seen from the equation:

$$f_{ACTUAL}\ BW \approx \frac{\left[f_{(A_V=+2)}\ BW\right] x (1.25)}{\left[1+\left(\dfrac{R_S}{R_{FB}}\right)\times\left(1+\dfrac{R_{FB}}{R_{FF}}\right)\right]} \quad (3)$$

This loss in bandwidth at high gains can be corrected without affecting stability by lowering the value of the feedback resistor from the specified value of 402Ω.

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the input offset voltage and bias current errors. The output offset for non-inverting operation is calculated by the following equation:

$$\text{Output Offset Voltage} = \pm Ib_N \times R_N\left(1+\frac{R_{FB}}{R_{FF}}\right) \pm V_{IO}\left(1+\frac{R_{FB}}{R_{FF}}\right) \pm Ib_I \times R_{FB} \quad (4)$$

If all terms are divided by the gain $(1 + R_{FB}/R_{FF})$ it can be observed that input referred offsets improve as gain increases. The effective noise at the output can be determined by taking

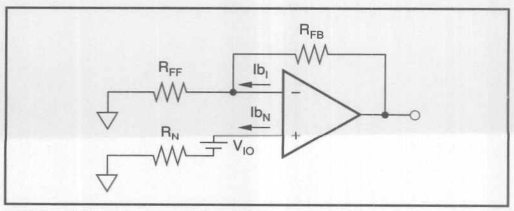


FIGURE 2. Output Offset Voltage Equivalent Circuit.

spectral noise values found in the Typical Performance Curve graph section. This applies to noise from the op amp only. Note that both the noise figure (NF) and the equivalent input offset voltages improve as the closed loop gain increases (by keeping R_{FB} fixed and reducing R_{FF} with $R_N = 0\Omega$).

INCREASING BANDWIDTH AT HIGH GAINS

The closed-loop bandwidth can be extended at high gains by reducing the value of the feedback resistor R_{FB}. This bandwidth reduction is caused by the feedback current being split between R_S and R_{FF} (refer to Figure 1). As the gain increases (for a fixed R_{FB}), more feedback current is shunted through R_{FF}, which reduces closed-loop bandwidth.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA658 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the two power pins to high frequency 0.1µF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA658. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Other network components, such as non-inverting input termination resistors, should also be placed close to the package.

The feedback resistor value acts as the frequency response compensation element for a current feedback type amplifier. The recommended feedback resistor values are chosen to give a nominal maximally flat butterworth response while assuming a 2pF output pin parasitic. Increasing the feedback resistor will over compensate the amplifier, rolling off the frequency response, while decreasing it will decrease phase margin, peaking up the frequency response. Note that a non-inverting, unity gain buffer application still requires a feedback resistor for stability (560Ω for SO-8 and 402Ω for PDIP).

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA658 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) Socketing a high speed part like the OPA658 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

The OPA658 is nominally specified for operation using ±5V power supplies. A 10% tolerance on the supplies, or an ECL –5.2V for the negative supply, is within the maximum

specified total supply voltage of 11V. Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single supply operation. Figure 3 shows one approach to single-supply operation.

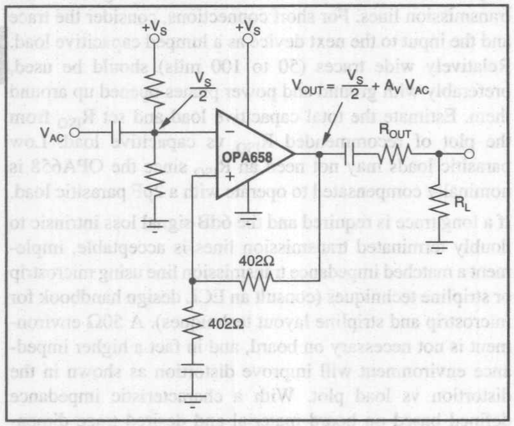


FIGURE 3. Single Supply Operation.

ESD PROTECTION

ESD static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA658.

OUTPUT DRIVE CAPABILITY

The OPA658 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA658 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 4, the OPA658 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

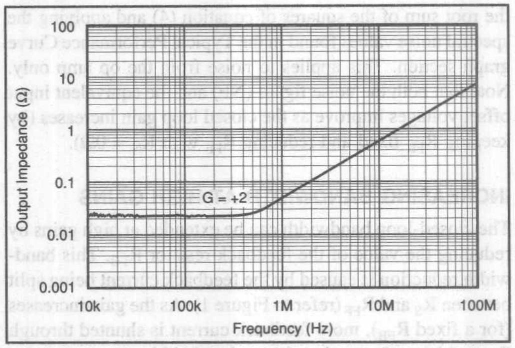


FIGURE 4. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA658 will not require heatsinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As an example, compute the maximum T_J for an OPA658N at $A_V = +2$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, $\pm V_S = \pm 5V$, and the specified maximum $T_A = +85°C$. $P_D = 10V \bullet 8.5mA + 5^2/[4 \bullet (100\Omega \parallel 804\Omega)] = 155mW$. Maximum $T_J = 85°C + 0.155W \bullet 150°C/W = 108°C$.

DRIVING CAPACITIVE LOADS

The OPA658's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 10Ω to 35Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated with its characteristic impedance.

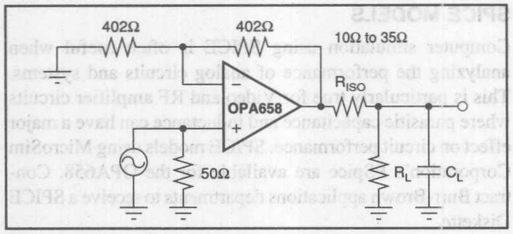


FIGURE 5. Driving Capacitive Loads.

COMPENSATION

The OPA658 is internally compensated and is stable in unity gain with a phase margin of approximately 62°, and approximately 64° in a gain of +2V/V when used with the recommended feedback resistor value. Frequency response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA658 in a good layout is very flat with frequency.

DISTORTION

The OPA658's Harmonic Distortion characteristics into a 100Ω load are shown versus frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

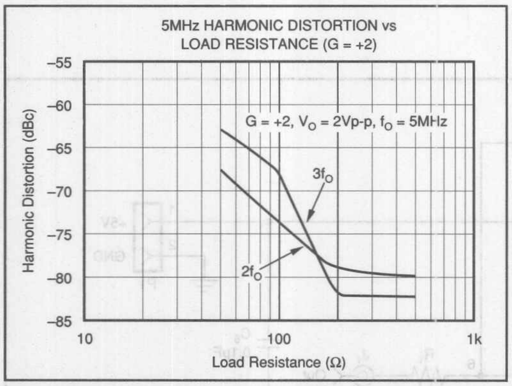


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

Narrowband communication channel requirements will benefit from the OPA658's wide bandwidth and low intermodulation distortion on low quiescent power. If output signal power at two closely spaced frequencies is required, third-order nonlinearities in any amplifier will cause spurious power at frequencies very near the two fundamental frequencies. If the two test frequencies, f_1 and f_2, are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $\Delta f = |f_2 - f_1|$, the two, third-order, close-in spurious tones will appear at $f_O \pm 3 \bullet \Delta f$. The two tone, third-order spurious plot shown in Figure 7 indicates how far below these two equal power, closely spaced, tones the intermodulation spurious will be. The single tone power is at a matched 50Ω load. The unique design of the OPA658 provides much greater spurious free range than what a two-tone third-order intermodulation intercept specification would predict. This can be seen in Figure 7 as the spurious free range actually increases at the higher output power levels.

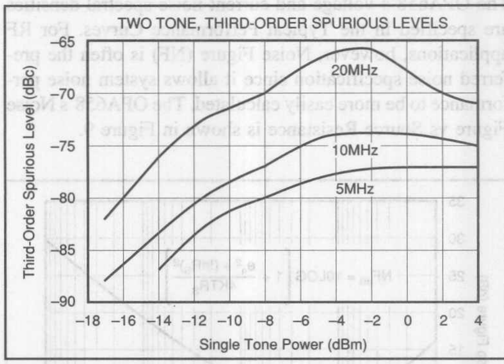


FIGURE 7. Third-Order Intercept Point vs Frequency.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (dG) and Differential Phase (dP) are among the more important specifications for video applications. dG is defined as the percent change in closed-loop gain over a specified change in output voltage level. dP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both dG and dP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL sub-carrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

dG/dP of the OPA658 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 8 delivered a 100IRE modulated ramp to the 75Ω input of the videoanalyzer. The signal averaging feature of the analyzer

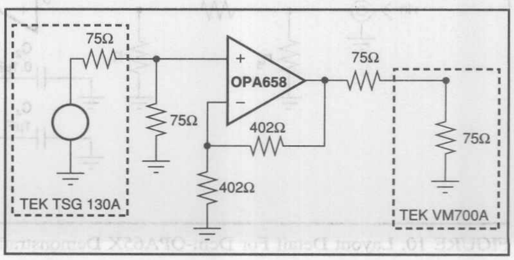


FIGURE 8. Configuration for Testing Differential Gain/Phase.

to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA658 is 0.025% differential gain and 0.02° differential phase to both NTSC and PAL standards.

NOISE FIGURE

The OPA658's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA658's Noise Figure vs Source Resistance is shown in Figure 9.

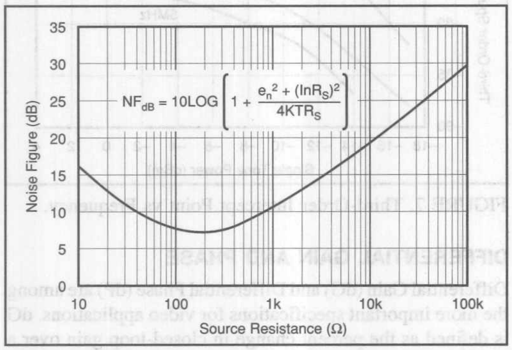


FIGURE 9. Noise Figure vs Source Resistance.

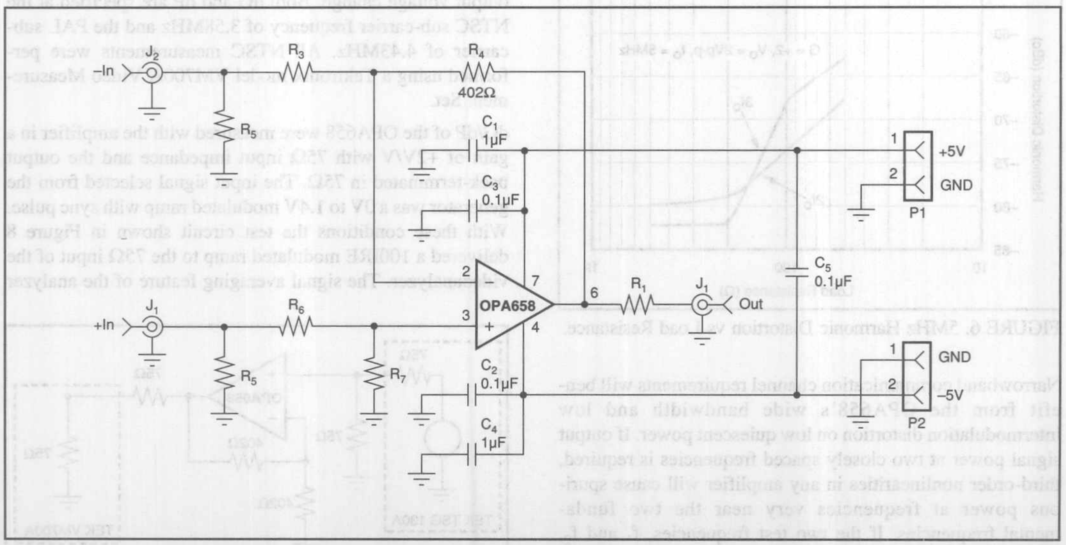


FIGURE 10. Layout Detail For Dem-OPA65X Demonstration Board.

analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA658. Contract Burr-Brown applications departments to receive a SPICE Diskette.

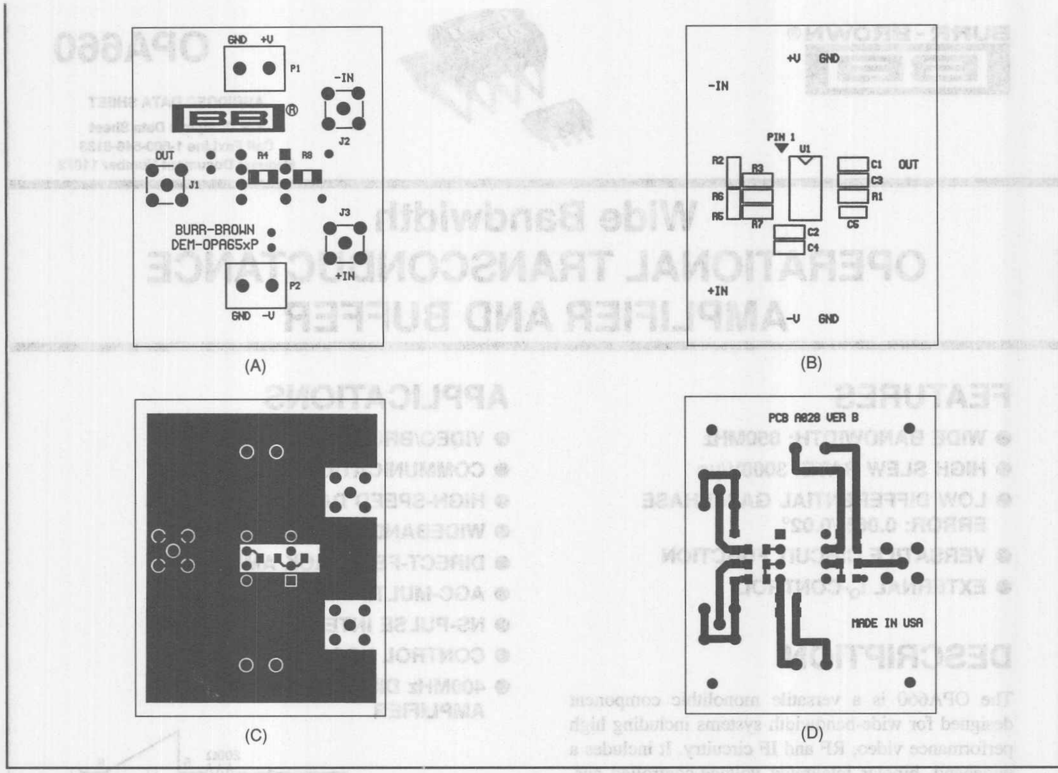


FIGURE 11a. Evaluation Board Silkscreen (Bottom). 11b. Evaluation Board Silkscreen (Top). 11c. Evaluation Board Layout (Solder Side). 11d. Evaluation Board Layout (Layout Side).

TYPICAL APPLICATION

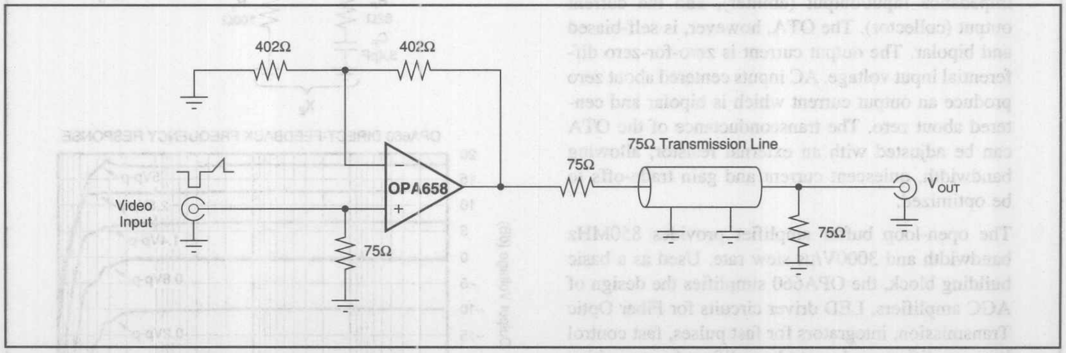
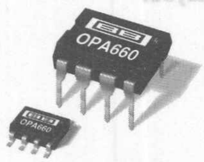


FIGURE 12. Low Distortion Video Amplifier.

BURR-BROWN®



OPA660

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11072

Wide Bandwidth OPERATIONAL TRANSCONDUCTANCE AMPLIFIER AND BUFFER

FEATURES

- WIDE BANDWIDTH: 850MHz
- HIGH SLEW RATE: 3000V/µs
- LOW DIFFERENTIAL GAIN/PHASE ERROR: 0.06%/0.02°
- VERSATILE CIRCUIT FUNCTION
- EXTERNAL I_Q-CONTROL

APPLICATIONS

- VIDEO/BROADCAST EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION
- WIDEBAND LED DRIVER
- DIRECT-FEEDBACK AMPLIFIER
- AGC-MULTIPLIER
- NS-PULSE INTEGRATOR
- CONTROL LOOP AMPLIFIER
- 400MHz DIFFERENTIAL INPUT AMPLIFIER

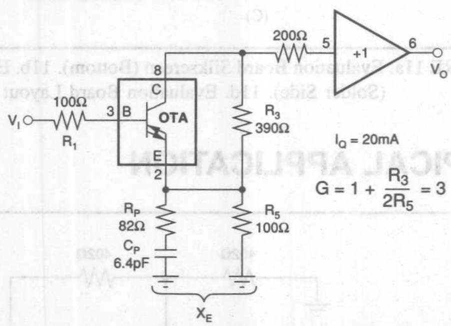
DESCRIPTION

The OPA660 is a versatile monolithic component designed for wide-bandwidth systems including high performance video, RF and IF circuitry. It includes a wideband, bipolar integrated voltage-controlled current source and voltage buffer amplifier.

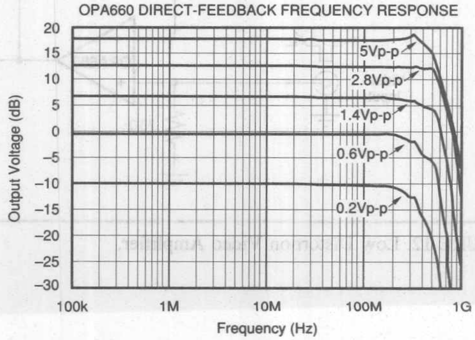
The voltage-controlled current source or Operational Transconductance Amplifier (OTA) can be viewed as an "ideal transistor." Like a transistor, it has three terminals—a high-impedance input (base), a low-impedance input/output (emitter), and the current output (collector). The OTA, however, is self-biased and bipolar. The output current is zero-for-zero differential input voltage. AC inputs centered about zero produce an output current which is bipolar and centered about zero. The transconductance of the OTA can be adjusted with an external resistor, allowing bandwidth, quiescent current and gain trade-offs to be optimized.

The open-loop buffer amplifier provides 850MHz bandwidth and 3000V/µs slew rate. Used as a basic building block, the OPA660 simplifies the design of AGC amplifiers, LED driver circuits for Fiber Optic Transmission, integrators for fast pulses, fast control loop amplifiers, and control amplifiers for capacitive sensors and active filters.

The OPA660 is packaged in SO-8 surface-mount, and 8-pin plastic DIP, specified from –40°C to +85°C.



OPA660 DIRECT-FEEDBACK FREQUENCY RESPONSE



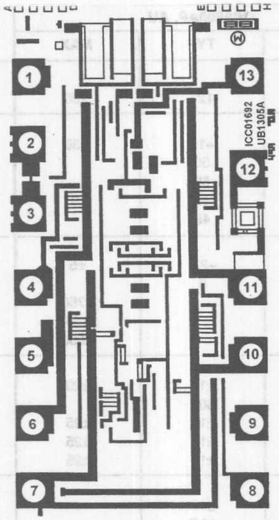
International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1072E

SPECIFICATIONS

Typical at I_Q = 20mA, V_S = ±5V, T_A = +25°C, and R_L = 500Ω unless otherwise specified.

PARAMETER	CONDITIONS	OPA660AP, AU MIN	TYP	MAX	UNITS
OTA TRANSCONDUCTANCE					
Transconductance	V_C = 0V	75	125	200	mA/V
OTA INPUT OFFSET VOLTAGE	V_B = 0				
Initial			+10	±30	mV
vs Temperature			50		µV/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V	55	60		dB
vs Supply (non-tracking)	V+ = 4.5V to 5.5V	40	45		dB
vs Supply (non-tracking)	V– = –4.5V to –5.5V	40	48		dB
OTA B-INPUT BIAS CURRENT					
Initial			–2.1	±5	µA
vs Temperature			5		nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V			±750	nA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V			±1500	nA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V			±500	nA/V
OTA OUTPUT BIAS CURRENT					
Output Bias Current	V_B = 0, V_C = 0V		±10	±20	µA
vs Temperature			500		nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V		±10	±25	µA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V		±10	±25	µA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V		±10	±25	µA/V
OTA OUTPUT					
Output Current		±10	±15		mA
Output Voltage Compliance	I_C = ±1mA	±4.0	±4.7		V
Output Impedance			25k || 4.2		Ω || pF
Open-Loop Gain	f = 1kHz		70		dB
BUFFER OFFSET VOLTAGE					
Initial			+7	±30	mV
vs Temperature			50		µV/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V	55	60		dB
vs Supply (non-tracking)	V+ = 4.5V to 5.5V	40	45		dB
vs Supply (non-tracking)	V– = –4.5V to –5.5V	40	48		dB
BUFFER INPUT BIAS CURRENT					
Initial			–2.1	±5	µA
vs Temperature			5		nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V			±750	nA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V			±1500	nA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V			±500	nA/V
BUFFER and OTA INPUT IMPEDANCE					
Input Impedance			1.0 || 2.1		MΩ || pF
BUFFER INPUT NOISE					
Voltage Noise Density, f = 100kHz			4		nV/√Hz
BUFFER DYNAMIC RESPONSE					
Small Signal Bandwidth	V_O = ±100mV		850		MHz
Full Power Bandwidth	V_O = ±1.4V		800		MHz
	V_O = ±2.5V		570		MHz
Differential Gain Error	3.58MHz, at 0.7V		0.06		%
Differential Phase Error	3.58MHz, at 0.7V		0.02		Degrees
Harmonic Distortion, 2nd Harmonic	f = 10MHz, V_O = 0.5Vp-p		–68		dBc
Slew Rate	5V Step		3000		V/µs
Settling Time 0.1%	2V Step		25		ns
Rise Time (10% to 90%)	V_O = 100mVp-p		1		ns
	5V Step		1.5		ns
Group Delay Time			250		ps
BUFFER RATED OUTPUT					
Voltage Output	I_O = ±1mA	±3.7	±4.2		V
Current Output		±10	±15		mA
Gain	R_L = 500Ω	0.96	0.975		V/V
	R_L = 5kΩ		0.99		V/V
Output Impedance			7 || 2		Ω || pF
POWER SUPPLY					
Voltage, Rated			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current (Programmable, Useful Range)			±3 to ±26		mA



OPA660 DIE TOPOGRAPHY

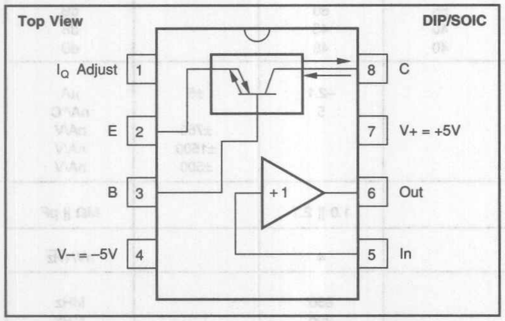
PAD	FUNCTION
1	Enable
2	NC
3	NC
4	OTA Input, Low Impedance
5	OTA Input, High Impedance
6	–5V Supply, Output
7	–5V Supply
8	Buffer Input
9	Buffer Output
10	+5V Supply
11	+5V Supply, Output
12	NC
13	OTA Output
14	NC

Substrate Bias: Negative Supply
NC: No Connection
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	41 x 77, ±5	1.05 x 1.95, ±0.13
Die Thickness	14 ±1	0.55, ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02,+0.05,–0.0	0.0005,+0.0013, –0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage(1)	$\pm V_S$ ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to $\pm V_S$.

PACKAGING INFORMATION

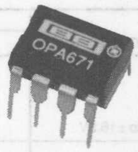
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA660AP	8-Pin Plastic DIP	006
OPA660AU	SO-8 Surface-Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA660AP	Plastic 8-Pin DIP	–25°C to +85°C
OPA660AU	SO-8 Surface-Mount	–25°C to +85°C

BURR - BROWN®



OPA671

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11120

Wide Bandwidth, Fast Settling *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- **WIDE GAIN-BANDWIDTH: 35MHz**
- **HIGH SLEW RATE: 100V/µs**
- **FAST SETTLING: 240ns to 0.01%**
- **FET INPUT: I_B = 50pA max**
- **HIGH OUTPUT CURRENT: 50mA**
- **WIDE SUPPLY RANGE: V_S = ±4.5 // ±18V**

APPLICATIONS

- **HIGH-SPEED DATA ACQUISITION**
- **OPTOELECTRONICS**
- **TRANSIMPEDANCE AMPLIFIER**
- **LINE DRIVER**

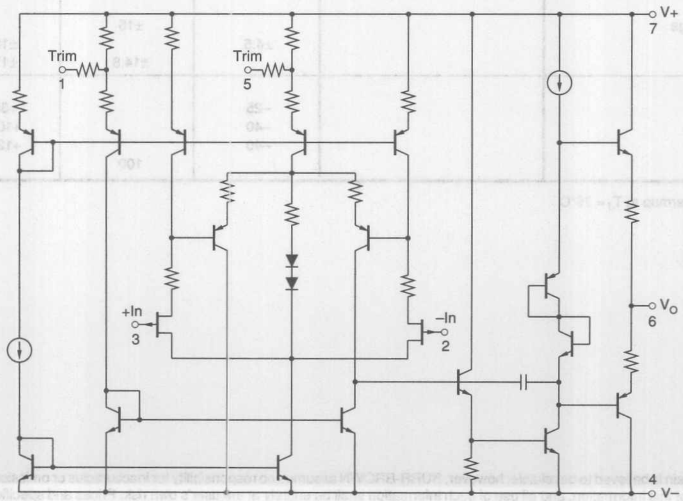
DESCRIPTION

The OPA671 is a FET-input monolithic operational amplifier featuring wide bandwidth and fast settling time. Fabricated using Burr-Brown's ***Difet***, complementary bipolar process, it provides an excellent combination of high speed, accuracy, and high output current.

The OPA671 is versatile, operating from ±4.5V to ±18V power supplies. It can deliver ±10V signals into a 200Ω load at slew rates of 100V/µs. OPA671's ***Difet*** input provides input bias current thousands of times lower than bipolar-input wideband op amps.

The OPA671 is internally compensated and is unity-gain stable, allowing use in the widest range of applications.

The OPA671 is available in an 8-pin plastic DIP, rated for the industrial temperature range.



Difet® Burr-Brown Corporation

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

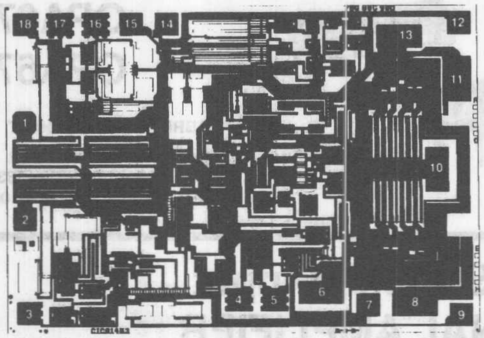
SPECIFICATIONS

At $T_A = +25°C$, $V_S = ±15V$ unless otherwise noted.

PARAMETER	CONDITION	OPA671AP MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±0.5	±5	mV
Average Drift			±10		µV/°C
Power Supply Rejection	$V_S = ±4.5$ to $±16.5V$	72	94		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	$V_{CM} = 0V$		5	50	pA
Input Offset Current	$V_{CM} = 0V$		2		pA
NOISE					
Input Voltage Noise					
Noise Density, f = 100Hz			24		nV/√Hz
f = 1kHz			15		nV/√Hz
f = 10kHz			12		nV/√Hz
f = 100kHz			10		nV/√Hz
Voltage Noise, BW = 10Hz to 1MHz			60		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 10Hz to 1MHz			2		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±12	±13		V
Common-Mode Rejection	$V_{CM} = ±10V$	74	92		dB
INPUT IMPEDANCE					
Differential			10^{12} || 4.5		Ω || pF
Common-Mode			10^{12} || 6		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	$V_O = ±10V$, $R_L = 1kΩ$		80		dB
	$V_O = ±10V$, $R_L = 200Ω$	74	78		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			35		MHz
Slew Rate	G = –1, 10V Step		107		V/µs
Settling Time 0.01%	G = –1, 10V Step		240		ns
0.1%	G = –1, 10V Step		150		ns
1%	G = –1, 10V Step		85		ns
Total Harmonic Distortion	G = 1, f = 100kHz $V_O = 3V$, $R_L = 200Ω$		0.0006		%
OUTPUT					
Voltage Output	$R_L = 200Ω$	±10.5	±11.5		V
Current Output	$V_O = ±10V$		50		mA
Short Circuit Current			–90/+105		mA
Output Resistance, Open-Loop	DC		20		Ω
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±18	V
Quiescent Current			±14.8	±17	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–40		+100	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTE: (1) Tested without warmup at $T_J = 25°C$.

DIE INFORMATION

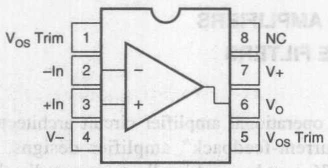


PAD	FUNCTION
1	–In
2	+In
3	IQ
4	Comp In
5	Comp Out
6	–Short Circuit Bypass
7	–V
8	–V for O/P Stage
9	Balance 2A
10	Output
11	+V for O/P Stage
12	+V
13	+Short Circuit Bypass
14	Balance 2B
15	Balance 1
16	Slope
17	R_{CM}
18	R9

OPA671 DIE TOPOGRAPHY

PIN CONFIGURATION

Top View DIP



NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	(V+) +1V to (V–) –1V
Operating Temperature	–40°C to +100°C
Storage Temperature	–40°C to +125°C
Output Short-Circuit to Ground	15s
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

An integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ORDERING INFORMATION

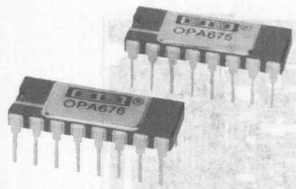
MODEL	PACKAGE	TEMP. RANGE
OPA671AP	8-Pin Plastic DIP	–25°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA671AP	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®



OPA675
OPA676

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10864

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 9ns (1%)
- WIDE BANDWIDTH: 185MHz (A_V = 10)
- LOW OFFSET VOLTAGE: ±250µV
- TWO LOGIC SELECTABLE INPUTS
- FAST INPUT SWITCHING: 8ns (TTL)
- 16-PIN DIP PACKAGE

APPLICATIONS

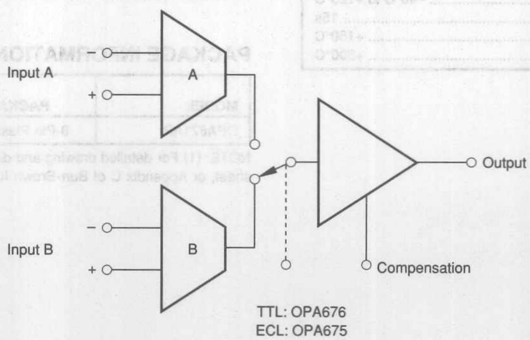
- PROGRAMMABLE-GAIN AMPLIFIER
- FAST 2-INPUT MULTIPLEXER
- SYNCHRONOUS DEMODULATOR
- PULSE/RF AMPLIFIERS
- VIDEO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

The OPA675 and OPA676 are wideband monolithic operational amplifiers with two independent differential inputs. Either input can be selected by an external logic signal. The OPA675 is compatible with ECL logic while the OPA676 is TTL compatible. Both amplifiers are externally compensated and feature very fast input selection speed: ECL = 4ns, TTL = 6ns. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA675/676 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make these amplifiers suitable for RF and video applications.

The OPA675 and OPA676 are available in KG (0°C to +70°C) and SG (–55°C to +125°C) grades. All grades are packaged in a 16-pin DIP.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

At $V_{CC} = \pm5VDC$, $R_L = 150\Omega$, and $T_A = +25°C$, unless otherwise noted.

		OPA675/676JG, SG			OPA675/676KG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT NOISE(1)								
Voltage: f_O = 10Hz	$R_S = 0\Omega$		27			*		$nV/\sqrt{Hz}$
f_O = 100Hz			10			*		$nV/\sqrt{Hz}$
f_O = 1kHz			3.8			*		$nV/\sqrt{Hz}$
f_O = 10kHz			2.6			*		$nV/\sqrt{Hz}$
f_O = 100kHz			2.4			*		$nV/\sqrt{Hz}$
f_B = 10Hz to 10MHz			7.9			*		µVrms
Current: f_O = 10Hz to 1MHz			2.7			*		$pA/\sqrt{Hz}$
OFFSET VOLTAGE(1)								
Input Offset Voltage	V_{CM} = 0VDC		±500	±2mV		±250	±1mV	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	65	86		70	*		dB
BIAS CURRENT(1)								
Input Bias Current	V_{CM} = 0VDC		23	35		*	30	µA
OFFSET CURRENT(1)								
Input Offset Current	V_{CM} = 0VDC		0.8	5		*	*	µA
INPUT IMPEDANCE(1)								
Differential			4k || 2			*		Ω || pF
Common-Mode			10^5 || 5			*		Ω || pF
INPUT VOLTAGE RANGE(1)								
Common-Mode Input Range		±1.25	±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	75	100		85	*		dB
OPEN LOOP GAIN, DC(1)								
Open-Loop Voltage Gain		65	70		*	*		dB
FREQUENCY RESPONSE								
Closed-Loop Bandwidth	Gain = +2V/V		100			*		MHz
	Gain = +5V/V		145			*		MHz
	Gain = +10V/V		185			*		MHz
	Gain = +50V/V		60			*		MHz
Crosstalk	Gain = +10V/V, f = 100kHz		–100			*		dBC(2)
	f = 1MHz		–80			*		dBC
	f = 10MHz		–68			*		dBC
	f = 100MHz		–35			*		dBC
Harmonic Distortion: 10MHz	G = +10V/V, $R_L = 50\Omega$, V_O = 0.5Vp-p							
	Second Harmonic		–61			*		dBC
	Third Harmonic		–73			*		dBC
Full Power Response	V_O = 2.5Vp-p, Gain = +10V/V	25	44		30	*		MHz
Slew Rate	Gain = +10V/V	200	350		240	*		V/µs
Settling Time: 1%			9			*		ns
0.1%	Gain = +10V/V		15			*		ns
0.01%	0.625V Output Step		25			*		ns
INPUT SELECTION(3)								
Transition Time	ECL: OPA675		5			*		ns
50% In to 50% Out	TTL: OPA676		7.5			*		ns
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		–0.05	–0.2		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		1	20		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.81		–1.475	*		*	V
V_{IH}	Logic "HI"	–1.15		– 0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		–50	–100		*	*	µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		–50	–100		*	*	µA
RATED OUTPUT								
Voltage Output	$R_L = 150\Omega$	±2.1	±2.6		*	*		V
	$R_L = 50\Omega$	+1.25	+1.8		*	*		V
		–0.95	–1.1		–1.0	*		V
Current Output			±30			*		mA
Output Resistance	1MHz, Open-Loop, C_C = 5pF		5			*		Ω
Load Capacitance Stability	Gain = +2V/V		50			*		pF
Short Circuit Current	Continuous to Gnd		+45			*		mA
			–25			*		mA

* Same specifications as for JG.

SPECIFICATIONS (CONT)

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C, unless otherwise noted.

		OPA675/676JG, SG			OPA675/676KG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY								
Rated Voltage	$\pm V_{CC}$		5			*		VDC
Derated Performance	$\pm V_{CC}$	4.5		6.5	*		*	VDC
Current, Quiescent	I_O = 0mADC		22	30		*	*	mA
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG	0		+70	*		*	°C
	SG	–55		+125				°C
Operating:	Ambient Temp JG, KG, SG	–55		+125	*		*	°C
θ_{JA}			125			*		°C/W

* Same specifications as for JG.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

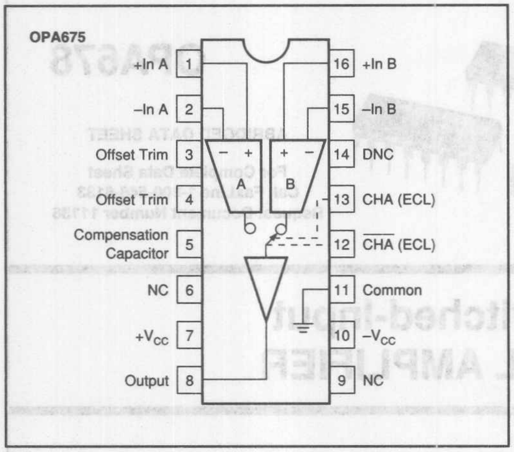
At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

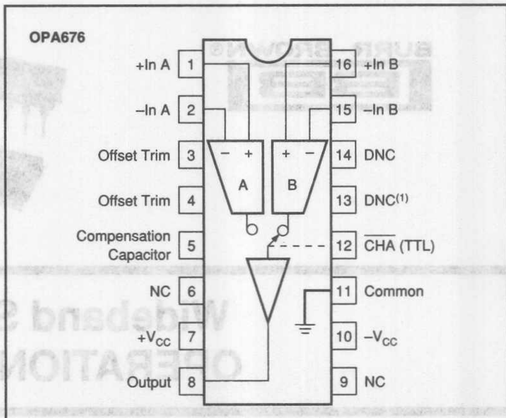
		OPA675/676JG, SG			OPA675/676KG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG	0		+70	*		*	°C
	SG	–55		+125				°C
OFFSET VOLTAGE								
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	60	85		65	*		dB
BIAS CURRENT								
Input Bias Current	V_{CM} = 0VDC		29	50		*	*	µA
OFFSET CURRENT								
Input Offset Current	V_{CM} = 0VDC		0.8	10		*	*	µA
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.0	±2.3		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	60	80		65	*		dB
OPEN LOOP GAIN, DC								
Open-Loop Voltage Gain		60	68		63	69		dB
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		–0.08	–0.4		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		5	50		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.81		–1.475	*		*	V
V_{IH}	Logic "HI"	–1.15		–0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		–50			*		µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		–50			*		µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.0	±2.5		*	*		V
	R_L = 50Ω	+1.25	+1.6		*	*		V
		–0.8	–1.0		–0.9	*		V
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		25	35		*	*	mA

* Same specifications as for JG.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Switching time from application of digital logic signal to input signal selection.

PIN CONFIGURATIONS





NOTE: (1) Capacitance on this node slows channel select.

PIN ASSIGNMENTS: OPA675

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	CHA (ECL)
5	Compensation Capacitor	12	$\overline{\text{CHA}}$ (ECL)
6	NC	11	Common
7	$+V_{CC}$	10	$-V_{CC}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

PIN ASSIGNMENTS: OPA676

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	DNC
5	Compensation Capacitor	12	$\overline{\text{CHA}}$ (TTL)
6	NC	11	Common
7	$+V_{CC}$	10	$-V_{CC}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Differential Input Voltage	Total V_{CC}
Input Voltage Range (Analog and Digital)	$\pm V_{CC}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

ORDERING INFORMATION

OPA675 ( ) ( )
OPA676 ( ) ( )

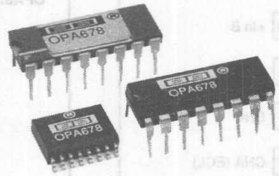
Basic Model Number
Performance Grade Code
J, K: 0°C to +70°C
S: –55°C to +125°C
Package Code
G: 16-pin Ceramic DIP

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA675/76JG	16-Pin Hermetic DIP	109
OPA675/76SG	16-Pin Hermetic DIP	109
OPA675/76KG	16-Pin Hermetic DIP	109

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®



OPA678

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11136

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 11ns (1%)
- WIDE BANDWIDTH: 200MHz
- TWO LOGIC SELECTABLE INPUTS
- LOW OFFSET VOLTAGE: ±380μV
- FAST INPUT SWITCHING: 4ns
- ACCEPTS TTL/ECL SWITCHING SIGNALS
- UNITY GAIN STABLE
- 16-PIN DIP AND SOIC PACKAGES

APPLICATIONS

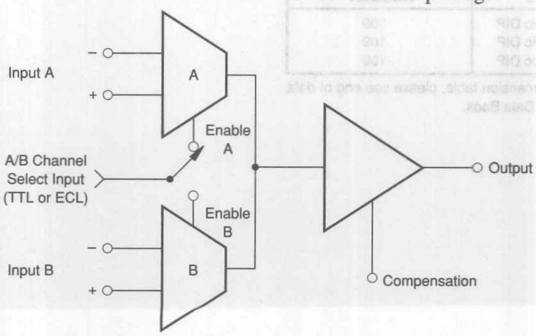
- VIDEO AMPLIFICATION AND SWITCHING
- FAST 2-INPUT MULTIPLEXER
- PULSE/RF AMPLIFIERS
- PROGRAMMABLE-GAIN AMPLIFIER
- ACTIVE FILTERS
- SYNCHRONOUS DEMODULATOR

DESCRIPTION

The OPA678 is a wideband monolithic operational amplifier with two independent differential inputs. Either input can be selected by an external TTL or ECL logic signal. The amplifier is externally compensated and features a very fast input selection speed, 4ns for either ECL or TTL. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA678 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make this amplifier suitable for RF and video applications.

The OPA678 is available in DIP, SOIC, and sidebraze packages. A military temperature range part is available in the sidebraze package.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1136C

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, C_{COMP} = 5pF, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA678AG, AP, AU MIN	OPA678AG, AP, AU TYP	OPA678AG, AP, AU MAX	OPA678SG MIN	OPA678SG TYP	OPA678SG MAX	UNITS
INPUT NOISE(1)								
Voltage: f_O = 100Hz	R_S = 0Ω		55			*		nV/√Hz
f_O = 1kHz			21			*		nV/√Hz
f_O = 10kHz			7.8			*		nV/√Hz
f_O = 100kHz			4.9			*		nV/√Hz
f_B = 10Hz to 10MHz			18			*		μVrms
Current: f_O = 10Hz to 1MHz			2.1			*		pA/√Hz
OFFSET VOLTAGE(1)								
Input Offset Voltage	V_{CM} = 0VDC		±380	±1.5mV		±380	±1mV	μV
Offset Voltage Drift	T_A = T_{MIN} to T_{MAX}		±3	±15		±3	±10	μV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	65	71		*	*		dB
BIAS CURRENT(1)								
Input Bias Current	V_{CM} = 0VDC		14	50		*	*	μA
OFFSET CURRENT(1)								
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	1.5	μA
INPUT IMPEDANCE(1)								
Differential			25k || 2			*		Ω || pF
Common-Mode			10^6 || 5			*		Ω || pF
INPUT VOLTAGE RANGE(1)								
Common-Mode Input Range		2.0	±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	75	85		*	*		dB
OPEN-LOOP GAIN, DC(1)								
Open-Loop Voltage Gain		50	60		*	*		dB
FREQUENCY RESPONSE								
Closed-Loop Bandwidth	Gain = +1V/V, C_C = 9pF	140	200		*	*		MHz
	Gain = +2V/V, C_C = 7pF		100			*		MHz
	Gain = +5V/V, C_C = 1pF		70			*		MHz
Crosstalk	Gain = +1V/V, f = 100kHz		–102			*		dBC(2)
	f = 1MHz		–83			*		dBC
	f = 10MHz		–64			*		dBC
	f = 100MHz		–44			*		dBC
Harmonic Distortion: 5MHz	G = +1V/V, R_L = 150Ω, V_O = 0.25Vp-p							
	Second Harmonic		–71			*		dBC(3)
	Third Harmonic		–82			*		dBC
Large Signal Response(4)	V_O = 2.5Vp-p, Gain = +1V/V	32	45		*	*		MHz
Slew Rate	Gain = +1V/V	250	350		*	*		V/μs
Settling Time: 1%	Gain = –1V/V, $1V_{OUT}$ Step		11			*		ns
0.1%			22			*		ns
0.01%			30			*		ns
Differential Gain (0V to 0.7V)	4.5MHz, Gain = +2V/V, C_C = 2.2pF		0.02					%
Differential Phase (0V to 0.7V)	4.5MHz, Gain = +2V/V, C_C = 2.2pF		0.02					Degrees
INPUT SELECTION(5)								
Transition Time	ECL: Operation		4	8		*	9	ns
50% In to 50% Out	TTL: Operation		4	8		*	9	ns
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		–0.05	–0.2		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		1	20		*	*	μA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.81		–1.475	*		*	V
V_{IH}	Logic "HI"	–1.15		– 0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		–50	–100		*		μA
I_{IH}	Logic "HI", V_{IH} = –1.0V		–50	–100		*		μA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.5	±3.75		*	*		V
	R_L = 50Ω	±1.7	±2.2		*	*		V
Current Output		±30	±44			*		mA
Output Resistance	1MHz, Open Loop, C_C = 5pF		5			*		Ω
Load Capacitance Stability	R_F = 100Ω, Gain = +1V/V, C_C = 10pF		17			*		pF
Short Circuit Current	Continuous to Gnd		+45			±45		mA

SPECIFICATIONS (CONT)

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, C_{COMP} = 5pF, and T_A = +25°C unless otherwise noted.

		OPA678AG, AP, AU			OPA678SG			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY								
Rated Voltage	$\pm V_{CC}$		5			*		VDC
Derated Performance	$\pm V_{CC}$	4.5		5.5	*		*	VDC
Current, Quiescent	I_O = 0mADC		26	30		*	*	mA
TEMPERATURE RANGE								
Specification	Ambient Temp AG, AP, AU	–40		+85	*		*	°C
	SG	–55		+125				°C
θ_{JA}	AG, SG		125			*		°C/W
	AP		90					°C/W
	AU		100					°C/W

* Same specifications as for OPA678AG/AP/AU.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

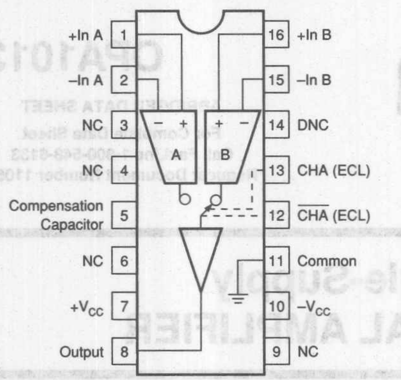
At V_{CC} = ±5VDC, R_L = 150Ω, C_{COMP} = 5pF, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

		OPA678AG, AP, AU			OPA678SG			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TEMPERATURE RANGE								
Specification	Ambient Temp AG/AP/AU	–40		+85	*		*	°C
	SG				–55		+125	°C
OFFSET VOLTAGE								
Input Offset Voltage	$T_A = T_{MIN}$ to T_{MAX}		600	±2.4mV		*	±2mV	μV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±15		*	±10	μV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	60	70		*	73		dB
BIAS CURRENT								
Input Bias Current	V_{CM} = 0VDC		15	85		*	*	μA
OFFSET CURRENT								
Input Offset Current	V_{CM} = 0VDC		0.5	5		*	7	μA
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.0	±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	60	80		*	*		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain		50	60		*	*		dB
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		–0.08	–0.4		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		5	50		*	*	μA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.81		–1.475	*		*	V
V_{IH}	Logic "HI"	–1.15		–0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		–50			*		μA
I_{IH}	Logic "HI", V_{IH} = –1.0V		–50			*		μA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.5	±3.75		*	*		V
	R_L = 50Ω	±1.5	±2.0		±1.5	*		V
Output Current			44			40		mA
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		25	35		*	*	mA

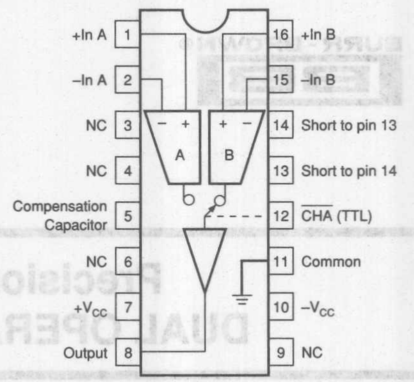
* Same specifications as for AG/AP/AU.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Harmonic distortion will typically be improved significantly in the inverting mode. (4) Large Signal Response is calculated from the formula LSBW = $\frac{SR}{2\pi V_{PEAK}}$. (5) Switching time from application of digital logic signal to input signal selection.

Pin Assignments for Differential ECL Channel Switching



Pin Assignments for TTL Channel Switching



ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Differential Input Voltage	Total V_{CC}
Input Voltage Range (Analog and Digital)	$\pm V_{CC}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

ORDERING INFORMATION

OPA678 ( ) ( )

Basic Model Number

Performance Grade Code
- A: –40°C to +85°C
- S: –55°C to +125°C

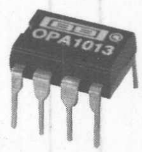
Package Code
- G: 16-pin Ceramic DIP
- P: 16-pin Plastic DIP
- U: 16-pin SOIC

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA678AG	16-Pin Hermetic DIP	109
OPA678AP	16-Pin Plastic DIP	180
OPA678AU	16-Pin SOIC	211
OPA678SG	16-Pin Hermetic DIP	109

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®



OPA1013

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11059

Precision, Single-Supply DUAL OPERATIONAL AMPLIFIER

FEATURES

- SINGLE POWER SUPPLY OPERATION
- INPUT VOLTAGE RANGE TO GROUND
- OUTPUT SWINGS NEAR GROUND
- LOW QUIESCENT CURRENT: 550µA max
- LOW V_{OS}: 300µV max
- LOW DRIFT: 2.5µV/°C max
- LOW I_{OS}: 1.5nA max
- LOW NOISE: 0.55µVp-p, 0.1Hz to 10Hz

APPLICATIONS

- PRECISION INSTRUMENTATION
- BATTERY-POWERED EQUIPMENT
- BRIDGE AMPLIFIERS
- 4-20mA CURRENT TRANSMITTERS
- VOLTAGE COMPARATOR

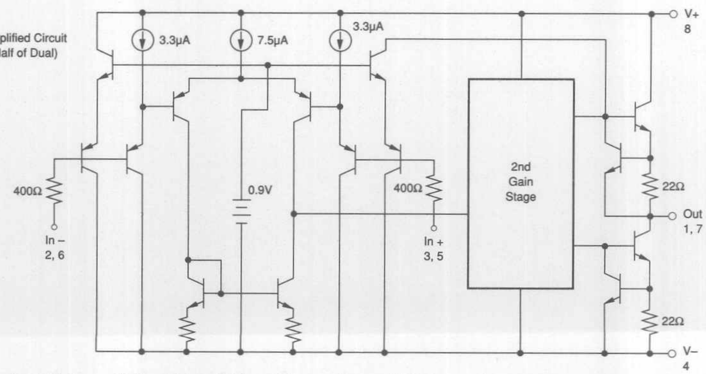
DESCRIPTION

The OPA1013 dual operational amplifier provides precision performance in single power supply and low power applications. It is laser trimmed for low offset voltage and drift, greatly reducing the large errors common with LM324-type op amps. Input offset current is also trimmed to reduce errors in high impedance applications.

The OPA1013 is characterized for operation at both +5V (single supply) and ±15V power supplies. When operated from a single supply, the input common-mode range includes ground and the output can swing to within 15mV of ground. Completely independent biasing networks eliminate interaction between the two amplifiers—even when one is used as a comparator.

The OPA1013 is available in an 8-pin plastic DIP specified for the 0°C to +70°C temperature range.

Simplified Circuit
(Half of Dual)



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

V_S = ±15V, V_{CM} = 0V, T_A = +25°C unless otherwise noted.

		OPA1013CN8			OPA1013DN8			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage			±50	±300		±200	±800	µV
Time Stability			0.5			*		µV/Mo
Input Offset Current			±0.08	±1.5		*	*	nA
Input Bias Current			7	30		*	*	nA
Voltage Noise, BW = 0.1 to 10Hz			0.55			*		µVp-p
Noise Density, f = 10Hz			28			*		nV/√Hz
f = 1kHz			25			*		nV/√Hz
Current Noise Density, f = 10Hz			0.12			*		pA/√Hz
Input Resistance: Differential		70	300		*	*		MΩ
Input Resistance: Common-Mode			4			*		GΩ
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	1.2	2.9		*	*		V/µV
	V_O = ±10V, R_L = 600Ω	0.5	1.9		*	*		V/µV
Common-Mode Input Range		+13.5	+13.8		*	*		V
		–15	–15.3		*	*		V
Common-Mode Rejection	V_{CM} = +13.5 to –15V	97	114		*	*		dB
Power Supply Rejection	V_S = ±2 to ±18V	100	117		*	*		dB
Channel Separation	V_O = ±10V, R_L = 2kΩ	120	137		*	*		dB
Voltage Output	R_L = 2kΩ	±12.5	±14		*	*		V
Slew Rate		0.2	0.35		*	*		V/µs
Quiescent Current (per amplifier)			±0.35	±0.55		*	*	mA

*Specification same as OPA1013CN8.

V_S = +5V/0V, V_{CM} = 0V, V_O = +1.4V, T_A = +25°C unless otherwise noted.

		OPA1013CN8			OPA1013DN8			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage			±90	±450		±250	±950	µV
Input Offset Current			±3.0	±2.0		*	*	nA
Input Bias Current			10	50		*	*	nA
Open-Loop Voltage Gain	V_O = 5mV to 4V, R_L = 500Ω		0.1			*		V/µV
Common-Mode Input Range		+3.5	+3.8		*	*		V
		0	–0.3		*	*		V
Voltage Output Low	No Load		15	25		*	*	mV
Low	R_L = 600Ω to Ground		5	10		*	*	mV
Low	I_{SINK} = 1mA		200	350		*	*	mV
High	No Load	4	4.4		*	*		V
High	R_L = 600Ω to Ground	3.4	4		*	*		V
Quiescent Current (per amplifier)			0.33	0.5		*	*	mA

*Specification same as OPA1013CN8.

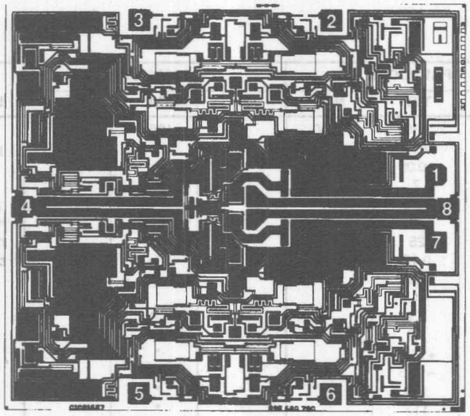
T_A = 0°C to +70°C, V_S = ±15V, V_{CM} = 0V unless otherwise noted.

		OPA1013CN8			OPA1013DN8			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage			±80	±400		±230	±1000	µV
	V_S = +5/0V, V_O = +1.4V		±110	±570		±280	±1200	µV
Input Offset Voltage Drift(1)			0.4	2.5		0.7	5	µV/°C
Input Offset Current			±0.3	±2.8		*	*	nA
	V_S = +5/0V, V_O = +1.4V		±0.5	±6		*	*	nA
Input Bias Current			9	38		*	*	nA
	V_S = +5/0V, V_O = +1.4V		13	90		*	*	nA
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	0.7	2.2		*	*		V/µV
Common-Mode Rejection	V_{CM} = +13 to –15V	94	113		*	*		dB
Power Supply Rejection	V_S = ±2 to ±18V	97	116		*	*		dB
Voltage Output	R_L = 2kΩ	±12.0	±13.9		*	*		V
V_O Low	V_S = +5/0V, R_L = 600Ω		6	13		*	*	mV
V_O High	V_S = +5/0V, R_L = 600Ω	3.2	3.9		*	*		V
Quiescent Current (per amplifier)			±0.37	±0.6		*	*	mA
	V_S = +5/0V, V_O = +1.4V		0.34	0.55		*	*	mA

*Specification same as OPA1013CN8.

NOTE: (1) Guaranteed by design. This specification is established to a 98% confidence level.

DICE INFORMATION



OPA1013 DIE TOPOGRAPHY

PAD	FUNCTION
1	Output A
2	–In A
3	+In A
4	V–
5	+In B
6	–In B
7	Output B
8	V+

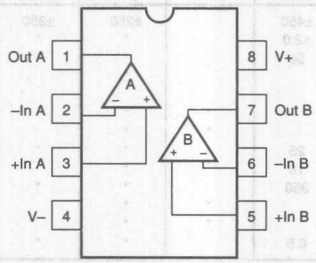
Substrate Bias: $-V_S$

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	112 x 100 ±5	2.84 x 2.54 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count		92
Backing		Gold

CONNECTION DIAGRAM

N8 — Plastic Package — Top View



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	V+ to (V–) –5V
Output Short Circuit (T_A = 25°C)	Continuous
Operating Temperature:	0°C to +70°C
Storage Temperature	–65 to +150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

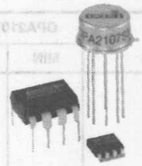
MODEL	PACKAGE	TEMPERATURE RANGE
OPA1013CN8	Plastic DIP	0°C to +70°C
OPA1013DN8	Plastic DIP	0°C to +70°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA1013CN8	Plastic DIP	006
OPA1013DN8	Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®



OPA2107

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10863

Precision Dual *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW NOISE: 8nV/√Hz at 10kHz
- LOW V_{OS}: 500µV max
- LOW DRIFT: 5µV/°C max
- LOW I_B: 5pA max
- FAST SETTLING TIME: 2µs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

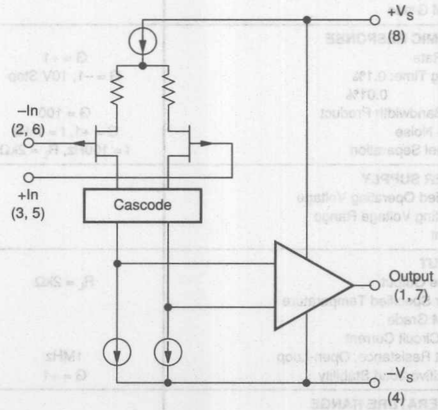
- DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- MEDICAL EQUIPMENT, CT SCANNERS

DESCRIPTION

The OPA2107 dual operational amplifier provides precision ***Difet*** performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET® type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (***Difet***) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent DC performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in plastic DIP, metal TO-99, and SOIC packages. Industrial and Military temperature range versions are available.



Difet® Burr-Brown Corp.
BIFET® National Semiconductor

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

$T_A = +25°C$, $V_S = ±15V$ unless otherwise noted.

		OPA2107AM, SM, AP, AU			OPA2107BM			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE(1)								
Input Offset Voltage	$V_{CM} = 0V$		100	1mV		50	500	µV
Over Specified Temperature			0.5	2		0.2	1	mV
SM Grade			0.8	2.5				mV
Average Drift Over Specified Temperature			3	10		2	5	µV/°C
Power Supply Rejection	$V_S = ±10$ to $±18V$	80	96		84	100		dB
INPUT BIAS CURRENT(1)								
Input Bias Current	$V_{CM} = 0V$		4	10		2	5	pA
Over Specified Temperature			0.25	1.5		0.15	1	nA
SM Grade			4	35				nA
Input Offset Current	$V_{CM} = 0V$		1	8		0.5	3	pA
Over Specified Temperature				1			0.5	nA
SM Grade			1	28				nA
INPUT NOISE								
Voltage: f = 10Hz	$R_S = 0$		30			*		nV/√Hz
f = 100Hz			12			*		nV/√Hz
f = 1kHz			9			*		nV/√Hz
f = 10kHz			8			*		nV/√Hz
BW = 0.1 to 10Hz			1.2			*		µVp-p
BW = 10 to 10kHz			0.85			*		µVrms
Current: f = 0.1Hz thru 20kHz			1.2			0.9		fA/√Hz
BW = 0.1Hz to 10Hz			23			17		fAp-p
INPUT IMPEDANCE								
Differential			$10^{13} \parallel 2$			*		Ω ‖ pF
Common-Mode			$10^{14} \parallel 4$			*		Ω ‖ pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±10.5	±11		*	*		V
Over Specified Temperature		±10.2	±10.5		*	*		V
SM Grade		±10	±10.3					V
Common-Mode Rejection	$V_{CM} = ±10V$	80	94		84	100		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	$V_O = ±10V$, $R_L = 2kΩ$	82	96		84	100		dB
Over Specified Temperature		80	94		82	96		dB
SM Grade		80	92					dB
DYNAMIC RESPONSE								
Slew Rate	G = +1	13	18		*	*		V/µs
Settling Time: 0.1%	G = –1, 10V Step		1.5			*		µs
0.01%			2			*		µs
Gain-Bandwidth Product	G = 100		4.5			*		MHz
THD + Noise	G = +1, f = 1kHz		0.001			*		%
Channel Separation	f = 100Hz, $R_L = 2kΩ$		120			*		dB
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Current			±4.5	±5		*	*	mA
OUTPUT								
Voltage Output	$R_L = 2kΩ$	±11	±12		*	*		V
Over Specified Temperature		±10.5	±11.5		*	*		V
SM Grade		±10.2	±11.3					V
Short Circuit Current		±10	±40		*	*		mA
Output Resistance, Open-Loop	1MHz		70			*		Ω
Capacitive Load Stability	G = +1		1000			*		pF
TEMPERATURE RANGE								
Specification								
AP, AU, AM, BM		–25		+85	*		*	°C
SM		–55		+125				°C
Operating								
AP, AU		–25		+85				°C
AM, BM, SM		–55		+125	*		*	°C
Storage								
AP, AU		–40		+125				°C
AM, BM, SM		–65		+150	*		*	°C
Thermal Resistance (θ_{J-A})								
AP			90					°C/W
AU			175					°C/W
AM, BM, SM			200			*		°C/W

* Specifications same as OPA2107AM. NOTE: (1) Specified with devices fully warmed up.

Differential Input Voltage	Total $V_S \pm 4V$
Operating Temperature	
M Package	–55°C to +125°C
P and U Packages	–25°C to + 85°C
Storage Temperature	
M Package	–65°C to +150°C
P and U Packages	–40°C to +125°C
Output Short Circuit to Ground (T_A = +25°C)	Continuous
Junction Temperature	+175°C
Lead Temperature	
M and P Packages (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C

OPA2107AP	Plastic DIP	006
OPA2107AM	Metal TO-99	001
OPA2107BM	Metal TO-99	001
OPA2107SM	Metal TO-99	001
OPA2107AU	SO-8 SOIC	182

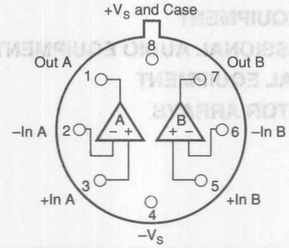
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

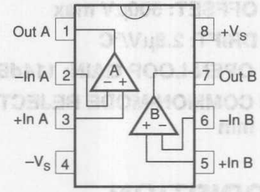
MODELS	PACKAGE	SPECIFICATION TEMPERATURE RANGE
OPA2107AP	Plastic DIP	–25 to +85°C
OPA2107AM	Metal TO-99	–25 to +85°C
OPA2107BM	Metal TO-99	–25 to +85°C
OPA2107SM	Metal TO-99	–55 to +125°C
OPA2107AU	SO-8 SOIC	–25 to +85°C

PIN CONFIGURATIONS

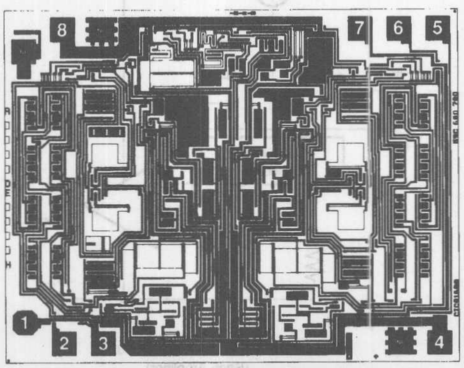
Top View – M Package



Top View – P & U Packages



DICE INFORMATION



OPA2107 DIE TOPOGRAPHY

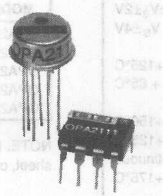
PAD	FUNCTION
1	Out A
2	–In A
3	+In A
4	–V_S
5	+In B
6	–In B
7	Out B
8	+V_S

Substrate Bias: –V_S

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	97 x 77 ±3	2.46 x 1.96 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count		53
Backing		None

BURR - BROWN®



OPA2111

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10540

Dual Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- **LOW NOISE: 100% Tested, 8nV/√Hz max at 10kHz**
- **LOW BIAS CURRENT: 4pA max**
- **LOW OFFSET: 500μV max**
- **LOW DRIFT: 2.8μV/°C**
- **HIGH OPEN-LOOP GAIN: 114dB min**
- **HIGH COMMON-MODE REJECTION: 96dB min**

APPLICATIONS

- **PRECISION INSTRUMENTATION**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**
- **PROFESSIONAL AUDIO EQUIPMENT**
- **MEDICAL EQUIPMENT**
- **DETECTOR ARRAYS**

DESCRIPTION

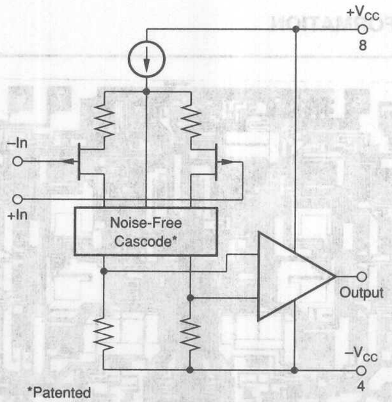
The OPA2111 is a high precision monolithic dielectrically isolated FET (***Difet***) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op amp pin configuration allows upgrading of existing designs to higher performance levels.



OPA2111 Simplified Circuit
(Each Amplifier)

BIFET® National Semiconductor Corp., ***Difet***® Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted

PARAMETER	CONDITION	OPA2111AM MIN	OPA2111AM TYP	OPA2111AM MAX	OPA2111BM MIN	OPA2111BM TYP	OPA2111BM MAX	OPA2111SM MIN	OPA2111SM TYP	OPA2111SM MAX	OPA2111KM, KP MIN	OPA2111KM, KP TYP	OPA2111KM, KP MAX	UNITS
INPUT NOISE														
Voltage, f_O = 10Hz	100% Tested		40	80		30	60		40	80		40		nV/√Hz
f_O = 100Hz	100% Tested		15	40		11	30		15	40		15		nV/√Hz
f_O = 1kHz	100% Tested		8	15		7	12		8	15		8		nV/√Hz
f_O = 10kHz	(1)		6	8		6	8		6	8		6		nV/√Hz
f_B = 10Hz to 10kHz	(1)		0.7	1.2		0.6	1		0.7	1.2		0.7		µVrms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3		1.6		µVp-p
Current, f_B = 0.1Hz to 10Hz	(1)		15	24		12	19		15	24		15		fAp-p
f_O = 0.1Hz to 20kHz	(1)		0.8	1.3		0.6	1		0.8	1		0.8		fA/√Hz
OFFSET VOLTAGE(2)														
Input Offset Voltage	V_{CM} = 0VDC		±0.1	±0.75		±0.05	±0.5		±0.1	±0.75		±0.3	±2	mV
Average Drift	T_A = T_{MIN} to T_{MAX}		±2	±6		±0.5	±2.8		±2	±6		±8	±15	µV/°C
Match			±1			±0.5			2			2		µV/°C
Supply Rejection		90	110		96	110		90	110		86	110		dB
			±3	±31		±3	±16		±3	±31		±3	±50	µV/V
Channel Separation	100Hz, R_L = 2kΩ		136			136			136			136		dB
BIAS CURRENT(2)														
Input Bias Current	V_{CM} = 0VDC		±2	±8		±1.2	±4		±2	±8		±3	±15	pA
Match			±1			±0.5			±1			2		pA
OFFSET CURRENT(2)														
Input Offset Current	V_{CM} = 0VDC		±1.2	±6		±0.6	±3		±1.2	±6		±3	±12	pA
IMPEDANCE														
Differential			10^{13} || 1			10^{13} || 1			10^{13} || 1			10^{13} || 1		Ω || pF
Common-Mode			10^{14} || 3			10^{14} || 3			10^{14} || 3			10^{14} || 3		Ω || pF
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		96	110		90	110		82	110		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	R_L ≥ 2kΩ	110	125		114	125		110	125		106	125		dB
Match			3			2			3			3		dB
FREQUENCY RESPONSE														
Unity Gain, Small Signal			2			2			2			2		MHz
Full Power Response	20Vp-p, R_L = 2kΩ	16	32		16	32		16	32			32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2		1	2			2			2		V/µs
Settling Time, 0.1%	Gain = –1, R_L = 2kΩ		6			6			6			6		µs
0.01%	10V Step		10			10			10			10		µs
Overload Recovery, 50% Overdrive(3)	Gain = –1		5			5			5			5		µs
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10	±11		±10	±11		±10	±11		±10	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, Open-Loop		100			100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Rated Voltage			±15			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		5	7		5	7		5	7		5	9	mA
TEMPERATURE RANGE														
Specification	Ambient Temp.	–25		+85	–25		+85	–55		+125	0		+70	°C
Operating "M" Package	Ambient Temp.	–55		+125	–55		+125	–55		+125	–55		+125	°C
"P" Package											–40		+85	°C
Storage "M" Package	Ambient Temp.	–65		+150	–65		+150	–65		+150	–65		+150	°C
"P" Package											–40		+85	°C
θ Junction-Ambient			200			200			200			200(4)		°C/W

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Typical θ_{J-A} = 150°C/W for plastic DIP.

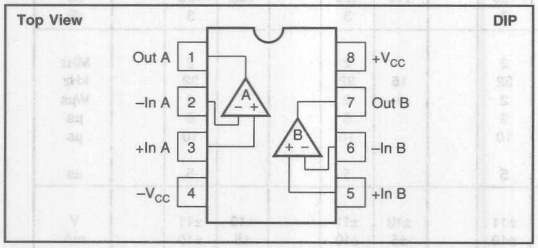
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

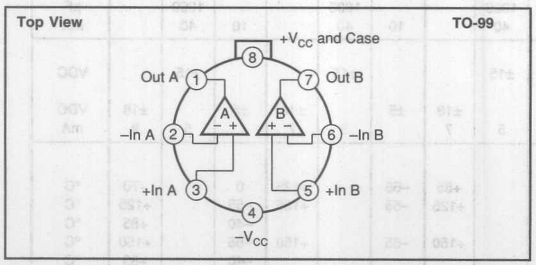
At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

		OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM, KP			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TEMPERATURE RANGE														
Specification Range	Ambient Temp.	–25		+85	–25		+85	–55		+125	0		+70	°C
INPUT OFFSET VOLTAGE(1)														
Input Offset Voltage	V_{CM} = 0VDC		±0.22	±1.2		±0.08	±0.75		±0.3	±1.5		±0.9	±5	mV
Average Drift			±2	±6		±0.5	±2.8		±2	±6		±8	±15	µV/°C
Match			1			0.5			2			2		µV/°C
Supply Rejection		86	100		90	100		86	100		82	100		dB
			±10	±50		±10	±32		±10	±50		±10	±80	µV/V
BIAS CURRENT(1)														
Input Bias Current	V_{CM} = 0VDC		±125	±1nA		±75	±500		±2nA	±16.3nA		±125	±500	pA
Match			60			30			1nA					pA
OFFSET CURRENT(1)														
Input Offset Current	V_{CM} = 0VDC		±75	±750		±38	±375		±1.3nA	±12nA		±75	±375	pA
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		80	100		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	120		110	120		106	120		100	120		dB
Match			5			3			5			5		dB
RATED OUTPUT														
Voltage Output	$R_L = 2k\Omega$	±10.5	±11		±10.5	±11		±10.5	±11		±10.5	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Current, Quiescent	I_O = 0mADC		5	8		5	8		5	8		5	10	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

CONNECTION DIAGRAMS





The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation ($T_J \leq$ +175°C)	500mW
Differential Input Voltage	Total V_{CC}
Input Voltage Range	$\pm V_{CC}$
Storage Temperature Range: "M" Package	–65°C to +150°C
"P" Package	–40°C to +85°C
Operating Temperature Range: "M" Package	–55°C to +125°C
"P" Package	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA2111AM	TO-99	001
OPA2111BM	TO-99	001
OPA2111KM	TO-99	001
OPA2111SM	TO-99	001
OPA2111KP	8-Pin Plastic DIP	006

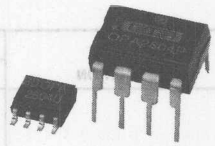
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE, max (mV)
OPA2111AM	TO-99	–25°C to +85°C	±0.75
OPA2111BM	TO-99	–25°C to +85°C	±0.5
OPA2111KM	TO-99	0°C to +70°C	±2
OPA2111SM	TO-99	–55°C to +125°C	±0.75
OPA2111KP	8-Pin Plastic DIP	0°C to +70°C	±2

BURR - BROWN®

OPA2604



Dual FET-Input, Low Distortion OPERATIONAL AMPLIFIER

FEATURES

- LOW DISTORTION: 0.0003% at 1kHz
- LOW NOISE: $10nV/\sqrt{Hz}$
- HIGH SLEW RATE: 25V/μs
- WIDE GAIN-BANDWIDTH: 20MHz
- UNITY-GAIN STABLE
- WIDE SUPPLY RANGE: $V_S = \pm4.5$ to $\pm24V$
- DRIVES 600Ω LOADS

APPLICATIONS

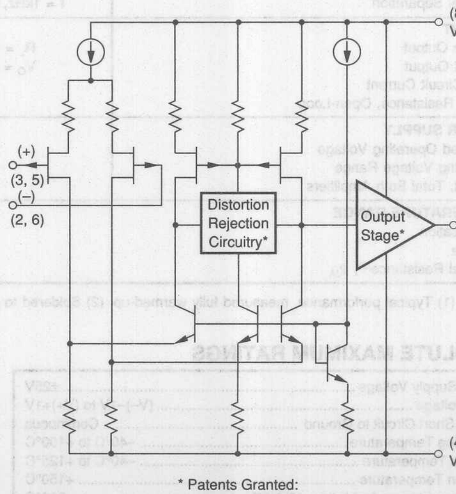
- PROFESSIONAL AUDIO EQUIPMENT
- PCM DAC I/V CONVERTER
- SPECTRAL ANALYSIS EQUIPMENT
- ACTIVE FILTERS
- TRANSDUCER AMPLIFIER
- DATA ACQUISITION

DESCRIPTION

The OPA2604 is a dual, FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio and other applications requiring excellent dynamic performance.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA2604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

The OPA2604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the –25°C to +85°C temperature range.



* Patents Granted: #5053718, 5019789

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

$T_A = +25°C$, $V_S = ±15V$ unless otherwise noted.

PARAMETER	CONDITION	OPA2604AP, AU MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±1	±5	mV
Average Drift			±8		µV/°C
Power Supply Rejection	V_S = ±5 to ±24V	80	100		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		100		pA
Input Offset Current	V_{CM} = 0V		±4		pA
NOISE					
Input Voltage Noise					
Noise Density: f = 10Hz			25		nV/√Hz
f = 100Hz			15		nV/√Hz
f = 1kHz			11		nV/√Hz
f = 10kHz			10		nV/√Hz
Voltage Noise, BW = 20Hz to 20kHz			1.5		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			6		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±12	±13		V
Common-Mode Rejection	V_{CM} = ±12V	80	100		dB
INPUT IMPEDANCE					
Differential			10^{12} || 8		Ω || pF
Common-Mode			10^{12} || 10		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	80	100		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product	G = 100		20		MHz
Slew Rate	20Vp-p, R_L = 1kΩ	15	25		V/µs
Settling Time: 0.01%	G = –1, 10V Step		1.5		µs
0.1%			1		µs
Total Harmonic Distortion + Noise (THD+N)	G = 1, f = 1kHz V_O = 3.5Vrms, R_L = 1kΩ		0.0003		%
Channel Separation	f = 1kHz, R_L = 1kΩ		142		dB
OUTPUT					
Voltage Output	R_L = 600Ω	±11	±12		V
Current Output	V_O = ±12V		±35		mA
Short Circuit Current			±40		mA
Output Resistance, Open-Loop			25		W
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±24	V
Current, Total Both Amplifiers			±10.5	±12	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+125	°C
Thermal Resistance(2), θ_{JA}			90		°C/W

NOTES: (1) Typical performance, measured fully warmed-up. (2) Soldered to circuit board—see text.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±25V
Input Voltage	(V–)–1V to (V+)+1V
Output Short Circuit to Ground	Continuous
Operating Temperature	–40°C to +100°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) AP	+300°C
Lead Temperature (soldering, 3s) AU	+260°C

PACKAGING INFORMATION

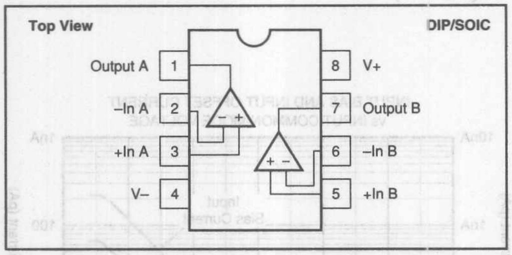
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA2604AP	8-Pin Plastic DIP	006
OPA2604AU	SO-8 Surface-Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA2604AP	8-Pin Plastic DIP	–25°C to +85°C
OPA2604AU	SO-8 Surface-Mount	–25°C to +85°C

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

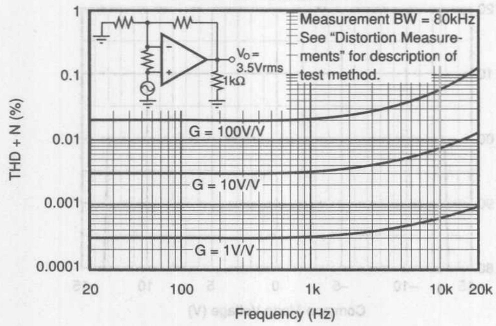
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

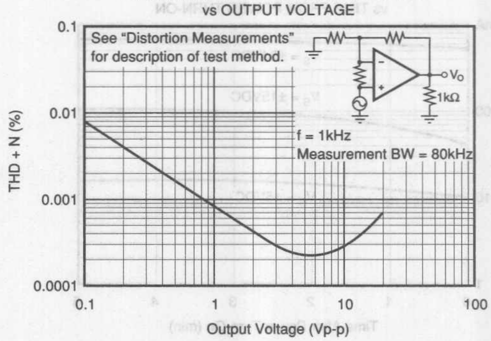
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = \pm15V$ unless otherwise noted.

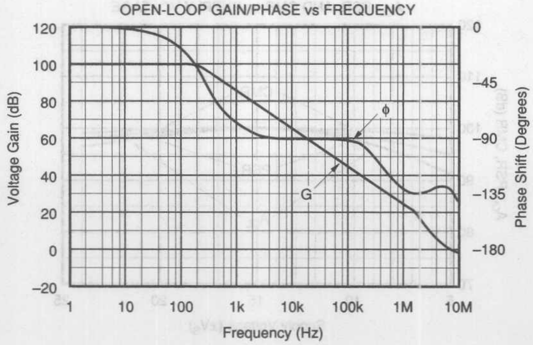
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



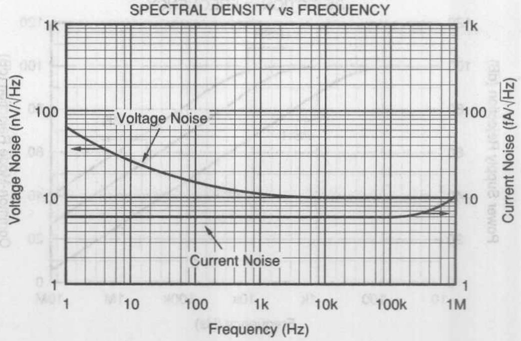
TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE



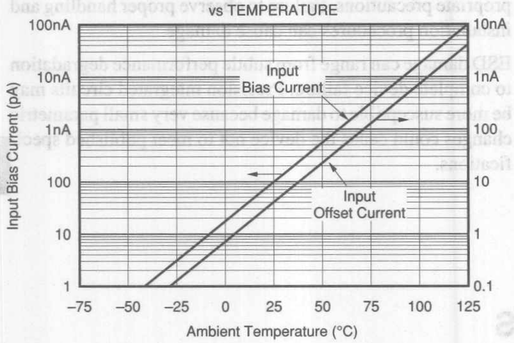
OPEN-LOOP GAIN/PHASE vs FREQUENCY



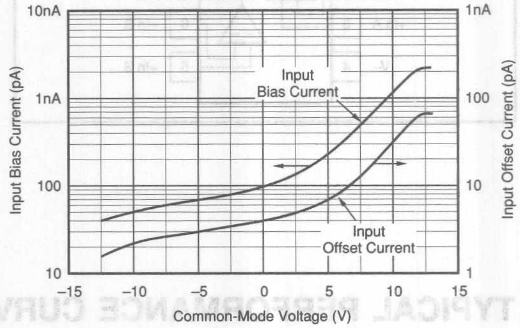
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



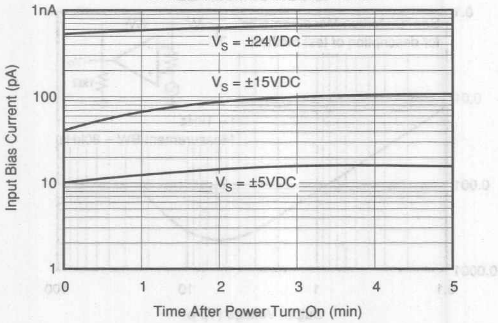
INPUT BIAS AND INPUT OFFSET CURRENT
vs TEMPERATURE



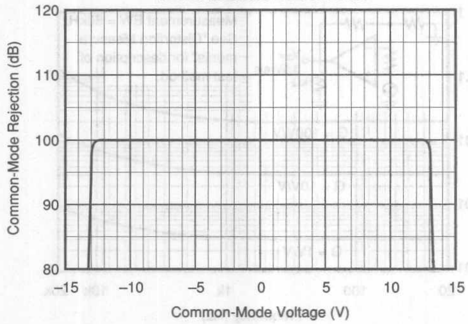
INPUT BIAS AND INPUT OFFSET CURRENT
vs INPUT COMMON-MODE VOLTAGE



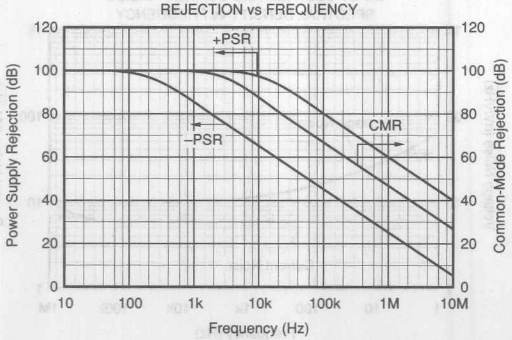
INPUT BIAS CURRENT
vs TIME FROM POWER TURN-ON



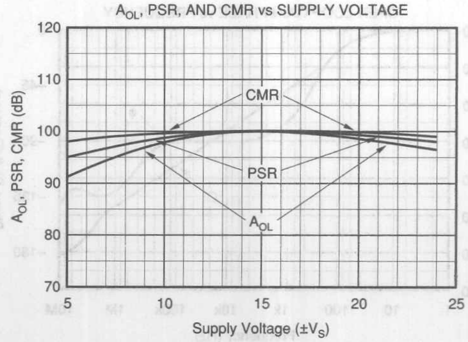
COMMON-MODE REJECTION
vs COMMON-MODE VOLTAGE



POWER SUPPLY AND COMMON-MODE
REJECTION vs FREQUENCY

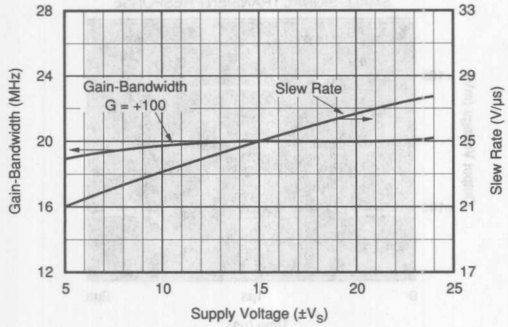


A_{OL}, PSR, AND CMR vs SUPPLY VOLTAGE

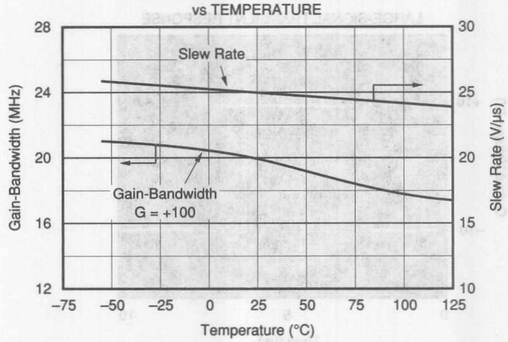


T_A = +25°C, V_S = ±15V unless otherwise noted.

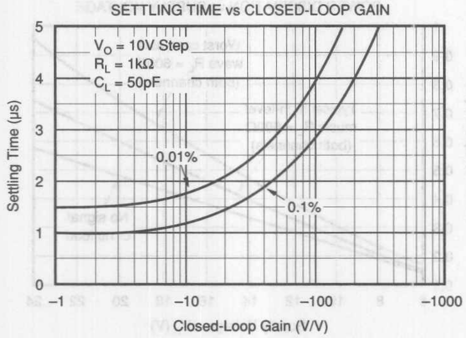
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



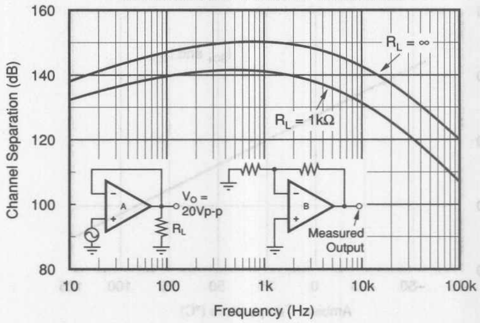
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



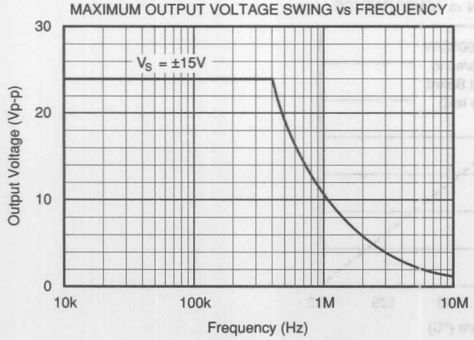
SETTLING TIME vs CLOSED-LOOP GAIN



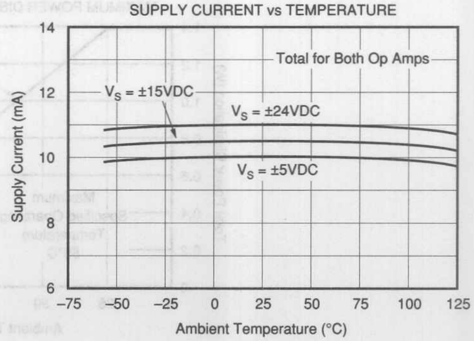
CHANNEL SEPARATION vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



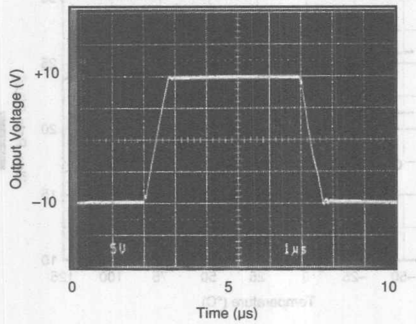
SUPPLY CURRENT vs TEMPERATURE



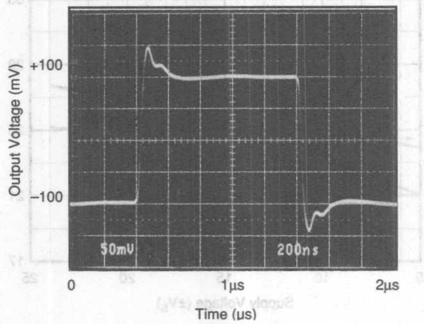
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

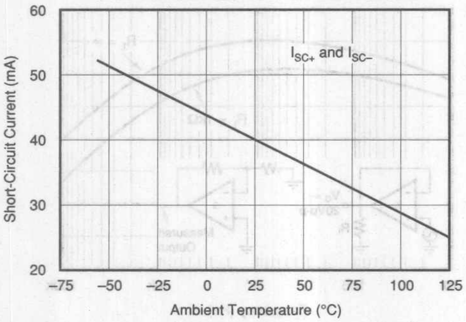
LARGE-SIGNAL TRANSIENT RESPONSE



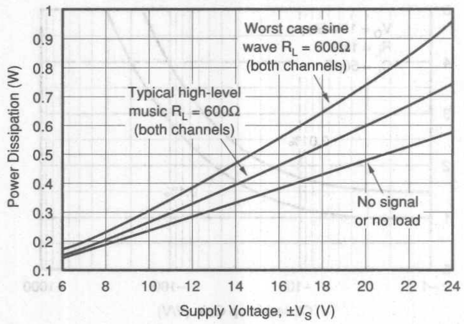
SMALL-SIGNAL TRANSIENT RESPONSE



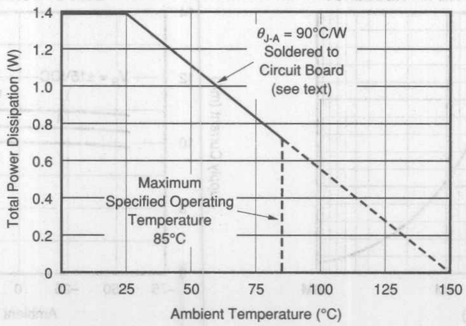
SHORT-CIRCUIT CURRENT vs TEMPERATURE



POWER DISSIPATION vs SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION vs TEMPERATURE



APPLICATIONS INFORMATION

The OPA2604 is unity-gain stable, making it easy to use in a wide range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 1µF tantalum capacitors are adequate.

DISTORTION MEASUREMENTS

The distortion produced by the OPA2604 is below the measurement limit of virtually all commercially available equipment. A special test circuit, however, can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source which can be referred to the input. Figure 1 shows a circuit which causes the op amp distortion to be 101 times greater than normally produced by the op amp. The addition of R_3 to the otherwise standard non-inverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101. This extends the measurement limit, including the effects of the signal-source purity, by a factor of 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with the Audio Precision System One which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

CAPACITIVE LOADS

The dynamic characteristics of the OPA2604 have been optimized for commonly encountered gains, loads and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. Figure 2 shows various circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details of analysis techniques and applications circuits.

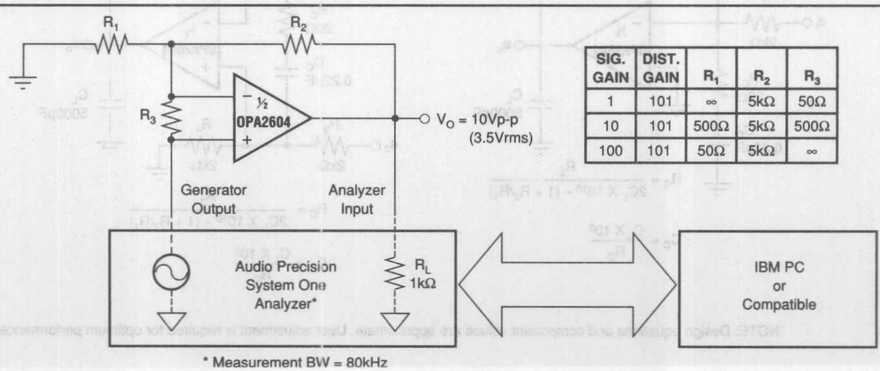
For the unity-gain buffer, Figure 2a, stability is preserved by adding a phase-lead network, R_C and C_C. Voltage drop across R_C will reduce output voltage swing with heavy loads. An alternate circuit, Figure 2b, does not limit the output with low load impedance. It provides a small amount of positive feedback to reduce the net feedback factor. Input impedance of this circuit falls at high frequency as op amp gain rolloff reduces the bootstrap action on the compensation network.

Figures 2c and 2d show compensation techniques for noninverting amplifiers. Like the follower circuits, the circuit in Figure 2d eliminates voltage drop due to load current, but at the penalty of somewhat reduced input impedance at high frequency.

Figures 2e and 2f show input lead compensation networks for inverting and difference amplifier configurations.

NOISE PERFORMANCE

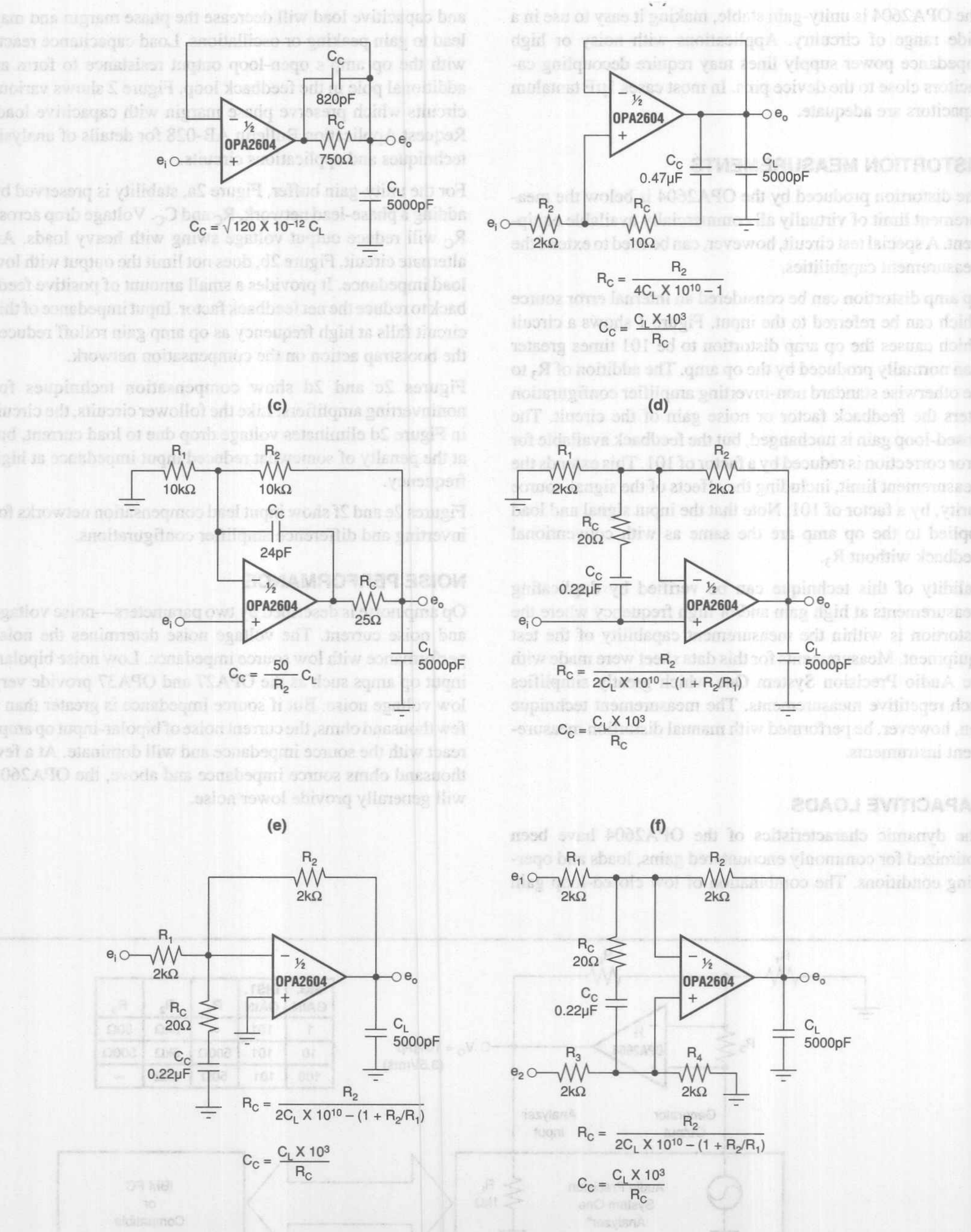
Op amp noise is described by two parameters—noise voltage and noise current. The voltage noise determines the noise performance with low source impedance. Low noise bipolar-input op amps such as the OPA27 and OPA37 provide very low voltage noise. But if source impedance is greater than a few thousand ohms, the current noise of bipolar-input op amps react with the source impedance and will dominate. At a few thousand ohms source impedance and above, the OPA2604 will generally provide lower noise.



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	5kΩ	50Ω
10	101	500Ω	5kΩ	500Ω
100	101	50Ω	5kΩ	∞

FIGURE 1. Distortion Test Circuit.

OPA2604 2 OPERATIONAL AMPLIFIERS



NOTE: Design equations and component values are approximate. User adjustment is required for optimum performance.

FIGURE 2. Driving Large Capacitive Loads.

POWER DISSIPATION

The OPA2604 is capable of driving 600Ω loads with power supply voltages up to ±24V. Internal power dissipation is increased when operating at high power supply voltage. The typical performance curve, Power Dissipation vs Power Supply Voltage, shows quiescent dissipation (no signal or no load) as well as dissipation with a worst case continuous sine wave. Continuous high-level music signals typically produce dissipation significantly less than worst case sine waves.

Copper leadframe construction used in the OPA2604 improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately ±40mA at 25°C. The limit current decreases with increasing temperature as shown in the typical curves.

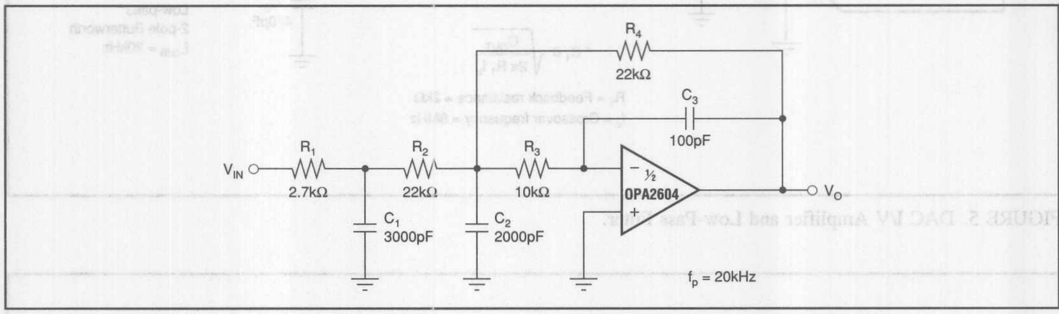


FIGURE 3. Three-Pole Low-Pass Filter.

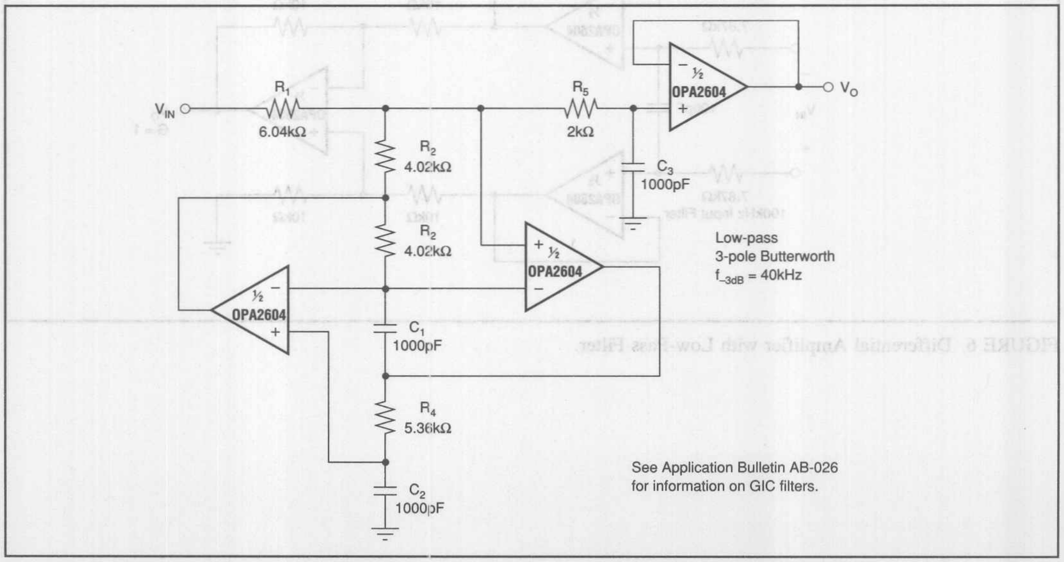


FIGURE 4. Three-Pole Generalized Immittance Converter (GIC) Low-Pass Filter.

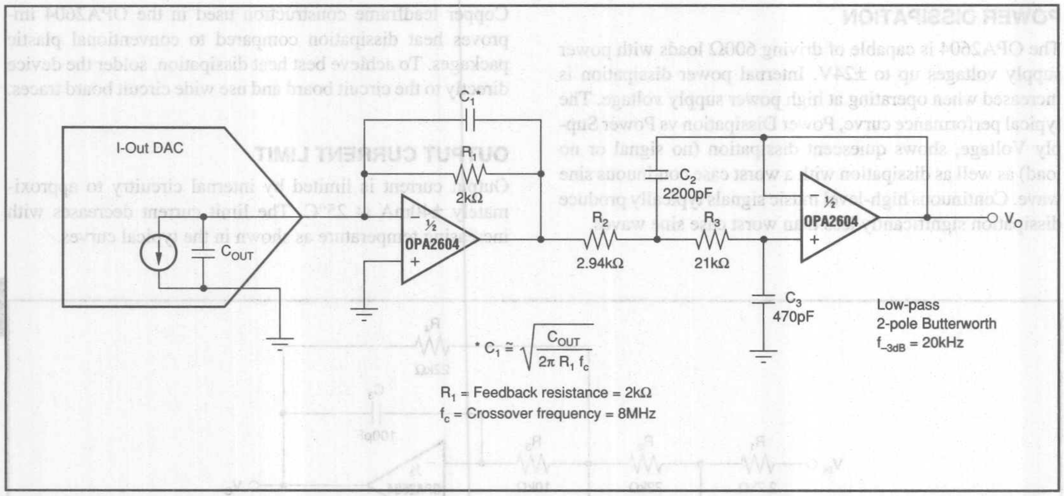


FIGURE 5. DAC I/V Amplifier and Low-Pass Filter.

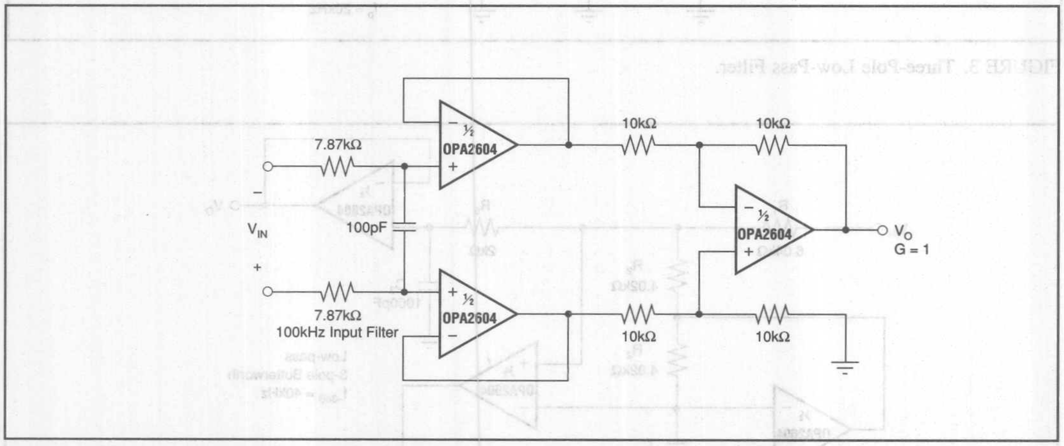


FIGURE 6. Differential Amplifier with Low-Pass Filter.

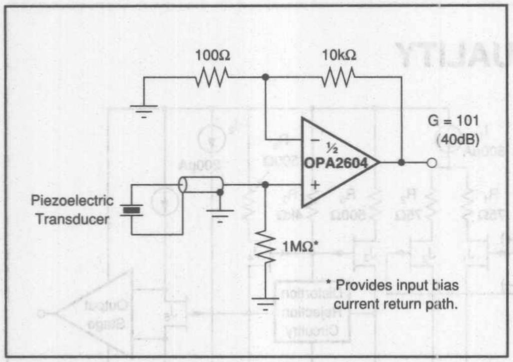


FIGURE 7. High Impedance Amplifier.

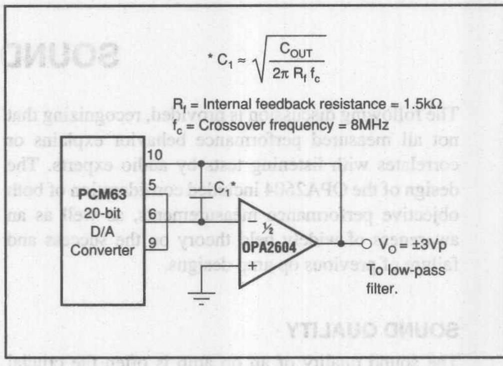


FIGURE 8. Digital Audio DAC I-V Amplifier.

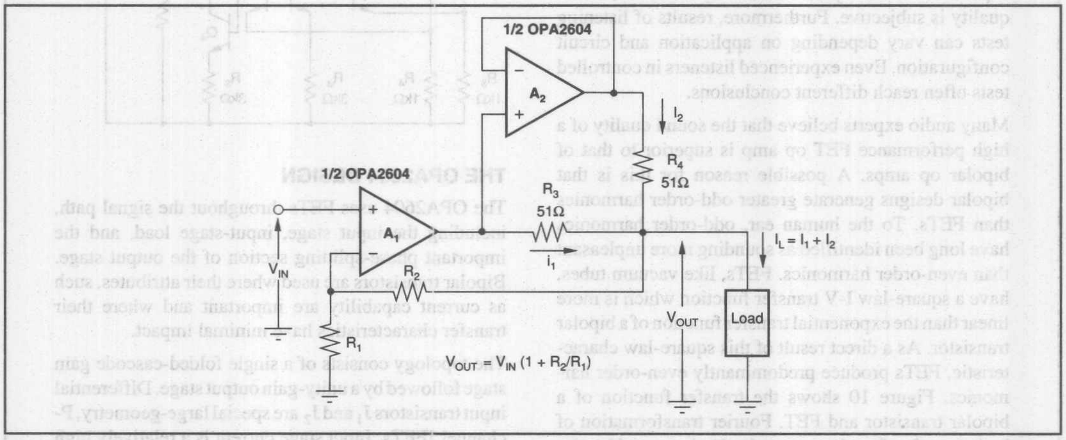


FIGURE 9. Using the Dual OPA2604 Op Amp to Double the Output Current to a Load.

SOUND QUALITY

The following discussion is provided, recognizing that not all measured performance behavior explains or correlates with listening tests by audio experts. The design of the OPA2604 included consideration of both objective performance measurements, as well as an awareness of widely held theory on the success and failure of previous op amp designs.

SOUND QUALITY

The sound quality of an op amp is often the crucial selection criteria—even when a data sheet claims exceptional distortion performance. By its nature, sound quality is subjective. Furthermore, results of listening tests can vary depending on application and circuit configuration. Even experienced listeners in controlled tests often reach different conclusions.

Many audio experts believe that the sound quality of a high performance FET op amp is superior to that of bipolar op amps. A possible reason for this is that bipolar designs generate greater odd-order harmonics than FETs. To the human ear, odd-order harmonics have long been identified as sounding more unpleasant than even-order harmonics. FETs, like vacuum tubes, have a square-law I-V transfer function which is more linear than the exponential transfer function of a bipolar transistor. As a direct result of this square-law characteristic, FETs produce predominantly even-order harmonics. Figure 10 shows the transfer function of a bipolar transistor and FET. Fourier transformation of both transfer functions reveals the lower odd-order harmonics of the FET amplifier stage.

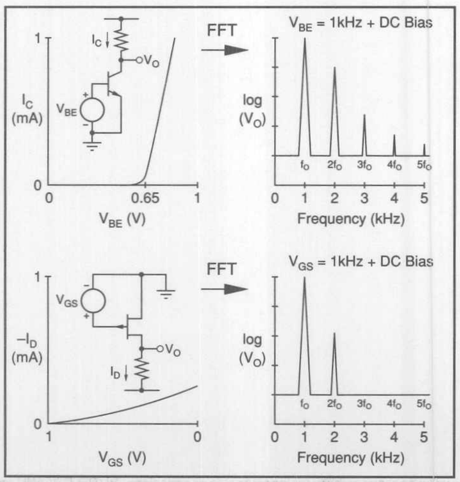
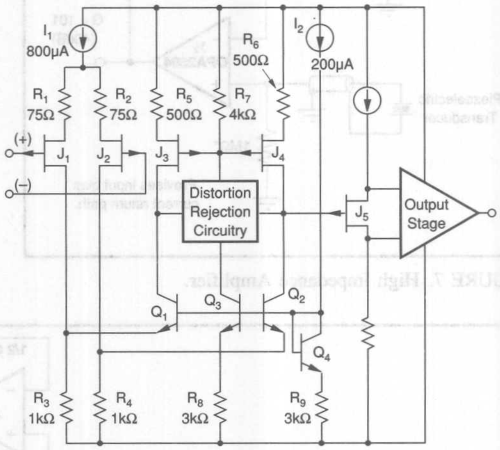


FIGURE 10. I-V and Spectral Response of NPN and JFET.



THE OPA2604 DESIGN

The OPA2604 uses FETs throughout the signal path, including the input stage, input-stage load, and the important phase-splitting section of the output stage. Bipolar transistors are used where their attributes, such as current capability are important and where their transfer characteristics have minimal impact.

The topology consists of a single folded-cascode gain stage followed by a unity-gain output stage. Differential input transistors J_1 and J_2 are special large-geometry, P-channel JFETs. Input stage current is a relatively high 800µA, providing high transconductance and reducing voltage noise. Laser trimming of stage currents and careful attention to symmetry yields a nearly symmetrical slew rate of ±25V/µs.

The JFET input stage holds input bias current to approximately 100pA, or roughly 3000 times lower than common bipolar-input audio op amps. This dramatically reduces noise with high-impedance circuitry.

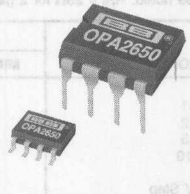
The drains of J_1 and J_2 are cascoded by Q_1 and Q_2, driving the input stage loads, FETs J_3 and J_4. Distortion reduction circuitry (patent pending) linearizes the open-loop response and increases voltage gain. The 20MHz bandwidth of the OPA2604 further reduces distortion through the user-connected feedback loop.

The output stage consists of a JFET phase-splitter loaded into high speed all-NPN output drivers. Output transistors are biased by a special circuit to prevent cutoff, even with full output swing into 600Ω loads.

The two channels of the OPA2604 are completely independent, including all bias circuitry. This eliminates any possibility of crosstalk through shared circuits—even when one channel is overdriven.

BURR - BROWN®

OPA2650



Dual Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- LOW POWER: 50mW/Amp
- UNITY GAIN STABLE BANDWIDTH: 360MHz
- FAST SETTLING TIME: 20ns to 0.01%
- LOW HARMONICS: –77dBc at 5MHz
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.025°
- HIGH OUTPUT CURRENT: 85mA

APPLICATIONS

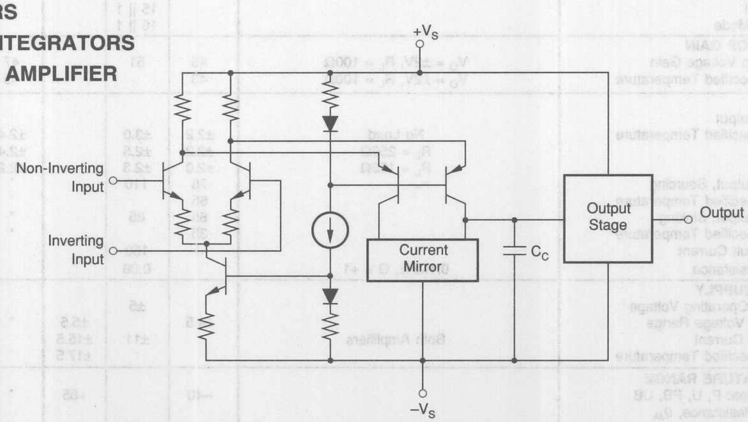
- HIGH RESOLUTION VIDEO
- BASEBAND AMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- ACTIVE FILTERS
- HIGH SPEED INTEGRATORS
- DIFFERENTIAL AMPLIFIER

DESCRIPTION

The OPA2650 is a dual, low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 360MHz as well as a 12-bit settling time of only 20ns. The low distortion allows its use in communications applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA2650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA2650 is also available in single (OPA650) and quad (OPA4650) configurations.



NOTE: Diagram shows only one-half of the OPA2650.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

$T_A = +25°C$, $V_S = ±5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

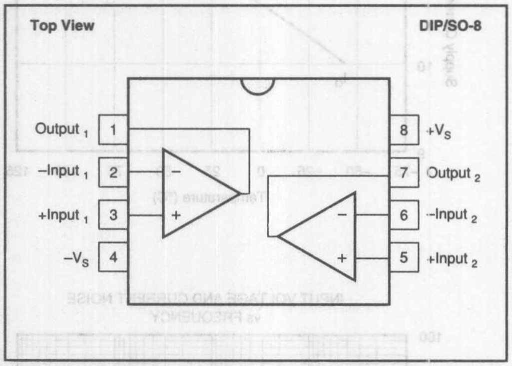
		OPA2650P, U			OPA2650PB, UB			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
FREQUENCY RESPONSE								
Closed-Loop Bandwidth[2]	G = +1		360			*[1]		MHz
	G = +2		108			*		MHz
	G = +5		32			*		MHz
	G = +10		16			*		MHz
Gain Bandwidth Product			160					MHz
Slew Rate	G = +1, 2V Step		240			*		V/µs
Over Specified Temperature			220			*		V/µs
Rise Time	0.2V Step		1			*		ns
Fall Time	0.2V Step		1			*		ns
Settling Time 0.01%	G = +1, 2V Step		20			*		ns
0.1%	G = +1, 2V Step		11			*		ns
1%	G = +1, 2V Step		6.7			*		ns
Spurious Free Dynamic Range	G = +1, f = 5.0MHz, V_O = 2Vp-p							
	$R_L = 100\Omega$		72			*		dBc
	$R_L = 402\Omega$		77			*		dBc
Differential Gain	G = +1, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$		0.01			*		%
Differential Phase	G = +1, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$		0.025			*		Degrees
Bandwidth for 0.1dB Gain Flatness	G = +2		21			*		MHz
Crosstalk	Input Referred, 5MHz, Channel-to-Channel		–84			*		dB
INPUT OFFSET VOLTAGE								
Input Offset Voltage			±1	±5		±1	±3	mV
Average Drift			±3			*		µV/°C
Power Supply Rejection (+V_S)	V_S = ±4.5V to ±5.5V	60	76		70	*		dB
(–V_S)		47	54		50	*		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		5	20		*	10	µA
Over Temperature				30			20	µA
Input Offset Current	V_{CM} = 0V		0.5	1		0.2	0.5	µA
Over Temperature				3			2	µA
INPUT NOISE								
Input Voltage Noise								
Noise Density, f = 100Hz			43			*		nV/√Hz
f = 10kHz			9.4			*		nV/√Hz
f = 1MHz			8.4			*		nV/√Hz
f = 1MHz to 100MHz			8.4			*		nV/√Hz
Integrated Noise, BW = 10Hz to 100MHz			84			*		µVp-p
Input Bias Current Noise								
Current Noise Density, f = 0.1MHz to 100MHz			1.2			*		pA/√Hz
Noise Figure (NF)								
	$R_S = 10k\Omega$		4			*		dB
	$R_S = 50\Omega$		19.5			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range			±2.8			*		V
Over Specified Temperature		±2.2			*			V
Common-Mode Rejection	V_{CM} = ±0.5V	65	90		70	*		dB
INPUT IMPEDANCE								
Differential			15 || 1			*		KΩ || pF
Common-Mode			16 || 1			*		MΩ || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±2V, $R_L = 100\Omega$	45	51		47	*		dB
Over Specified Temperature	V_O = ±2V, $R_L = 100\Omega$	43			45			dB
OUTPUT								
Voltage Output								
Over Specified Temperature	No Load	±2.2	±3.0		±2.4	*		V
	$R_L = 250\Omega$	±2.2	±2.5		±2.4	*		V
	$R_L = 100\Omega$	±2.0	±2.3		±2.2	*		V
Current Output, Sourcing		75	110		*	*		mA
Over Specified Temperature		65			*			mA
Current Output, Sinking		65	85		*	*		mA
Over Specified Temperature		35			*			mA
Short Circuit Current			150			*		mA
Output Resistance	0.1MHz, G = +1		0.08			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Operating Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current	Both Amplifiers		±11	±15.5		*	±13.5	mA
Over Specified Temperature				±17.5		*	±16	mA
TEMPERATURE RANGE								
Specification: P, U, PB, UB		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
P			100			*		°C/W
U			125			*		°C/W

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The OPA2650 is nominally compensated assuming 2pF parasitic load. The demonstration board, DEM-265xP, shows a low parasitic layout for this device.

ABSOLUTE MAXIMUM RATINGS

Supply	±5.5V
Internal Power Dissipation	See Thermal Considerations
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

PIN CONFIGURATION



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA2650U, UB	SO-8 Surface Mount	182
OPA2650P, PB	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION(1)

MODEL	PACKAGE	TEMPERATURE RANGE
OPA2650U, UB	SO-8 Surface Mount	–40°C to +85°C
OPA2650P, PB	8-Pin Plastic DIP	–40°C to +85°C

NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by pin 8. Refer to mechanical section for the location.

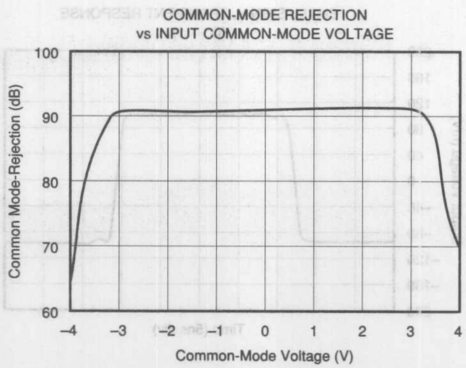
ELECTROSTATIC DISCHARGE SENSITIVITY

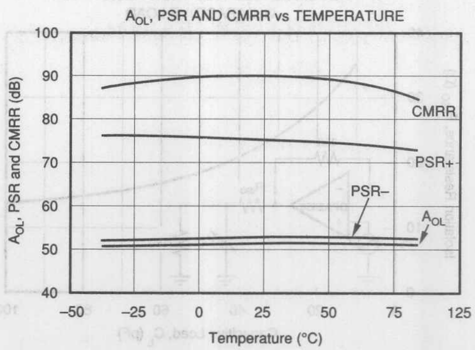
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

TYPICAL PERFORMANCE CURVES

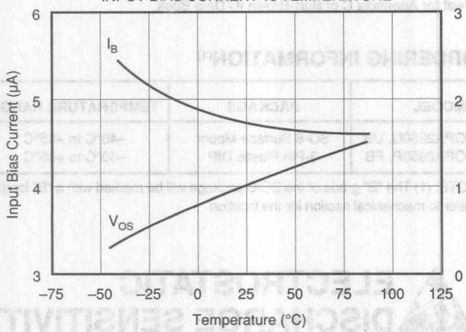
$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.



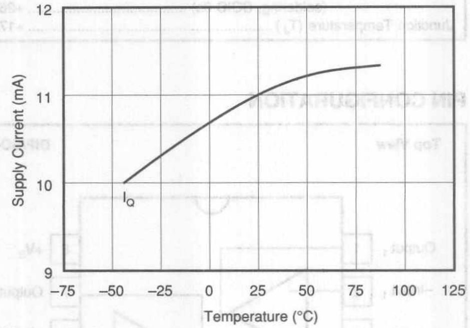


$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

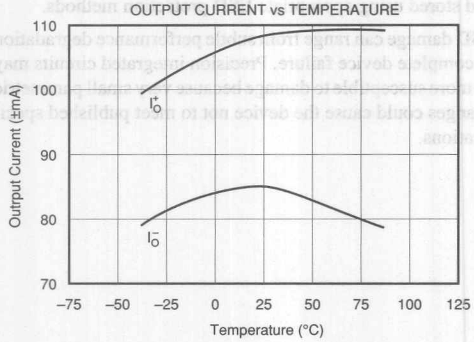
INPUT BIAS CURRENT vs TEMPERATURE



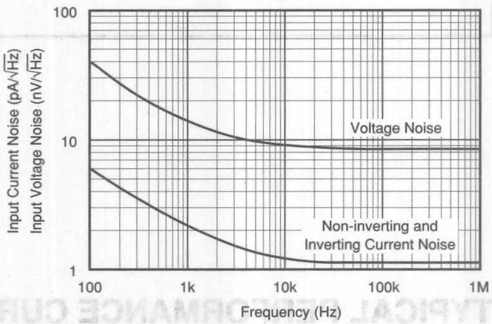
SUPPLY CURRENT vs TEMPERATURE



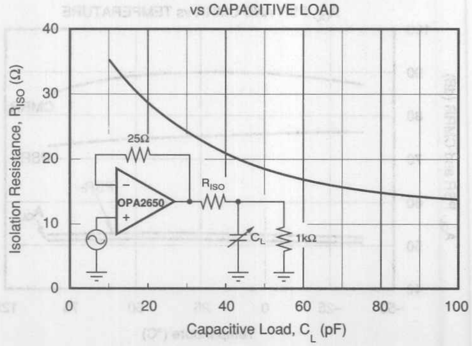
OUTPUT CURRENT vs TEMPERATURE



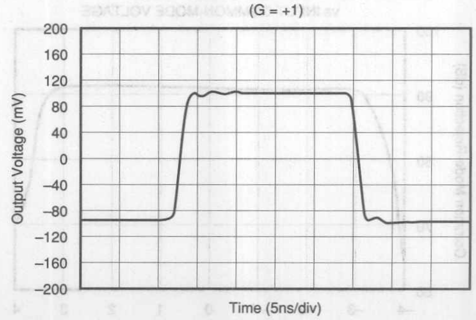
INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY



RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD

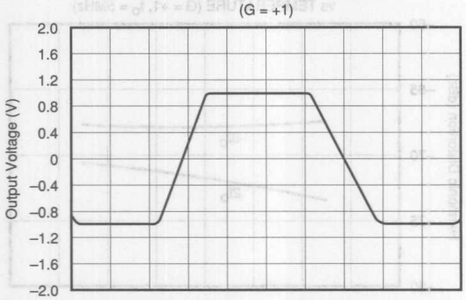


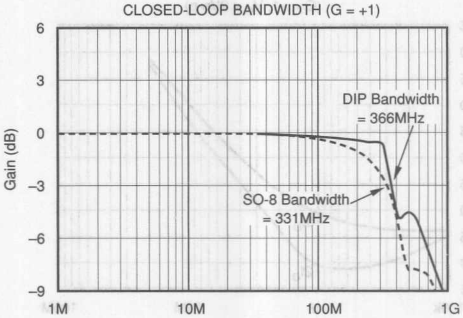
SMALL SIGNAL TRANSIENT RESPONSE (G = +1)

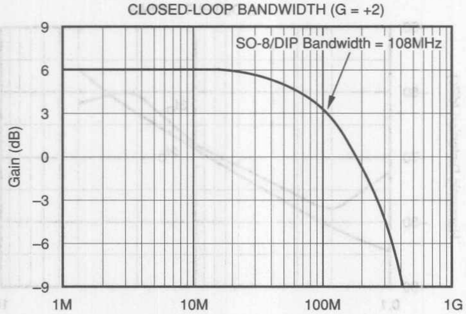


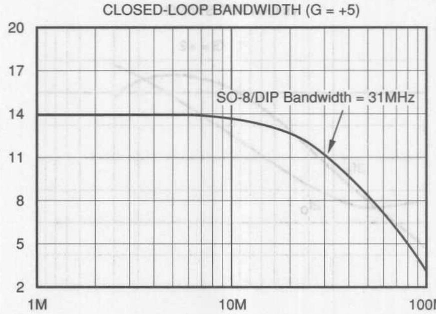
TYPICAL PERFORMANCE CURVES (CONT)

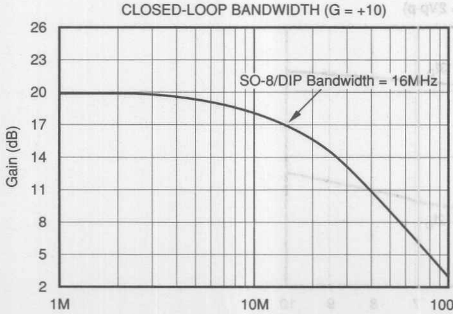
$T_A = +25°C$, $V_S = ±5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

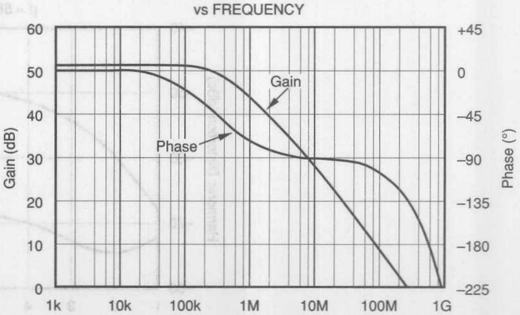








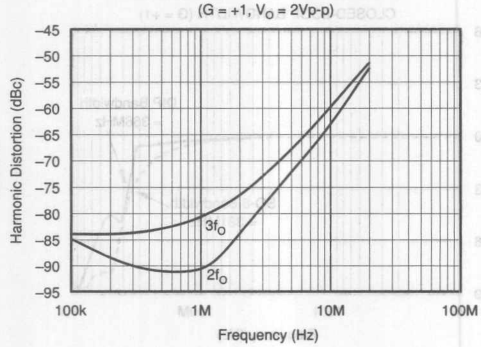




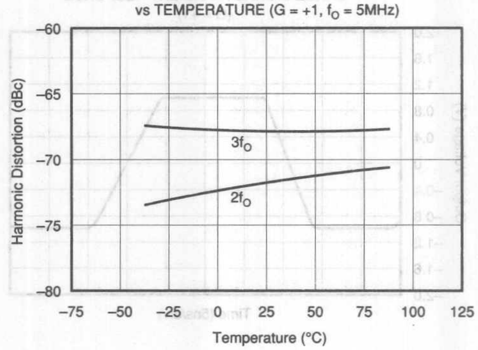
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

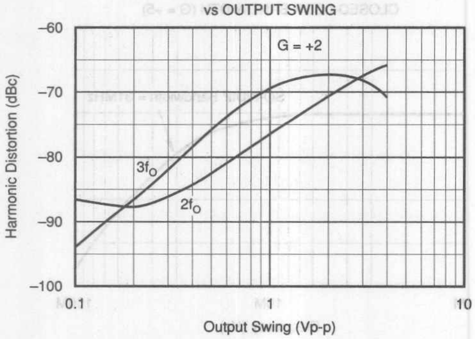
HARMONIC DISTORTION vs FREQUENCY (G = +1, V_O = 2Vp-p)



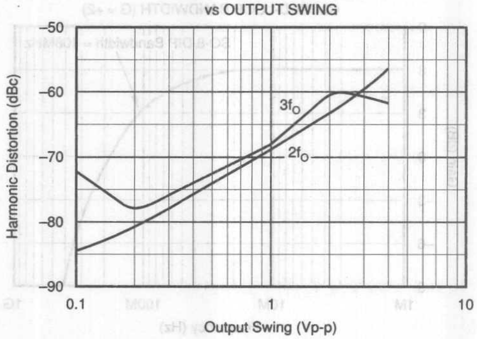
HARMONIC DISTORTION vs TEMPERATURE (G = +1, f_O = 5MHz)



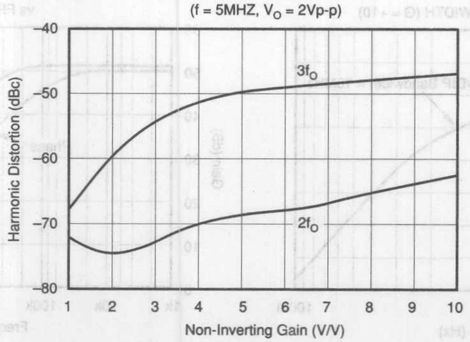
5MHz HARMONIC DISTORTION vs OUTPUT SWING



10MHz HARMONIC DISTORTION vs OUTPUT SWING



HARMONIC DISTORTION vs GAIN (f = 5MHZ, V_O = 2Vp-p)



DISCUSSION OF PERFORMANCE

The OPA2650 is a dual low power, wideband voltage feedback operational amplifier. Each channel is internally compensated to provide unity gain stability. The OPA2650's voltage feedback architecture features true differential and fully symmetrical inputs. This minimizes offset errors, making the OPA2650 well suited for implementing filter and instrumentation designs. As a dual operational amplifier, OPA2650 is an ideal choice for designs requiring multiple channels where reduction of board space, power dissipation and cost are critical. Its AC performance is optimized to provide a gain bandwidth product of 160MHz and a fast 0.1% settling time of 11ns, which is an important consideration in high speed data conversion applications. Along with its excellent settling characteristics, the low DC input offset of ±1mV and drift of ±3μV/°C support high accuracy requirements. In applications requiring a higher slew rate and wider bandwidth, such as video and high bit rate digital communications, consider the dual current feedback OPA2658.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA2650 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the two power pins to high frequency 0.1μF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA2650. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Surface mount feedback resistors directly adjacent to the output and inverting input pins work well for the dual pinout. Other network components, such as non-inverting input termination resistors, should also be placed close to the package.

Even with a low parasitic capacitance shunting the resistor, excessively high resistor values can create significant time constants and degrade performance. Good metal film or surface mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this adds a pole and/or zero below 500MHz that can affect circuit operation. Keep resistor values as low as possible consistent with output loading considerations. The 402Ω feedback used for the Typical Performance Plots is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for a unity gain follower. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA2650 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) Socketing a high speed part like the OPA2650 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable response. Best results

mount pins (e.g., McKenzie Technology #710C) can give good results.

The OPA2650 is nominally specified for operation using ±5V power supplies. A 10% tolerance on the supplies, or an ECL –5.2V for the negative supply, is within the maximum specified total supply voltage of 11V. Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single supply operation. Figure 1 shows one approach to single-supply operation.

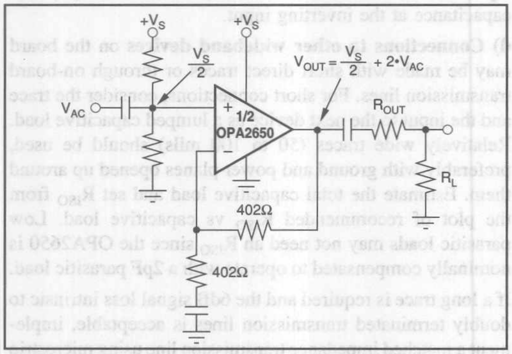


FIGURE 1. Single Supply Operation.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 2 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current.

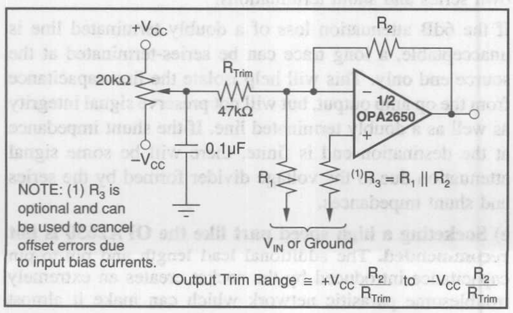


FIGURE 2. Offset Voltage Trim.

ESD damage has been well recognized for MOSFET devices, but any semiconductor device is vulnerable to this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are strongly recommended when handling the OPA2650.

OUTPUT DRIVE CAPABILITY

The OPA2650 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA2650 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as driving A/D converters require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA2650 maintains very low-closed loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

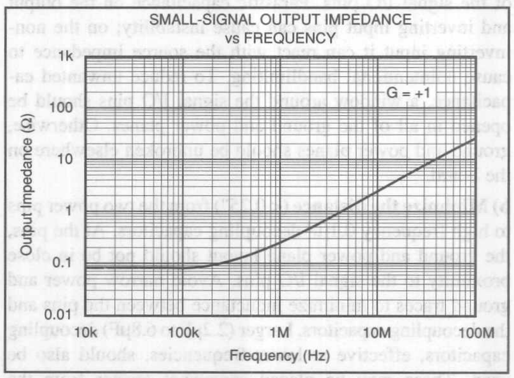


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA2650 will not require heatsinking under most operating conditions. Maximum desired junction temperature will limit the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D\theta_{JA}$. The total internal power dissipation (P_D) is a combination of the total quiescent power for all channels (P_{DQ}) and the sum of the powers dissipated in each of the output stages (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total

resistive load, be at a maximum when the output is a fixed DC voltage equal to 1/2 of either supply voltage (assuming equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \cdot R_L)$ where R_L includes feedback network loading. Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation. As an example, compute the maximum T_J for an OPA2650U at $A_V = +2$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, $\pm V_S = \pm 5V$, with both outputs at $|V_S/2|$, and the specified maximum $T_A = +85°C$. $P_D = 10V \cdot 17.5mA + 2 \cdot (5^2)/(4 \cdot (100\Omega \| 804\Omega)) = 316mW$. Maximum $T_J = +85°C + 0.316W \cdot 125°C/W = 124°C$.

DRIVING CAPACITIVE LOADS

The OPA2650's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be isolated by connecting a small resistance, usually 15Ω to 30Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

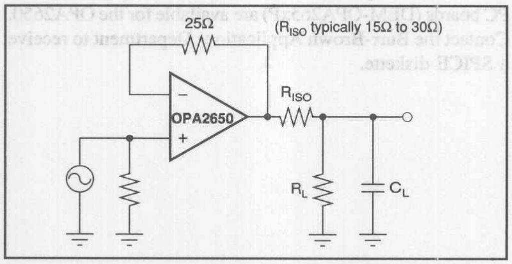


FIGURE 4. Driving Capacitive Loads.

FREQUENCY RESPONSE COMPENSATION

Each channel of the OPA2650 is internally compensated to be stable at unity gain with a nominal 60° phase margin. This lends itself well to wideband integrator and buffer applications. Phase margin and frequency response flatness will improve at higher gains. Recall that an inverting gain of –1 is equivalent to a gain of +2 for bandwidth purposes, i.e., noise gain = 2. The external compensation techniques developed for voltage feedback op amps can be applied to this device. For example, in the non-inverting configuration, inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, thereby limiting the bandwidth for the inverting input signal through the gain-bandwidth product.

At higher gains, the gain-bandwidth of this voltage feedback topology will limit bandwidth according to the open-loop frequency response curve. For applications requiring a wider bandwidth at higher gains, consider the dual current feedback model, OPA2658. In applications where a large feedback resistor is required (such as photodiode transimpedance circuits), precautions must be taken to avoid gain peaking due to the pole formed by the feedback resistor and the summing junction capacitance. This pole can be compensated by connecting a small capacitor in parallel with the feedback resistor, creating a cancelling zero term. In other high-gain applications, use of a three-resistor "T" connection will reduce the feedback network impedance which reacts with the parasitic capacitance at the summing node.

PULSE SETTLING TIME

High speed amplifiers like the OPA2650 are capable of extremely fast settling time with a pulse input. Excellent frequency response flatness and phase linearity are required to get the best settling times. As shown in the specifications table, settling time for a ±1V step at a gain of +1 for the OPA2650 is extremely fast. The specification is defined as the time required, after the input transition, for the output to settle within a specified error band around its final value. For a 2V step, 1% settling corresponds to an error band of ±20mV, 0.1% to an error band of ±2mV, and 0.01% to an error band of ±0.2mV. For the best settling times, particularly into an ADC capacitive load, little or no peaking in the frequency response can be allowed. Using the recommended R_{ISO} for capacitive loads will limit this peaking and reduce the settling times. Fast, extremely fine scale settling (0.01%) requires close attention to ground return currents in the supply decoupling capacitors. For highest performance, consider the OPA642 which isolates the output stage decoupling from the rest of the amplifier.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. The percentage change in closed-loop gain over a specified change in output voltage level is defined as DG. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. DG and DP are both specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA2650's harmonic distortion characteristics into a 100Ω load are shown versus frequency and power output in the typical performance curves. Distortion can be significantly improved by increasing the load resistance as illustrated in Figure 5. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

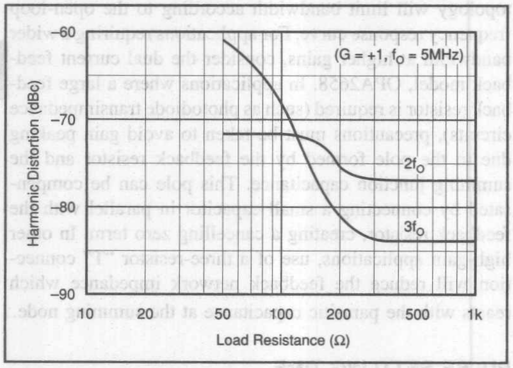


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

CROSSTALK

Crosstalk is the undesired result of the signal of one channel mixing with and reproducing itself in the output of the other channel. Crosstalk is inclined to occur in most multichannel integrated circuits. In dual devices, the effect of crosstalk is measured by driving one channel and observing the output of the undriven channel over various frequencies. The magnitude of this effect is referenced in terms of channel-to-channel crosstalk and expressed in decibels. "Input referred" points to the fact that there is a direct correlation between gain and crosstalk, therefore at increased gain, crosstalk also increases by a factor equal to that of the gain. Figure 6 illustrates the measured effect of crosstalk in the OPA2650U.

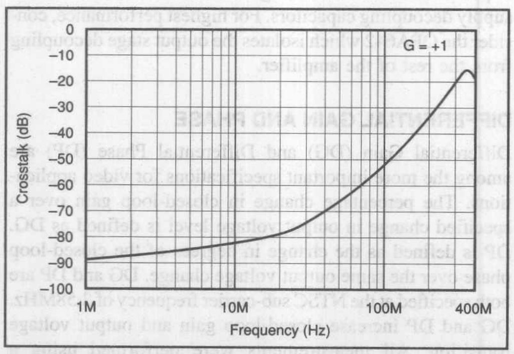


FIGURE 6. Channel-to-Channel Crosstalk.

NOISE FIGURE

The OPA2650 voltage spectral density is specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA2650's Noise Figure Vs Source Resistance is shown in Figure 7.

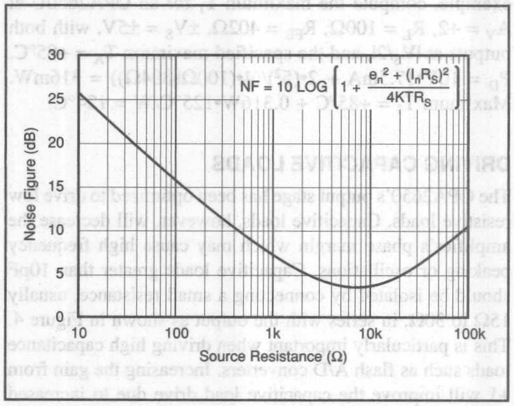


FIGURE 7. Noise Figure vs Source Resistance.

SPICE MODELS AND EVALUATION BOARD

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models and evaluation PC boards (DEM-OPA265xP) are available for the OPA2650. Contact the Burr-Brown Applications Department to receive a SPICE diskette.

TYPICAL APPLICATION

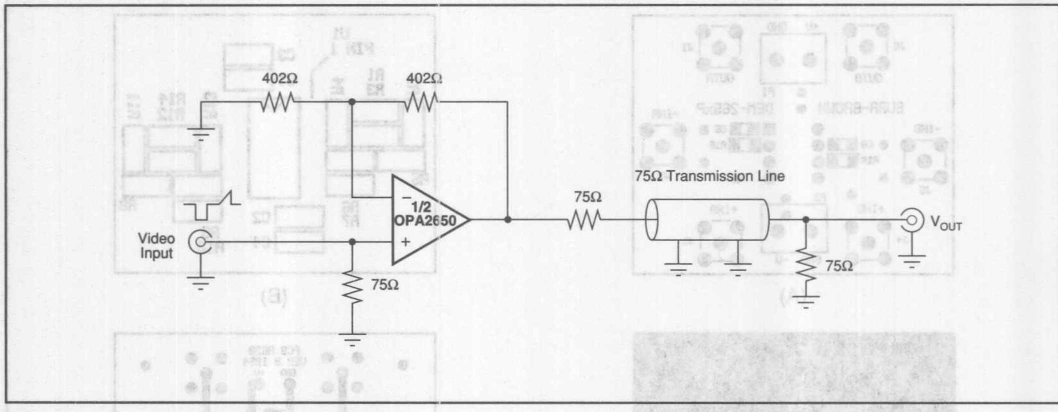


FIGURE 8. Low Distortion Video Amplifier.

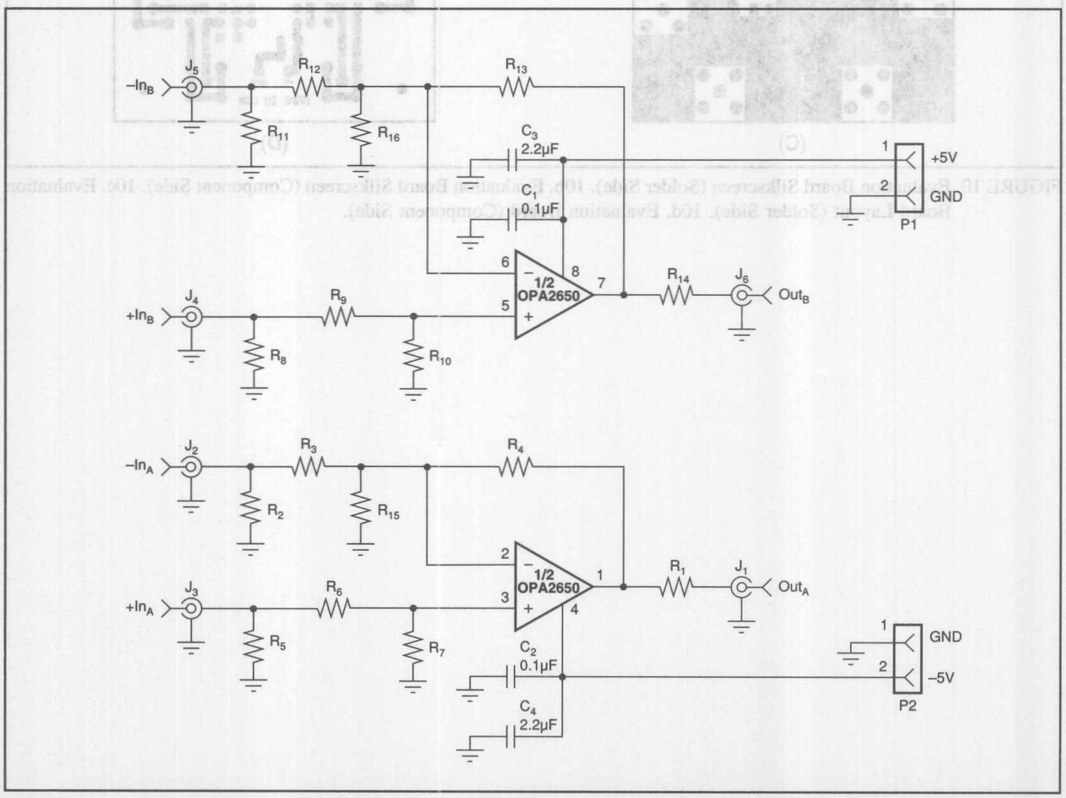


FIGURE 9. Layout Detail for DEM-OPA265X Demonstration Board.

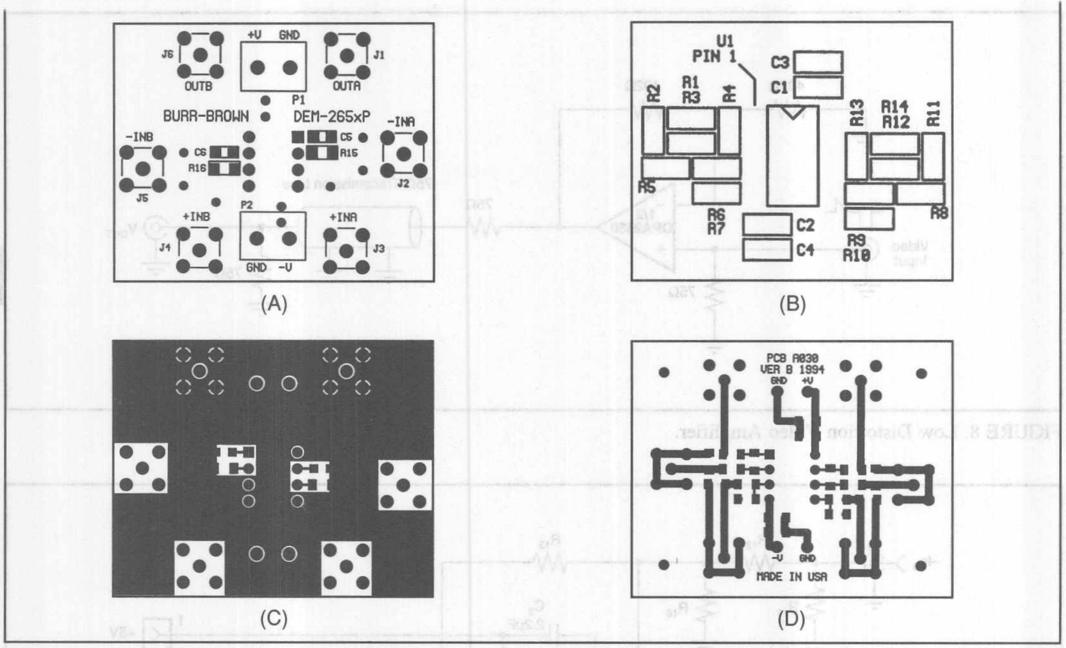
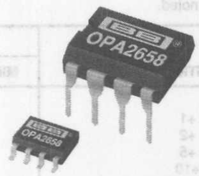


FIGURE 10. Evaluation Board Silkscreen (Solder Side). 10b. Evaluation Board Silkscreen (Component Side). 10c. Evaluation Board Layout (Solder Side). 10d. Evaluation Board (Component Side).

BURR - BROWN®



OPA2658

Dual Wideband, Low Power, Current Feedback OPERATIONAL AMPLIFIER

FEATURES

- UNITY GAIN STABLE BANDWIDTH: 750MHz
- LOW POWER: 50mW/Channel
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.01%/0.03°
- HIGH SLEW RATE: 1700V/μs
- PACKAGE: 8-Pin DIP and 8-Pin SO-8

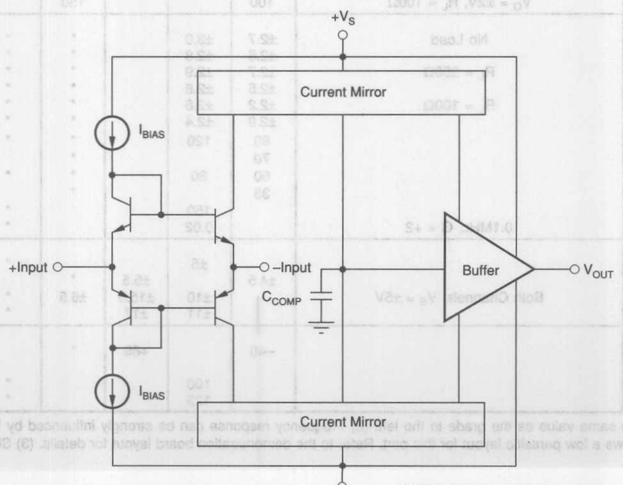
APPLICATIONS

- MEDICAL IMAGING
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- COMMUNICATIONS
- PULSE AMPLIFIERS
- ADC/DAC GAIN AMPLIFIER
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER

DESCRIPTION

The OPA2658 is a dual, ultra-wideband, low power current feedback video operational amplifier featuring high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low quiescent current make the OPA2658 a perfect choice for numerous video, imaging and communications applications.

The OPA2658 is optimized for low gain operation, and is also available in single, OPA658 and quad, OPA4658 configurations.



NOTE: Diagram reflects only one-half of the OPA2658

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

$T_A = +25°C$, $V_S = ±5V$, $R_L = 100Ω$, $R_{FB} = 402Ω$, unless otherwise noted.

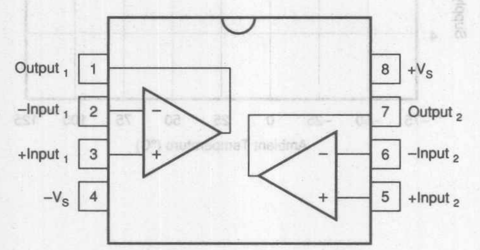
		OPA2658P, U			OPA2658PB, UB			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE								
Closed-Loop Bandwidth(2)	G = +1		800			*(1)		MHz
	G = +2		500			*		MHz
	G = +5		210			*		MHz
	G = +10		130			*		MHz
Slew Rate(3)	G = +2, 2V Step		1700		1000	*		V/µs
At Minimum Specified Temperature			1500		900	*		V/µs
Settling Time: 0.01%	G = +2, 2V Step		15			*		ns
0.1%	G = +2, 2V Step		12.6			*		ns
1%	G = +2, 2V Step		4.8			*		ns
Spurious Free Dynamic Range	f = 5MHz, G = +2, V_O = 2Vp-p		68			*		dBc
	f = 20MHz, G = +2, V_O = 2Vp-p		55			*		dBc
Third-Order Intercept Point	f = 10MHz, 4dBm, each tone		39			*		dBm
Differential Gain	G = +2, NTSC, V_O = 1.4Vp-p, R_L = 150Ω		0.01			*		%
Differential Phase	G = +2, NTSC, V_O = 1.4Vp-p, R_L = 150Ω		0.03			*		degrees
Crosstalk	Input Referred, 5MHz, channel-to-channel		78			*		dB
OFFSET VOLTAGE								
Input Offset Voltage			±3	±5.5		*	±4.5	mV
Over Temperature			±5	±8		*	±7	mV
Power Supply Rejection	V_S = ±4.5 to ±5.5V	55	64		58	*		dB
INPUT BIAS CURRENT								
Non-Inverting	V_{CM} = 0V		±4.0	±30		*	±18	µA
Over Temperature			±10	±80		*	±35	µA
Inverting	V_{CM} = 0V		±2.9	±35		*	*	µA
Over Temperature			±30	±75		*	*	µA
NOISE								
Input Voltage Noise Density								
f = 100Hz			11			*		nV/√Hz
f = 10kHz			2.7			*		nV/√Hz
f = 50kHz			2.7			*		nV/√Hz
f_B = 100Hz to 200MHz			38			*		µVrms
Input Bias Current Noise Density								
Inverting: f =10MHz			12.6			*		pA/√Hz
Non-Inverting: f =10MHz			12.6			*		pA/√Hz
Noise Figure (NF)	R_S = 50Ω		10			*		dBm
	R_S = 100Ω		8			*		dBm
INPUT VOLTAGE RANGE								
Common-mode Input Range			±2.9			*		V
Over Temperature		±2.5			*			V
Common-mode Rejection	V_{CM} = ±1V	45	50		*	*		dB
INPUT IMPEDANCE								
Non-Inverting			500 ‖ 1			*		kΩ ‖ pF
Inverting			50			*		Ω
OPEN-LOOP TRANSIMPEDANCE								
Open-loop Transimpedance	V_O = ±2V, R_L = 100Ω	150	180		200	*		kΩ
Over Temperature	V_O = ±2V, R_L = 100Ω	100			150			kΩ
OUTPUT								
Voltage Output	No Load	±2.7	±3.0		*	*		V
Over Temperature		±2.5	±2.8		*	*		V
Voltage Output	R_L = 250Ω	±2.7	±2.9		*	*		V
Over Temperature		±2.5	±2.8		*	*		V
Voltage Output	R_L = 100Ω	±2.2	±2.6		*	*		V
Over Temperature		±2.0	±2.4		*	*		V
Output Current, Sourcing		80	120		*	*		mA
Over Temperature		70			*			mA
Output Current, Sinking		60	80		*	*		mA
Over Temperature		35			*			mA
Short Circuit Current			150			*		mA
Output Resistance	0.1MHz, G = +2		0.02			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Operating Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current	Both Channels, V_S = ±5V		±10	±15.5	±6.5	*	±11.5	mA
Over Temperature			±11	±17		*	±13	mA
TEMPERATURE RANGE								
Specification: P, U, PB, UB		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
P 8-Pin DIP			100			*		°C/W
U SO-8			125			*		°C/W

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The demonstration board, DEM-OPA65X shows a low parasitic layout for this part. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

ABSOLUTE MAXIMUM RATINGS

Supply	±5.5V
Internal Power Dissipation	See Thermal Considerations
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

PIN CONFIGURATION



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA2658P, PB OPA2658U, UB	8-Pin Plastic DIP 8-Pin Plastic SO-8	006 182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION[1]

MODEL	PACKAGE	TEMPERATURE RANGE
OPA2658P, PB OPA2658U, UB	8-Pin Plastic DIP 8-Pin Plastic SO-8	–40°C to +85°C –40°C to +85°C

NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by pin 8. Refer to mechanical section for the location.

ELECTROSTATIC DISCHARGE SENSITIVITY

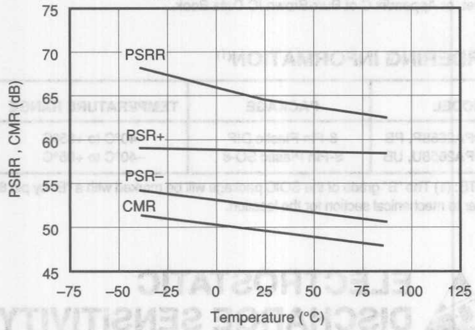
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

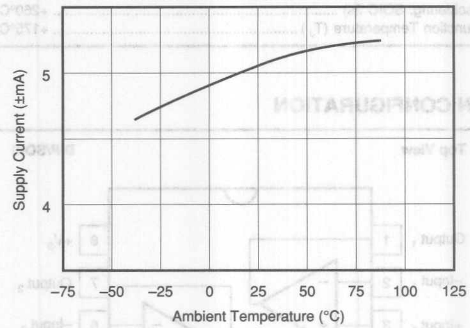
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, unless otherwise noted.

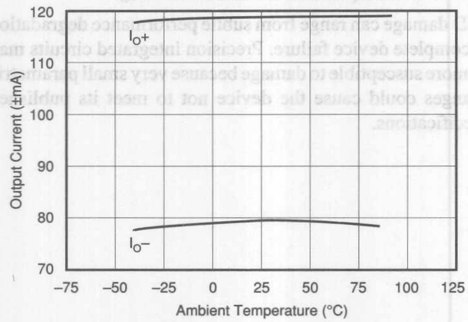
PSRR AND CMR vs TEMPERATURE



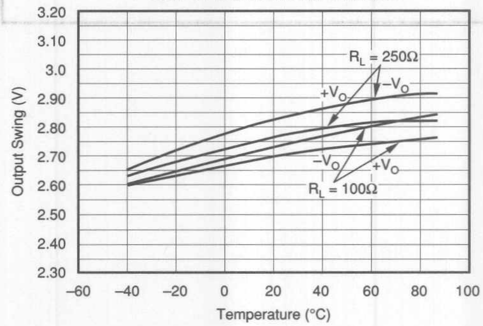
SUPPLY CURRENT vs TEMPERATURE



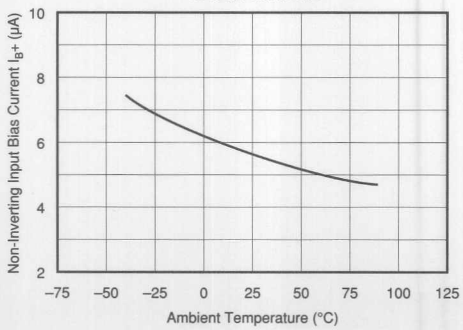
OUTPUT CURRENT vs TEMPERATURE



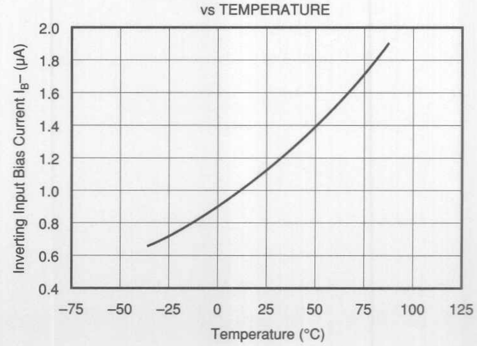
OUTPUT SWING vs TEMPERATURE



NON-INVERTING INPUT BIAS CURRENT
vs TEMPERATURE



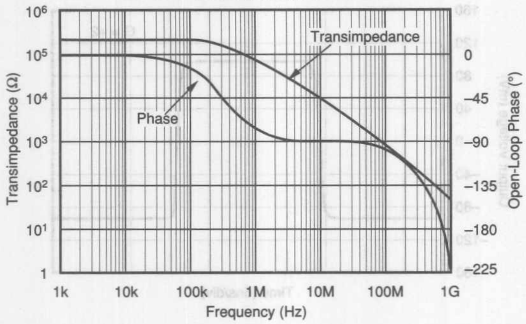
INVERTING INPUT BIAS CURRENT
vs TEMPERATURE



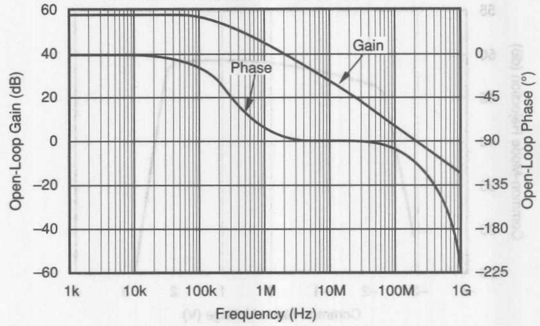
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, R_{FB} = 402Ω, unless otherwise noted.

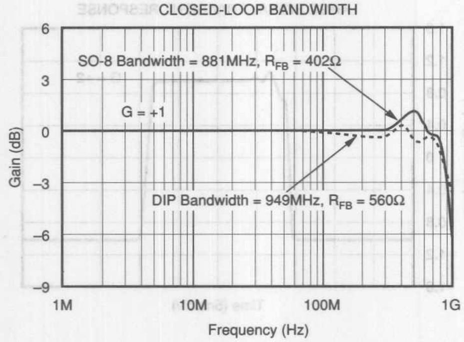
OPEN-LOOP TRANSIMPEDANCE AND PHASE vs FREQUENCY



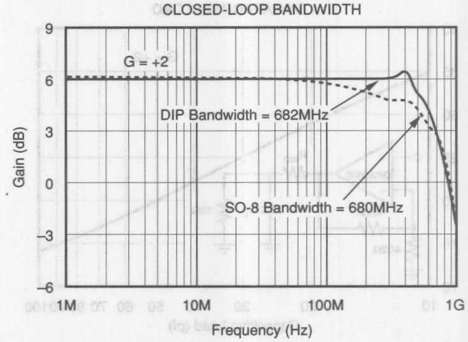
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



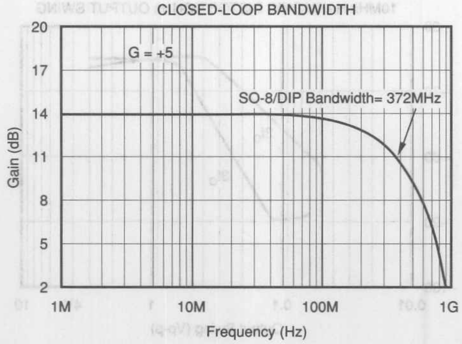
CLOSED-LOOP BANDWIDTH



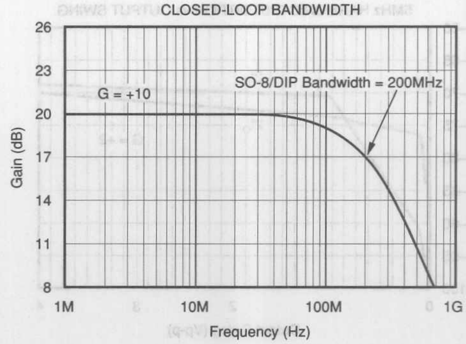
CLOSED-LOOP BANDWIDTH



CLOSED-LOOP BANDWIDTH



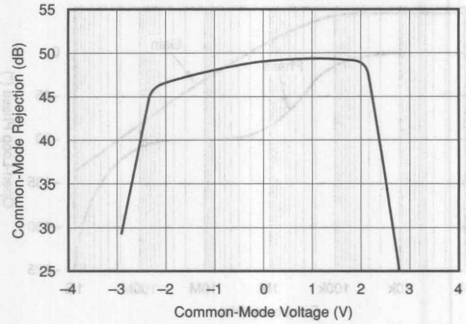
CLOSED-LOOP BANDWIDTH



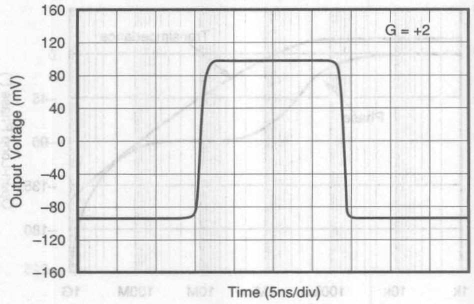
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, unless otherwise noted.

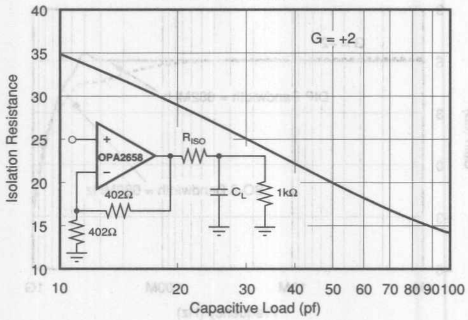
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



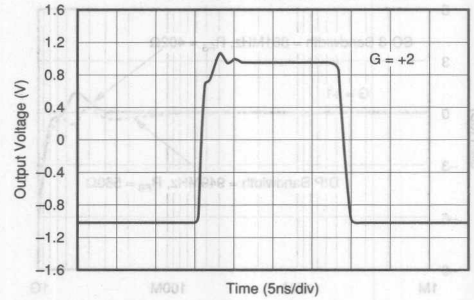
SMALL SIGNAL TRANSIENT RESPONSE



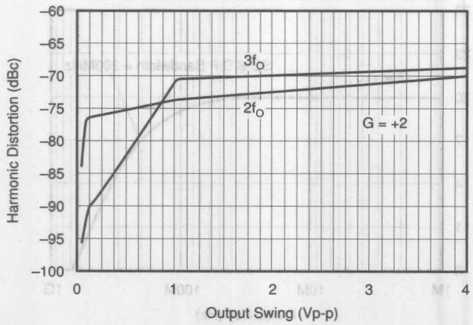
RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD



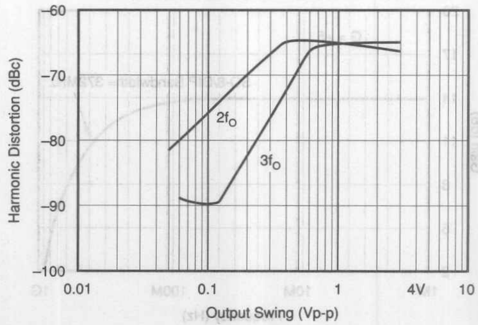
LARGE SIGNAL TRANSIENT RESPONSE



5MHz HARMONIC DISTORTION vs OUTPUT SWING



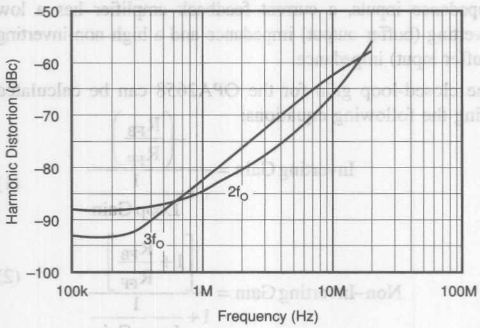
10MHz HARMONIC DISTORTION vs OUTPUT SWING



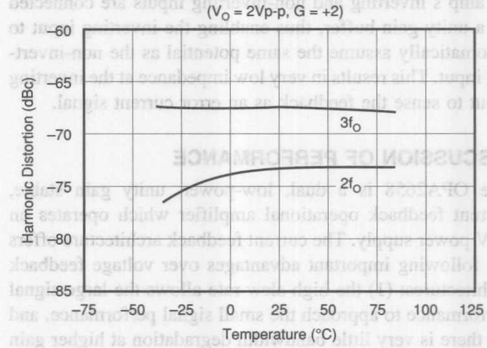
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm 5V$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, unless otherwise noted.

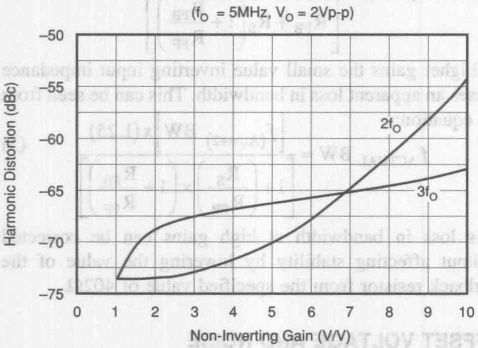
HARMONIC DISTORTION vs FREQUENCY



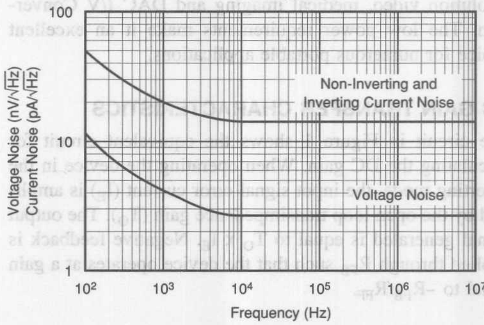
HARMONIC DISTORTION vs TEMPERATURE (V_O = 2Vp-p, G = +2)



HARMONIC DISTORTION vs GAIN (f_O = 5MHz, V_O = 2Vp-p)



INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY



APPLICATIONS INFORMATION

THEORY OF OPERATION

Conventional op amps depend on feedback to drive their inputs to the same potential, however the current feedback op amp's inverting and non-inverting inputs are connected by a unity gain buffer, thus enabling the inverting input to automatically assume the same potential as the non-inverting input. This results in very low impedance at the inverting input to sense the feedback as an error current signal.

DISCUSSION OF PERFORMANCE

The OPA2658 is a dual, low-power, unity gain stable, current feedback operational amplifier which operates on ±5V power supply. The current feedback architecture offers the following important advantages over voltage feedback architectures: (1) the high slew rate allows the large signal performance to approach the small signal performance, and (2) there is very little bandwidth degradation at higher gain settings.

The current feedback architecture of the OPA2658 provides the traditional strength of excellent large signal response plus wide bandwidth, making it a good choice for use in high resolution video, medical imaging and DAC I/V Conversion. The low power requirements make it an excellent choice for numerous portable applications.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output signal generated is equal to T_O x I_E. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

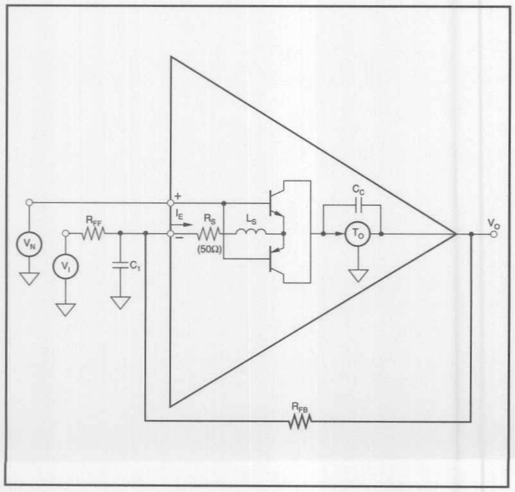


FIGURE 1. Equivalent Circuit. (1/2 of OPA2658)

For non-inverting operation, the input signal is applied to the non-inverting (high impedance buffer) input. The output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the overall gain is $(1 + R_{FB}/R_{FF})$. Where a voltage-feedback amplifier has two symmetrical high impedance inputs, a current feedback amplifier has a low inverting (buffer output) impedance and a high non-inverting (buffer input) impedance.

The closed-loop gain for the OPA2658 can be calculated using the following equations:

$$\text{Inverting Gain} = \frac{-\left(\dfrac{R_{FB}}{R_{FF}}\right)}{1+\dfrac{1}{\text{Loop Gain}}} \qquad (1)$$

$$\text{Non–Inverting Gain} = \frac{\left[1+\dfrac{R_{FB}}{R_{FF}}\right]}{1+\dfrac{1}{\text{Loop Gain}}} \qquad (2)$$

$$\text{where Loop Gain} = \left[\frac{T_O}{R_{FB}+R_S\left(1+\dfrac{R_{FB}}{R_{FF}}\right)}\right]$$

At higher gains the small value inverting input impedance causes an apparent loss in bandwidth. This can be seen from the equation:

$$f_{\text{ACTUAL}}\ \text{BW} \approx \frac{\left[f_{(A_V=+2)}\ \text{BW}\right] x\,(1.25)}{\left[1+\left(\dfrac{R_S}{R_{FB}}\right)\times\left(1+\dfrac{R_{FB}}{R_{FF}}\right)\right]} \qquad (3)$$

This loss in bandwidth at high gains can be corrected without affecting stability by lowering the value of the feedback resistor from the specified value of 402Ω.

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the input offset voltage and bias current errors. The output offset for non-inverting operation is calculated by the following equation:

$$\text{Output Offset Voltage} = \pm Ib_N \times R_N\left(1+\frac{R_{FB}}{R_{FF}}\right) \pm \qquad (4)$$

$$V_{IO}\left(1+\frac{R_{FB}}{R_{FF}}\right) \pm Ib_I \times R_{FB}$$

If all terms are divided by the gain $(1 + R_{FB}/R_{FF})$ it can be observed that input referred offsets improve as gain increases. The effective noise at the output can be determined by taking

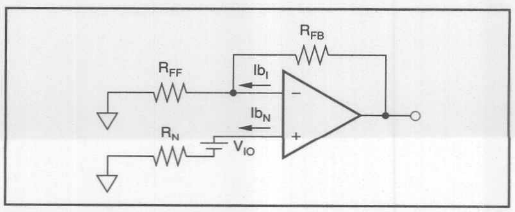


FIGURE 2. Output Offset Voltage Equivalent Circuit.

Note that both the noise figure (NF) and the equivalent input offset voltages improve as the closed loop gain increases (by keeping R_{FB} fixed and reducing R_{FF} with $R_N = 0\Omega$).

INCREASING BANDWIDTH AT HIGH GAINS

The closed-loop bandwidth can be extended at high gains by reducing the value of the feedback resistor R_{FB}. This bandwidth reduction is caused by the feedback current being split between R_S and R_{FF} (refer to Figure 1). As the gain increases (for a fixed R_{FB}), more feedback current is shunted through R_{FF}, which reduces closed-loop bandwidth.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA2658 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the two power pins to high frequency 0.1µF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA2658. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Other network components, such as non-inverting input termination resistors, should also be placed close to the package.

The feedback resistor value acts as the frequency response compensation element for a current feedback type amplifier. Increasing it will over compensate the amplifier, rolling off the frequency response, while decreasing it will decrease phase margin, peaking up the frequency response. Note that a non-inverting, unity gain buffer application still requires a feedback resistor for stability (560Ω for SO-8 and 402Ω for PDIP).

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA2658 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) Socketing a high speed part like the OPA2658 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

The OPA2658 is nominally specified for operation using ±5V power supplies. A 10% tolerance on the supplies, or an ECL −5.2V for the negative supply, is within the

maximumspecified total supply voltage of 11V. Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single supply operation. Figure 3 shows one approach to single-supply operation.

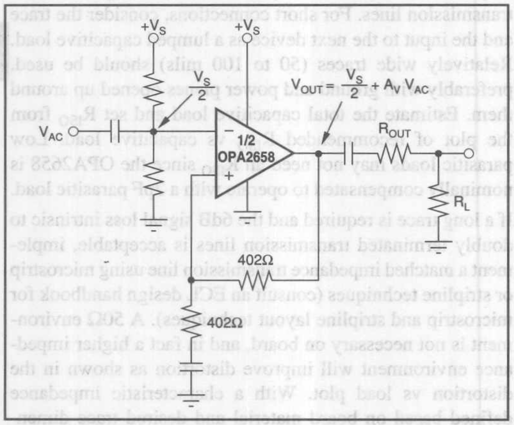


FIGURE 3. Single Supply Operation.

ESD PROTECTION

ESD static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA2658.

OUTPUT DRIVE CAPABILITY

The OPA2658 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA2658 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 4, the OPA2658 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

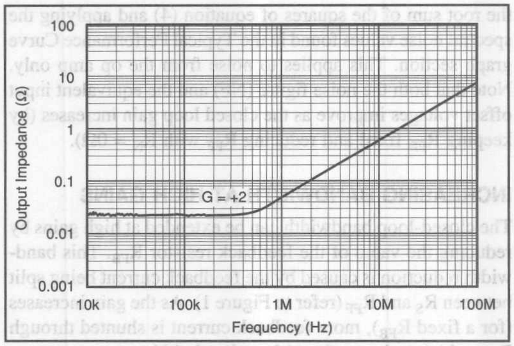


FIGURE 4. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA2658 will not require heatsinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D\theta_{JA}$. The total internal power dissipation (P_D) is a combination of the total quiescent power for all channels (P_{DQ}) and the sum of the powers dissipated in each of the output stages (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is a fixed DC voltage equal to 1/2 of either supply voltage (assuming equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading. Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As an example, compute the maximum T_J for an OPA2658U at $A_V = +2$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, $\pm V_S = \pm 5V$, with both outputs at $|V_S/2|$, and the specified maximum $T_A = +85°C$. $P_D = 10V \bullet 17mA + 2 \bullet (5^2)/(4 \bullet (100\Omega \parallel 804\Omega)] = 311mW$. Maximum $T_J = +85°C + 0.311W \bullet 125°C/W = 124°C$.

DRIVING CAPACITIVE LOADS

The OPA2658's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 10Ω to 35Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax

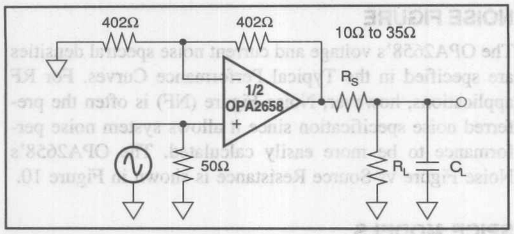


FIGURE 5. Driving Capacitive Loads.

cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated with its characteristic impedance.

COMPENSATION

The OPA2658 is internally compensated and is stable in unity gain with a phase margin of approximately 62°, and approximately 64° in a gain of +2V/V when used with the recommended feedback resistor value. Frequency response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA2658 in a good layout is very flat with frequency.

DISTORTION

The OPA2658's Harmonic Distortion characteristics into a 100Ω load are shown versus frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

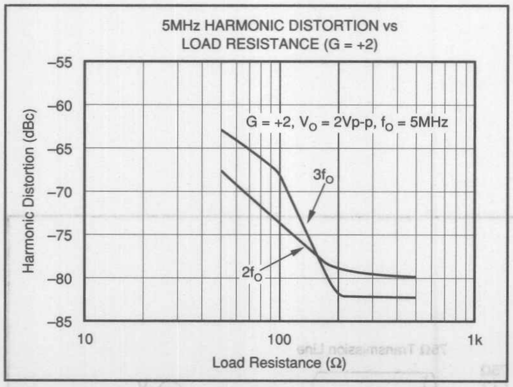


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

Narrowband communication channel requirements will benefit from the OPA2658's wide bandwidth and low intermodulation distortion on low quiescent power. If output signal power at two closely spaced frequencies is required, third-order nonlinearities in any amplifier will cause spurious power at frequencies very near the two fundamental frequencies. If the two test frequencies, f_1 and f_2, are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $\Delta f = |f_2 - f_1|$, the two, third-order, close-in spurious tones will appear at $f_O \pm 3 \bullet \Delta f$. The two tone, third-order spurious plot shown in Figure 7 indicates how far below these two equal power, closely spaced, tones the intermodulation spurious will be. The single tone power is at a matched 50Ω load. The unique design of the OPA2658 provides much greater spurious free range than what a two-tone third-order intermodulation intercept specification would predict. This can be seen in Figure 7 as the spurious free range actually increases at the higher output power levels.

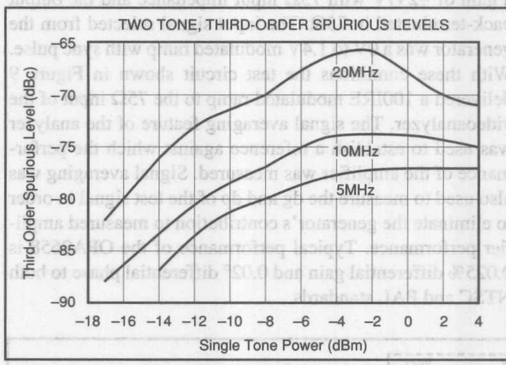


FIGURE 7. Third-Order Intercept Point vs Frequency.

CROSS TALK

Crosstalk is the undesired result of the signal of one channel mixing with and reproducing itself in the output of the other channel. Crosstalk is inclined to occur in most multichannel integrated circuits. In dual devices, the effect of crosstalk is measured by driving one channel and observing the output of the undriven channel over various frequencies. The magnitude of this effect is referenced in terms of channel- to-channel isolation and expressed in decibels. "Input referred" points to the fact that there is a direct correlation between gain and crosstalk, therefore at increased gain, crosstalk also increases by a factor equal to that of the gain. Figure 8 illustrates the measured effect of crosstalk in the OPA2658U.

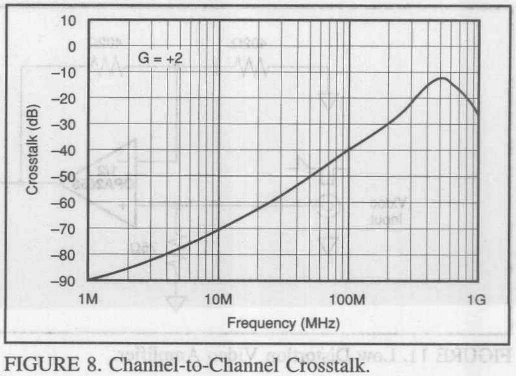


FIGURE 8. Channel-to-Channel Crosstalk.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (dG) and Differential Phase (dP) are among the more important specifications for video applications. dG is defined as the percent change in closed-loop gain over a specified change in output voltage level. dP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both dG and dP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL sub-carrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

dG/dP of the OPA2658 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 9 delivered a 100IRE modulated ramp to the 75Ω input of the videoanalyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the dg and dp of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA2658 is 0.025% differential gain and 0.02° differential phase to both NTSC and PAL standards.

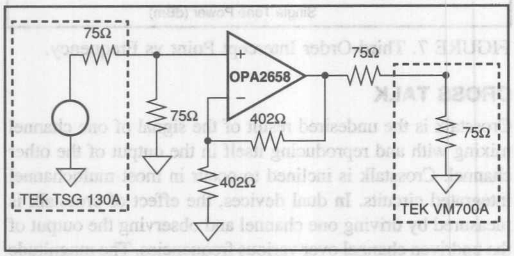


FIGURE 9. Configuration for Testing Differential Gain/Phase.

NOISE FIGURE

The OPA2658's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA2658's Noise Figure vs Source Resistance is shown in Figure 10.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA2658. Contract Burr-Brown applications departments to receive a SPICE Diskette.

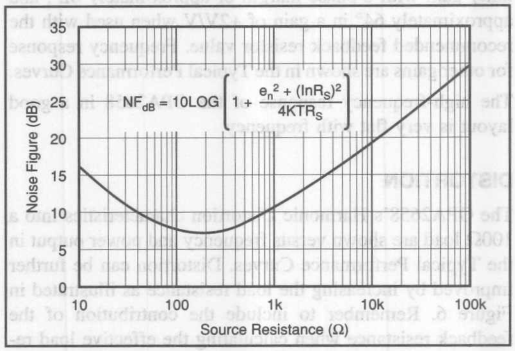


FIGURE 10. Noise Figure vs Source Resistance.

TYPICAL APPLICATION

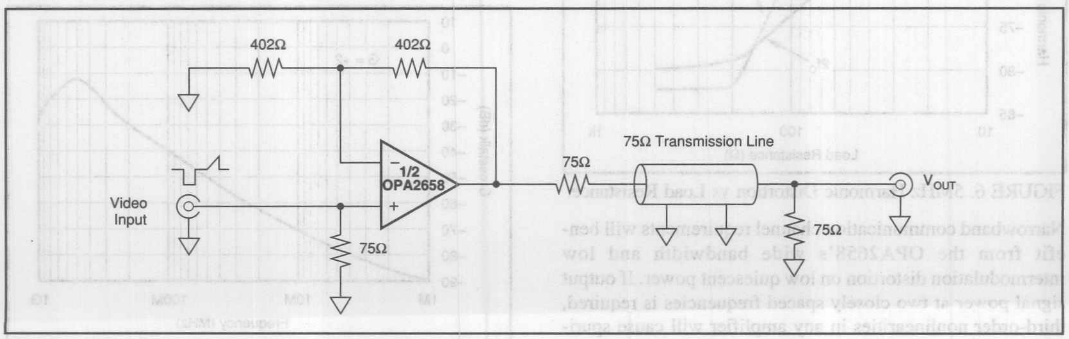


FIGURE 11. Low Distortion Video Amplifier.

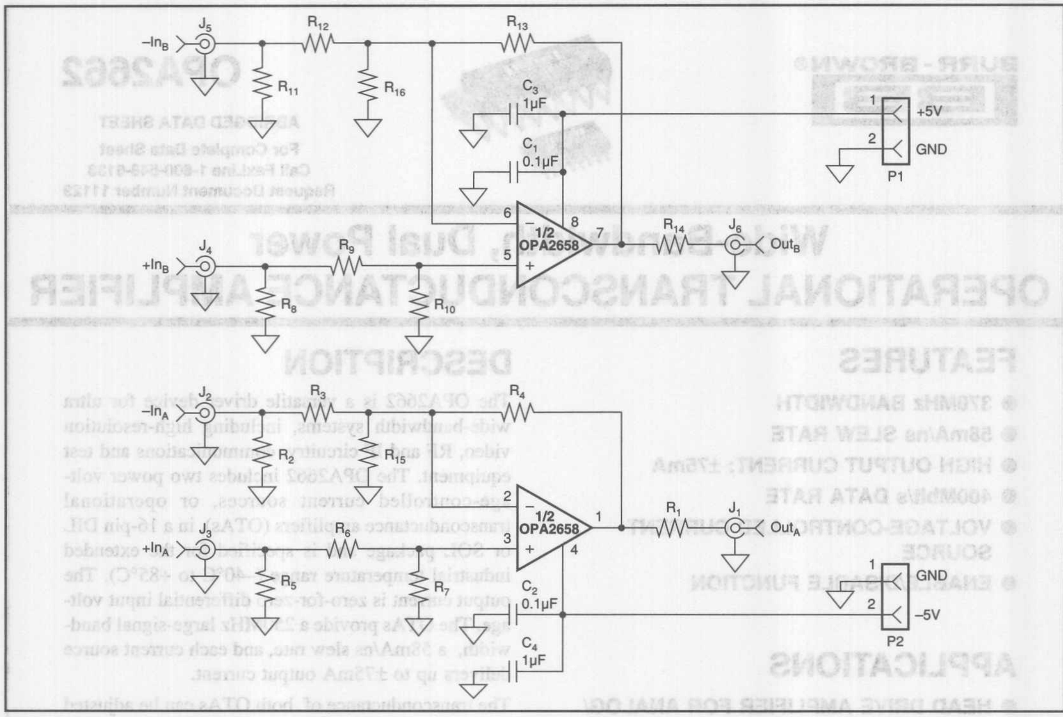


FIGURE 12. Circuit Detail For the PC Board Below.

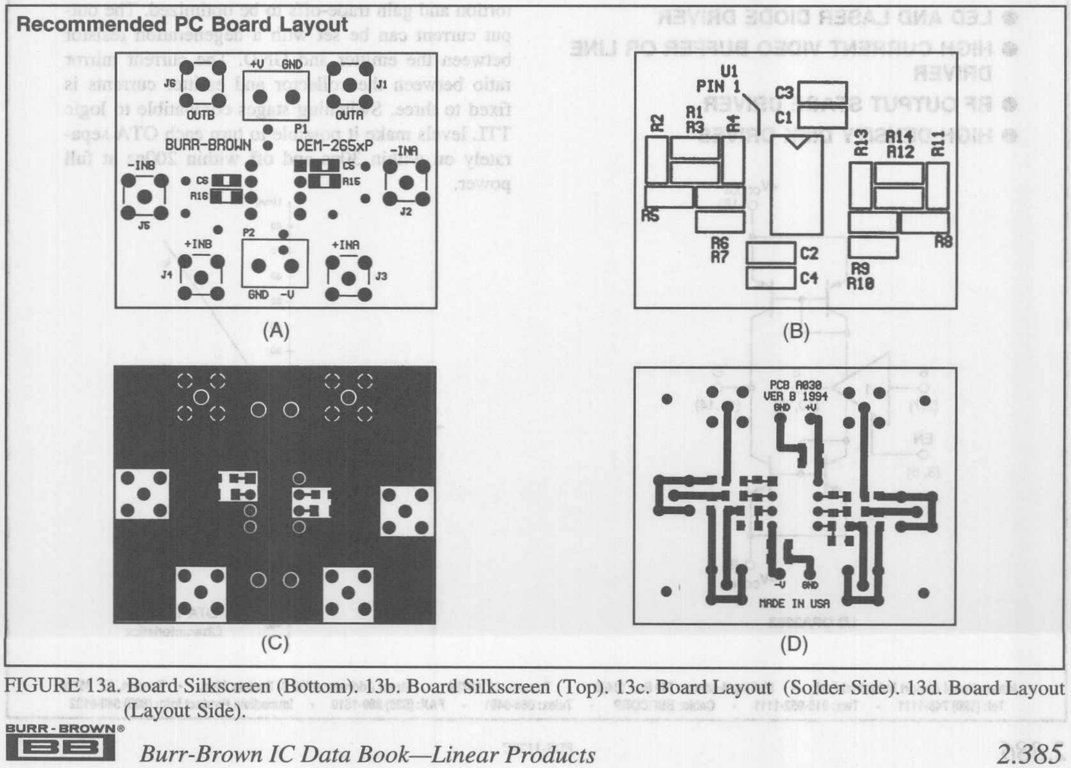
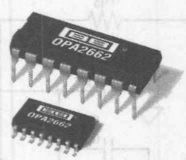


FIGURE 13a. Board Silkscreen (Bottom). 13b. Board Silkscreen (Top). 13c. Board Layout (Solder Side). 13d. Board Layout (Layout Side).

BURR - BROWN®



OPA2662

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11129

Wide-Bandwidth, Dual Power OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

FEATURES

- 370MHz BANDWIDTH
- 58mA/ns SLEW RATE
- HIGH OUTPUT CURRENT: ±75mA
- 400Mbit/s DATA RATE
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ENABLE/DISABLE FUNCTION

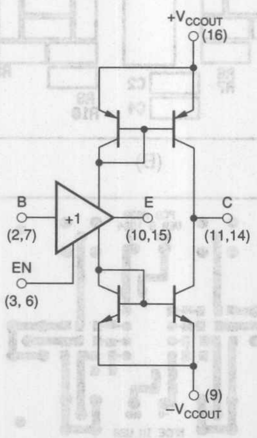
APPLICATIONS

- HEAD DRIVE AMPLIFIER FOR ANALOG/ DIGITAL VIDEO TAPES AND DATA RECORDERS
- LED AND LASER DIODE DRIVER
- HIGH CURRENT VIDEO BUFFER OR LINE DRIVER
- RF OUTPUT STAGE DRIVER
- HIGH DENSITY DISK DRIVES

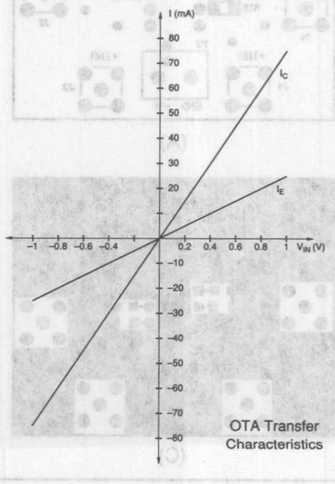
DESCRIPTION

The OPA2662 is a versatile driver device for ultra wide-bandwidth systems, including high-resolution video, RF and IF circuitry, communications and test equipment. The OPA2662 includes two power voltage-controlled current sources, or operational transconductance amplifiers (OTAs), in a 16-pin DIL or SOL package and is specified for the extended industrial temperature range (–40°C to +85°C). The output current is zero-for-zero differential input voltage. The OTAs provide a 250MHz large-signal bandwidth, a 58mA/ns slew rate, and each current source delivers up to ±75mA output current.

The transconductance of both OTAs can be adjusted between pin 5 and $-V_{CC}$ by an external resistor, allowing bandwidth, quiescent current, harmonic distortion and gain trade-offs to be optimized. The output current can be set with a degeneration resistor between the emitter and GND. The current mirror ratio between the collector and emitter currents is fixed to three. Switching stages compatible to logic TTL levels make it possible to turn each OTA separately on within 30ns and off within 200ns at full power.



1/2 OPA2662



OTA Transfer Characteristics

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1129C

SPECIFICATIONS

ELECTRICAL

DC-SPECIFICATIONS

At $V_{CC} = \pm5V$, $R_Q = 750\Omega$, $T_A = +25°C$, and configured as noted under "CONDITIONS".

PARAMETER	CONDITIONS	OPA2662AP, AU MIN	TYP	MAX	UNITS
OTA INPUT OFFSET VOLTAGE					
Initial	$R_E = 50k\Omega$, $R_C = 40\Omega$		12	±30	mV
vs Temperature			35		µV/°C
vs Supply (tracking)	$V_{CC} = \pm4.5V$ to $\pm5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		27		dB
vs Supply (non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		15		dB
vs Supply (non-tracking)	$V_{CC} = -4.5V$ to $-5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		40		dB
Matching			2	±7	mV
OTA B-INPUT BIAS CURRENT					
Initial	$R_E = 100\Omega$, $R_C = 40\Omega$		1	−1/+5	µA
vs Temperature			−5		nA/°C
vs Supply (tracking)	$V_{CC} = \pm4.5V$ to $\pm5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		60		nA/V
vs Supply (non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		160		nA/V
vs Supply (non-tracking)	$V_{CC} = -4.5V$ to $-5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		40		nA/V
Matching			0.2	±1	µA
OTA C-OUTPUT BIAS CURRENT	$R_E = 100\Omega$, $R_C = 1k\Omega$				
Initial			0.5	−0.5/+1.5	mA
vs Temperature			1.5		µA/°C
vs Supply (tracking)	$V_{CC} = \pm4.5V$ to $\pm5.5V$		72		µA/V
vs Supply (non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		236		µA/V
vs Supply (non-tracking)	$V_{CC} = -4.5V$ to $-5.5V$		92		µA/V
Matching			0.06	±0.5	mA
B-INPUT IMPEDANCE					
Impedance	$I_Q = \pm17mA$		4.5 || 1.5		MΩ || pF
OTA INPUT NOISE					
Input Noise Voltage Density	f = 20kHz to 100MHz		4.4		$nV/\sqrt{Hz}$
Output Noise Current Density			0.09		$nA/\sqrt{Hz}$
Signal-to-Noise Ratio	$S/N = 20 \log \cdot (0.7/V_N \cdot \sqrt{5MHz})$		97		dB
OTA C-RATED OUTPUT					
Output Voltage Compliance	$I_C = \pm5mA$, $R_E = 100\Omega$, $R_C = 1k\Omega$		±3.4		V
Output Current	$R_C = 40\Omega$, $R_E = 100\Omega$ $V_{IN} = \pm3V$		±75		mA
Output Impedance, r_C	$I_Q = \pm17mA$		4.5 || 6.5		kΩ || pF
OTA E-RATED OUTPUT					
Voltage Output	$R_E = 100\Omega$, $R_C = 40\Omega$		±3.0		V
DC Current Output	$R_E = 100\Omega$, $R_C = 40\Omega$ $V_{IN} = \pm4V$		±25		mA
Voltage Gain	$V_{IN} = \pm2.5V$				
	$R_E = 100\Omega$		0.86		V/V
	$R_E = 50k\Omega$		0.98		V/V
Output Impedance, r_E	$I_Q = \pm17mA$		16 || 2.2		Ω || pF
POWER SUPPLY					
Rated Voltage	$R_E = 50k\Omega$, $R_C = 1k\Omega$	±4.5		±5.5	VDC
Derated Performance	$R_E = 50k\Omega$, $R_C = 40\Omega$	±3		±6	VDC
Positive Quiescent Current for both OTAs(4)	$R_Q = 750\Omega$, $R_E = 50k\Omega$, $R_C = 1k\Omega$, Both Channels Enabled	+15	+17	+18	mA
Positive Quiescent Current for both OTAs(4)	$R_Q = 750\Omega$, $R_E = 50k\Omega$, $R_C = 1k\Omega$, Both Channels Disabled		+4		mA
Quiescent Current Range	Programmable $R_Q = 3k\Omega$ to 30Ω	±3		±65	mA
TEMPERATURE RANGE					
Specification	Ambient Temperature	−40		+85	°C
Thermal Resistance, θ_{JA}					
AP			90		°C/W
AU			100		°C/W

NOTES: (1) Characterization sample. (2) "Typical Values" are Mean values. The average of the two amplifiers is used for amplifier specific parameters. (3) "Min" and "Max" Values are mean ±3 Standard Deviations. Worst case of the two amplifiers (Mean ±3 Standard Deviations) is used for amplifier specific parameters. (4) I^-_Q typically 2mA less than I^+_Q due to OTA C-Output Bias Current and TTL Select Circuit Current.

SPECIFICATIONS (CONT)

ELECTRICAL

AC-SPECIFICATION

Typical at V_{CC} = ±5VDC, R_Q = 750Ω, I_C = ±37.5mA (V_{IN} = 2.5Vpp, R_E = 100Ω), I_C = ±75mA (V_{IN} = 2.5Vpp, R_E = 50Ω), R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2662AP, AU MIN	TYP	MAX	UNITS
FREQUENCY DOMAIN					
LARGE SIGNAL BANDWIDTH					
I_C = ±37.5mA	R_E = 100Ω, R_C = 50Ω		150		MHz
I_C = ±75mA	R_E = 100Ω, R_C = 25Ω		200		MHz
I_C = ±37.5mA (Optimized)	R_E = 100Ω, R_C = 50Ω, C_E = 5.6pF		370		MHz
I_C = ±75mA (Optimized)	R_E = 100Ω, R_C = 25Ω, C_E = 5.6pF		250		MHz
GROUP DELAY TIME	R_E = 100Ω, R_C = 50Ω				
Measured Input to Output	B to E		1.2		ns
(Demo Board Used)	B to C		2.5		ns
HARMONIC DISTORTION					
Second Harmonic	f = 10MHz, I_C = ±37.5mA		–31		dBc
Third Harmonic			–37		dBc
Second Harmonic	f = 10MHz, I_C = ±75mA		–33		dBc
Third Harmonic			–32		dBc
Second Harmonic	f = 30MHz, I_C = ±37.5mA		–29		dBc
Third Harmonic			–32		dBc
Second Harmonic	f = 30MHz, I_C = ±75mA		–30		dBc
Third Harmonic			–25		dBc
Second Harmonic	f = 50MHz, I_C = ±37.5mA		–31		dBc
Third Harmonic			–30		dBc
Second Harmonic	f = 50MHz, I_C = ±75mA		–28		dBc
Third Harmonic			–23		dBc
CROSSTALK	Typical Curve Number 3				
	I_C = ±37.5mA, f = 30MHz		–51		dB
	I_C = ±75mA, f = 30MHz		–56		dB
FEEDTHROUGH					
Off Isolation	R_E = 100Ω, f = 30MHz		–90		dB
	R_E = 50Ω, f = 30MHz		–90		dB
TIME DOMAIN					
Rise Time	10% to 90%				
	75mA Step I_C		2		ns
	150mA Step I_C		2.6		ns
Slew Rate	I_C = 75mA		37.5		mA/ns
	I_C = 150mA		58		mA/ns

CHANNEL SELECTION

PARAMETER	CONDITIONS	OPA2662AP, AU MIN	TYP	MAX	UNITS
ENABLE INPUTS					
Logic 1 Voltage		2		V_{CC} + 0.6	V
Logic 0 Voltage		0		0.8	V
Logic 1 Current	V_{SEL} = 2.0V to 5V	0.8	1.1	10	µA
Logic 0 Current	V_{SEL} = 0V to 0.8V	–1	0.05		µA
SWITCHING CHARACTERISTICS	I_C = 150mAp-p, f = 5MHz				
EN to Channel ON Time	90% Point of V_O = 1Vp-p		30		ns
EN to Channel OFF Time	10% Point of V_O = 1Vp-p		200		ns
Switching Transient, Positive	(Measured While Switching		30		mV
Switching Transient, Negative	Between the Grounded Channels)		–80		mV

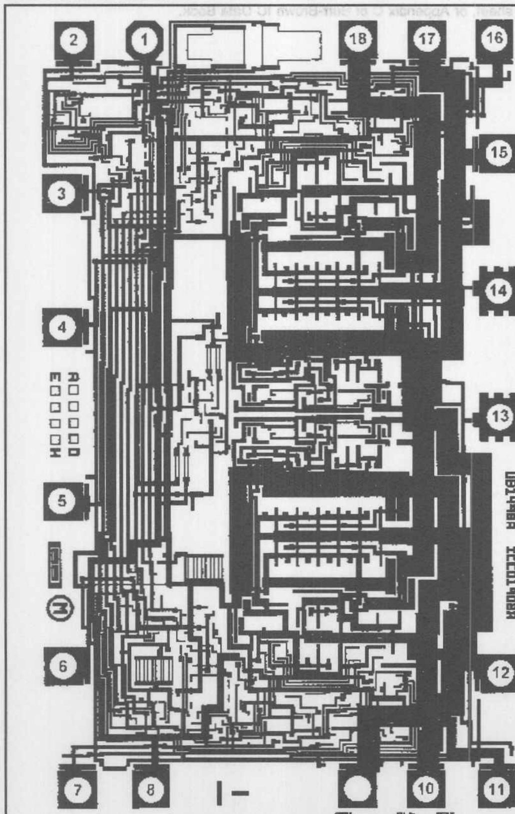
SPECIFICATIONS (CONT)

ELECTRICAL (Full Temperature Range –40°C to +85°C)

At V_{CC} = ±5VDC, R_Q = 750Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, and configured as noted under "CONDITIONS".

PARAMETER	CONDITIONS	OPA2662AP, AU MIN	TYP	MAX	UNITS
OTA INPUT OFFSET VOLTAGE	R_E = 50kΩ, R_C = 40Ω				
Initial			12	±36	mV
Matching			2	±7.2	mV
OTA INPUT BIAS CURRENT	R_E = 100Ω, R_C = 40Ω				
Initial		–1.9	1	5.9	µA
Matching		–1.2	0.2	1.2	µA
OTA TRANSCONDUCTANCE					
Transconductance	I_C = 75mA, R_E = 0	580		610	mA/V
OTA C-RATED OUTPUT					
Output Voltage Compliance	I_C = ±5mA, R_E = 100Ω, R_C = 16Ω	±3.2			V
POWER SUPPLY					
Positive Quiescent Current for both OTAs(4)	R_Q = 750Ω, R_E = 50kΩ, R_C = 1kΩ, Both Channels Selected	+8	+17	+25	mA

DICE INFORMATION



OPA2662 DIE TOPOGRAPHY

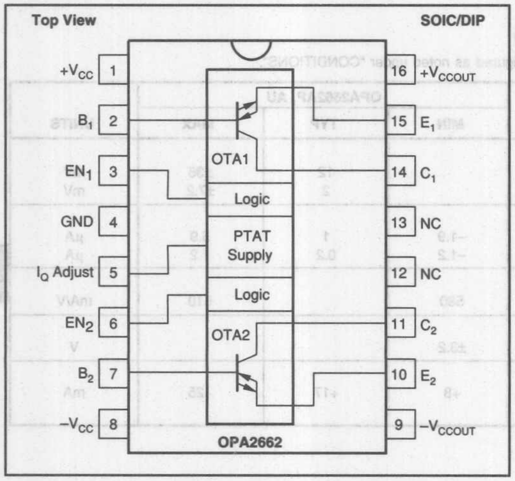
PAD	FUNCTION
1	+5V Supply
2	Input, Amplifier 1
3	TTL, Amplifier 1
4	Ground
5	Enable
6	TTL, Amplifier 2
7	Input, Amplifier 2
8	–5V Supply
9	–5V Supply, Output 2
10	–5V Supply, Output 1
11	Buffer, Amplifier 2
12	OTA Output, Amplifier 2
13	OTA Output, Amplifier 1
14	Buffer, Amplifier 1
15	+5V Supply, Output 2
16	+5V Supply, Output 1

Substrate Bias: Negative Supply
NC: No Connection
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	57 x 69 ±5	1.44 x 1.76 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing:		
Titanium	0.02, +0.05, –0	0.0005, +0.0013, –0
Gold	0.30, ±0.05	0.0076, ±0.0013

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage(1)	$\pm V_{CC}$ to ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Digital Input Voltages (EN_1, EN_2)	–0.5 to $+V_{CC}$ +0.7V

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
OPA2662AP	16-Pin Plastic DIP	–40°C to +85°C
OPA2662AU	16-Pin SOIC	–40°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA2662AP	16-Pin Plastic DIP	180
OPA2662AU	16-Pin SOIC	211

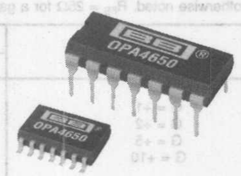
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5kΩ) applied to each pin.

BURR - BROWN®



OPA4650

Wideband, Low Power, Quad Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- LOW POWER: 50mW/channel
- UNITY GAIN STABLE BANDWIDTH: 360MHz
- FAST SETTLING TIME: 20ns to 0.01%
- LOW INPUT BIAS CURRENT: 5µA
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.025°
- 14-PIN DIP and SO-14 SURFACE MOUNT PACKAGES AVAILABLE

APPLICATIONS

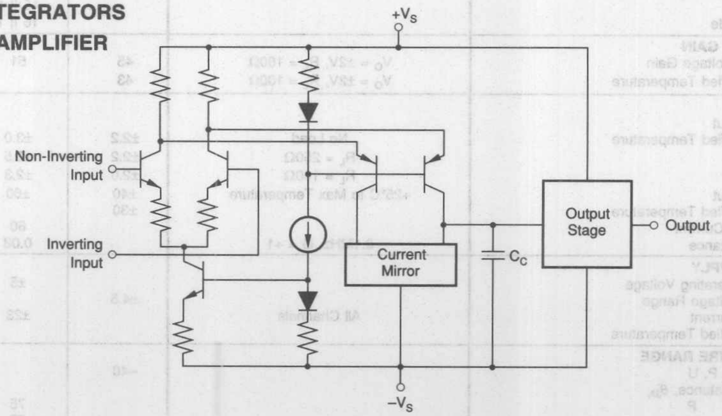
- HIGH RESOLUTION VIDEO
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC BUFFER AMPLIFIER
- ACTIVE FILTERS
- HIGH SPEED INTEGRATORS
- DIFFERENTIAL AMPLIFIER

DESCRIPTION

The OPA4650 is a quad, low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 360MHz as well as a 12-bit settling time of only 20ns. The low input bias current allows its use in high speed integrator applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA4650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA4650 is also available in single (OPA650) and dual (OPA2650) configurations.



Simplified Schematic
1 of 4 Channels

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

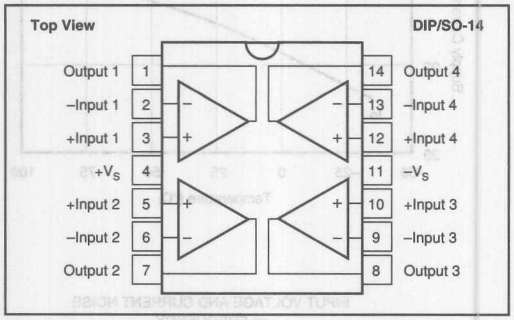
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE					
Closed-Loop Bandwidth(1)	G = +1		360		MHz
	G = +2		120		MHz
	G = +5		35		MHz
	G = +10		16		MHz
Gain Bandwidth Product			160		MHz
Slew Rate(2)	G = +1, 2V Step		240		V/µs
Over Specified Temperature			220		V/µs
Rise Time	0.2V Step		1		ns
Fall Time	0.2V Step		1		ns
Settling Time 0.01%	G = +1, 2V Step		20		ns
0.1%	G = +1, 2V Step		10.3		ns
1%	G = +1, 2V Step		7.9		ns
Spurious Free Dynamic Range	G = +1, f = 5.0 MHz, V_O = 2Vp-p				
	R_L = 100Ω		68		dBc
	R_L = 402Ω		74		dBc
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, R_L = 150Ω		0.01		%
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, R_L = 150Ω		0.025		Degrees
Bandwidth for 0.1dB Flatness	G = +2		21		MHz
Crosstalk	Input Referred, 5MHz, all hostile		–63		dB
	Input Referred, 5MHz, Channel-to-Channel		–66		dB
OFFSET VOLTAGE					
Input Offset Voltage			±1	±5.5	mV
Average Drift			±3		µV/°C
Power Supply Rejection (+V_S)	$\lvert V_S \rvert$ = 4.5V to 5.5V	60	76		dB
(–V_S)		47	52		dB
INPUT BIAS CURRENT					
Input Bias Current	V_{CM} = 0V		5	20	µA
Over Temperature				30	µA
Input Offset Current	V_{CM} = 0V		0.5	1.0	µA
Over Temperature				3.0	µA
INPUT NOISE					
Input Voltage Noise					
Noise Density, f = 100Hz			43		nV/√Hz
f = 10kHz			9.4		nV/√Hz
f = 1MHz			8.4		nV/√Hz
f = 1MHz to 100MHz			8.4		nV/√Hz
Integrated Noise, BW = 10Hz to 100MHz			84		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 0.1MHz to 100MHz			1.2		pA/√Hz
Noise Figure (NF)					
	R_S = 10kΩ		4.0		dBm
	R_S = 50Ω		19.5		dBm
INPUT VOLTAGE RANGE					
Common-Mode Input Range			±2.8		V
Over Specified Temperature		±2.2			V
Common-Mode Rejection	V_{CM} = ±0.5V	65	90		dB
INPUT IMPEDANCE					
Differential			15 ‖ 1		kΩ ‖ pF
Common-Mode			16 ‖ 1		MΩ ‖ pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	45	51		dB
Over Specified Temperature	V_O = ±2V, R_L = 100Ω	43			dB
OUTPUT					
Voltage Output					
Over Specified Temperature	No Load	±2.2	±3.0		V
	R_L = 250Ω	±2.2	±2.5		V
	R_L = 100Ω	±2.0	±2.3		V
Current Output	+25°C to Max Temperature	±40	±60		mA
Over Specified Temperature		±30			mA
Short Circuit Current			60		mA
Output Resistance	0.1MHz, G = +1		0.08		Ω
POWER SUPPLY					
Specified Operating Voltage			±5		V
Operating Voltage Range		±4.5		±5.5	V
Quiescent Current	All Channels		±23	±32	mA
Over Specified Temperature				±35	mA
TEMPERATURE RANGE					
Specification: P, U		–40		+85	°C
Thermal Resistance, θ_{JA}					
P			75		°C/W
U			75		°C/W

NOTES: (1) Frequency response can be strongly influenced by PC board parasites. The OPA4650 is nominally compensated assuming 2pF parasitic load. The demonstration board, DEM-OPA465xP, shows a low parasitic layout for this part. (2) Slew rate is rate of change from 10% to 90% of output voltage step.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage Across Device	11V
Internal Power Dissipation	See Thermal Considerations
Differential Input Voltage	±2.7V
Common-Mode Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, U,	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

PIN CONFIGURATION



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA4650U	SO-14 Surface Mount	235
OPA4650P	14-Pin Plastic DIP	010

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA4650U	SO-14 Surface Mount	–40°C to +85°C
OPA4650P	14-Pin Plastic DIP	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

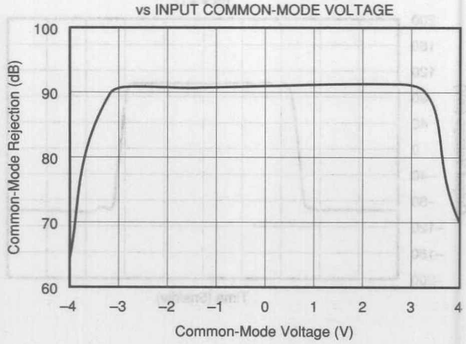
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

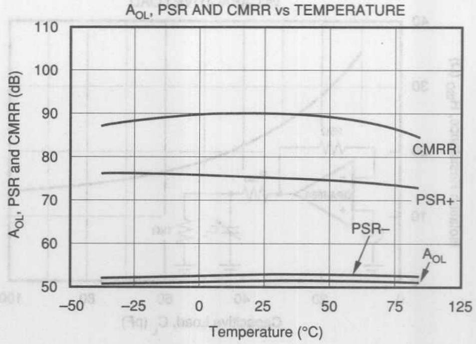
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



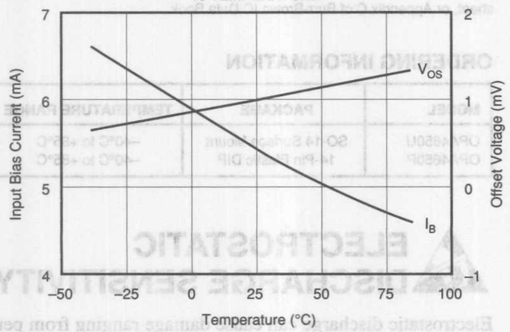
A_{OL}, PSR AND CMRR vs TEMPERATURE



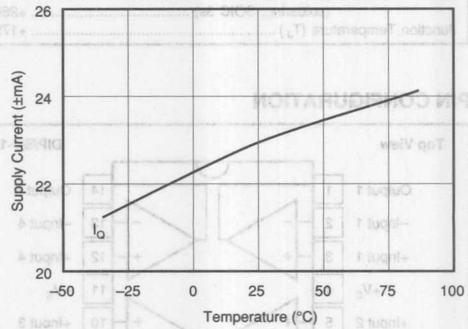
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

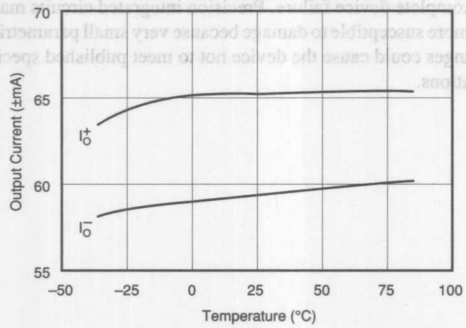
INPUT BIAS CURRENT AND OFFSET VOLTAGE vs TEMPERATURE



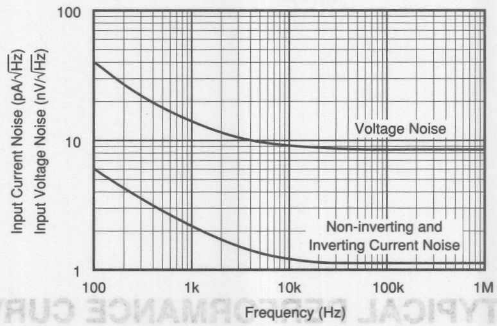
SUPPLY CURRENT vs TEMPERATURE



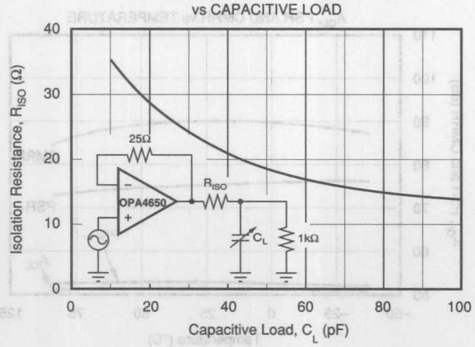
OUTPUT CURRENT vs TEMPERATURE



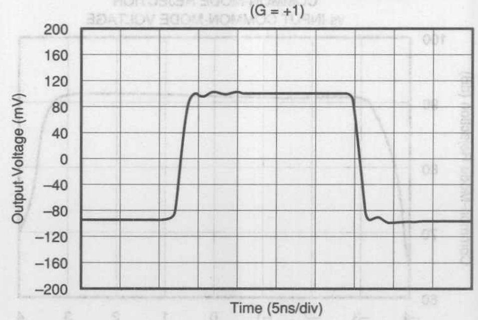
INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY



RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD



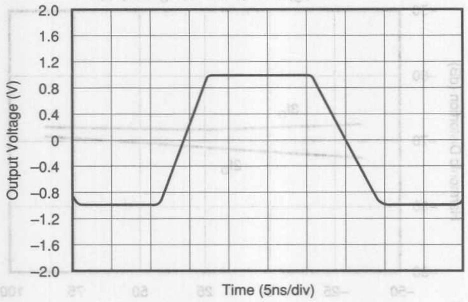
SMALL SIGNAL TRANSIENT RESPONSE (G = +1)



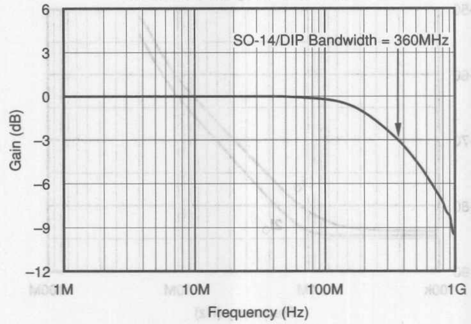
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

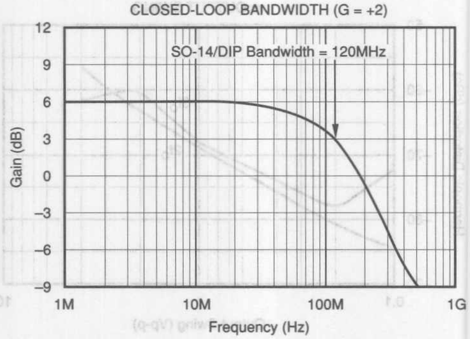
LARGE SIGNAL TRANSIENT RESPONSE (G = +1)



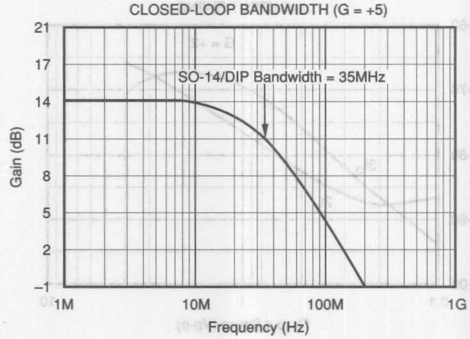
CLOSED-LOOP BANDWIDTH (G = +1)



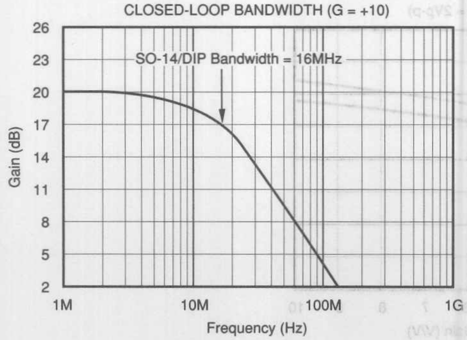
CLOSED-LOOP BANDWIDTH (G = +2)



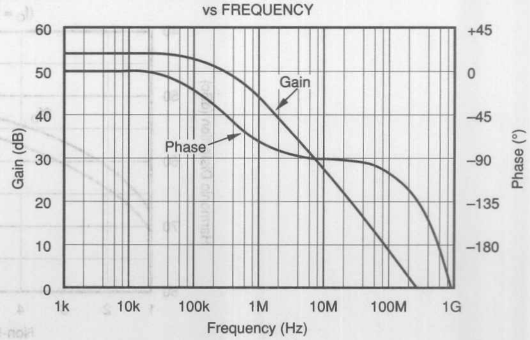
CLOSED-LOOP BANDWIDTH (G = +5)



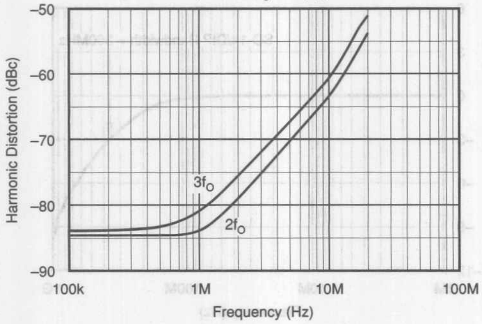
CLOSED-LOOP BANDWIDTH (G = +10)



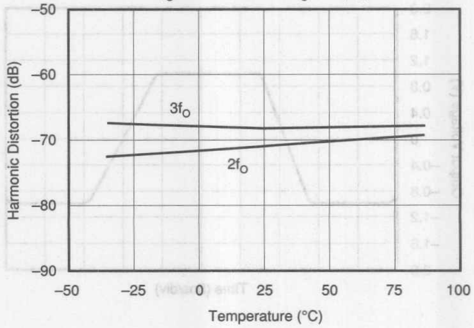
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



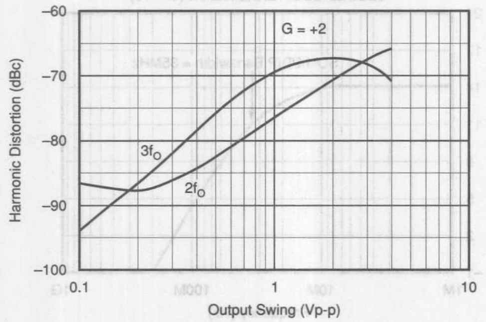
HARMONIC DISTORTION vs FREQUENCY
(G = +1, V_O = 2Vp-p)



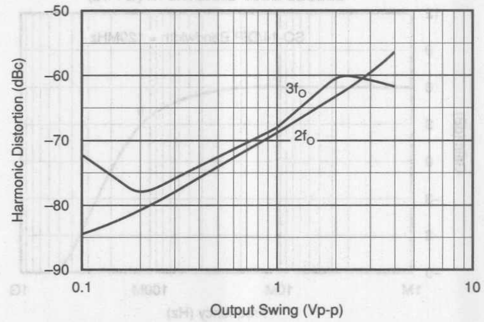
HARMONIC DISTORTION vs TEMPERATURE
(f_O = 5MHz, G = +1, V_O = 2Vp-p)



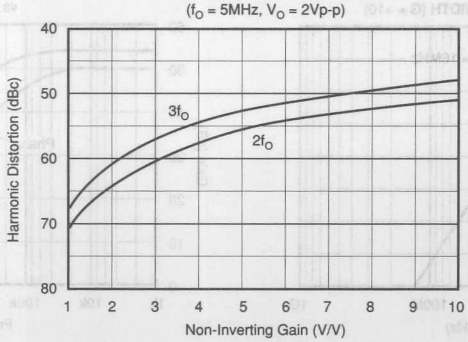
5MHz HARMONIC DISTORTION
vs OUTPUT SWING



10MHz HARMONIC DISTORTION
vs OUTPUT SWING



HARMONIC DISTORTION vs GAIN
(f_O = 5MHz, V_O = 2Vp-p)



DISCUSSION OF PERFORMANCE

The OPA4650 is a quad low power, wideband voltage feedback operational amplifier. Each channel is internally compensated to provide unity gain stability. The OPA4650's voltage feedback architecture features true differential and fully symmetrical inputs. This minimizes offset errors, making the OPA4650 well suited for implementing filter and instrumentation designs. As a quad operational amplifier, OPA4650 is an ideal choice for designs requiring multiple channels where reduction of board space, power dissipation and cost are critical. Its ac performance is optimized to provide a gain bandwidth product of 160MHz and a fast 0.1% settling time of 10.3ns, which is an important consideration in high speed data conversion applications. Along with its excellent settling characteristics, the low dc input offset of ±1mV and drift of ±3μV/°C support high accuracy requirements. In applications requiring a higher slew rate and wider bandwidth, such as video and high bit rate digital communications, consider the quad current feedback OPA4658.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA4650 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the two power pins to high frequency 0.1μF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA4650. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Surface mount feedback resistors directly adjacent to the output and inverting input pins work well for the quad pinout. Other network components, such as non-inverting input termination resistors, should also be placed close to the package.

Even with a low parasitic capacitance shunting the resistor, excessively high resistor values can create significant time constants and degrade performance. Good metal film or surface mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this adds a pole and/or zero below 500MHz that can affect circuit operation. Keep resistor values as low as possible consistent with output loading considerations. The 402Ω feedback used for the Typical Performance Plots is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for a unity gain follower. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA4650 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) Socketing a high speed part like the OPA4650 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost

impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

The OPA4650 is nominally specified for operation using ±5V power supplies. A 10% tolerance on the supplies, or an ECL –5.2V for the negative supply, is within the maximum specified total supply voltage of 11V. Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single supply operation. Figure 1 shows one approach to single-supply operation.

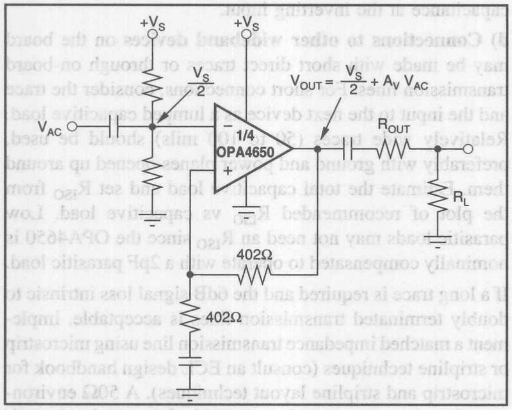


FIGURE 1. Single Supply Operation.

OFFSET VOLTAGE ADJUSTMENT

One simple way to null the initial offset voltage while retaining the low offset drift of the OPA4650 is shown in Figure 2. The 20kΩ potentiometer and the 47kΩ series resistor R_{TRIM} create a small correction current which is summed into the inverting node. The 0.1µF capacitor keeps high-frequency power supply noise from coupling into the signal path. Although the initial offset will be nulled to zero with this technique, issues of temperature drift must also be considered. The additional resistor R_3 is shown matched to the parallel combination R_1 and R_2 (the R_{TRIM} path is assumed to be negligible in this calculation). This will eliminate the first-order offset drift due to input bias current leaving only the input offset current (I_{OS}) drift multiplied by the feedback resistor R_2.

ESD PROTECTION

ESD damage has been a well recognized source of degradation for MOSFET type circuits, but any semiconductor device can be vulnerable to damage. This becomes more of an issue for very high speed processes like that used for the

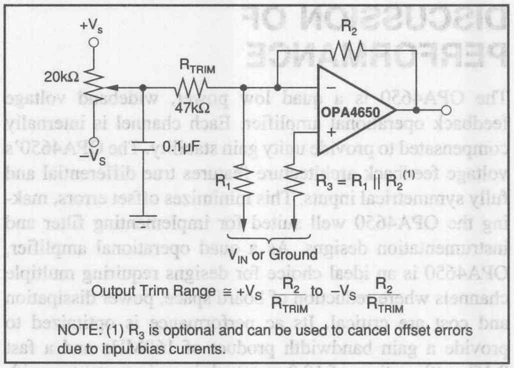


FIGURE 2. Offset Voltage Trim.

OPA4650. ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. ESD handling precautions are strongly recommended when handling the OPA4650.

OUTPUT DRIVE CAPABILITY

The OPA4650 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 1Vp-p into a 75Ω load. This high output drive capability makes the OPA4650 an ideal choice for a wide range of RF, IF and video applications. In many cases, additional buffer amplifiers are unnecessary.

Many demanding high speed applications, such as driving Analog-to-Digital converters, require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitance at the input of a flash A/D converter. As shown in Figure 3, the OPA4650 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing.

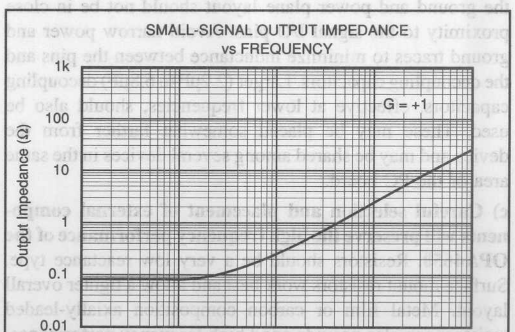


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA4650 will not require heatsinking under most operating conditions. Maximum desired junction temperature will limit the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D\theta_{JA}$. The total internal power dissipation (P_D) is a combination of the total quiescent power for all channels (P_{DQ}) and the sum of the powers dissipated in each of the output stages (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is a fixed dc voltage equal to 1/2 of either supply voltage (assuming equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading. Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation. As an example, compute the maximum T_J for an OPA4650U at $A_V = +2$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, $\pm V_S = \pm 5V$, with all 4 outputs at $|V_S/2|$, and the specified maximum $T_A = +85°C$. $P_D = 10V \bullet 35mA + 4 \bullet (5^2)/(4 \bullet (100\Omega \| 804\Omega)) = 631mW$. Maximum $T_J = +85°C + 0.641W \bullet 75°C/W = 133°C$.

DRIVING CAPACITIVE LOADS

The OPA4650's output stage has been optimized to drive low resistive loads. Capacitive loads will decrease phase margin which may result in high frequency oscillations or peaking. Capacitive loads greater than 10pF should be isolated by connecting a small resistance (15Ω to 30Ω) in series with the output as shown in Figure 4. This is especially important when driving the capacitive input of high-speed A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/ft for RG-58) will not load the amplifier when the cable is source and load terminated in its characteristic impedance.

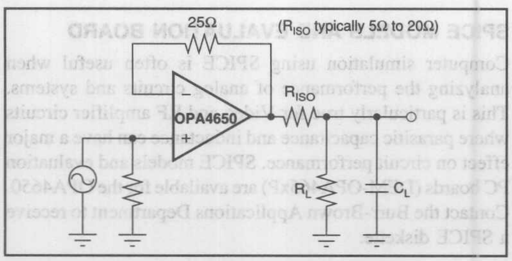


FIGURE 4. Driving Capacitive Loads.

FREQUENCY RESPONSE COMPENSATION

Each channel of the OPA4650 is internally compensated to be stable at unity gain with a nominal 60° phase margin. This lends itself well to wideband integrator and buffer applications. Phase margin and frequency response flatness will improve at higher gains. Recall that an inverting gain of –1 is equivalent to a gain of +2 for bandwidth purposes, i.e., noise gain = 2. The external compensation techniques developed for voltage feedback op amps can be applied to this device. For example, in the non-inverting configuration, placing a capacitor across the feedback resistor will reduce the gain to +1 starting at $f = (1/2\pi R_F C_F)$. Alternatively, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, thereby limiting the bandwidth for the inverting input signal through the gain-bandwidth product.

At higher gains, the gain-bandwidth of this voltage feedback topology will limit bandwidth according to the open-loop frequency response curve. For applications requiring a wider bandwidth at higher gains, consider the quad current feedback model, OPA4658. In applications where a large feedback resistor is required (such as photodiode transimpedance circuits), precautions must be taken to avoid gain peaking due to the pole formed by the feedback resistor and the summing junction capacitance. This pole can be compensated by connecting a small capacitor in parallel with the feedback resistor, creating a cancelling zero term. In other high-gain applications, use of a three-resistor "T" connection will reduce the feedback network impedance which reacts with the parasitic capacitance at the summing node.

PULSE SETTLING TIME

High speed amplifiers like the OPA4650 are capable of extremely fast settling time with a pulse input. Excellent frequency response flatness and phase linearity are required to get the best settling times. As shown in the specifications table, settling time for a ±1V step at a gain of +1 for the OPA4650 is extremely fast. The specification is defined as the time required, after the input transition, for the output to settle within a specified error band around its final value. For a 2V step, 1% settling corresponds to an error band of ±20mV, 0.1% to an error band of ±2mV, and 0.01% to an error band of ±0.2mV. For the best settling times, particularly into an ADC capacitive load, little or no peaking in the frequency response can be allowed. Using the recommended R_{ISO} for capacitive loads will limit this peaking and reduce the settling times. Fast, extremely fine scale settling (0.01%) requires close attention to ground return currents in the supply decoupling capacitors. For highest performance, consider the OPA642 which isolates the output stage decoupling from the rest of the amplifier.

among the more important specifications for video applications. The percentage change in closed-loop gain over a specified change in output voltage level is defined as DG. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. For the OPA4650, DG and DP are both specified at the NTSC color sub-carrier frequency of 3.58MHz and measured using industry standard video test equipment.

DISTORTION

The OPA4650's harmonic distortion characteristics for a 100Ω load are shown in the Typical Performance Curves. Distortion can be improved by increasing the load resistance as illustrated in Figure 5. Remember to include the contribution of the feedback network when calculating the effective load resistance seen by the amplifier.

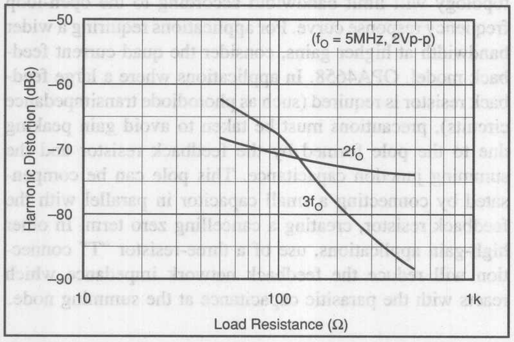


FIGURE 5. Harmonic Distortion vs Load Resistance.

CROSSTALK

Crosstalk is the undesired coupling of one channel's signal into the output of the other channels. Crosstalk is a consideration in all multichannel integrated circuits. The effect of crosstalk is measured by driving one ("channel-to-channel") or more ("all-hostile") channels and observing the output of the undriven channel. The magnitude of this effect is expressed in the crosstalk specification as decibels of gain. "Input referred" points to the fact that there is a direct correlation between gain and crosstalk, therefore output crosstalk increases proportionally at higher gains.

In quad devices, the effect of all-hostile crosstalk is observed by driving all three channels concurrently and measuring the output of the undriven fourth channel. The plots in Figure 6 illustrate both channel-to-channel and all-hostile crosstalk for the OPA4650.

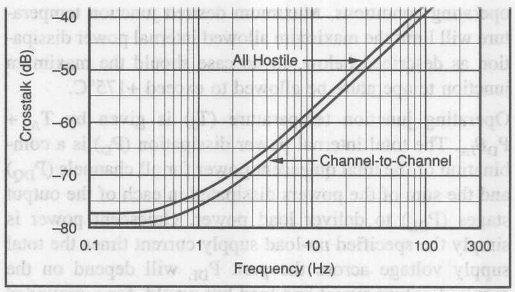


FIGURE 6. Channel-to-Channel Isolation and All Hostile Crosstalk.

NOISE FIGURE

The voltage and current noise spectral density are shown in the Typical Performance Curves. For RF and IF applications, however, Noise Figure (NF) is often the preferred specification. This specification shows a degradation in SNR through a device relative to the thermal noise of the source impedance alone.

The NF for the OPA4650, using 1MHz spot noise numbers and an unterminated non-inverting input, is shown in Figure 7.

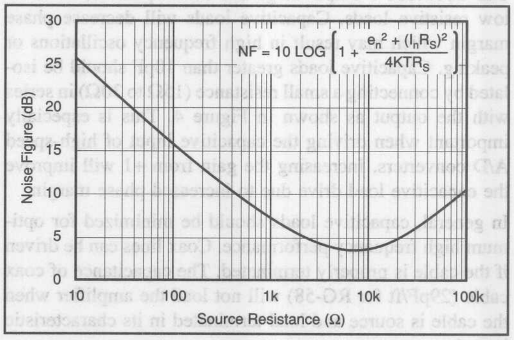


FIGURE 7. Noise Figure vs Source Resistance.

SPICE MODELS AND EVALUATION BOARD

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models and evaluation PC boards (DEM-OPA465xP) are available for the OPA4650. Contact the Burr-Brown Applications Department to receive a SPICE diskette.

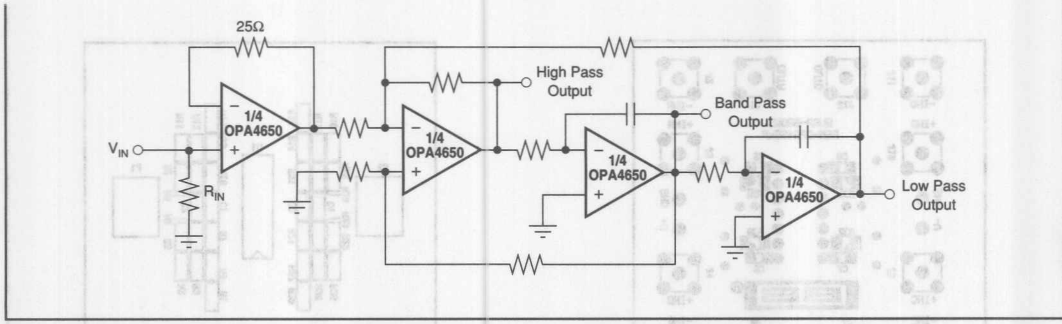


FIGURE 8. State-Variable Biquadratic Filter.

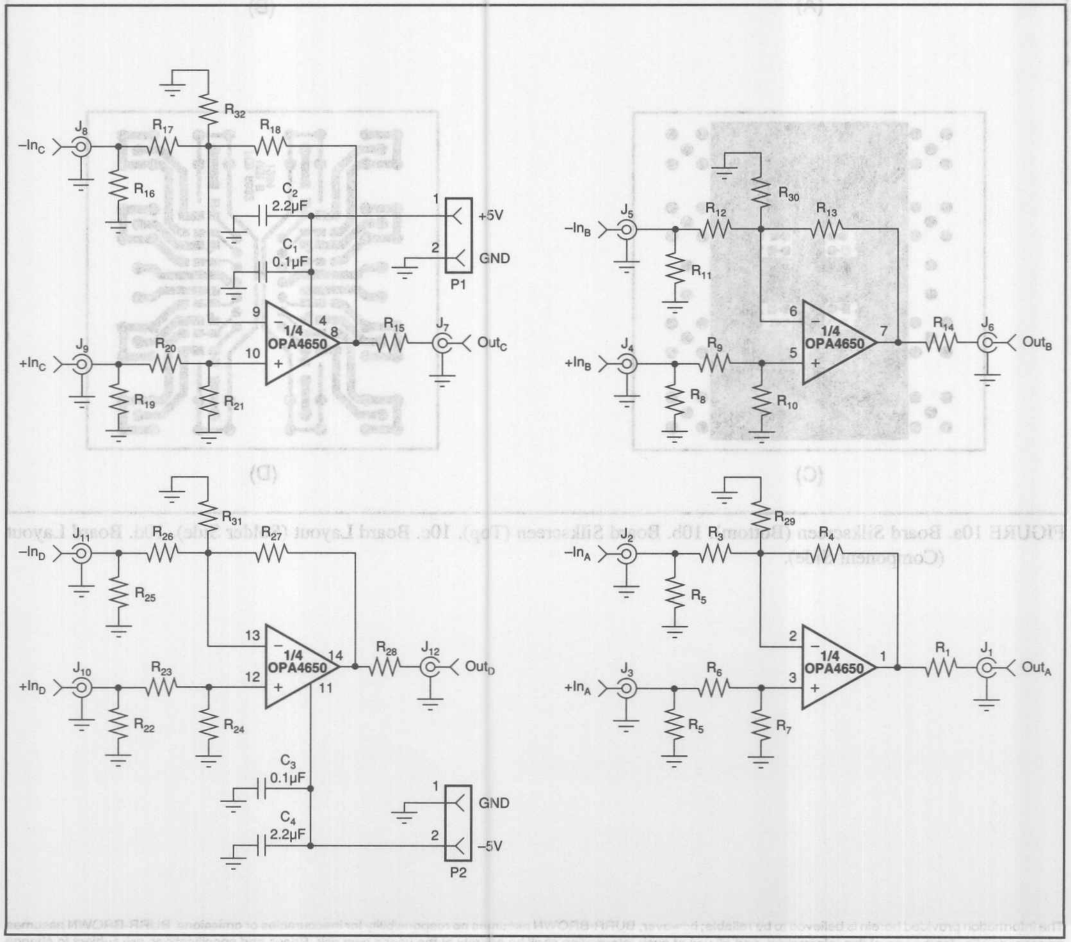


FIGURE 9. Circuit Detail for the DEM-OPA465xP Board.

DEM-OPA465xP Demonstration Board Layout

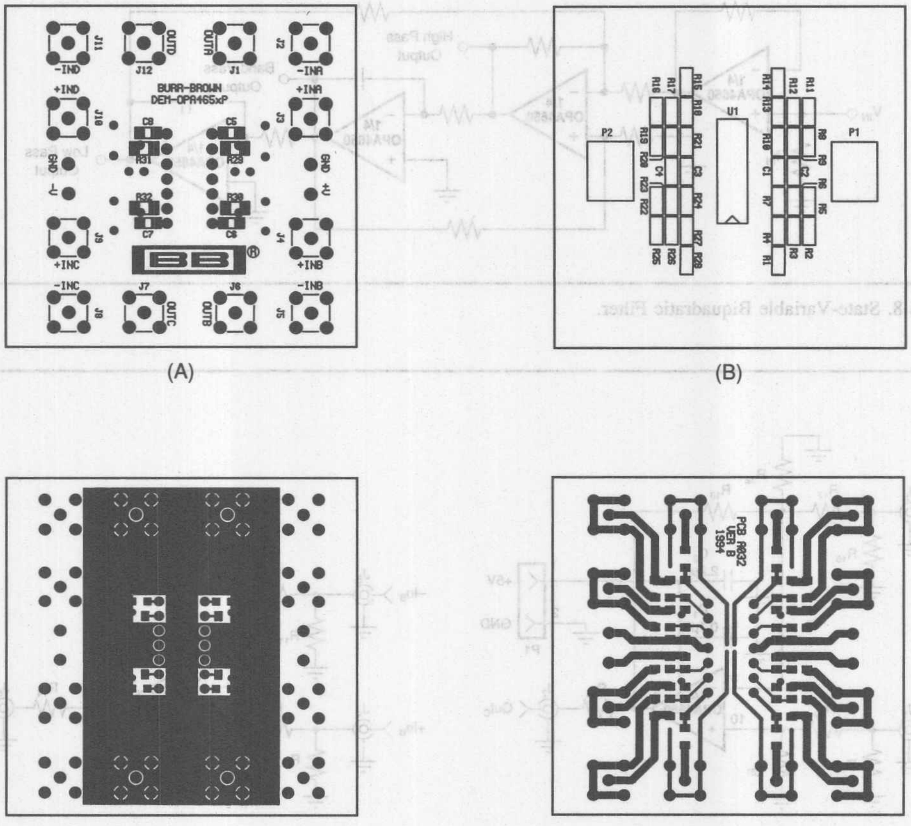
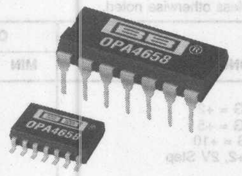


FIGURE 10a. Board Silkscreen (Bottom). 10b. Board Silkscreen (Top). 10c. Board Layout (Solder Side). 10d. Board Layout (Component Side).

BURR - BROWN®



OPA4658

Quad Wideband, Low Power Current Feedback OPERATIONAL AMPLIFIER

FEATURES

- GAIN BANDWIDTH: 900MHz at G = 2
- GAIN OF 2 STABLE
- LOW POWER: 50mW PER AMP
- LOW DIFF GAIN/PHASE ERRORS: 0.015%/0.02°
- HIGH SLEW RATE: 1700V/µs
- PACKAGE: 14-Pin DIP and 14-Pin SOIC

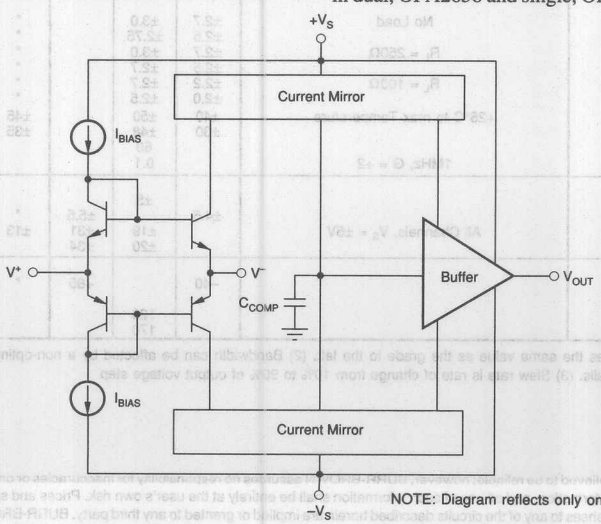
APPLICATIONS

- MEDICAL IMAGING
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- COMMUNICATIONS
- PULSE AMPLIFIERS
- ADC/DAC GAIN AMPLIFIER
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER

DESCRIPTION

The OPA4658 is a quad ultra-wideband, low power current feedback video operational amplifier featuring high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low quiescent current make the OPA4658 a perfect choice for numerous video, imaging and communications applications.

The OPA4658 is internally compensated for stability in gains of 2 or greater. The OPA4658 is also available in dual, OPA2658 and single, OPA658 configurations.



NOTE: Diagram reflects only one-fourth of the OPA4658.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PARAMETER	CONDITION	OPA4658P, U MIN	OPA4658P, U TYP	OPA4658P, U MAX	OPA4658PB, UB MIN	OPA4658PB, UB TYP	OPA4658PB, UB MAX	UNITS
FREQUENCY RESPONSE								
Closed-Loop Bandwidth(2)	G = +2		450			*(1)		MHz
	G = +5		195			*		MHz
	G = +10		130			*		MHz
Slew Rate(3)	G = +2, 2V Step		1700		1000	*		V/μs
At Minimum Specified Temperature			1500		900	*		V/μs
Settling Time: 0.01%	G = +2, 2V Step		20			*		ns
0.1%	G = +2, 2V Step		15.1			*		ns
1%	G = +2, 2V Step		4.8			*		ns
Spurious Free Dynamic Range	f = 5MHz, G = +2, V_O = 2Vp-p		66			*		dBc
	f = 20MHz, G = +2, V_O = 2Vp-p		57			*		dBc
Third-Order Intercept Point	f = 10MHz		38			*		dBm
Differential Gain	G = +2, NTSC, V_O = 1.4Vp-p, R_L = 150Ω		0.015			*		%
Differential Phase	G = +2, NTSC, V_O = 1.4Vp-p, R_L = 150Ω		0.02			*		degrees
Crosstalk	Input Referred, 5MHz, Three Active Channels		74			*		dB
	Input Referred, 5MHz, Channel-to-Channel		85			*		dB
OFFSET VOLTAGE								
Input Offset Voltage			±1.5	±5.5		±2	±5	mV
Over Temperature			±5	±8		±4	±8	mV
Power Supply Rejection	V_S = ±4.5 to ±5.5V	55	70		58	75		dB
INPUT BIAS CURRENT								
Non-Inverting	V_{CM} = 0V		±6.5	±30		*	±18	μA
Over Temperature			±10	±80		*	±35	μA
Inverting	V_{CM} = 0V		±1.1	±35		*	*	μA
Over Temperature			±30	±75		*	*	μA
NOISE								
Input Voltage Noise Density								
f = 100Hz			7.2			*		nV/√Hz
f = 10kHz			3.3			*		nV/√Hz
f = 1MHz			3.3			*		nV/√Hz
f_B = 100Hz to 200MHz			47			*		μVrms
Inverting Input Bias Current Noise Density: f = 10MHz			12.6			*		pA/√Hz
Non-Inverting Input Current Noise Density: f = 10MHz			12.6			*		pA/√Hz
Noise Figure (NF)	R_S = 100Ω		9.5			*		dBm
	R_S = 50Ω		11			*		dBm
INPUT VOLTAGE RANGE								
Common-Mode Input Range			±2.9			*		V
Over Temperature		±2.5			*			V
Common-Mode Rejection	V_{CM} = ±1V	45	52		*	*		dB
INPUT IMPEDANCE								
Non-Inverting			500 || 1			*		kΩ ||pF
Inverting			25			*		Ω
OPEN-LOOP TRANSIMPEDANCE								
Open-Loop Transimpedance	V_O = ±2V, R_L = 100Ω	150	350		200	360		kΩ
Over Temperature	V_O = ±2V, R_L = 100Ω	100	290		150	300		kΩ
OUTPUT								
Voltage Output	No Load	±2.7	±3.0		*	*		V
Over Temperature		±2.5	±2.75		*	*		V
Voltage Output	R_L = 250Ω	±2.7	±3.0		*	*		V
Over Temperature		±2.5	±2.7		*	*		V
Voltage Output	R_L = 100Ω	±2.2	±2.7		*	*		V
Over Temperature		±2.0	±2.5		*	*		V
Current Output	+25°C to max Temperature	±40	±50		±45	*		V
Over Temperature		±30	±48		±35	*		mA
Short Circuit Current			60			*		mA
Output Resistance	1MHz, G = +2		0.1			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Operating Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current	All Channels, V_S = ±5V		±19	±31	±13	±20	±23	mA
Over Temperature			±20	±34		±21	±26	mA
TEMPERATURE RANGE								
Specification: P, U, PB, UB		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
P			120			*		°C/W
U			170			*		°C/W

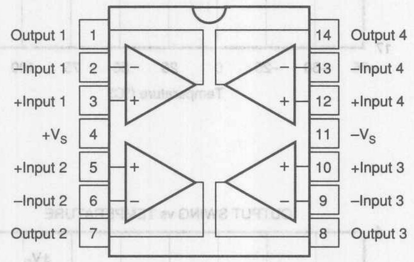
NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Bandwidth can be affected by a non-optimal PC board layout. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

Internal Power Dissipation(1) .... See Applications Information
Differential Input Voltage .... Total V_S
Input Voltage Range .... See Applications Information
Storage Temperature Range: P, PB, U, UB .... –40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
(soldering, SOIC 3s) .... +260°C
Junction Temperature (T_J) .... +175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PIN CONFIGURATION

Top View — DIP/SOIC



OPA4658P, PB OPA4658U, UB	14-Pin Plastic DIP 14-Pin Plastic SOIC	010 235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION(1)

MODEL	PACKAGE	TEMPERATURE RANGE
OPA4658P, PB OPA4658U, UB	14-Pin Plastic DIP 14-Pin Plastic SOIC	–40°C to +85°C –40°C to +85°C

NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by pin 8. Refer to mechanical section for the location.

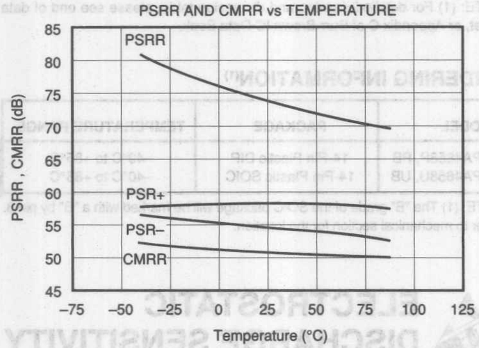
ELECTROSTATIC DISCHARGE SENSITIVITY

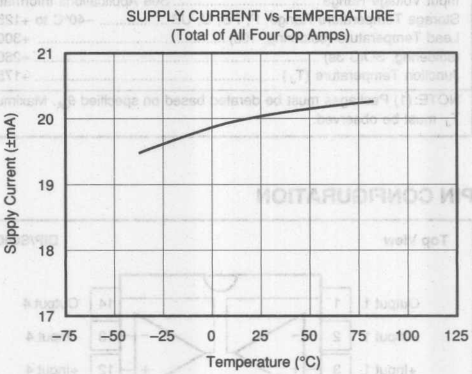
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

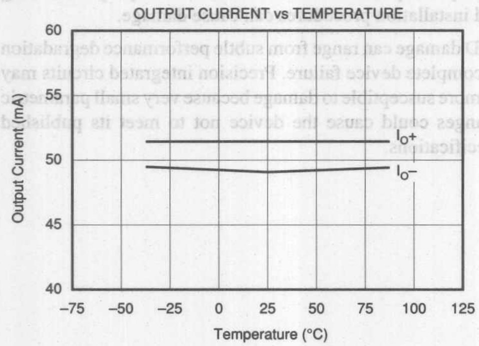
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

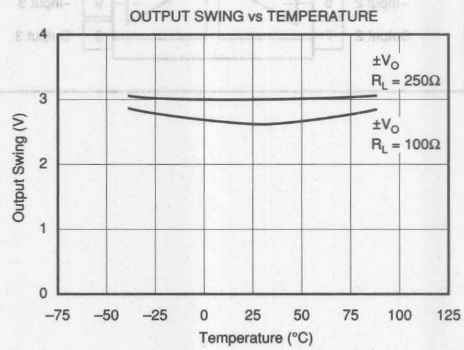
TYPICAL PERFORMANCE CURVES

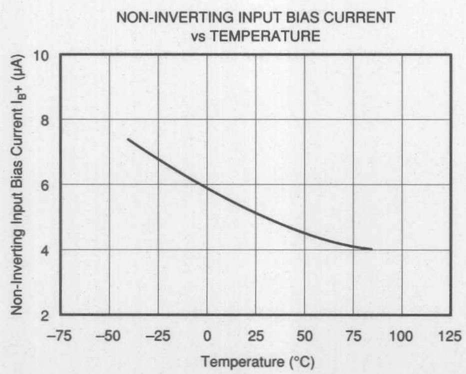
$T_A = +25°C$, $V_S = \pm5V$, $R_L = 100\Omega$, $C_L = 2pF$, $R_{FB} = 402\Omega$, unless otherwise noted.

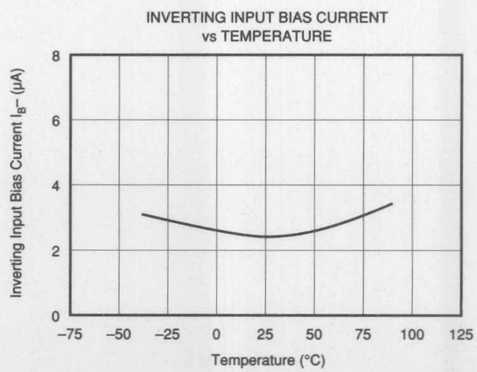








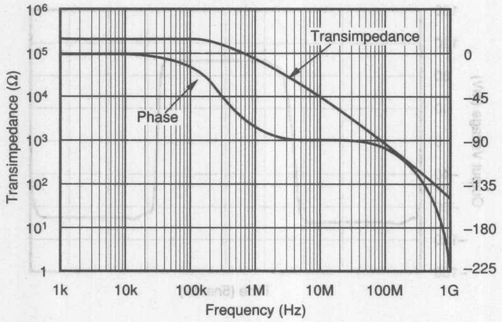




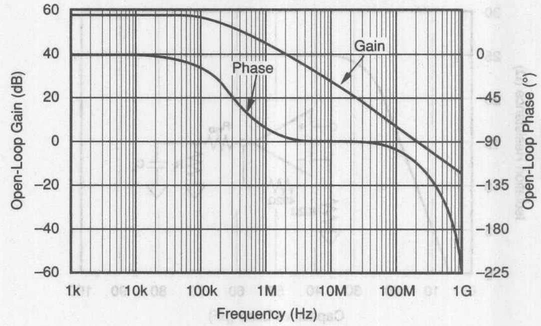
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = ±5V$, $R_L = 100Ω$, $C_L = 2pF$, $R_{FB} = 402Ω$, unless otherwise noted.

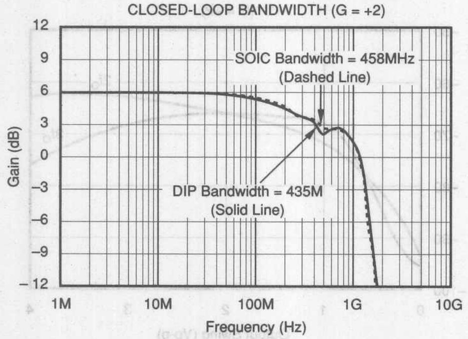
OPEN-LOOP TRANSIMPEDANCE AND PHASE vs FREQUENCY



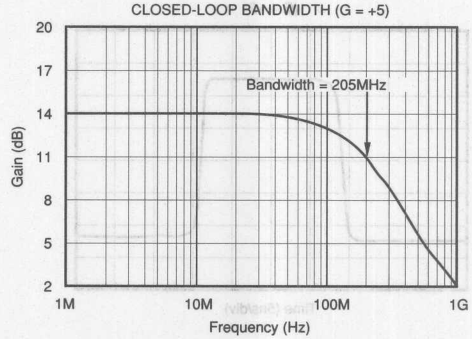
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



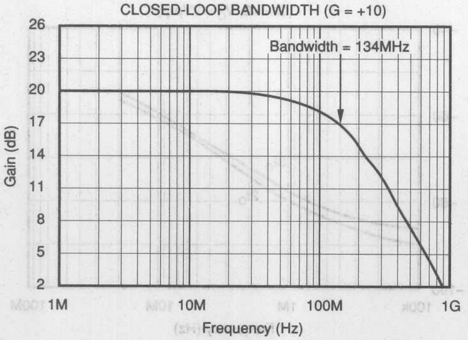
CLOSED-LOOP BANDWIDTH (G = +2)



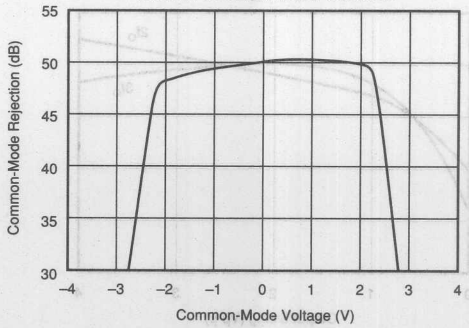
CLOSED-LOOP BANDWIDTH (G = +5)



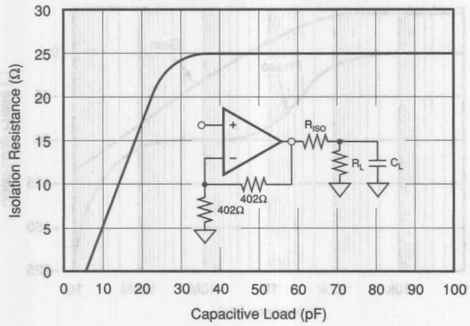
CLOSED-LOOP BANDWIDTH (G = +10)



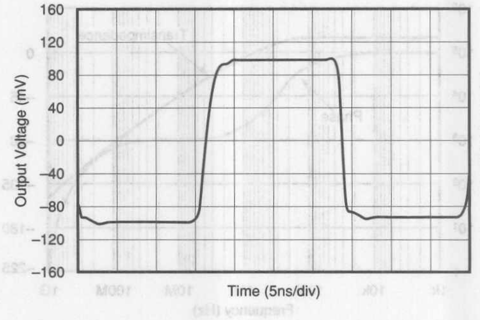
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



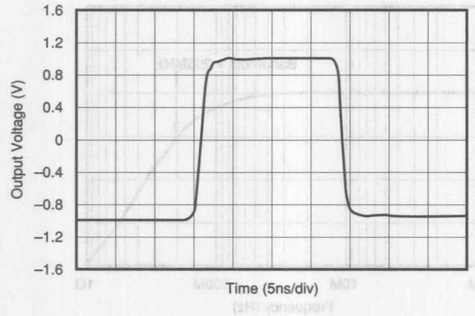
RECOMMENDED ISOLATION RESISTANCE
vs CAPACITIVE LOAD FOR G = +2



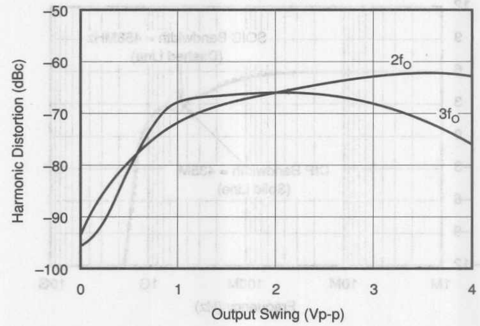
SMALL SIGNAL TRANSIENT RESPONSE
(G = +2)



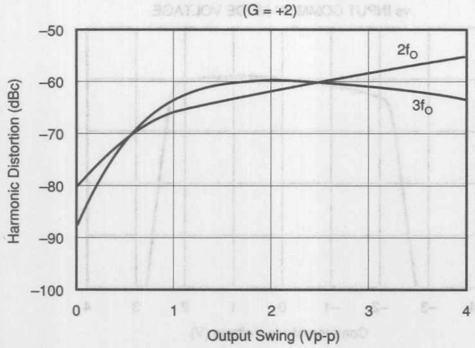
LARGE SIGNAL TRANSIENT RESPONSE
(G = +2)



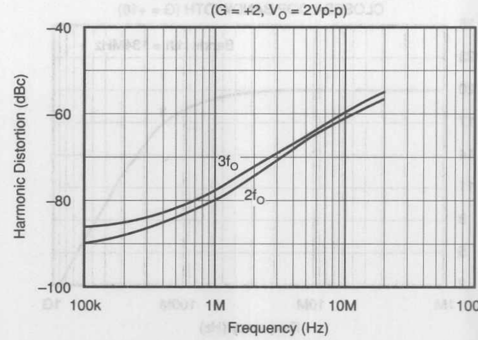
5MHz HARMONIC DISTORTION vs OUTPUT SWING
(G = +2)

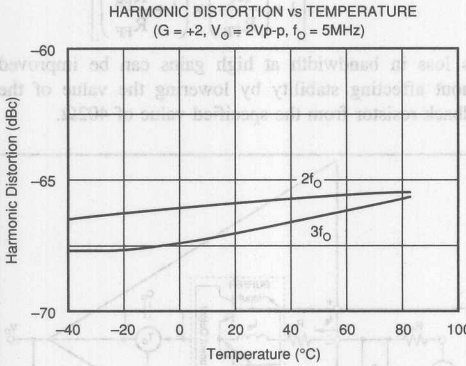


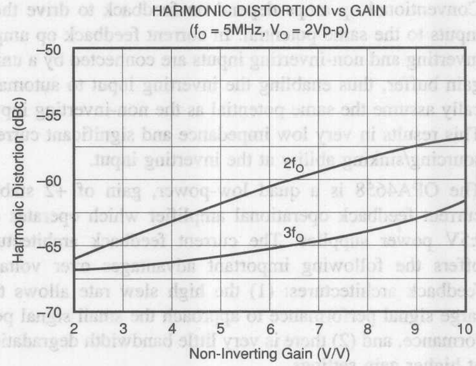
10MHz HARMONIC DISTORTION vs OUTPUT SWING
(G = +2)



HARMONIC DISTORTION vs FREQUENCY
(G = +2, V_O = 2Vp-p)




HARMONIC DISTORTION vs TEMPERATURE
(G = +2, V_O = 2Vp-p, f_O = 5MHz)
Harmonic Distortion (dBc)
–60
–65
–70
–40
–20
0
20
40
60
80
100
Temperature (°C)
2f_O
3f_O


HARMONIC DISTORTION vs GAIN
(f_O = 5MHz, V_O = 2Vp-p)
Harmonic Distortion (dBc)
–50
–55
–60
–65
–70
2
3
4
5
6
7
8
9
10
Non-Inverting Gain (V/V)
2f_O
3f_O

DISCUSSION OF PERFORMANCE

THEORY OF OPERATION

Conventional op amps depend on feedback to drive their inputs to the same potential. In current feedback op amps, inverting and non-inverting inputs are connected by a unity gain buffer, thus enabling the inverting input to automatically assume the same potential as the non-inverting input. This results in very low impedance and significant current sourcing/sinking ability at the inverting input.

The OPA4658 is a quad low-power, gain of +2 stable, current feedback operational amplifier which operates on ±5V power supplies. The current feedback architecture offers the following important advantages over voltage feedback architectures: (1) the high slew rate allows the large signal performance to approach the small signal performance, and (2) there is very little bandwidth degradation at higher gain settings.

The current feedback architecture of the OPA4658 provides the traditional strength of excellent large signal response plus wide bandwidth, making it a good choice for use in high resolution video, medical imaging and digital communications. The low power requirements make it an excellent choice for numerous portable applications.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output voltage is equal to T_O X I_E. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

For non-inverting operation, the input signal is applied to the non-inverting (high impedance buffer) input. The output error current (I_E) is generated by the buffer at the low impedance inverting input. The signal generated at the op-amp output is fed back to the inverting input such that the overall gain is $(1 + R_{FB}/R_{FF})$.

The closed-loop gain for the OPA4658 can be calculated using the following equations:

$$\text{Inverting Gain} = \frac{-\left(\dfrac{R_{FB}}{R_{FF}}\right)}{1+\dfrac{1}{\text{Loop Gain}}} \qquad (1)$$

$$\text{Non–Inverting Gain} = \frac{\left[1+\dfrac{R_{FB}}{R_{FF}}\right]}{1+\dfrac{1}{\text{Loop Gain}}} \qquad (2)$$

$$\text{where Loop Gain} = \left[\frac{T_O}{R_{FB}+R_S\left(1+\dfrac{R_{FB}}{R_{FF}}\right)}\right]$$

At higher gains the small inverting input impedance R_S causes an apparent loss in bandwidth. This can been seen from the equation:

$$BW_{ACTUAL} = \frac{BW_{IDEAL}}{\left[1+\left(\dfrac{R_S}{R_{FB}}\right)\times\left(1+\dfrac{R_{FB}}{R_{FF}}\right)\right]} \qquad (3)$$

This loss in bandwidth at high gains can be improved without affecting stability by lowering the value of the feedback resistor from the specified value of 402Ω.

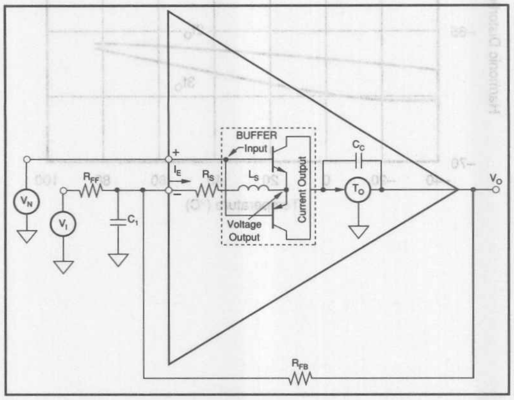


FIGURE 1. Equivalent Circuit.

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the gained-up input offset voltage and effects from current sources that influence DC operation. The output offset is calculated by the following equation (refer to Figure 2):

$$\text{Output Offset Voltage} = \pm Ib_N \times R_N\left(1+\frac{R_{FB}}{R_{FF}}\right)\pm V_{IO}\left(1+\frac{R_{FB}}{R_{FF}}\right)\pm Ib_I \times R_{FB} \qquad (4)$$

If all terms are divided by the gain $(1 + R_{FB}/R_{FF})$ it can be observed that the input referred offset improves as gain increases. The effective noise at the output can be determined by taking the root sum of the squares of equation (4) and substituting the spectral noise values for the DC current and voltage terms (found in the specification table). This applies

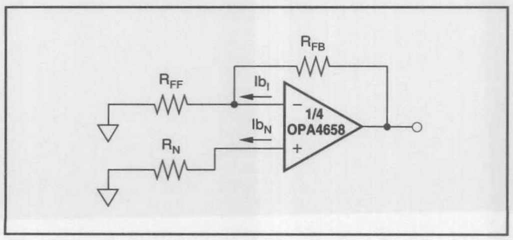


FIGURE 2. Output Offset Voltage Equivalent Circuit.

to noise from the op amp only. Note that both the noise figure (NF) and the equivalent input offset voltages improve as the closed loop gain increases (by keeping R_{FB} fixed and reducing R_{FF} with $R_N = 0\Omega$).

INCREASING BANDWIDTH AT HIGH GAINS

The closed-loop bandwidth can be extended at high gains by reducing the value of the feedback resistor R_{FB}. This bandwidth reduction is caused by the feedback current being split between R_S and R_{FF} (refer to Figure 1). As the gain increases (for a fixed R_{FB}), more feedback current is shunted through R_{FF}, which reduces closed-loop bandwidth.

WIRING PRECAUTIONS/CIRCUIT LAYOUT

Maximizing the OPA4658's capability requires some wiring precautions and use of high-frequency layout techniques. Oscillation, ringing, poor bandwidth, settling, gain peaking and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low impedance signal paths, and should be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit elements should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray parasitic circuits.

As with all high-frequency circuits, grounding is the most important application consideration for the OPA4658. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2 ounce copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low impedance common return path for signal and power, and conduct heat from active circuit package pins into ambient air by convection. However, do not place the ground plane under or near the inputs.

Supply bypassing is extremely critical and must **always** be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2μF) with very short leads are recommended. A parallel 0.1μF ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Power supply bypassing with 0.1μF and 2.2μF surface mount capacitors is recommended. It is essential to keep the 0.1μF capacitor very close to the power supply pins. Refer to the demonstration board layout in Figures 12a through d.

2) Whenever possible, use surface mount components. Do not use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if wires must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on the back side of the PC board. Good component selection is essential. Capacitors used in critical locations should be low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary p-n diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA4658 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade the AC performance or produce small oscillations.

5) Use a feedback resistor (usually 402Ω) in gain of 2 applications for the best performance. For higher gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely **unacceptable** in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. A longer feedback path than this will decrease the realized bandwidth substantially. Refer to the demonstration board layout at the end of the data sheet.

6) As mentioned above, surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA4658U (SOIC package) will offer the best AC performance. The parasitic package impedance for the SOIC is lower than the 14-pin PDIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) These amplifiers are designed for ±5V supplies. Although they will operate well with +5V and –5.2V, use of ±15V supplies will destroy them.

9) Standard commercial test equipment has not been designed to test devices in the OPA4658's speed range. Bench top op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; *there are no shortcuts.*

ESD PROTECTION

ESD damage has been well recognized for MOSFET devices, but any semiconductor device is vulnerable to this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are strongly recommended when handling the OPA4658.

OUTPUT DRIVE CAPABILITY

The OPA4658 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA4658 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA4658 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

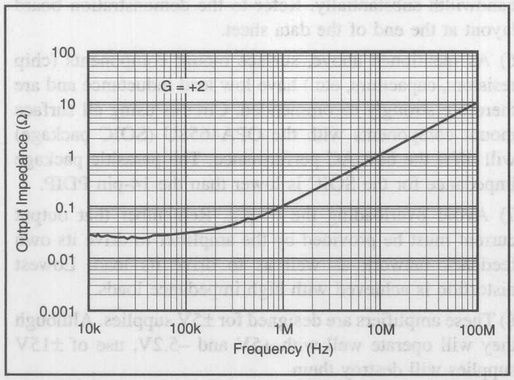


FIGURE 3. Closed-Loop Output Impedance vs Frequency.

most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_S = \pm 5V$, P_{DQ} = 10V x 34mA = 340mW, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_S/2$, and is equal to P_{DL}, max = $(\pm V_S)^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA4658's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated with its characteristic impedance.

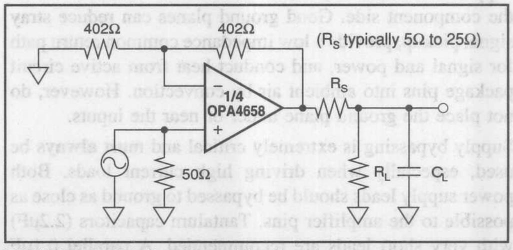


FIGURE 4. Driving Capacitive Loads.

COMPENSATION

The OPA4658 is internally compensated and is stable in gains of two or greater, with a phase margin of approximately 66° in a gain of +2V/V. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA4658 in a good layout is very flat with frequency.

DISTORTION

The OPA4658's Harmonic Distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 5. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

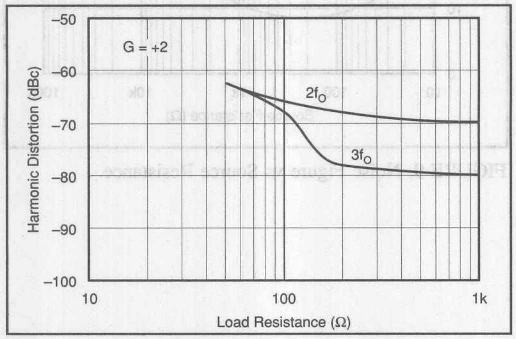


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept is an important parameter for many RF amplifier applications. Figure 6 shows the OPA4658's two tone, third-order intercept vs frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA4658 to operate in a gain of +2V/V and drive 2Vp-p into 100Ω at a frequency of 10MHz. Referring to Figure 6 we find that the intercept point is +38dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level, dBm

For this case OPI^3P = 38dBm, P_O = 7dBm, and the third Harmonic = 2(38 – 7) = 62dB below the fundamental. The OPA4658's low distortion makes the device an excellent choice for a variety of RF signal processing applications.

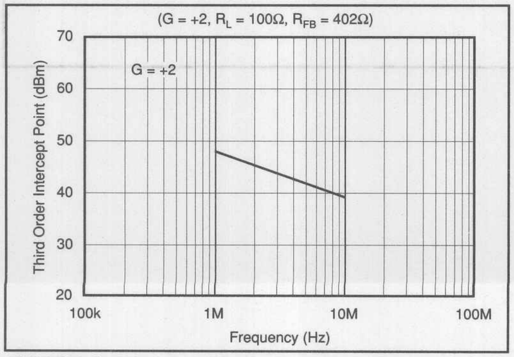


FIGURE 6. Third Order Intercept Point vs Frequency.

CROSSTALK

Crosstalk is the undesired result of the signal of one channel mixing with and reproducing itself in the output of another channel or channels. Crosstalk is inclined to occur in most multichannel integrated circuits. In quad devices, the effect of crosstalk is measured by driving three channels and observing the output of the undriven channel over various frequencies. The magnitude of this effect is referenced in terms of channel-to-channel isolation and expressed in decibels. Input referred points to the fact that there is a direct correlation between gain and crosstalk, therefore at increased gain, crosstalk also increases by a factor equal to that of the gain. Figure 7 illustrates the measured effect of crosstalk in the OPA4658U.

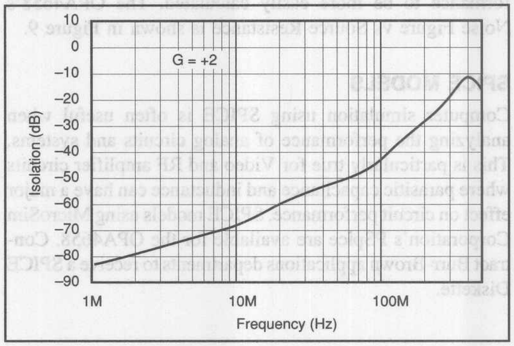


FIGURE 7. Channel-to-Channel Isolation (three active channels).

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are critical specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

DG and DP of the OPA4658 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 8 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer

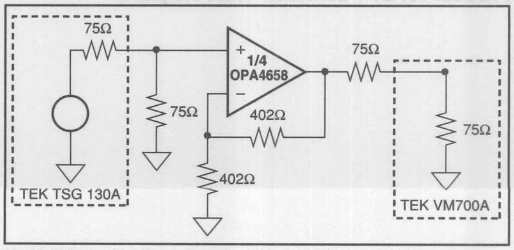


FIGURE 8. Configuration for Testing Differential Gain/Phase.

OPA4658 2 OPERATIONAL AMPLIFIERS

was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA4658 is 0.015% differential gain and 0.02° differential phase to both NTSC and PAL standards.

NOISE FIGURE

The OPA4658's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA4658's Noise Figure vs Source Resistance is shown in Figure 9.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA4658. Contract Burr-Brown applications departments to receive a SPICE Diskette.

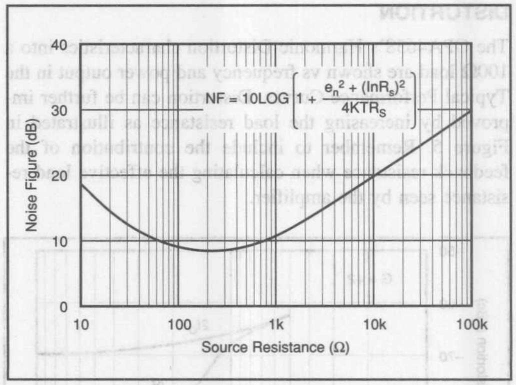


FIGURE 9. Noise Figure vs Source Resistance.

TYPICAL APPLICATIONS

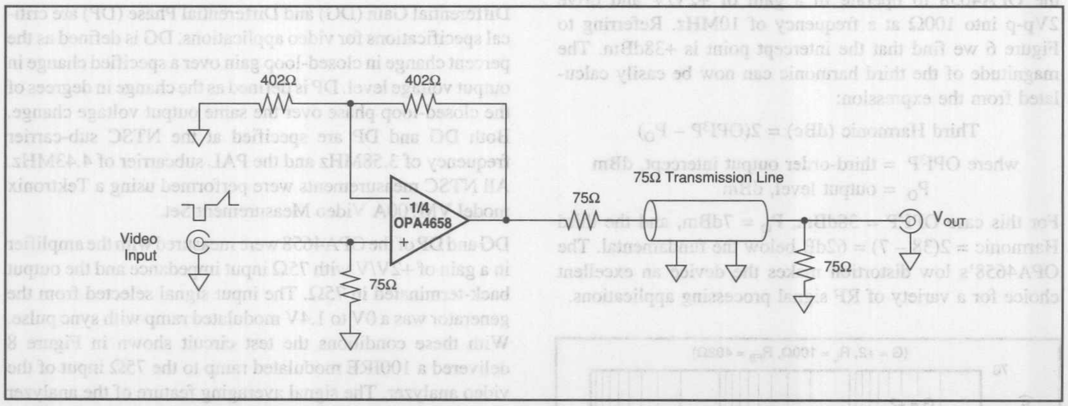


FIGURE 10. Low Distortion Video Amplifier.

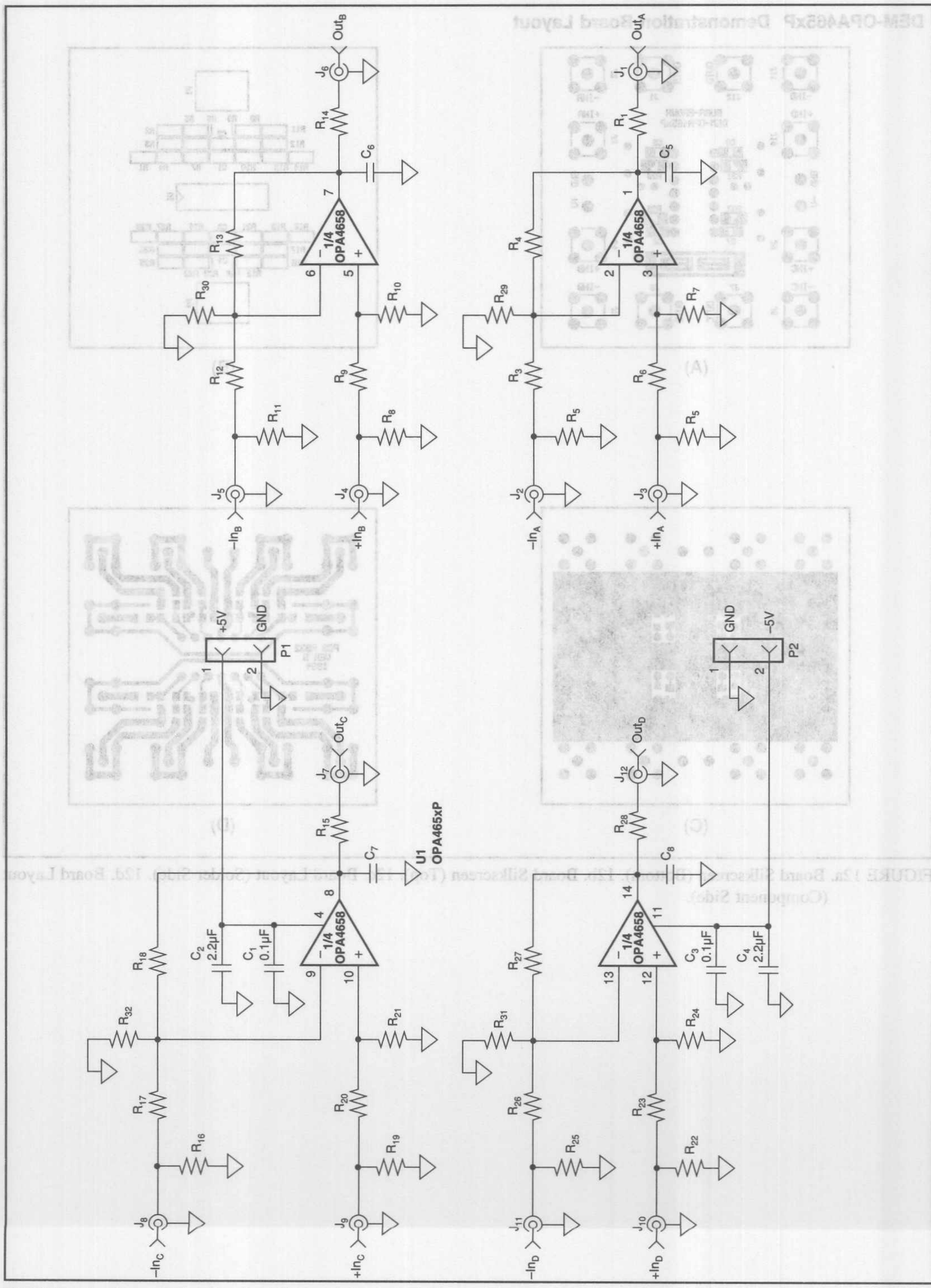


FIGURE 11. Circuit Detail for the PC Board Layout of Figure 12.

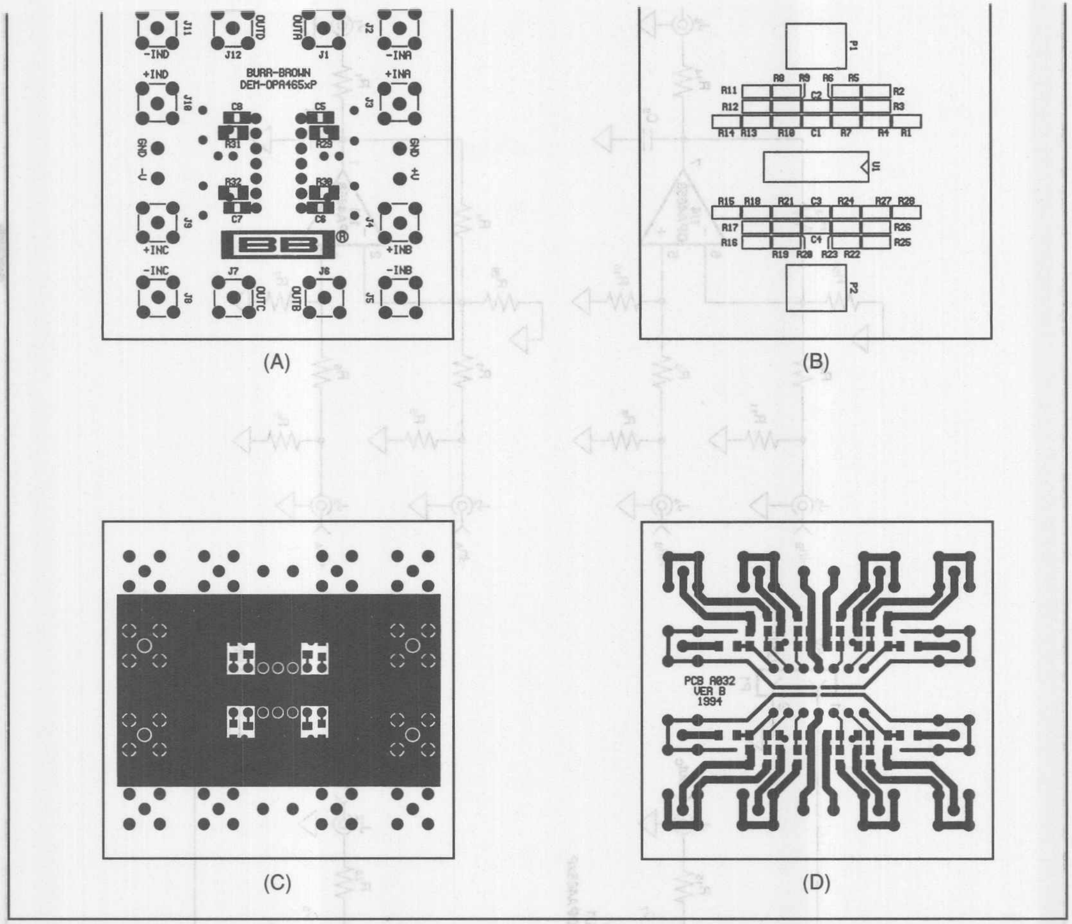
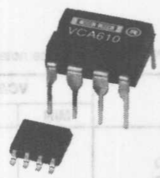


FIGURE 12a. Board Silkscreen (Bottom). 12b. Board Silkscreen (Top). 12c. Board Layout (Solder Side). 12d. Board Layout (Component Side).



WIDEBAND VOLTAGE CONTROLLED AMPLIFIER

FEATURES

- WIDE GAIN CONTROL RANGE: 80dB
- SMALL PACKAGE: 8-pin SOIC or DIP
- WIDE BANDWIDTH: 30MHz
- LOW VOLTAGE NOISE: $2.2nV/\sqrt{Hz}$
- FAST GAIN SLEW RATE: 300dB/µs
- EASY TO USE

APPLICATIONS

- ULTRASOUND
- AGC AMPLIFIER
- ANALYTICAL INSTRUMENTATION
- SONAR
- ACTIVE FILTERS
- LOG AMPLIFIER
- IF CIRCUITS
- CCD CAMERAS

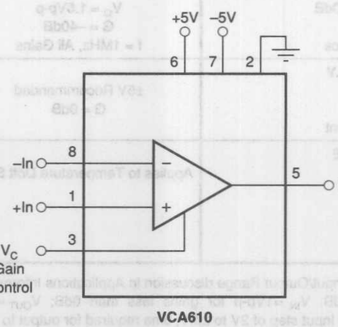
DESCRIPTION

The VCA610 is a wideband, continuously variable, voltage controlled gain amplifier. It provides linear-dB gain control with high impedance inputs. It is designed to be used as a flexible gain control element in a variety of electronic systems.

The VCA610 has a gain control range of 80dB (–40dB to +40dB) providing both gain and attenuation for maximum flexibility in a small 8-pin SOIC or plastic dual-in-line package. The broad attenuation range can be used for gradual or controlled channel turn-on and turn-off for applications in which abrupt gain changes can create artifacts or other errors. In addition, the output can be disabled to provide –80dB of attenuation. Group delay variation with gain is typically less than ±2ns across a bandwidth of 1 to 15MHz.

The VCA610 has a noise figure of 3.5dB (with an R_S of 200Ω) including the effects of both current and voltage noise. Instantaneous output dynamic range is 70dB for gains of 0dB to +40dB with 1MHz noise bandwidth. The output is capable of driving 100Ω. The high speed, 300dB/µs, gain control signal is a unipolar voltage that varies the gain linearly in dB/V.

The VCA610 is designed with a very fast overload recovery time of only 200ns. This allows a large signal transient to overload the output at high gain, without obscuring low-level signals following closely behind. The excellent overload recovery time and distortion specifications optimize this device for low-level doppler measurements.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

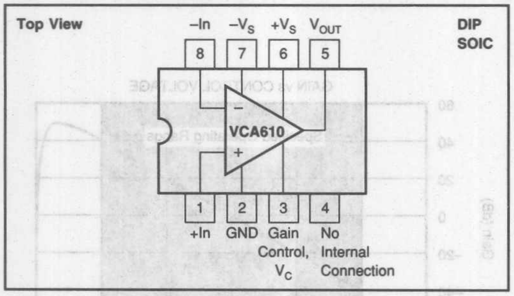
All specifications at $V_S = \pm5V$, $R_L = 500\Omega$, $R_S = 0\Omega$, and $T_A = +25°C$ unless otherwise noted.

		VCA610PA, UA			VCA610P, U			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT NOISE								
Input Voltage Noise	$G = +40dB$, $R_S = 0\Omega$		2.2			*		$nV/\sqrt{Hz}$
Input Current Noise	$G = -40dB$ to $+40dB$		1.4			*		$pA/\sqrt{Hz}$
Noise Figure	$G = +40dB$, $R_S = 200\Omega$		3.5			*		dB
INPUT								
Input Impedance	Common-Mode		1 || 1			*		MΩ || pF
Bias Current	All Gains		6			*		µA
Offset Current	All Gains		2			*		µA
Differential Voltage Range			(1)			*		
Common-Mode Voltage Range			±2.5			*		V
Common-Mode Rejection			50			*		dB
GAIN								
Specified Gain Range		–40		+40	*		*	dB
Gain Accuracy(2)	$-40dB \le G \le +40dB$		±0.5	±2		±2	±4	dB
Gain Accuracy Temperature Drift	$T_A = -25°C$ to $+85°C$		±0.01			*		dB/°C
Gain with Output Disabled	$+0.1V \le V_C \le +2.0V$, f = 1MHz		–80			*		dB
GAIN CONTROL								
Gain Scaling Factor	$-40dB \le G \le +40dB$		40			*		dB/V
Control Voltage (V_C)	$G = -40dB$ ($V_C = 0V$) to $+40dB$ ($V_C = -2V$)	0		–2	*		*	V
Bandwidth	–3dB		1			*		MHz
Slew Rate	80dB Gain Step		300			*		dB/µs
Settling Time: 1%	$V_{IN} = 10mVDC$, $\Delta G = 80dB$		800			*		ns
Input Impedance			1 || 1			*		MΩ || pF
Input Bias Current	All Gains		2			*		µA
Output Offset Change(3)	$\Delta G = 80dB$		±30	±75		*	±125	mV
FREQUENCY RESPONSE								
Bandwidth, Small-Signal	–3dB, All Gains		30			*		MHz
Bandwidth, Large-Signal	$V_O = 1Vp\text{-}p$, $G \ge 0dB$		25			*		MHz
Group Delay Unit-to-Unit Variation								
$0dB \le G \le +40dB$	f = 1 to 15MHz		±1			*		ns
$-40dB \le G < 0dB$	f = 1 to 15MHz		±2			*		ns
Output Slew Rate	$V_O = 1Vp\text{-}p$		60			*		V/µs
Overload Recovery(4)			200			*		ns
Two-tone Intermodulation Distortion(5)	Small-Signal		–50			*		dBc
Two-tone, 3rd Order IMD Intercept(5)	Small-Signal		15			*		dBm
OUTPUT								
Voltage Swing(1)								
G = +40dB		±1	±1.6		*	*		V
G = 0dB		±0.5	±0.75		*	*		V
Output Voltage Limit		Symmetrical to Ground (±10%)				*		
Short-Circuit Current	Continuous to Common		±80			*		mA
Instantaneous Dynamic Range (IDR)(6)								
G = 0dB to +40dB	$V_O = 1.5Vp\text{-}p$		70			*		dB
Offset	G = –40dB		±2	±30		*	*	mV
Output Resistance	f = 1MHz, All Gains		10			*		Ω
POWER SUPPLY								
Specification	±5V Recommended	±4.5		±5.5	*		*	V
PSR	G = 0dB	40	50			*		dB
Quiescent Current			–26/+30	±32		*	*	mA
TEMPERATURE								
Specification	Applies to Temperature Drift Specs	–25		+85	*		*	°C
Operation		–40		+125	*			°C
θ_{JA}								
DIP			90			*		°C/W
SO-8			100			*		°C/W

NOTES: (1) See Input/Output Range discussion in Applications Information Section (Figure 2). (2) Gain is laser trimmed and tested at gains of –40dB, 0dB, +15dB, +25dB, and +40dB; V_{IN} =1Vp-p for gains less than 0dB; V_{OUT} = 1V for gains of 0dB to +40dB. (3) Output offset change from offset at G = –40dB. (4) Gain = +40dB; Input step of 2V to 2mV; time required for output to return from saturation to linear operation. (5) V_{IN} = 7mVp-p, V_{OUT} = 700mVp-p (250mVrms); Output Power = –10dBm/tone, equal amplitude tones of 5MHz ±500Hz, G = +40dB. See typical performance curves. (6) With $R_S = 0\Omega$, and noise bandwidth of 1MHz. IDR = 20 log ($V_{ORMS}/(e_{ORMS} \times \sqrt{BW})$); where V_{ORMS} is rms output voltage, e_{ORMS} is output noise spectral density, and BW is noise bandwidth.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

PIN CONFIGURATION



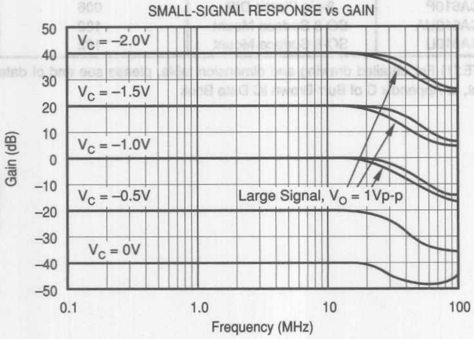
ABSOLUTE MAXIMUM RATINGS

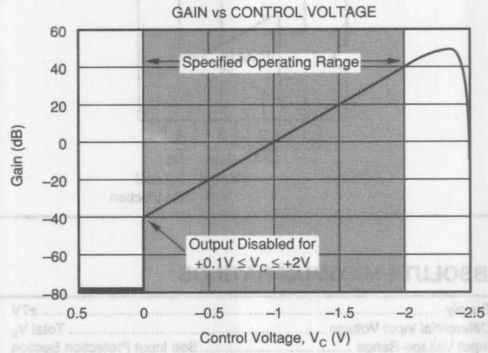
Supply	±7V
Differential Input Voltage	Total V_S
Input Voltage Range	See Input Protection Section
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, DIP, 10s)	+300°C
Lead Temperature (soldering, SOIC, 3s)	+260°C
Output Short-Circuit to Ground (+25°C)	Continuous
Junction Temperature (T_J)	+175°C

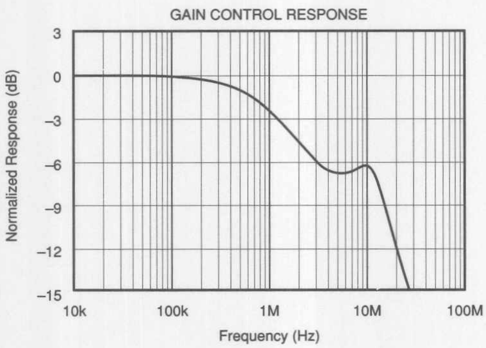
ORDERING AND PACKAGE INFORMATION

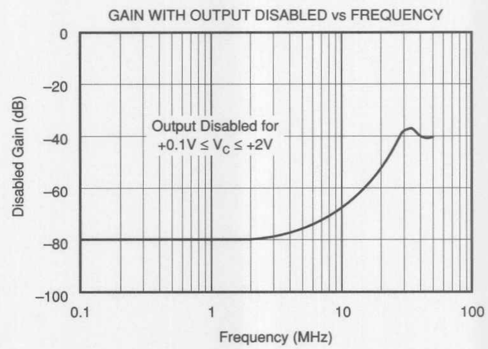
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
VCA610PA	8-pin Plastic DIP	006
VCA610P	8-pin Plastic DIP	006
VCA610UA	SO-8 Surface-Mount	182
VCA610U	SO-8 Surface-Mount	182

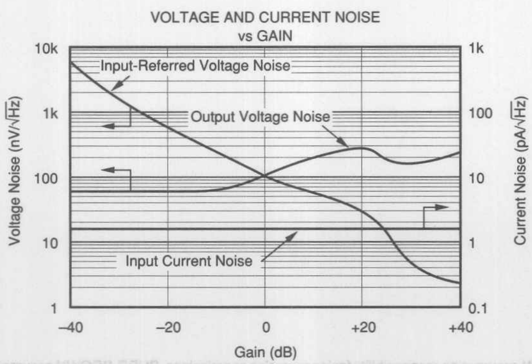
NOTE:(1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

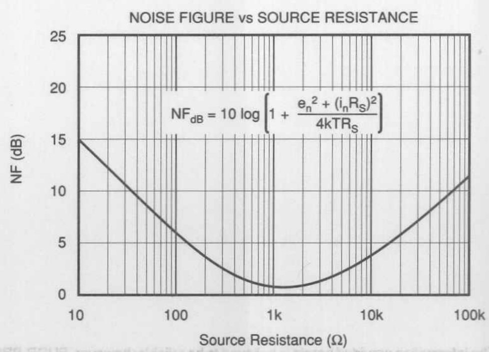

SMALL-SIGNAL RESPONSE vs GAIN
$V_C = -2.0V$
$V_C = -1.5V$
$V_C = -1.0V$
$V_C = -0.5V$
$V_C = 0V$
Large Signal, V_O = 1Vp-p
Gain (dB)
Frequency (MHz)


GAIN vs CONTROL VOLTAGE
Specified Operating Range
Output Disabled for
$+0.1V \leq V_C \leq +2V$
Gain (dB)
Control Voltage, V_C (V)


GAIN CONTROL RESPONSE
Normalized Response (dB)
Frequency (Hz)


GAIN WITH OUTPUT DISABLED vs FREQUENCY
Output Disabled for
$+0.1V \leq V_C \leq +2V$
Disabled Gain (dB)
Frequency (MHz)

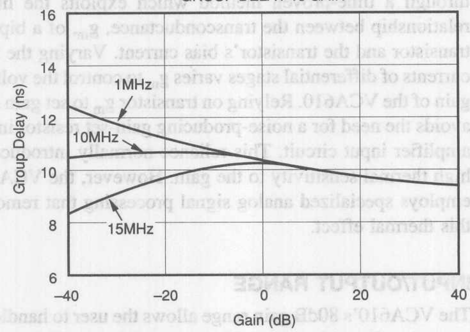

VOLTAGE AND CURRENT NOISE
vs GAIN
Input-Referred Voltage Noise
Output Voltage Noise
Input Current Noise
Voltage Noise ($nV/\sqrt{Hz}$)
Current Noise ($pA/\sqrt{Hz}$)
Gain (dB)


NOISE FIGURE vs SOURCE RESISTANCE
$NF_{dB} = 10 \log \left[1 + \frac{e_n^2 + (i_n R_S)^2}{4kTR_S} \right]$
NF (dB)
Source Resistance (Ω)

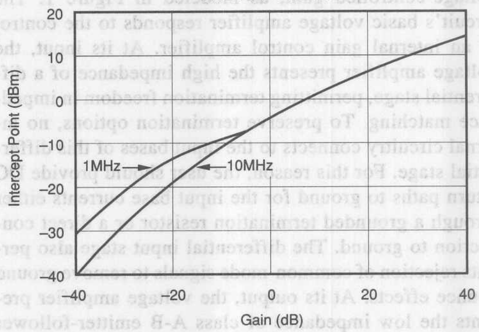
TYPICAL PERFORMANCE CURVES (CONT)

At $V_S = \pm5V$, $R_L = 500\Omega$, $R_S = 0\Omega$, and $T_A = +25°C$ unless otherwise noted.

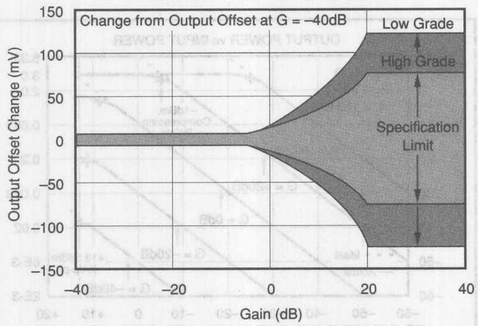
GROUP DELAY vs GAIN



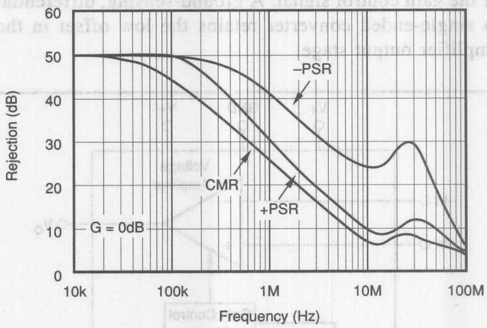
2-TONE, 3rd ORDER INTERMODULATION INTERCEPT vs GAIN



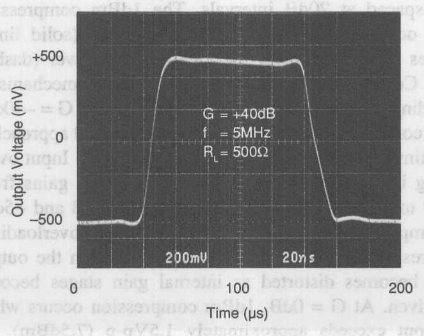
OUTPUT OFFSET CHANGE vs GAIN



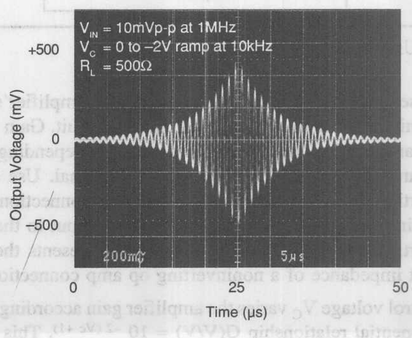
PSR and CMR vs FREQUENCY



LARGE SIGNAL RESPONSE



"DIAMOND PATTERN" RESPONSE



APPLICATIONS INFORMATION

CIRCUIT DESCRIPTION

The VCA610 is a wideband voltage amplifier with a voltage-controlled gain, as modeled in Figure 1. The circuit's basic voltage amplifier responds to the control of an internal gain control amplifier. At its input, the voltage amplifier presents the high impedance of a differential stage, permitting termination freedom in impedance matching. To preserve termination options, no internal circuitry connects to the input bases of this differential stage. For this reason, the user should provide DC return paths to ground for the input base currents either through a grounded termination resistor or a direct connection to ground. The differential input stage also permits rejection of common-mode signals to remove ground bounce effects. At its output, the voltage amplifier presents the low impedance of class A-B emitter-follower stage, again simplifying impedance matching. An open-loop design produces wide bandwidth at all gain levels and avoids the added overload-recovery and propagation delays of feedback designs. Repeated use of differential stages minimizes offset effects for reduced feedthrough of the gain control signal. A ground-sensing, differential to single-ended converter retains the low offset in the amplifier output stage.

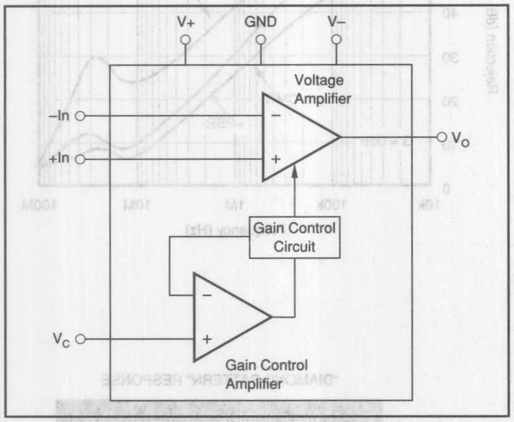


FIGURE 1. Block Diagram of the VCA610.

A user-applied voltage, V_C, controls the amplifier's gain magnitude through a high-speed control circuit. Gain polarity can be either inverting or noninverting depending upon the amplifier input driven by the input signal. Use of the inverting input is recommended since this connection tends to minimize positive feedback from the output to the noninverting input. The gain control circuit presents the high input impedance of a noninverting op amp connection.

Control voltage V_C varies the amplifier gain according to the exponential relationship $G(V/V) = 10^{-2(V_C+1)}$. This translates to the linear, logarithmic relationship $G(dB) = -40 - 40V_C$. Thus, G(dB) varies linearly over the specified –40dB to +40dB range as V_C varies from 0 to –2V. Optionally, making V_C slightly positive, ≥ 0.1V, effectively disables the amplifier, producing 80dB of attenuation.

Internally, the gain control circuit varies the amplifier gain through a time-proven method which exploits the linear relationship between the transconductance, g_m, of a bipolar transistor and the transistor's bias current. Varying the bias currents of differential stages varies g_m to control the voltage gain of the VCA610. Relying on transistor g_m to set gain also avoids the need for a noise-producing gain-set resistor in the amplifier input circuit. This reliance normally introduces a high thermal sensitivity to the gain. However, the VCA610 employs specialized analog signal processing that removes this thermal effect.

INPUT/OUTPUT RANGE

The VCA610's 80dB gain range allows the user to handle an exceptionally wide range of input signal levels. If the unit's input and output voltage range specifications are exceeded, however, signal distortion and amplifier overloading will occur. The VCA610's maximum input and output voltage range is best illustrated in Figure 2.

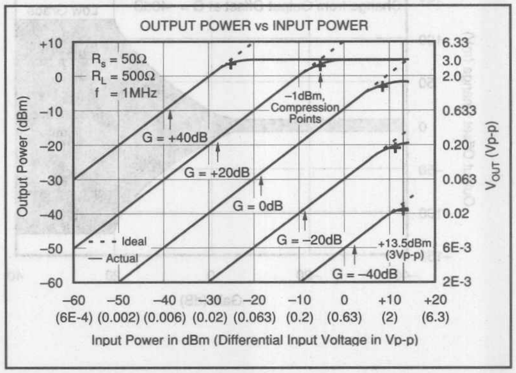


FIGURE 2. Input and Output Range.

Figure 2 plots output power vs input power for five voltage gains spaced at 20dB intervals. The 1dBm compression points occur where the actual output power (solid lines) deviates by –1dBm from the ideal output power (dashed lines). Compression is produced by different mechanisms depending on the selected gain. For example, at G = –40dB, 1dBm compression occurs when the input signal approaches approximately 3Vp-p (13.5dBm for R_S = 50Ω). Input overloading is the compression mechanism for all gains from –40dB to about –5dB. For gains between –5dB and +5dB, the compression is due to internal gain stage overloading. Compression over this gain range occurs when the output signal becomes distorted as internal gain stages become overdriven. At G = 0dB, 1dBm compression occurs when the input exceeds approximately 1.5Vp-p (7.5dBm). At gains greater than about 5dB, the compression mechanism is due to output stage overloading. Output overloading occurs

when either the maximum output voltage swing or output current is exceeded. The VCA610's high output current of ±80mA insures that virtually all output overloads will be limited by voltage swing rather than by current limiting. At G = +40dB, 1dBm compression occurs when the output voltage approaches 3Vp-p (3.5dBm for R_L = 500Ω). Table I below summarizes these results.

GAIN RANGE	OUTPUT COMPRESSION MECHANISM	TO PREVENT OPERATE WITHIN
–40dB < G < –5dB	Input Stage Overload	Input Voltage Range
–5dB < G < +5dB	Internal Stages Overloading	Output Voltage Range
+5dB < G < +40dB	Output Stage Overload	Output Voltage Range

TABLE I. Output Signal Compression.

WIRING PRECAUTIONS

Maximizing the VCA610's capability requires some wiring precautions and high-frequency layout techniques. In general, printed circuit board conductors should be as short and as wide as possible to provide low resistance, low impedance signal paths. Stray signal coupling from the output or power supplies to the inputs should be minimized. Unused inputs should be grounded as close to the package as possible.

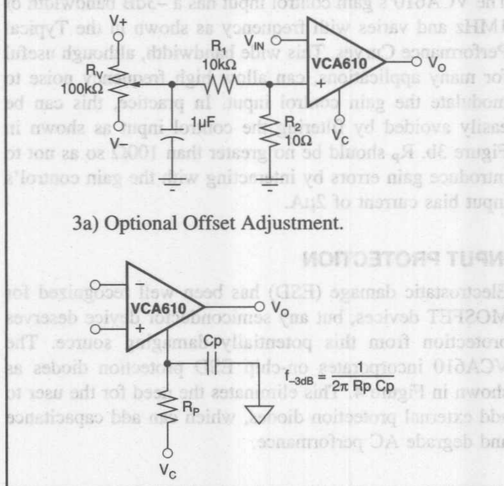
Low impedance ground returns for signal and power are essential. Proper supply bypassing is also extremely critical and must *always* be used. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1µF to 10µF) with very short leads are recommended. Surface mount bypass capacitors will provide excellent results due to their low lead inductance.

OVERLOAD RECOVERY

As shown in Figure 2, the onset of overload occurs whenever the actual output begins to deviate from the ideal expected output. If possible, the user should operate the VCA610 within the linear regions shown in order to minimize signal distortion and overload delay time. However, instances of amplifier overload are actually quite common in Automatic Gain Control (AGC) circuits which involve the application of variable gain to signals of varying levels. The VCA610's design incorporates circuitry which allows it to recover from most overload conditions in 200ns or less. Overload recovery time is defined as the time required for the output to return from overload to linear operation following the removal of either an input or gain control overdrive signal.

OFFSET ADJUSTMENT

Where desired, the offset of the VCA610 can be removed as shown in Figure 3. This circuit simply presents a DC voltage to one of the amplifier's inputs to counteract the offset error voltage. For best offset performance, the trim adjustment should be made with the amplifier set at the maximum gain of the intended application. The offset voltage of the VCA610 varies with gain, limiting the complete offset cancellation to one selected gain. Selecting the maximum gain optimizes offset performance for higher gains where high amplification of the offset effects produces the greatest output offset. Two features minimize the offset control circuit's noise contribution to the amplifier input circuit. First, making the resistance of R_2 a low value minimizes the noise directly introduced by the control circuit. This reduces both the thermal noise of the resistor and the noise produced by the resistor with the amplifier's input noise current. A second noise reduction results from capacitive bypass of the potentiometer output. This filters out power supply noise that would otherwise couple to the amplifier input.



3a) Optional Offset Adjustment.

3b) Control Line Filtering.

FIGURE 3. Optional Offset Adjustment and Control Line Filtering.

This filtering action would diminish as the wiper position approaches either end of the potentiometer but practical conditions prevent such settings. Over its full adjustment range, the offset control circuit produces a ±5mV offset correction for the values shown. However, the VCA610 only requires one tenth of this range for offset correction, assuring that the potentiometer wiper will always be near the potentiometer center. With this setting, the resistance seen at the wiper remains high and this stabilizes the filtering function.

GAIN CONTROL

The VCA610's gain is controlled by means of a unipolar negative voltage applied between ground and the gain control input, pin 3. If use of the output disable feature is required, a ground-referenced bipolar voltage is needed. Output disable occurs for $+0.1V \leq V_C \leq +2V$, and produces 80dB of attenuation. The control voltage should be limited to +2V in disable mode, and –2V in the gain mode in order to prevent saturation of internal circuitry.

Performance Curves. This wide bandwidth, although useful for many applications, can allow high frequency noise to modulate the gain control input. In practice, this can be easily avoided by filtering the control input as shown in Figure 3b. R_P should be no greater than 100Ω so as not to introduce gain errors by interacting with the gain control's input bias current of 2µA.

INPUT PROTECTION

Electrostatic damage (ESD) has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The VCA610 incorporates on-chip ESD protection diodes as shown in Figure 4. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

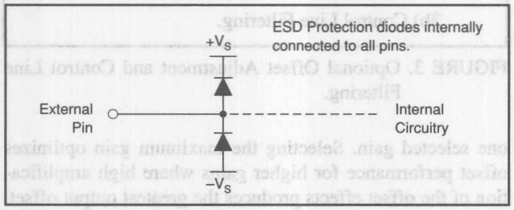


FIGURE 4. Internal ESD Protection.

All pins on the VCA610 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the pin voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and provides adequate ESD protection for most normal handling procedures. However, static protection is strongly recommended since static damage can cause subtle changes in amplifier operational characteristics without necessarily destroying the device.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM-VCA610AP-C for 8-pin DIP.

APPLICATIONS

The electronically variable gain of the VCA610 suits pulse-echo imaging systems well. Such applications include medical imaging, non-destructive structural inspection and sonar. nential amplifiers. The discussions below present examples of these applications.

ULTRASOUND TGC AMPLIFIER

The Figure 5 block diagram illustrates the fundamental configuration common to pulse-echo imaging systems. A piezoelectric crystal serves as both the ultrasonic pulse generator and the echo monitor transducer. A transmit/receive (T/R) switch isolates the monitor amplifier from the crystal during the pulse generation cycle and, then, connects the amplifier to the crystal during the echo monitor cycle.

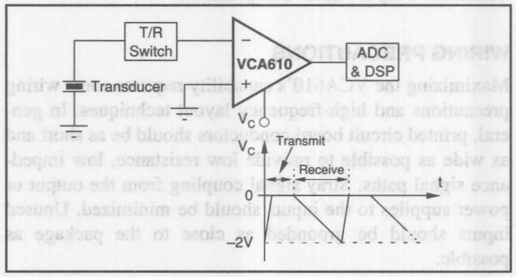


FIGURE 5. Typical Ultrasound Application.

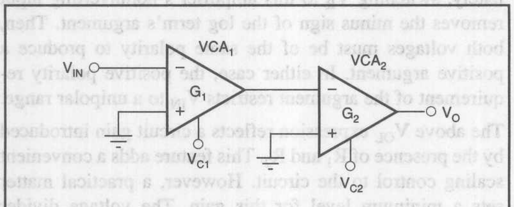
During the monitor (receive) cycle, the control voltage V_C, varies the amplifier gain. The gain is varied for three basic signal processing requirements of a transducer array based beamformer: compensation for depth attenuation effects, sometimes called Time Gain Compensation (TGC); receive apodization or windowing for reducing side lobe energy; and dynamic aperture sizing for better near field resolution.

Time gain compensation increases the amplifier's gain as the ultrasound signal moves through the material to compensate for signal attenuation versus material depth. For this purpose, a ramp signal applied to the VCA610 gain control input linearly increases the dB gain of the VCA610 with time. The gain control provides signal apodization or windowing with transducer arrays connected to amplifier arrays. Selective weighting of amplifier gains across the transducer aperture suppresses side lobe effects in the beamformer output to reduce image artifacts. Gain controlled attenuation or disabling the amplifier can be used to dynamically size the array aperture for better near field resolution. The controlled attenuation of the VCA610 minimizes switching artifacts and eliminates the bright radial rings that can result. The VCA610's 80dB gain range accommodates these functions.

WIDE-RANGE LOW-NOISE VCA

Figure 6 combines two VCA610s in series, extending the overall gain range and improving noise performance. This combination produces a gain equal to the sum of the two amplifier's logarithmic gains for a composite range of

–80dB to +80dB. Simply connecting V_{C1} and V_{C2} to the same 0 to –2V gain control voltage can produce this range, however, separate control voltages for the two amplifiers offer a noise performance improvement. In that configuration, each amplifier separately controls one half the gain range in a manner that always holds G_1 at the maximum level possible.



	GAIN	
	–80dB to 0dB	0dB to 80dB
V_{C1}	0 to –2V	–2V
G_1	–40dB to +40dB	+40dB
V_{C2}	0V	0 to –2V
G_2	–40dB	–40dB to +40dB

FIGURE 6. Two Series Connected VCA610s Expand the Gain Range and Improve Noise Performance.

At higher gains, variation of V_{C2} alone makes VCA_2 provide all of the gain control, leaving the gain of VCA_1 fixed at its maximum of 40dB. This gain maximum corresponds to the maximum bias currents in VCA_1, minimizing this amplifier's noise. Thus, for composite circuit gains of 0dB to +80dB, V_{CA1} serves as a low-noise, fixed-gain preamp.

For lower composite gains, VCA_1 provides the gain control and VCA_2 acts as a fixed attenuator. There, variation of V_{C1} varies G_1 from –40dB to +40dB while V_{C2} remains fixed at 0V for G_2 = –40dB. This mode produces the –80dB to 0dB segment of the composite gain range.

WIDE-RANGE AGC AMPLIFIER

The voltage-controlled gain feature of the VCA610 makes this amplifier ideal for precision AGC applications with control ranges as large as 60dB. The AGC circuit of Figure 7 adds an op amp and diode for amplitude detection, a holding capacitor to store the control voltage and resistors R_1 through R_3 that determine attack and release times. Resistor R_4 and capacitor C_C phase compensate the AGC feedback loop. The op amp compares the positive peaks of output V_O with a DC reference voltage V_R. Whenever a V_O peak exceeds V_R, the OPA620 output swings positive, forward biasing the diode and charging the holding capacitor. This drives the capacitor voltage in a positive direction, reducing the amplifier gain. R_3 and the C_H largely determine the attack time of this AGC correction.

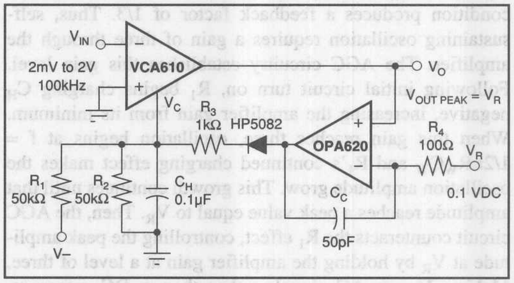


FIGURE 7. This AGC Circuit Maintains a Constant Output Amplitude for a 1000:1 Input Range.

Between gain corrections, resistor R_1 charges the capacitor in a negative direction, increasing the amplifier gain. R_1, R_2 and C_H determine the release time of this action. Resistor R_2 forms a voltage divider with R_1, limiting the maximum negative voltage developed on C_H. This limit prevents input overload of the VCA610's gain control circuit.

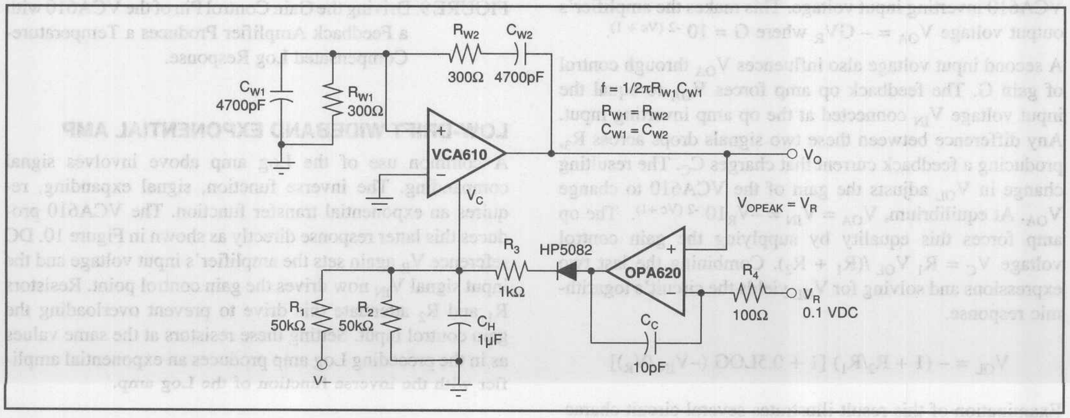


FIGURE 8. Adding Wein-bridge Feedback to the AGC Circuit of Figure 7 Produces an Amplitude Stabilized Oscillator.

STABILIZED WEIN-BRIDGE OSCILLATOR

Adding Wein-bridge feedback to the above AGC amplifier produces an amplitude-stabilized oscillator. Shown in Figure 8, this alternative requires the addition of just two resistors (R_{W1}, R_{W2}) and two capacitors (C_{W1}, C_{W2}).

Connecting the feedback network to the amplifier's noninverting input introduces positive feedback to induce oscillation. The feedback factor displays a frequency dependence due to the changing impedances of the C_W capacitors. As frequency increases, the decreasing impedance of the C_{W2} increases the feedback factor. Simultaneously, the decreasing impedance of the C_{W1} decreases this factor. Analysis shows that the maximum factor occurs at $f = 1/2\pi R_W C_W$, making this the frequency most conducive to oscillation. At this frequency the impedance magnitude of C_W equals R_W and inspection of the circuit shows that this condition produces a feedback factor of 1/3. Thus, self-sustaining oscillation requires a gain of three through the amplifier. The AGC circuitry establishes this gain level. Following initial circuit turn on, R_1 begins charging C_H negative, increasing the amplifier gain from its minimum. When this gain reaches three, oscillation begins at $f = 1/2\pi R_W C_W$ and R_1's continued charging effect makes the oscillation amplitude grow. This growth continues until that amplitude reaches a peak value equal to V_R. Then, the AGC circuit counteracts the R_1 effect, controlling the peak amplitude at V_R by holding the amplifier gain at a level of three. Making V_R an AC signal, rather than a DC reference, produces amplitude modulation of the oscillator output.

LOW-DRIFT WIDEBAND LOG AMP

The VCA610 can be used to provide a 250kHz (–3dB) log amp with low offset voltage and low gain drift.

The exponential gain control characteristic of the VCA610 permits simple generation of a temperature-compensated logarithmic response. Enclosing the exponential function in an op amp feedback path inverts this function, producing the log response. Figure 9 shows the practical implementation of this technique. A DC reference voltage, V_R, sets the VCA610 inverting input voltage. This makes the amplifier's output voltage $V_{OA} = -GV_R$ where $G = 10^{-2(V_C + 1)}$.

A second input voltage also influences V_{OA} through control of gain G. The feedback op amp forces V_{OA} to equal the input voltage V_{IN} connected at the op amp inverting input. Any difference between these two signals drops across R_3, producing a feedback current that charges C_C. The resulting change in V_{OL} adjusts the gain of the VCA610 to change V_{OA}. At equilibrium, $V_{OA} = V_{IN} = -V_R 10^{-2(V_C+1)}$. The op amp forces this equality by supplying the gain control voltage $V_C = R_1 V_{OL}/(R_1 + R_2)$. Combining the last two expressions and solving for V_{OL} yields the circuit's logarithmic response.

$$V_{OL} = -(1 + R_2/R_1)\,[1 + 0.5\text{LOG}(-V_{IN}/V_R)]$$

Examination of this result illustrates several circuit characteristics. First, the argument of the Log term, $-V_{IN}/V_R$, reveals an option and a constraint. In Figure 9, V_R represents a DC reference voltage. Optionally, making this voltage a second signal produces log-ratio operation. Either way, the Log term's argument constrains the polarities of V_R and V_{IN}. These two voltages must be of opposite polarities to ensure a positive argument. This polarity combination results when V_R connects to the inverting input of the VCA610. Alternately, switching V_R to this amplifier's noninverting input removes the minus sign of the log term's argument. Then, both voltages must be of the same polarity to produce a positive argument. In either case, the positive polarity requirement of the argument restricts V_{IN} to a unipolar range.

The above V_{OL} expression reflects a circuit gain introduced by the presence of R_1 and R_2. This feature adds a convenient scaling control to the circuit. However, a practical matter sets a minimum level for this gain. The voltage divider formed by R_1 and R_2 attenuates the voltage supplied to the V_C terminal by the op amp. This attenuation must be great enough to prevent any possibility of an overload voltage at the V_C terminal. Such an overload saturates the VCA610's gain control circuitry, reducing the amplifier's gain. For the feedback connection of Figure 9, this overload condition permits a circuit latch. To prevent this, choose R_1 and R_2 to ensure that the op amp can not possibly deliver more than 2.5V to the V_C terminal.

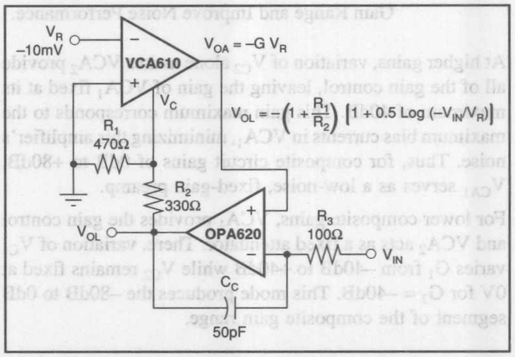


FIGURE 9. Driving the Gain Control Pin of the VCA610 with a Feedback Amplifier Produces a Temperature-Compensated Log Response.

LOW-DRIFT WIDEBAND EXPONENTIAL AMP

A common use of the Log amp above involves signal companding. The inverse function, signal expanding, requires an exponential transfer function. The VCA610 produces this latter response directly as shown in Figure 10. DC reference V_R again sets the amplifier's input voltage and the input signal V_{IN} now drives the gain control point. Resistors R_1 and R_2 attenuate this drive to prevent overloading the gain control input. Setting these resistors at the same values as in the preceding Log amp produces an exponential amplifier with the inverse function of the Log amp.

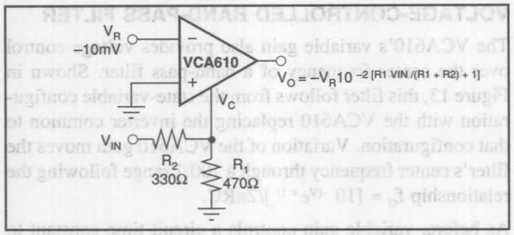


FIGURE 10. Signal Drive of the VCA610 Gain Control Pin Produces and Exponential Response, Re-expanding Signal Companded by Figure 9.

VOLTAGE-CONTROLLED LOW-PASS FILTER

In the circuit of Figure 11, the VCA610 serves as the variable gain element of a voltage-controlled low-pass filter. As will be described, this implementation expands the circuit's voltage swing capability over that normally achieved with the equivalent multiplier implementation. The circuit's response pole responds to control voltage V_C according to the relationship $f_P = G/2\pi R_2C$ where $G = 10^{-2\,(V_C + 1)}$. With the components shown, the circuit provides a linear variation of the low-pass cutoff from 300Hz to 1MHz.

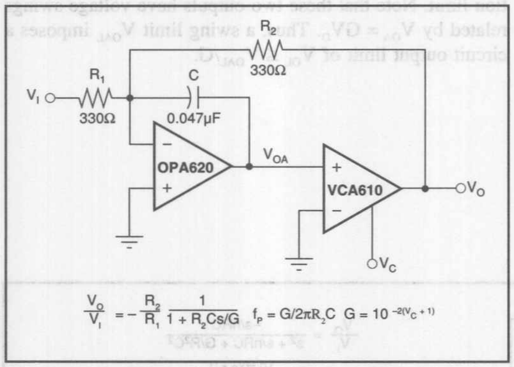


FIGURE 11. This Voltage-Tuneable Low-Pass Filter Produces a Variable Cutoff Frequency with a 3,000:1 Range.

The response control results from amplification of the feedback voltage applied to R_2. Consider first the case where the VCA610 produces G = 1. Then, the circuit performs as if this amplifier were replaced by a short circuit. Visually doing so leaves a simple voltage amplifier with a feedback resistor bypassed by a capacitor. This basic circuit produces a response pole at $f_P = 1/2\pi R_2C$.

For G > 1, the circuit applies a greater voltage to R_2, increasing the feedback current this resistor supplies to the summing junction of the OPA620. The increased feedback current produces the same result as if R_2 had been decreased in value in the basic circuit described above. Decreasing the effective R_2 resistance moves the circuit's pole to a higher frequency, producing the $f_P = G/2\pi R_2C$ response control.

Finite loop gain and a signal swing limitation set performance boundaries for the circuit. Both limitations occur when the VCA610 attenuates rather than amplifies the feedback signal. These two limitations reduce the circuit's utility at the lower extreme of the VCA610's gain range. For $-1 \le V_C \le 0$, this amplifier produces attenuating gains in the range from 0dB to –40dB. This directly reduces the net gain in the circuit's feedback loop, increasing gain error effects. Also, this attenuation transfers an output swing limitation from the OPA620 output to the overall circuit's output. Note that OPA620 output voltage, V_{OA}, relates to V_O through the expression $V_O = GV_{OA}$. Thus, a G < 1 limits the maximum V_O swing to a value less than the maximum V_{OA} swing.

However, the circuit shown provides greater output swing than the more common multiplier implementation. The latter replaces the VCA610 of the figure with an analog multiplier having a response of $V_O = XY/10$. Then, $X = V_{OA}$ and $Y = V_C$, making the circuit output voltage $V_O = V_{OA}V_C/10$. Thus, the multiplier implementation amplifies V_{OA} by a gain of $V_C/10$. Circuit constraints require that $V_C \le 10$, making this gain ≤ 1. Thus, the multiplier performs only as a variable attenuator and never provides amplification. As a result, the voltage swing limitation of V_{OA} restricts the V_O swing throughout most of the circuit's control range. Replacing the multiplier with the VCA610 shown permits equivalent gains greater > 1. Then, operating the VCA610 with gains in the range of one to 100 avoids the reduction in output swing capability.

VOLTAGE-CONTROLLED HIGH-PASS FILTER

A circuit analogous to the above low-pass filter produces a voltage-controlled high-pass response. The gain control provided by the VCA610 of Figure 12 varies this circuit's response zero from 1Hz to 10kHz according to the relationship $F_Z \approx 1/2\pi GR_1C$ where $G = 10^{-2\,(V_C + 1)}$.

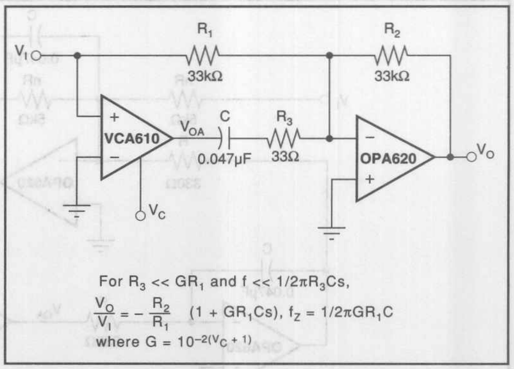


FIGURE 12. A Voltage-Tunable High-Pass Filter Produces a Response Zero Variable from 1Hz to 10kHz.

and R_3 with short circuits. First consider the case where the VCA610 produces G = 1. Then, replacing this amplifier with short circuit leaves the operation unchanged. In this shorted state, the circuit is simply a voltage amplifier with an R–C bypass around R_1. The resistance of this bypass, R_3, serves only to phase compensate the circuit and practical factors make $R_3 << R_1$. Neglecting R_3 for the moment, the circuit becomes just a voltage amplifier with capacitive bypass of R_1. This circuit produces a response zero at $f_Z = 1/2\pi R_1C$.

Adding the VCA610 as shown permits amplification of the signal applied to capacitor C and produces voltage control of the frequency f_Z. Amplified signal voltage on C increases the signal current conducted by the capacitor to the op amp feedback network. The result is the same as if C had been increased in value to GC. Replacing C with this effective capacitance value produces the circuit's control expression $f_Z = 1/2\pi R_1GC$.

Two factors limit the high-frequency performance of the resulting high-pass filter. The finite bandwidth of the op amp and the circuit's phase compensation produce response poles. These limit the frequency duration of the high-pass response. Selecting the R_3 phase compensation with the equation $R_3 = \sqrt{(R1/2\pi f_C C)}$ assures stability for all values of G and sets the circuit's bandwidth at $BW = \sqrt{(f_C/2\pi R_1C)}$. Here, f_C is the unity-gain crossover frequency of the op amp used. With the components shown, BW = 100kHz. This bandwidth provides a high-pass response duration of five decades of frequency for f_Z = 1Hz, dropping to one decade for f_Z = 10kHz.

The output voltage limit of the VCA610 imposes an input voltage limit for the filter. The expression $V_{OA} = GV_I$ relates these two voltages. Thus, an output voltage limit V_{OAL} constrains the input voltage to $V_I \leq V_{OAL}/G$.

over the center frequency of a band-pass filter. Shown in Figure 13, this filter follows from the state-variable configuration with the VCA610 replacing the inverter common to that configuration. Variation of the VCA610 gain moves the filter's center frequency through a 100:1 range following the relationship $f_O = [10^{-(V_C+1)}]/2\pi RC$.

As before, variable gain controls a circuit time constant to vary the filter response. The gain of the VCA610 amplifies or attenuates the signal driving the lower integrator of the circuit. This alters the effective resistance of the integrator time constant producing the response

$$\frac{V_O}{V_I} = \frac{-s/nRC}{s^2 + s/nRC + G/R^2C^2}$$

Evaluation of this response equation reveals a passband gain of $A_O = -1$, a bandwidth of $BW = 1/2\pi nRC$ and a selectivity of $Q = n10^{-(V_C+1)}$. Note that variation of control voltage V_C alters Q but not bandwidth.

The gain provided by the VCA610 restricts the output swing of the filter. Output signal V_O must be constrained to a level that does not drive the VCA610 output, V_{OA}, into its saturation limit. Note that these two outputs have voltage swings related by $V_{OA} = GV_O$. Thus, a swing limit V_{OAL} imposes a circuit output limit of $V_{OL} \leq V_{OAL}/G$.

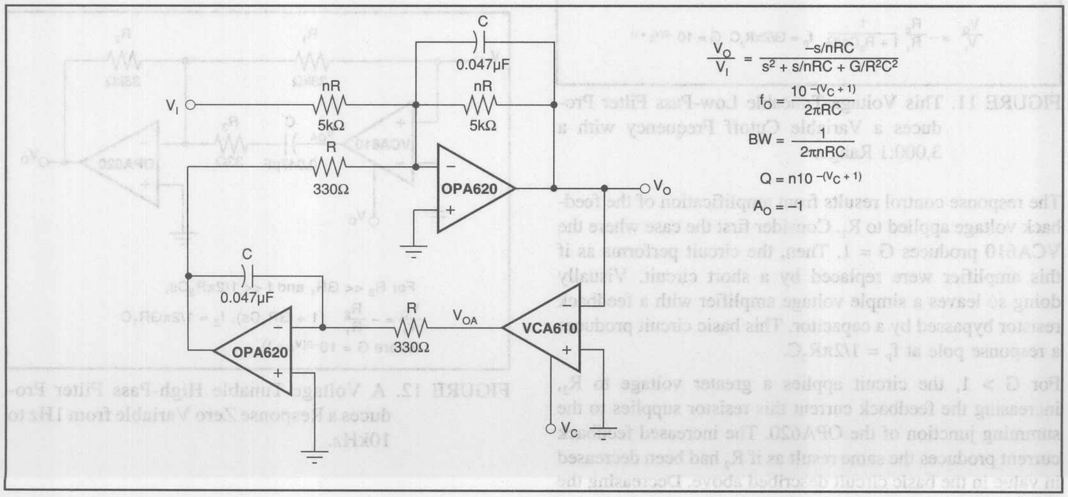


FIGURE 13. Adding the VCA610 to a State-Variable Filter Produces a Voltage-Controlled BandPass Filter With a Center Frequency Variable Over a 100:1 Range.

3 Power Operational Amplifiers

Burr-Brown power amplifiers are designed for high output voltage and/or high output current. Versatile power operational amplifiers can be used in virtually any op amp circuit configuration, yet can supply up to ±15A load current or ±140V output voltage.

Buffer amplifiers can be used with common op amps to drive long lines or heavy loads such as valves, voice-coils and actuators.

Choose from a wide variety of power amp types, including:

BUF634—250mA, 2000V/µs buffer amp. Used with a common op amp, this buffer amp boosts output current to 250mA and increases capacitive load drive capability. Versatile and rugged, it's available in SO-8, 8-pin DIP and 5-pin TO-220 packages.

OPA541—This monolithic power op amp delivers output current up to ±5A and operates from power supplies up to ±40V. Available in low cost plastic power SIP and hermetic 8-pin TO-3 packages.

OPA502—±10A output from ±40V supplies highlight this rugged performer. Ideal for programmable power sources, motor drivers, or even high performance audio amplifiers.

OPA544F—A new high-voltage/high-current op amp available in a surface-mount power package that solders flat on a circuit board for low profile, high density applications. Specifications include 2A output current, ±10V to ±35V power supply range, and 100pA max input bias current. It is also available in a 5-lead TO-220 plastic package.

OPA2544—This new dual version of the OPA544 packs two powerful amps in a single 11-lead plastic package that saves board space and reduces cost. It provides output of 2A, its power supply range extends to ±35V, and is designed to drive a wide variety of electro-mechanical devices.

3583—Power supply voltages up to ±150V and output current to 75mA suit many programmable V/I source or high voltage transducer applications.

3584—Power supplies to ±150V and slew rates to 150V/µs are ideal for piezoelectric transducers and electrostatic deflection circuitry.

Other products provide special features and performance. Use our detailed selection guide to locate the power amp for your application.

Power Operational Amplifiers

POWER OPERATIONAL AMPLIFIERS

High Current (Output Current, max)		High Voltage (Output Swing, max)		High Speed Buffers (GBW, typ)	
OPA512	(±15A)	3582	(±145V)	BUF601	(900MHz)
OPA501	(±10A)	3584	(±145V)	OPA660	(850MHz)
OPA502	(±10A)	3583	(±140V)	BUF600	(650MHz)
OPA511	(±5A)	3581	(±70V)	OPA633	(260MHz)
OPA541	(±5A)	OPA445	(±35V)	BUF634	(180MHz)
OPA2541	(±5A, Dual)	3580	(±30V)		
OPA544	(±2A)				
OPA2544	**(±2A, Dual)**				
3573	(±2A)				
OPA654	(±200mA)				
OPA633	(±80mA)				

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

POWER - HIGH CURRENT

Product	Rated Output Current min (±mA)	Rated Supply max (±V)	Offset Voltage 25°C max (±mV)	Offset Voltage Drift max (±μV/°C)	Bias Current 25°C max (pA)	Small Signal Unity Gain Bandwidth typ (MHz)	Slew Rate min (V/μs)	Open Loop Gain (dB)	Temp Range(1)	Pkg	Description
OPA501	10A	34	5	40	20nA	1	1.35	98	Ind	TO-3	High Current
OPA502	10A	45	5	5*	200	2	10	103	XInd/Mil	TO-3	High Current
OPA511	5A	22	10	65	40nA	1	1	91	Ind	TO-3	High Current, Still Available
OPA512BM	10A	45	6	65	30nA	4	2.5	110	Ind	TO-3	High Current
OPA512SM	15A	45	3	40	20nA	4	2.5	110	Mil	TO-3	
OPA541BM	5A	40	1	30	50	1.6	6	90	Ind/Mil	TO-3	Current
OPA541AM	5A	35	10	40	50	1.6	6	90	Ind	Power Plastic	
OPA544	2A	35	5	10*	100	1.4	8	90	XInd	5-Pin TO-220	
OPA547	***500****	***35***	***5***	***10****	***1000nA***	***1***	***10****	***90***	***XInd***	***TO-220, DDPAK***	***High Voltage and High Current***
OPA548	***3A****	***35***	***5***	***10****	***1000nA***	***1***	***10****	***90***	***XInd***	***TO-220, DDPAK***	***High Voltage and High Current***
OPA654	200*	18	3	40*	50	32	750	94	Ind	TO-3	Wideband
OPA2541	5A	40	1	30	50	1.6	6	90	Ind/Mil	TO-3	Dual
OPA2544	**2A**	**35**	**5**	**10***	**50**	**1.4**	**5**	**90**	**XInd/Mil**	**TO-3, 11-Pin Plastic**	**Dual**
3573	2A(3)	20	10	65	40nA	1	2.6	94	Ind	TO-3	Still Available

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, XInd = –40°C to +85°C, Mil = –55°C to +125°C. (2) Gain-bandwidth product. (3) 5A peak.

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

POWER - HIGH VOLTA

Product	Rated Output Current min (±mA)	Rated Supply max (±V)	Offset Voltage 25°C max (±mV)	Offset Voltage Drift max (±µV/°C)	Bias Current 25°C max (pA)	Unity Gain Bandwidth typ (MHz)	Slew Rate min (V/µs)	Open Loop Gain (dB)	Temp Range(1)	Pkg	Description
OPA445	15	35	3	10*	50	2	5	100	Ind/Mil	TO-99, DIP	
OPA547	***3A****	***35***	***5***	***10****	***1000nA***	***1***	***10****	***90***	***XInd***	***TO-220, DDPAK***	***High Current and High Volt***
OPA548	***500****	***35***	***5***	***10****	***1000nA***	***1***	***10****	***90***	***XInd***	***TO-220, DDPAK***	***High Current and High Volt***
3580	60	30	10	30	50	5	15	106	Com	TO-3	Still Available
3581	30	70	3	25	20	5	20	112	Com	TO-3	Still Available
3582	15	145	3	25	20	5	20	118	Com	TO-3	Still Available
3583	75	140	3	23	20	5	30*	118	Com/Ind	TO-3	
3584	15	145	3	25	20	20(2)	150*	120	Com	TO-3	

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, XInd = –40°C to +85°C, Mil = –55°C to +125°C. (2) Gain-bandwidth product.

POWER - HIGH SPEED BUFFI

Product	Rated Current Output min (±mA)	Rated Voltage Output min (±V)	Small Signal Bandwidth (MHz)	Full Power Bandwidth (MHz)	Slew Rate typ (V/µs)	Input Impedance typ (Ω ‖ pF)	Temp Range(1)	Pkg	Description
BUF600	20	2.5	650	320	3400	4.8M/1	XInd	DIP, SOIC	High Slew Rate, Open Loop
BUF601	20	2.5	900	320	3600	2.5M/1	XInd	DIP, SOIC	High Slew Rate, Open Loop
BUF634	250*	10	180	NS	2000	8M/8	Ind	DIP, SOIC, TO-220	Low Cost, Open Loop
OPA633	80	11	260	40	2500	1.5M/1.6	Ind	DIP	Low Cost, Open Loop
OPA660	10	3.7	850	570	3000	1M/2.1	XInd	DIP, SOIC	Transconductance Amp and Bu

NOTES: (1) Ind = –25°C to +85°C, XInd = –40°C to +85°C.

* DENOTES TYPICAL

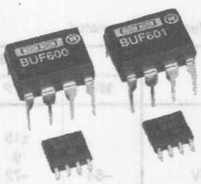
BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPM

Some specifications have been estimated for compari
purposes. Refer to data sheets for guaranteed specifi

BURR - BROWN®

BUF600
BUF601



HIGH-SPEED BUFFER AMPLIFIER

FEATURES

- OPEN-LOOP BUFFER
- HIGH-SLEW RATE: 3600V/μs, 5.0Vp-p
- BANDWIDTH: 320MHz, 5.0Vp-p
  900MHz, 0.2Vp-p
- LOW INPUT BIAS CURRENT: 0.7μA/1.5μA
- LOW QUIESCENT CURRENT: 3mA/6mA
- GAIN FLATNESS: 0.1dB, 0 to 300MHz

APPLICATIONS

- VIDEO BUFFER/LINE DRIVER
- INPUT/OUTPUT AMPLIFIER FOR MEASUREMENT EQUIPMENT
- PORTABLE SYSTEMS
- TRANSMISSION SYSTEMS
- TELECOMMUNICATIONS
- HIGH-SPEED ANALOG SIGNAL PROCESSING
- ULTRASOUND

DESCRIPTION

The BUF600 and BUF601 are monolithic open-loop unity-gain buffer amplifiers with a high symmetrical slew rate of up to 3600V/μs and a very wide bandwidth of 320MHz at 5Vp-p output swing. They use a complementary bipolar IC process, which incorporates pn-junction isolated high-frequency NPN and PNP transistors to achieve high-frequency performance previously unattainable with conventional integrated circuit technology.

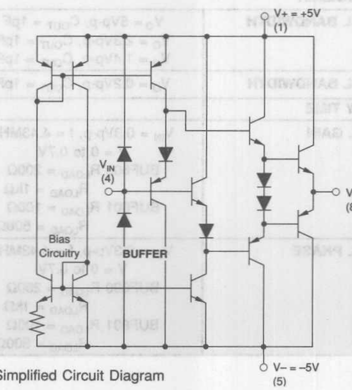
Their unique design offers a high-performance alternative to expensive discrete or hybrid solutions.

The BUF600 and BUF601 feature low quiescent current, low input bias current, small signal delay time and phase shift, and low differential gain and phase errors.

The BUF600 with 3mA quiescent current is well-suited for operation between high-frequency processing stages. It demonstrates outstanding performance even in feedback loops of wide-band amplifiers or phase-locked loop systems.

The BUF601 with 6mA quiescent current and therefore lower output impedance can easily drive 50Ω inputs or 75Ω systems and cables.

The broad range of analog and digital applications extends from decoupling of signal processing stages, impedance transformation, and input amplifiers for RF equipment and ATE systems to video systems, distribution fields, IF/communications systems, and output drivers for graphic cards.



Simplified Circuit Diagram

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

DC SPECIFICATION

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_{AMB} = +25°C, unless otherwise noted.

		BUF600AP, AU			BUF601AP, AU			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT OFFSET VOLTAGE								
Initial			±15	±30		±15	±30	mV
vs Temperature			9			25		μV/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V	–54	–72		–54	–77		dB
vs Supply (non-tracking)	V_{CC} = +4.5V to +5.5V		–55			–55		dB
vs Supply (non-tracking)	V_{CC} = –4.5V to –5.5V		–54			–54		dB
INPUT BIAS CURRENT								
Initial			+3.5	–2.5/+5		+3.5	–5/+10	μA
vs Temperature			0.4			0.7		nA/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V		0.15			0.3		μA/V
vs Supply (non-tracking)	V_{CC} = +4.5V to +5.5V		0.5			0.5		μA/V
vs Supply (non-tracking)	V_{CC} = –4.5V to –5.5V		20			20		nA/V
INPUT IMPEDANCE			4.8 ‖ 1			2.5 ‖ 1		MΩ ‖ pF
INPUT NOISE								
Voltage Noise Density	f = 100kHz to 100MHz		5.2			4.8		nV/√Hz
Signal-to-Noise Ratio	S/N = 20 Log (0.7/(Vn • √5MHz))		95			96		dB
TRANSFER CHARACTERISTICS	Voltage Gain; V_{IN} = ±2.5V							
	R_{LOAD} = 100Ω					0.95		V/V
	R_{LOAD} = 200Ω		0.96					V/V
	R_{LOAD} = 10kΩ		0.99			0.99		V/V
RATED OUTPUT								
Voltage Output	V_{IN} = ±2.7V							
	R_{LOAD} = 100Ω				±2.5	±2.6		V
	R_{LOAD} = 200Ω	±2.5	±2.6					V
DC Current Output	DC, R_{LOAD} = 100Ω	±20			±20			mA
Output Impedance			6.2			3.6		Ω
POWER SUPPLY								
Rated Voltage			±5			±5		V
Derated Performance		±4.5		±5.5	±4.5		±5.5	V
Quiescent Current		±2.6	±3	±3.4	±5.4	±6	±6.6	mA
TEMPERATURE RANGE								
Specification		–40		85	–40		85	°C
Storage		–40		125	–40		125	°C

AC SPECIFICATION

At V_{CC} = ±5V, R_{LOAD} = 200Ω (BUF600) and 100Ω (BUF601), R_{SOURCE} = 50Ω, and T_{AMB} = +25°C, unless otherwise noted.

		BUF600AP, AU			BUF601AP, AU			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
FREQUENCY DOMAIN								
LARGE SIGNAL BANDWIDTH (–3dB)	V_O = 5Vp-p, C_{OUT} = 1pF		320			320		MHz
	V_O = 2.8Vp-p, C_{OUT} = 1pF		400			400		MHz
	V_O = 1.4Vp-p, C_{OUT} = 1pF		700			700		MHz
SMALL SIGNAL BANDWIDTH	V_O = 0.2Vp-p, C_{OUT} = 1pF		650			900		MHz
GROUP DELAY TIME			250			200		ps
DIFFERENTIAL GAIN	V_{IN} = 0.3Vp-p, f = 4.43MHz							
	V = 0 to 0.7V							
	BUF600 R_{LOAD} = 200Ω		0.5					%
	R_{LOAD} = 1kΩ		0.075					%
	BUF601 R_{LOAD} = 100Ω					0.4		%
	R_{LOAD} = 500Ω					0.05		%
DIFFERENTIAL PHASE	V_{IN} = 0.3Vp-p, f = 4.43MHz							
	V = 0 to 0.7V							
	BUF600 R_{LOAD} = 200Ω		0.02					Degrees
	R_{LOAD} = 1kΩ		0.04					Degrees
	BUF601 R_{LOAD} = 100Ω					0.025		Degrees
	R_{LOAD} = 500Ω					0.03		Degrees

AC-SPECIFICATIONS (CONT)

At V_{CC} = ±5V, R_{LOAD} = 200Ω (BUF600) and 100Ω (BUF601), R_{SOURCE} = 50Ω, and T_{AMB} = +25°C, unless otherwise noted.

		BUF600AP, AU			BUF601AP, AU			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
HARMONIC DISTORTION								
Second Harmonic	f = 10MHz, V_O = 1.4Vp-p		–65			–65		dBc
Third Harmonic			–64			–67		dBc
Second Harmonic	f = 30MHz, V_O = 1.4Vp-p		–51			–59		dBc
Third Harmonic			–56			–62		dBc
Second Harmonic	f = 50MHz, V_O = 1.4Vp-p		–43			–53		dBc
Third Harmonic			–48			–54		dBc
GAIN FLATNESS PEAKING								
	V_O = 0.4Vp-p, DC to 30MHz		0.01			0.005		dB
	V_O = 0.4Vp-p, 30MHz to 300MHz		0.3			0.1		dB
LINEAR PHASE DEVIATION								
	V_O = 0.4Vp-p, DC to 30MHz		5.5			3.8		Degrees
	V_O = 0.4Vp-p, 30 to 300MHz		55			45		Degrees
TIME DOMAIN								
RISE TIME	10% to 90%, 700ps							
	1.4Vp-p Step		0.82			0.87		ns
	2.8Vp-p Step		0.97			0.95		ns
	5.0Vp-p Step		1.18			1.13		ns
SLEW RATE								
	V_O = 1.4Vp-p		1500			1500		V/µs
	V_O = 2.8Vp-p		2400			2400		V/µs
	V_O = 5.0Vp-p		3400			3600		V/µs

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage(1)	$\pm V_{CC}$ ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

ORDERING INFORMATION

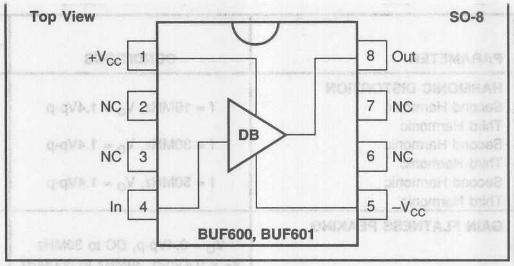
MODEL	PACKAGE	TEMPERATURE RANGE
BUF600AP	Plastic 8-Pin DIP	–40°C to +85°C
BUF600AU	SO-8 Surface-Mount	–40°C to +85°C
BUF601AP	Plastic 8-Pin DIP	–40°C to +85°C
BUF601AU	SO-8 Surface-Mount	–40°C to +85°C

PACKAGE INFORMATION

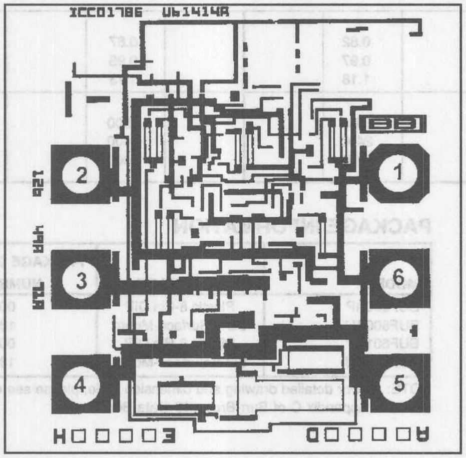
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
BUF600AP	Plastic 8-Pin DIP	006
BUF600AU	SO-8 Surface-Mount	182
BUF601AP	Plastic 8-Pin DIP	006
BUF601AU	SO-8 Surface-Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

FUNCTION	DESCRIPTION
In	Analog Input
Out	Analog Output
$+V_{CC}$	Positive Supply Voltage; typical +5VDC
$-V_{CC}$	Negative Supply Voltage; typical –5VDC



DICE INFORMATION



BUF600 AND BUF601 DIE TOPOGRAPHY

PAD	FUNCTION
1	Analog Input
2	–5V Supply
3	–5V, Output
4	Analog Output
5	+5V Supply, Output
6	+5V Supply

Substrate Bias: Negative Supply
NC: No Connection
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	39 x 42 ±5	0.99 x 1.07 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Minimum Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02 +0.05-0.0	0.0005 +0.0013-0.0
Gold	0.30 ±0.05	0.0076 ±0.0013

vices, but any semiconductor device deserves protection from this potentially damaging source. The BUF600 and BUF601 incorporate on-chip ESD protection diodes as shown in Figure 1. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

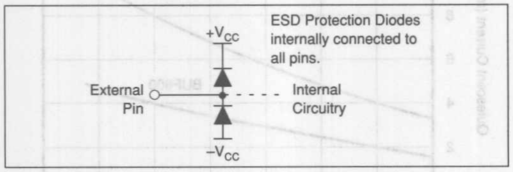


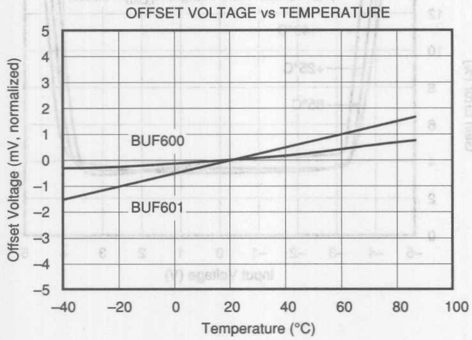
FIGURE 1. Internal ESD Protection.

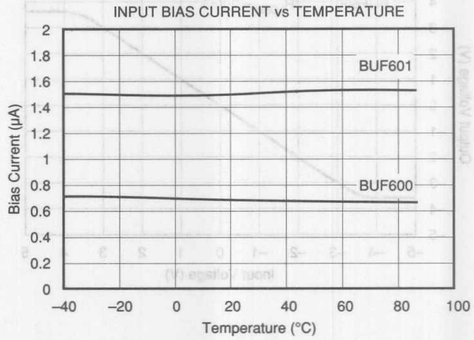
reverse-biased diodes to the power supplies as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, the diode current should be externally limited to 10mA or so whenever possible.

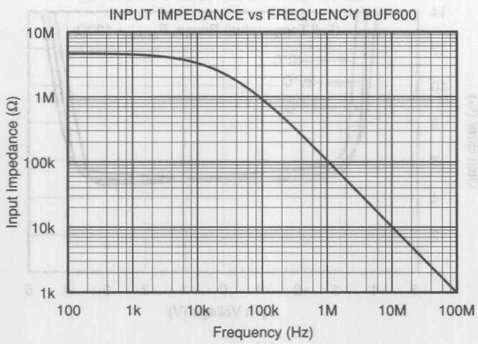
The internal protection diodes are designed to withstand 2.5kV (using the Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision amplifiers, this may cause a noticeable degradation of offset and drift. Therefore, static protection is strongly recommended when handling the BUF600 and BUF601.

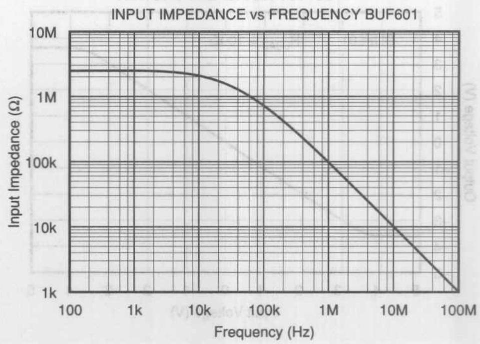
TYPICAL PERFORMANCE CURVES

At $V_{CC} = \pm5V$, $R_{LOAD} = 10k\Omega$, and $T_A = 25°C$ unless otherwise noted.



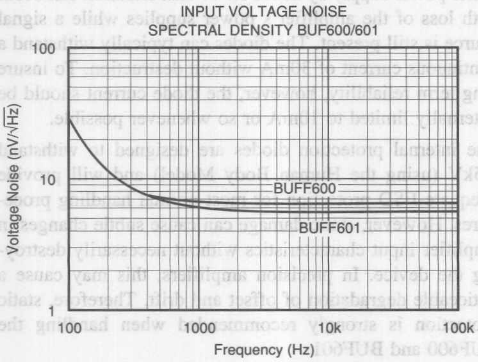


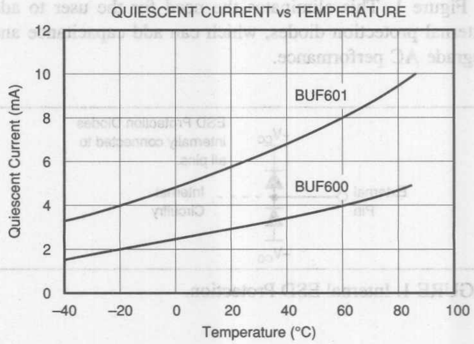


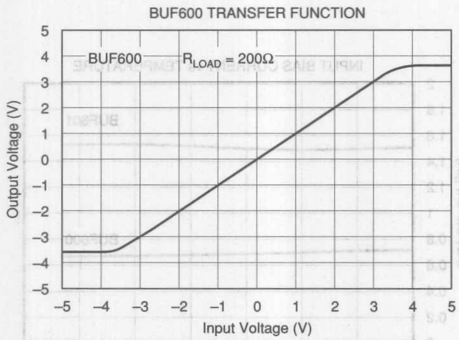


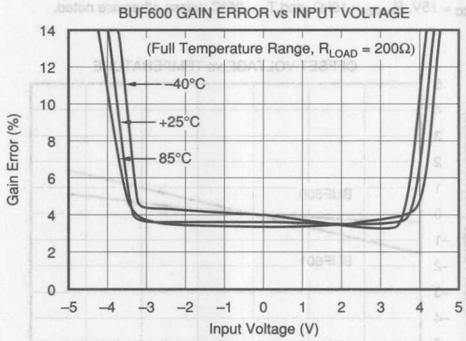
TYPICAL PERFORMANCE CURVES (CONT)

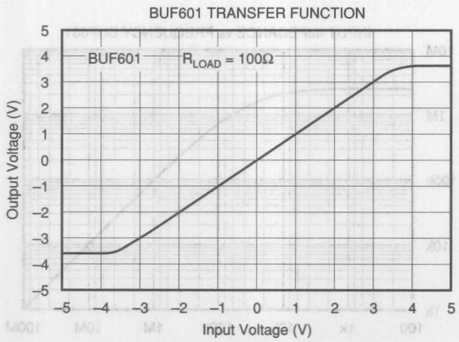
At $V_{CC} = \pm5V$, $R_{LOAD} = 10k\Omega$, and $T_A = 25°C$ unless otherwise noted.

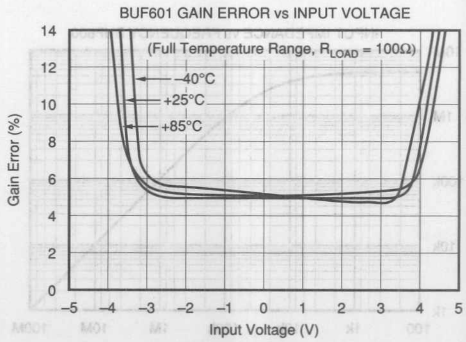






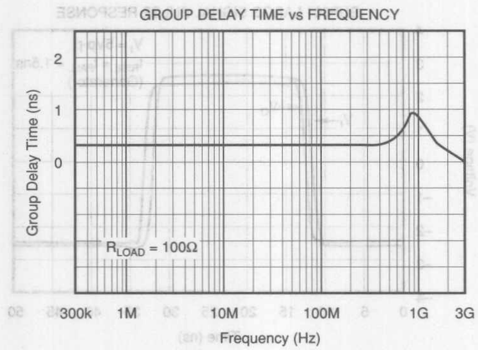


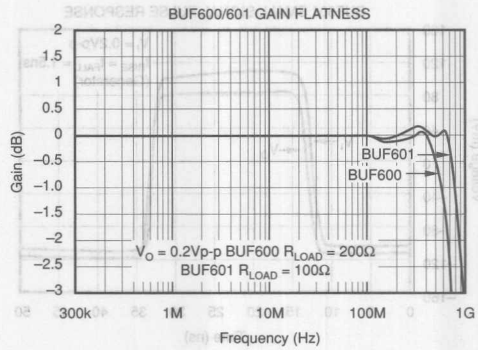


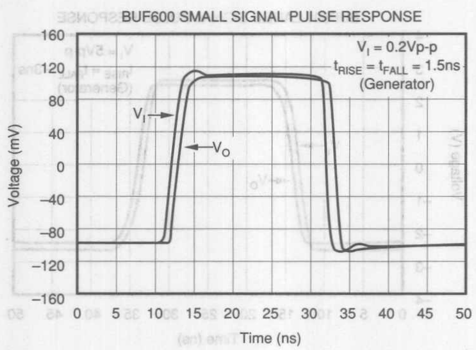


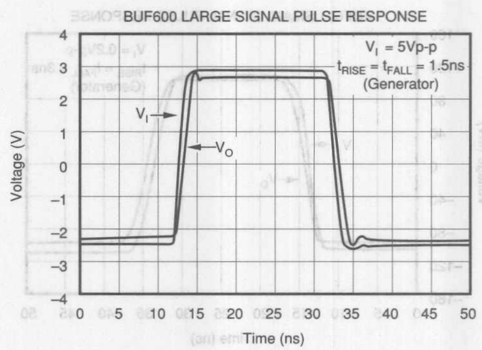
TYPICAL PERFORMANCE CURVES (CONT)

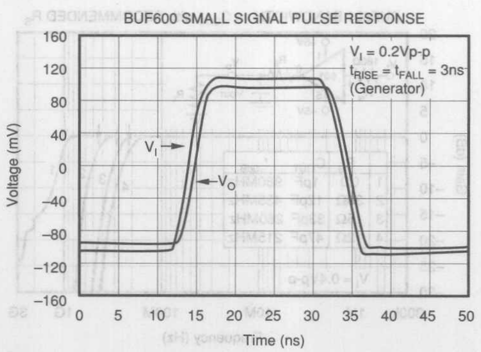
At $V_{CC} = \pm5V$, $R_{LOAD} = 100\Omega$ (BUF601), $R_{LOAD} = 200\Omega$ (BUF600), and $T_A = 25°C$ unless otherwise noted.

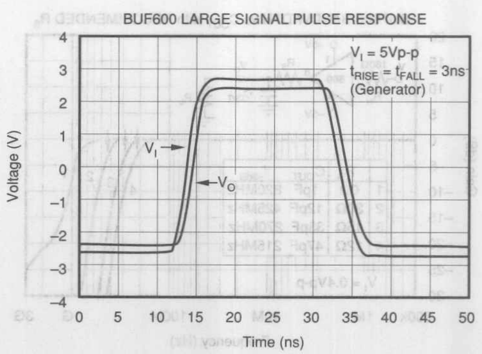






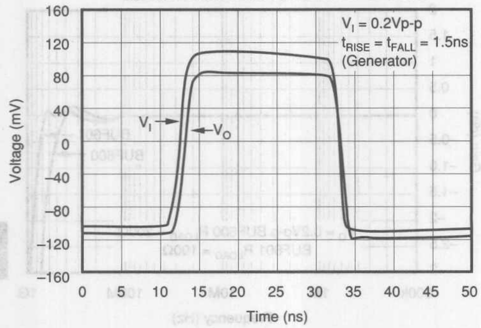




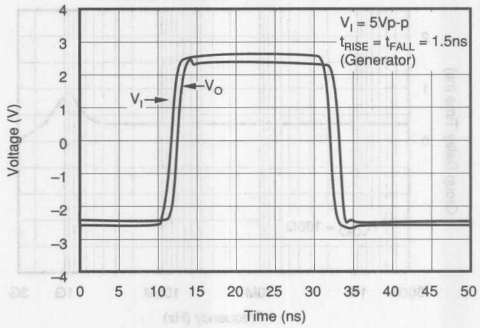


At $V_{CC} = \pm5V$, $R_{LOAD} = 100\Omega$ (BUF601), $R_{LOAD} = 200\Omega$ (BUF600), and $T_A = 25°C$ unless otherwise noted.

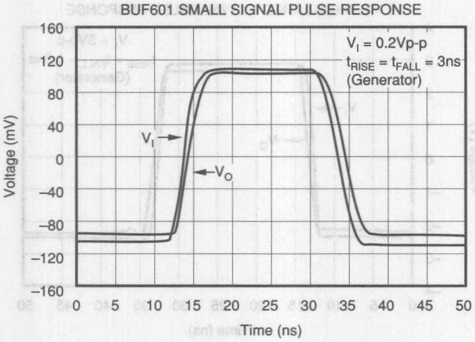
BUF601 SMALL SIGNAL PULSE RESPONSE



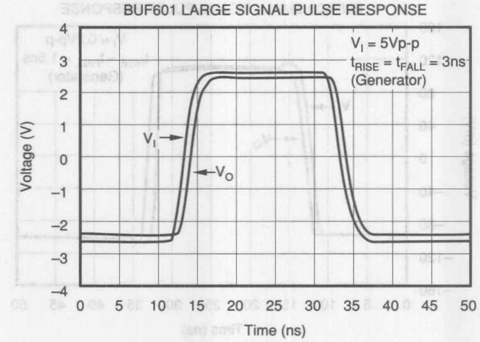
BUF601 LARGE SIGNAL PULSE RESPONSE



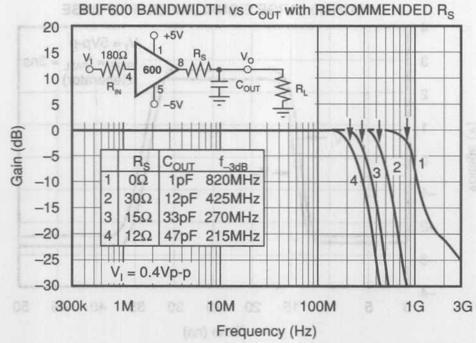
BUF601 SMALL SIGNAL PULSE RESPONSE



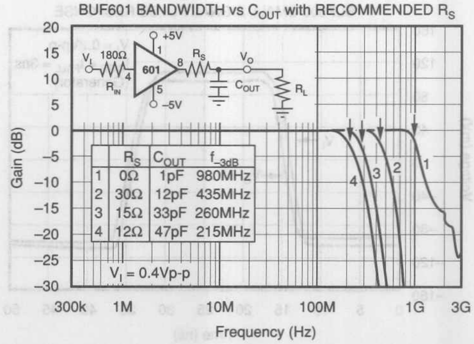
BUF601 LARGE SIGNAL PULSE RESPONSE

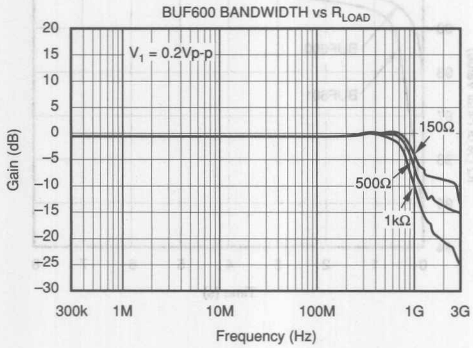


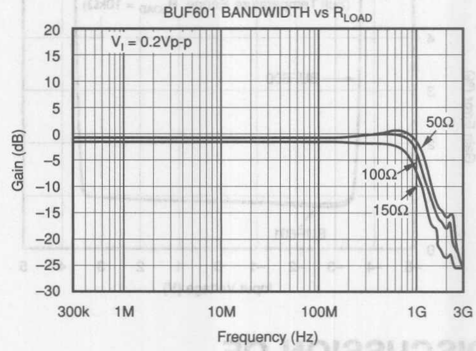
BUF600 BANDWIDTH vs C_{OUT} with RECOMMENDED R_S

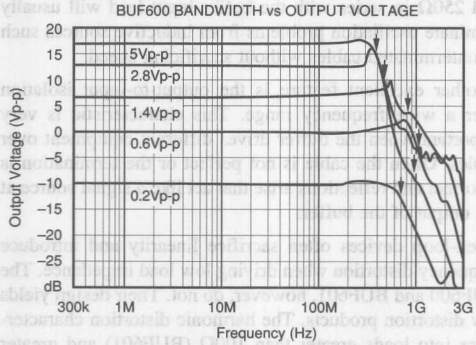


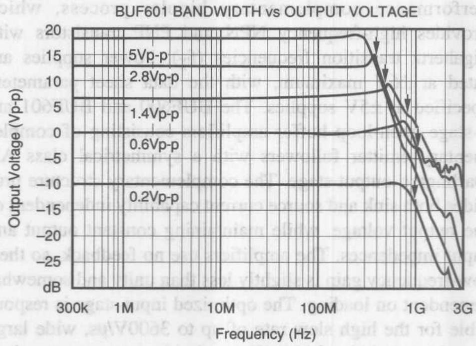
BUF601 BANDWIDTH vs C_{OUT} with RECOMMENDED R_S

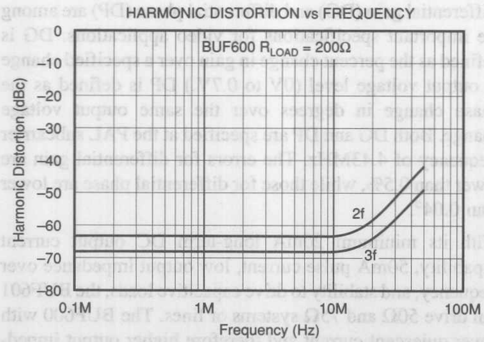


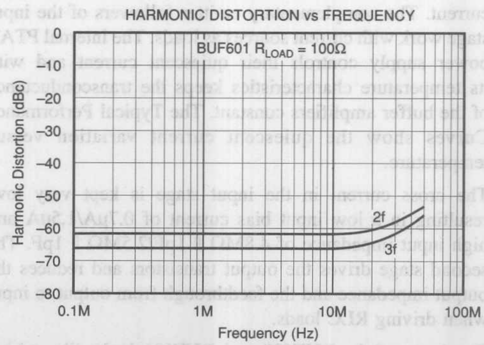

BUF600 BANDWIDTH vs R_{LOAD}
V_1 = 0.2Vp-p
150Ω
500Ω
1kΩ
Gain (dB)
20 15 10 5 0 –5 –10 –15 –20 –25 –30
300k 1M 10M 100M 1G 3G
Frequency (Hz)


BUF601 BANDWIDTH vs R_{LOAD}
V_I = 0.2Vp-p
50Ω
100Ω
150Ω
Gain (dB)
20 15 10 5 0 –5 –10 –15 –20 –25 –30
300k 1M 10M 100M 1G 3G
Frequency (Hz)


BUF600 BANDWIDTH vs OUTPUT VOLTAGE
5Vp-p
2.8Vp-p
1.4Vp-p
0.6Vp-p
0.2Vp-p
Output Voltage (Vp-p)
20 15 10 5 0 –5 –10 –15 –20 –25
dB
300k 1M 10M 100M 1G 3G
Frequency (Hz)

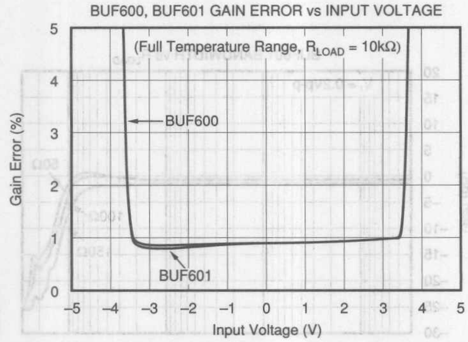

BUF601 BANDWIDTH vs OUTPUT VOLTAGE
5Vp-p
2.8Vp-p
1.4Vp-p
0.6Vp-p
0.2Vp-p
Output Voltage (Vp-p)
20 15 10 5 0 –5 –10 –15 –20 –25
dB
300k 1M 10M 100M 1G 3G
Frequency (Hz)

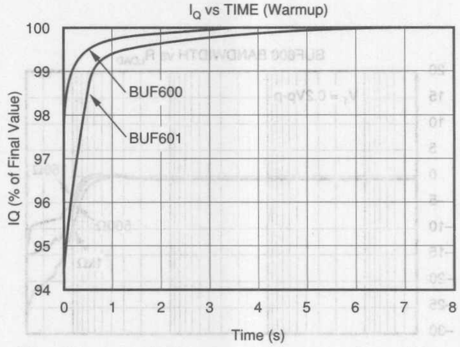

HARMONIC DISTORTION vs FREQUENCY
BUF600 R_{LOAD} = 200Ω
2f
3f
Harmonic Distortion (dBc)
0 –10 –20 –30 –40 –50 –60 –70 –80
0.1M 1M 10M 100M
Frequency (Hz)


HARMONIC DISTORTION vs FREQUENCY
BUF601 R_{LOAD} = 100Ω
2f
3f
Harmonic Distortion (dBc)
0 –10 –20 –30 –40 –50 –60 –70 –80
0.1M 1M 10M 100M
Frequency (Hz)

TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm5V$, $R_{LOAD} = 100\Omega$ (BUF601), $R_{LOAD} = 200\Omega$ (BUF600), and $T_A = 25°C$ unless otherwise noted.





DISCUSSION OF PERFORMANCE

The BUF600 and BUF601 are fabricated using a high-performance complementary bipolar process, which provides high-frequency NPN and PNP transistors with gigahertz transition frequencies (f_T). Power supplies are rated at ±6V maximum, with the data sheet parameters specified at ±5V supplies. The BUF600 and BUF601 are 3-stage open-loop buffer amplifiers consisting of complementary emitter followers with a symmetrical class AB Darlington output stage. The complementary structure provides both sink and source current capability independent of the output voltage, while maintaining constant output and input impedances. The amplifiers use no feedback, so their low-frequency gain is slightly less than unity and somewhat dependent on loading. The optimized input stage is responsible for the high slew rate of up to 3600V/µs, wide large signal bandwidth of 320MHz, and quiescent current reduction to ±3mA (BUF600) and ±6mA (BUF601). These features yield an excellent large signal bandwidth/quiescent current ratio of 320MHz, 5Vp-p at 3mA/6mA quiescent current. The complementary emitter followers of the input stage work with current sources as loads. The internal PTAT power supply controls their quiescent current and with its temperature characteristics keeps the transconductance of the buffer amplifiers constant. The Typical Performance Curves show the quiescent current variation versus temperature.

The cross current in the input stage is kept very low, resulting in a low input bias current of 0.7µA/1.5µA and high input impedance of 4.8MΩ || 1pF/2.5MΩ || 1pF. The second stage drives the output transistors and reduces the output impedance and the feedthrough from output to input when driving RLC loads.

The input of the BUF600 and BUF601 looks like a high resistance in parallel with a 1pF capacitance. The input characteristics change very little with output loading and input voltage swing. The BUF600 and BUF601 have excellent input-to-output isolation and feature high tolerance to variations in source impedances. A resistor between 100Ω and 250Ω in series with the buffer input lead will usually eliminate oscillation problems from inductive sources such as unterminated cables without sacrificing speed.

Another excellent feature is the output-to-input isolation over a wide frequency range. This characteristic is very important when the buffer drives different equipment over cables. Often the cable is not perfect or the termination is incorrect and reflections arise that act like a signal source at the output of the buffer.

Open-loop devices often sacrifice linearity and introduce frequency distortion when driving low load impedance. The BUF600 and BUF601, however, do not. Their design yields low distortion products. The harmonic distortion characteristics into loads greater than 100Ω (BUF601) and greater than 200Ω (BUF600) are shown in the Typical Performance Curves. The distortion can be improved even more by increasing the load resistance.

Differential gain (DG) and differential phase (DP) are among the important specifications for video applications. DG is defined as the percent change in gain over a specified change in output voltage level (0V to 0.7V.) DP is defined as the phase change in degrees over the same output voltage change. Both DG and DP are specified at the PAL subcarrier frequency of 4.43MHz. The errors for differential gain are lower than 0.5%, while those for differential phase are lower than 0.04°.

With its minimum 20mA long-term DC output current capability, 50mA pulse current, low output impedance over frequency, and stability to drive capacitive loads, the BUF601 can drive 50Ω and 75Ω systems or lines. The BUF600 with lower quiescent current and therefore higher output impedance is well-suited primarily to interstage buffering. This type of open-loop amplifier is a new and easy-to-use step to prevent an interaction between two points in complex high-speed analog circuitry.

The buffer outputs are not current-limited or protected. If the output is shorted to ground, high currents could arise when the input voltage is ±3.6V. Momentary shorts to ground (a few seconds) should be avoided but are unlikely to cause permanent damage.

CIRCUIT LAYOUT

The high-frequency performance of the BUF600 and BUF601 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions, not as absolute musts. Oscillations, ringing, poor bandwidth and settling, and peaking are all typical problems that plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF); a parallel 470nF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.
- PC board traces for power lines should be wide to reduce impedance or inductance.
- Make short and low inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.
- Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile solderless sockets.
- Use low-inductance and surface-mounted components. Using all surface-mount components will offer the best AC performance.
- A resistor (100Ω to 250Ω) in series with the input of the buffers may help to reduce peaking.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.

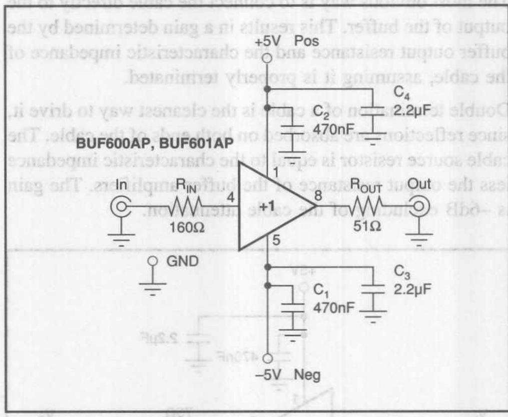


FIGURE 2. Test Circuit.

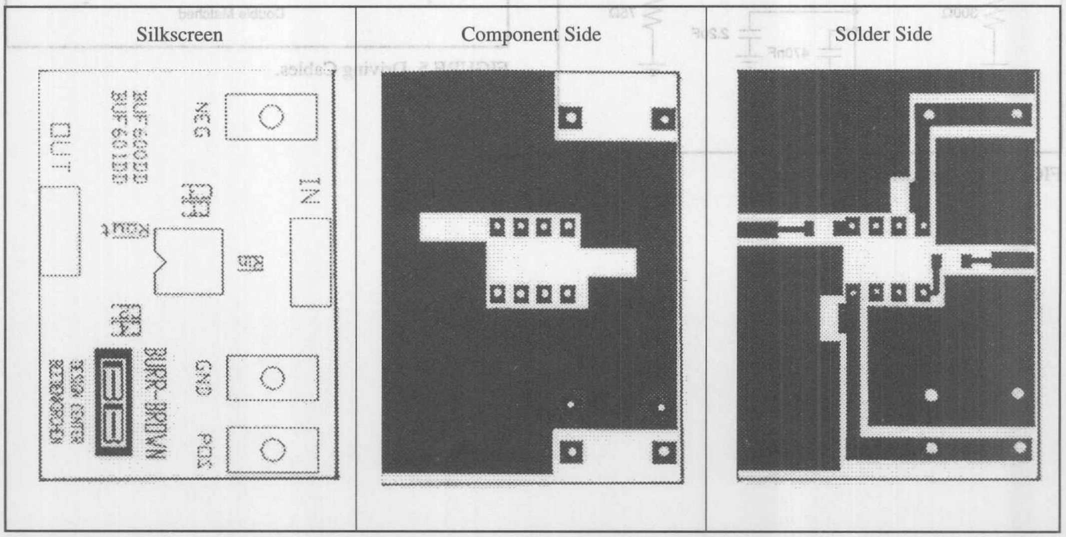


FIGURE 3. Test Circuit Layout.

BUFFER AMPLIFIERS BUF600/601

3.1

The BUF600 and BUF601 provide power gain and isolation between source and load when used as an active tap or impedance matching device as illustrated in Figure 4. In this example, there is no output matching path between the buffer and the 75Ω line. Such matching is not needed when the distant end of the cable is properly terminated, since there is no reflected signal when the buffer isolates the source. This technique allows the full output voltage of the buffer to be applied to the load.

DRIVING CABLES

The most obvious way is to connect the cable directly to the output of the buffer. This results in a gain determined by the buffer output resistance and the characteristic impedance of the cable, assuming it is properly terminated.

Double termination of a cable is the cleanest way to drive it, since reflections are absorbed on both ends of the cable. The cable source resistor is equal to the characteristic impedance less the output resistance of the buffer amplifiers. The gain is –6dB excluding of the cable attenuation.

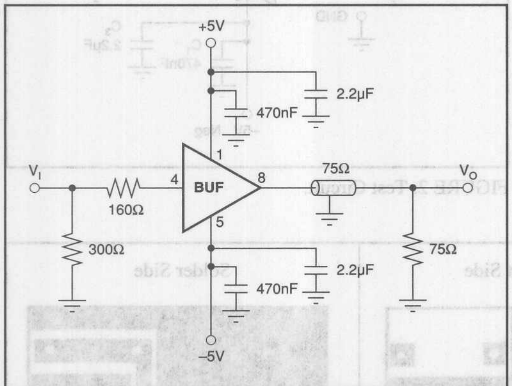


FIGURE 4. Impedance Converter.

In this broadcast quality circuit, the OPA623 provides a very high input impedance so that it may be used with a wide variety of signal sources including video DACs, CCD cameras, video switches or 75Ω cables. The OPA623 provides a voltage gain of 2.5V/V, while the potentiometer of 200Ω allows the overall gain to be adjusted to drive the standard signal levels into the back-terminated 75Ω cables. Back matching prevents multiple reflections in the event that the remote end of the cable is not properly terminated.

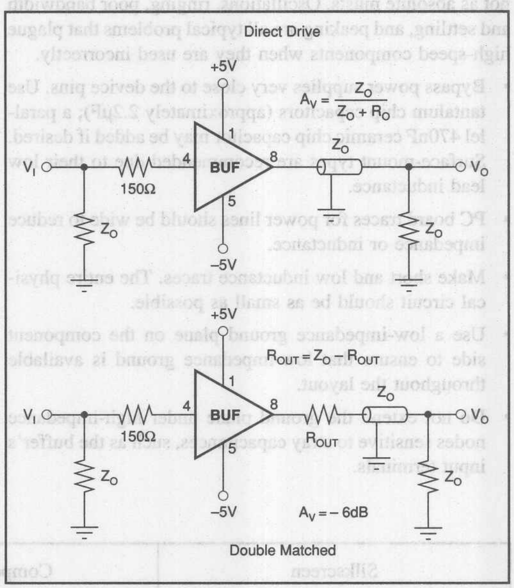


FIGURE 5. Driving Cables.

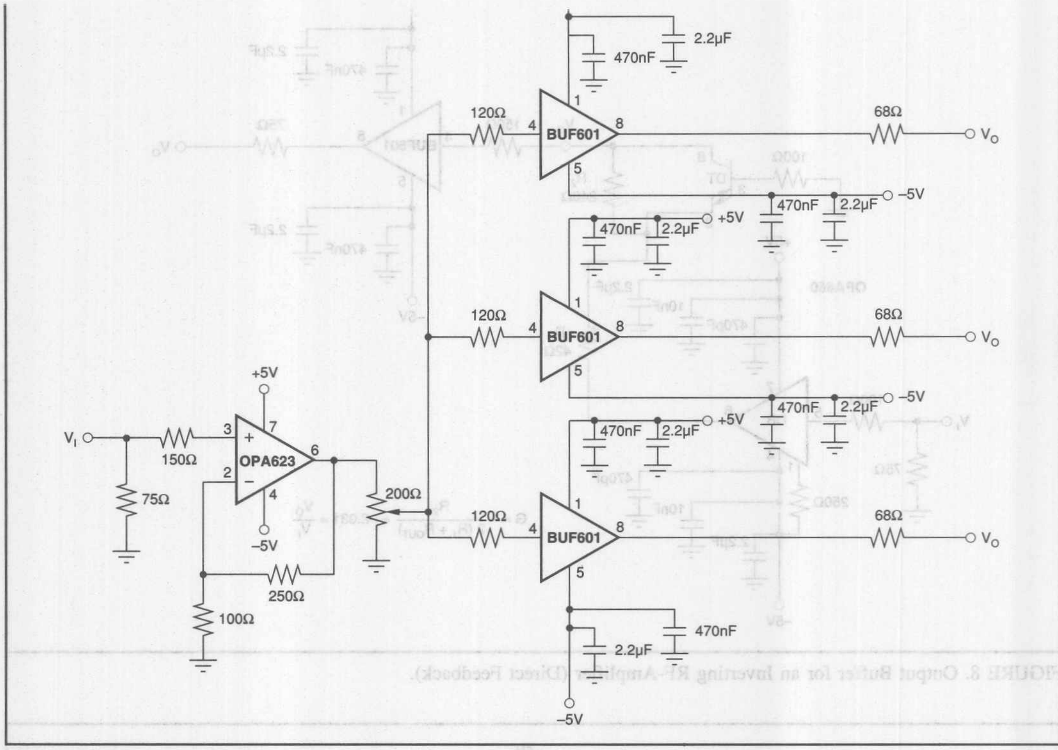


FIGURE 6. Video Distribution Amplifier.

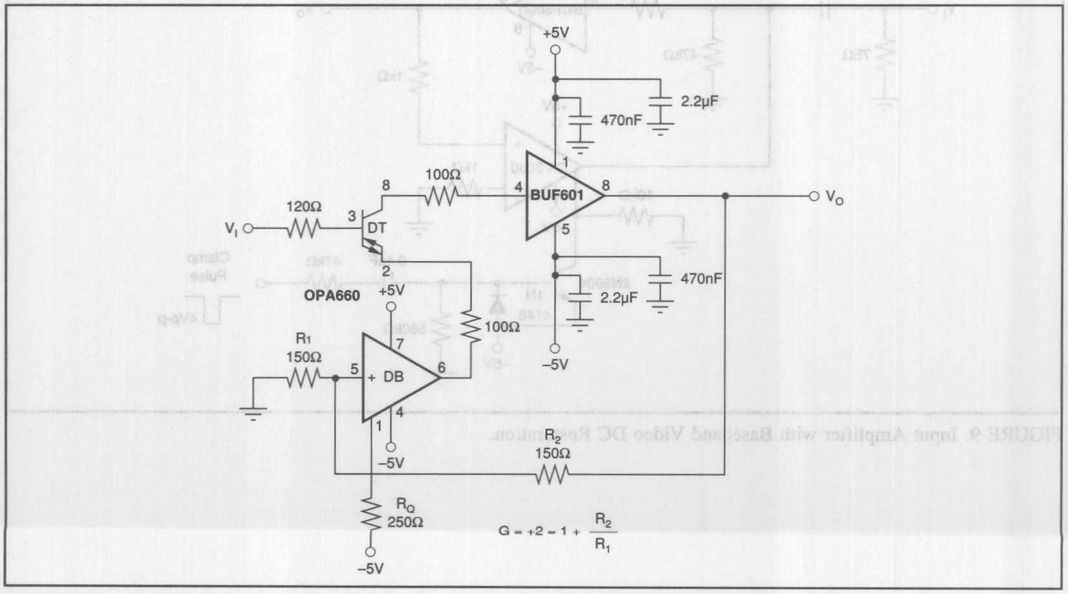


FIGURE 7. Inside a Feedback Loop of a Voltage Feedback Amplifier (BUF601 and OPA660).

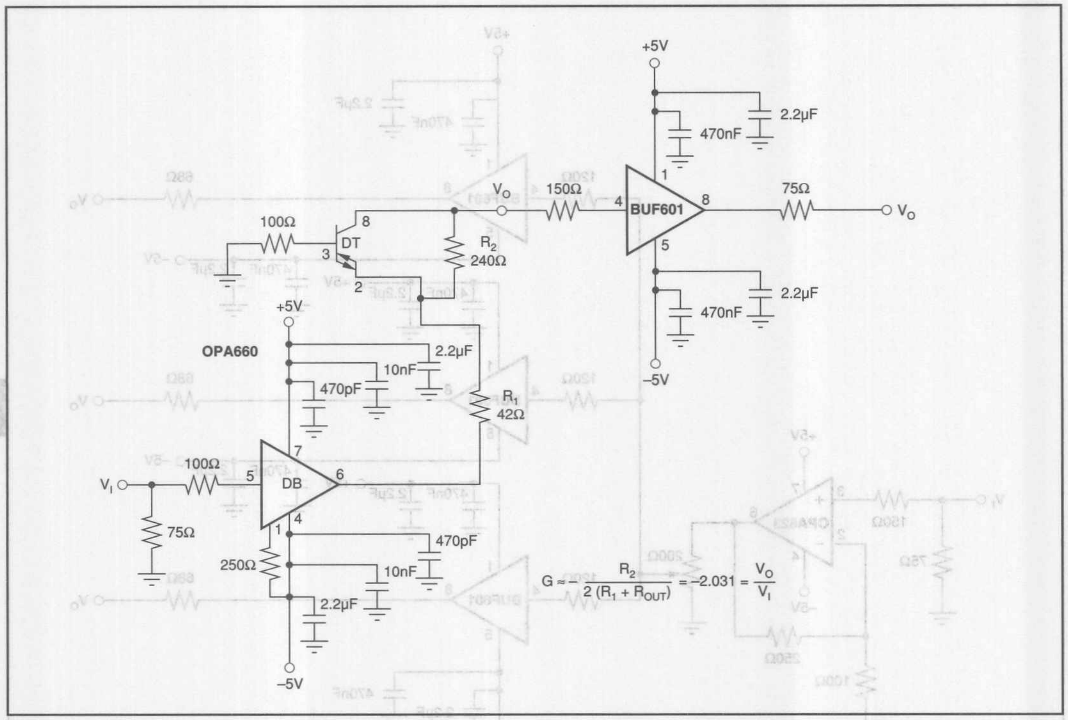


FIGURE 8. Output Buffer for an Inverting RF-Amplifier (Direct Feedback).

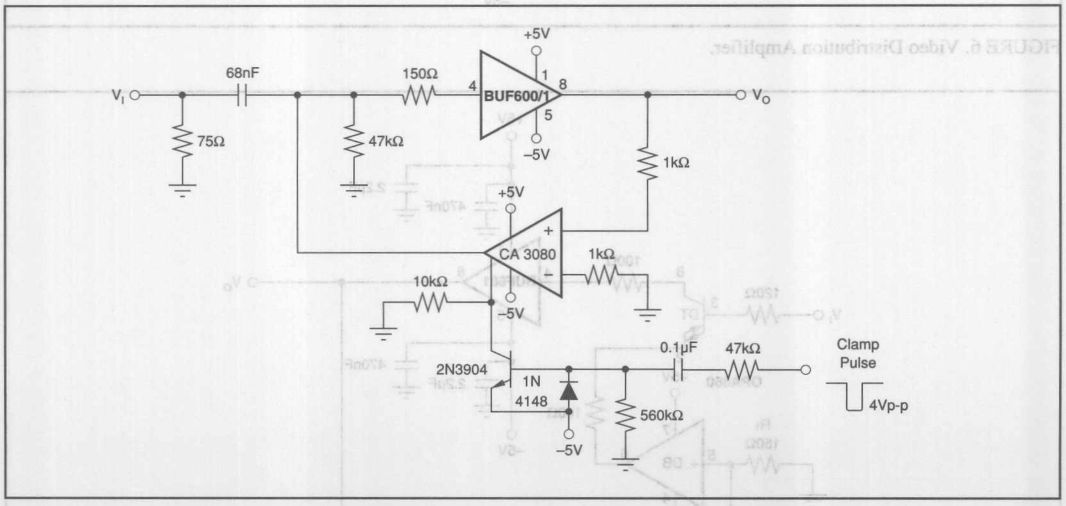


FIGURE 9. Input Amplifier with Baseband Video DC Restoration.

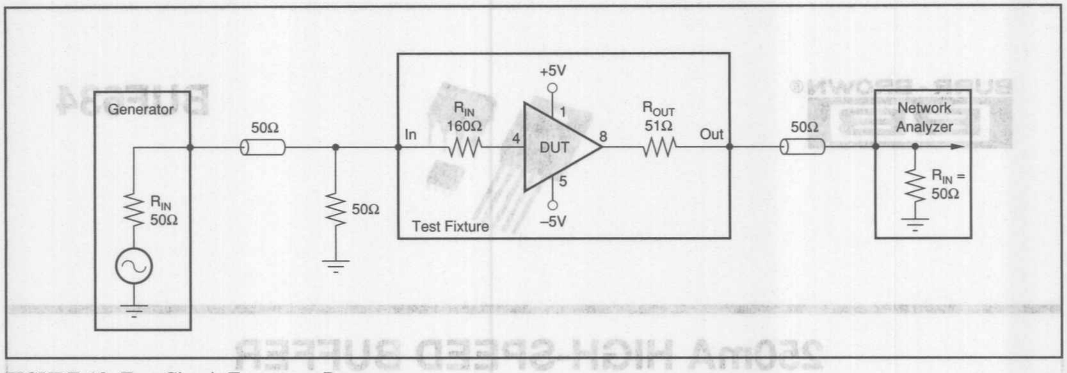


FIGURE 10. Test Circuit Frequency Response.

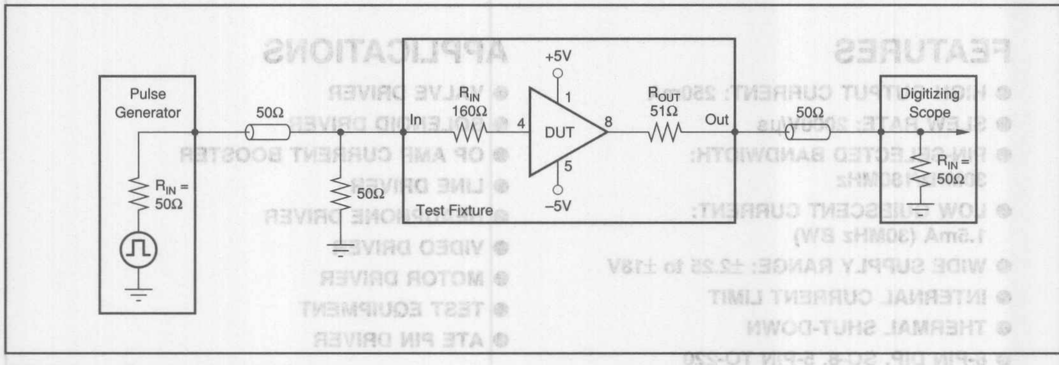


FIGURE 11. Test Circuit Pulse Response.

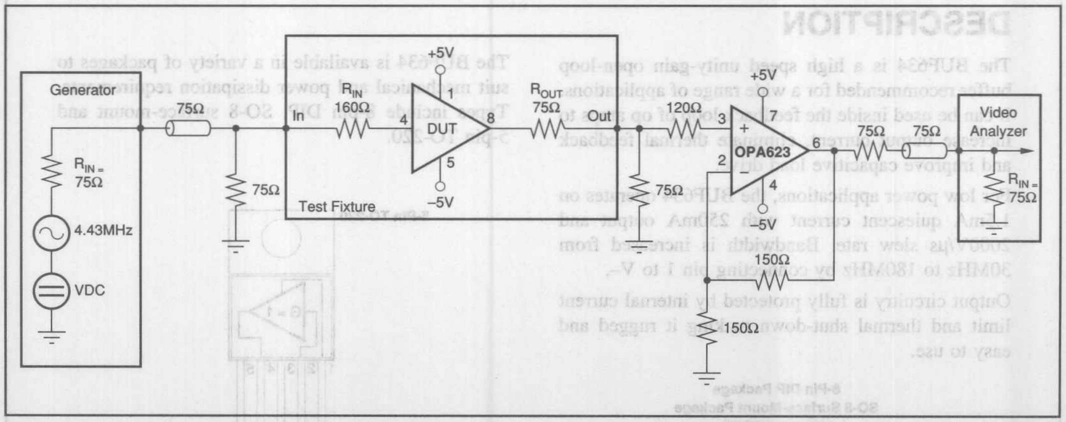
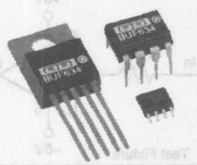


FIGURE 12. Test Circuit Differential Gain and Phase.

BURR - BROWN®



BUF634

250mA HIGH-SPEED BUFFER

FEATURES

- HIGH OUTPUT CURRENT: 250mA
- SLEW RATE: 2000V/µs
- PIN-SELECTED BANDWIDTH: 30MHz/180MHz
- LOW QUIESCENT CURRENT: 1.5mA (30MHz BW)
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- INTERNAL CURRENT LIMIT
- THERMAL SHUT-DOWN
- 8-PIN DIP, SO-8, 5-PIN TO-220 PACKAGES

APPLICATIONS

- VALVE DRIVER
- SOLENOID DRIVER
- OP AMP CURRENT BOOSTER
- LINE DRIVER
- HEADPHONE DRIVER
- VIDEO DRIVER
- MOTOR DRIVER
- TEST EQUIPMENT
- ATE PIN DRIVER

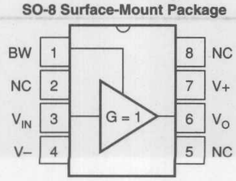
DESCRIPTION

The BUF634 is a high speed unity-gain open-loop buffer recommended for a wide range of applications. It can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback and improve capacitive load drive.

For low power applications, the BUF634 operates on 1.5mA quiescent current with 250mA output and 2000V/µs slew rate. Bandwidth is increased from 30MHz to 180MHz by connecting pin 1 to V–.

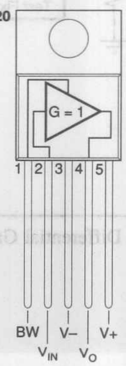
Output circuitry is fully protected by internal current limit and thermal shut-down making it rugged and easy to use.

8-Pin DIP Package
SO-8 Surface-Mount Package



The BUF634 is available in a variety of packages to suit mechanical and power dissipation requirements. Types include 8-pin DIP, SO-8 surface-mount and 5-pin TO-220.

5-Pin TO-220

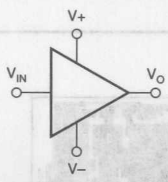


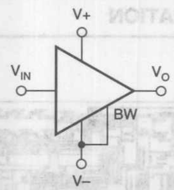
International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1206A

$T_A = +25°C^{(1)}$, $V_S = \pm15V$ unless otherwise noted.

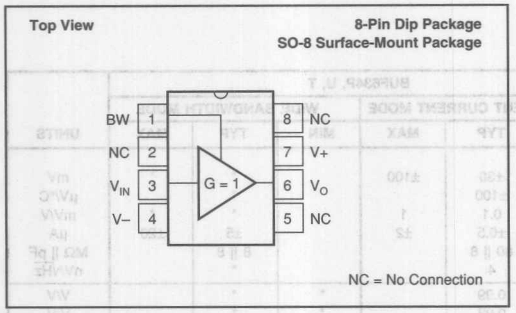
		BUF634P, U, T						
		LOW QUIESCENT CURRENT MODE			WIDE BANDWIDTH MODE			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT								
Offset Voltage			±30	±100		*	*	mV
vs Temperature	Specified Temperature Range		±100			*		μV/°C
vs Power Supply	$V_S = \pm2.25V^{(2)}$ to ±18V		0.1	1		*	*	mV/V
Input Bias Current	$V_{IN} = 0V$		±0.5	±2		±5	±20	μA
Input Impedance	$R_L = 100\Omega$		80 || 8			8 || 8		MΩ || pF
Noise Voltage	f = 10kHz		4			*		$nV/\sqrt{Hz}$
GAIN	$R_L = 1k\Omega$, $V_O = \pm10V$	0.95	0.99		*	*		V/V
	$R_L = 100\Omega$, $V_O = \pm10V$	0.85	0.93		*	*		V/V
	$R_L = 67\Omega$, $V_O = \pm10V$	0.8	0.9		*	*		V/V
OUTPUT								
Current Output, Continuous			±250			*		mA
Voltage Output, Positive	$I_O = 10mA$	(V+) –2.1	(V+) –1.7		*	*		V
Negative	$I_O = -10mA$	(V–) +2.1	(V–) +1.8		*	*		V
Positive	$I_O = 100mA$	(V+) –3	(V+) –2.4		*	*		V
Negative	$I_O = -100mA$	(V–) +4	(V–) +3.5		*	*		V
Positive	$I_O = 150mA$	(V+) –4	(V+) –2.8		*	*		V
Negative	$I_O = -150mA$	(V–) +5	(V–) +4		*	*		V
Short-Circuit Current			±350	±550		±400	*	mA
DYNAMIC RESPONSE								
Bandwidth, –3dB	$R_L = 1k\Omega$		30			180		MHz
	$R_L = 100\Omega$		20			160		MHz
Slew Rate	20Vp-p, $R_L = 100\Omega$		2000			*		V/μs
Settling Time, 0.1%	20V Step, $R_L = 100\Omega$		200			*		ns
1%	20V Step, $R_L = 100\Omega$		50			*		ns
Differential Gain	3.58MHz, $V_O = 0.7V$, $R_L = 150\Omega$		4			0.4		%
Differential Phase	3.58MHz, $V_O = 0.7V$, $R_L = 150\Omega$		2.5			0.1		°
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±2.25(2)		±18	*		*	V
Quiescent Current, I_Q	$I_O = 0$		±1.5	±2		±15	±20	mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operating		–40		+125	*		*	°C
Storage		–40		+125	*		*	°C
Thermal Shutdown								
Temperature, T_J			175					°C
Thermal Resistance, θ_{JA}	"P" Package(3)		100					°C/W
θ_{JA}	"U" Package(3)		150			*		°C/W
θ_{JA}	"T" Package(3)		65			*		°C/W
θ_{JC}	"T" Package		6			*		°C/W

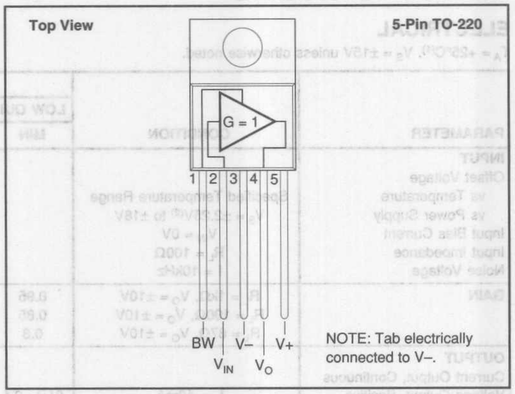




NOTES: (1) Tests are performed on high speed automatic test equipment, at approximately 25°C junction temperature. The power dissipation of this product will cause some parameters to shift when warmed up. See typical performance curves for over-temperature performance. (2) Limited output swing available at low supply voltage. See Output voltage specifications. (3) Typical when all leads are soldered to a circuit board. See text for recommendations.

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering,10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION

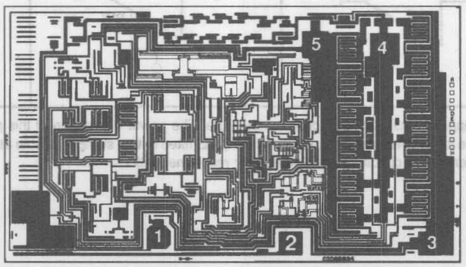
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
BUF634P	8-Pin PDIP	006
BUF634U	SO-8 Surface Mount	182
BUF634T	5-Pin TO-220	315

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
BUF634P	8-Pin Plastic DIP	–40 to +85°C
BUF634U	SO-8 Surface-Mount	–40 to +85°C
BUF634T	5-Pin TO-220	–40 to +85°C

DICE INFORMATION



BUF634 DIE TOPOGRAPHY

PAD	FUNCTION
1	BW
2	V_{IN}
3	V–
4	V_O
5	V+

Substrate Bias: Internally connected to V– power supply.

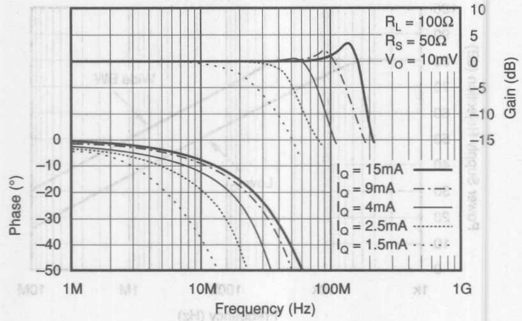
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	120 x 70 ±5	3.05 x 1.78 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Chromium-Silver

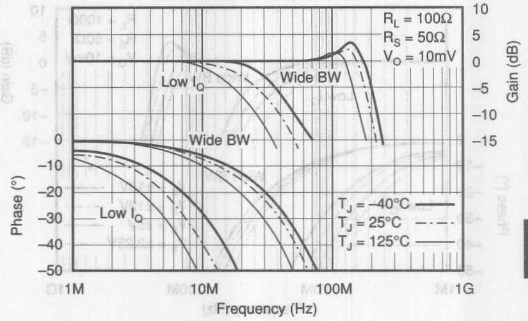
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

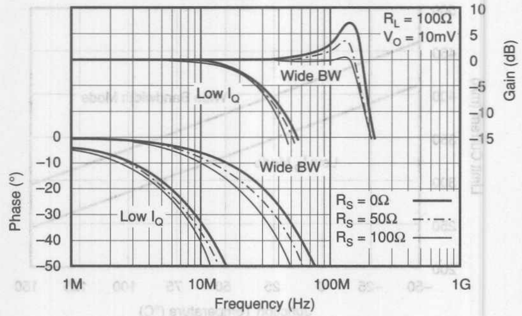
GAIN and PHASE vs FREQUENCY vs QUIESCENT CURRENT



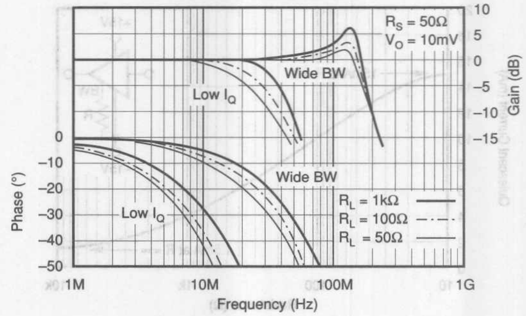
GAIN and PHASE vs FREQUENCY vs TEMPERATURE



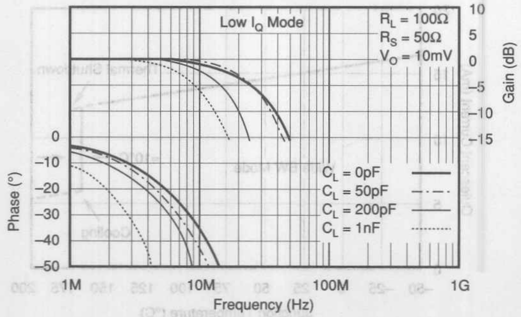
GAIN and PHASE vs FREQUENCY vs SOURCE RESISTANCE



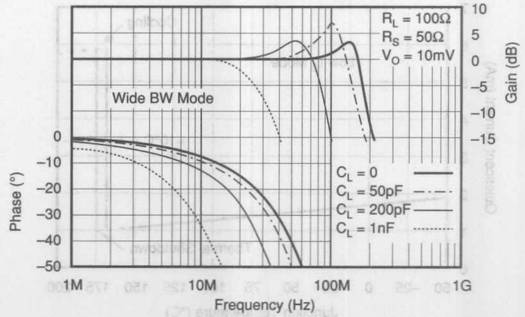
GAIN and PHASE vs FREQUENCY vs LOAD RESISTANCE



GAIN and PHASE vs FREQUENCY vs LOAD CAPACITANCE



GAIN and PHASE vs FREQUENCY vs LOAD CAPACITANCE



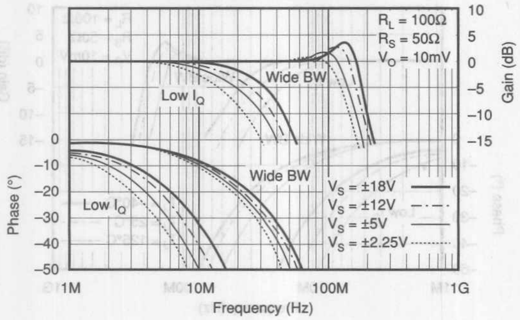
BUF634

3.1

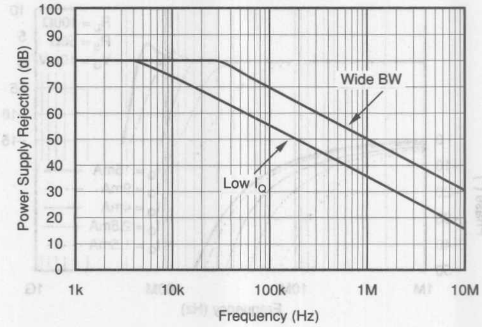
BUFFER AMPLIFIERS

$T_A = +25°C$, $V_S = ±15V$ unless otherwise noted.

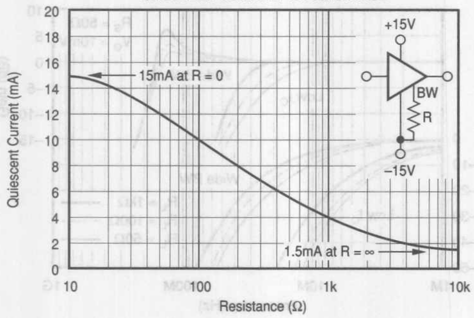
GAIN and PHASE vs FREQUENCY vs POWER SUPPLY VOLTAGE



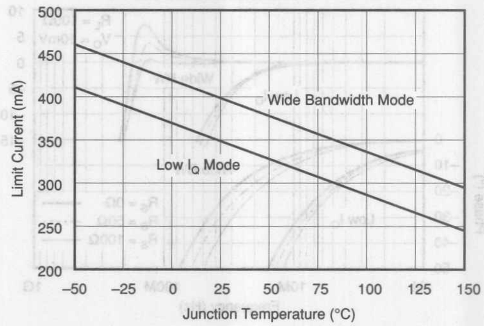
POWER SUPPLY REJECTION vs FREQUENCY



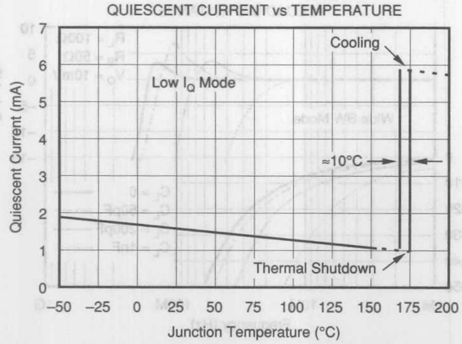
QUIESCENT CURRENT vs RESISTANCE



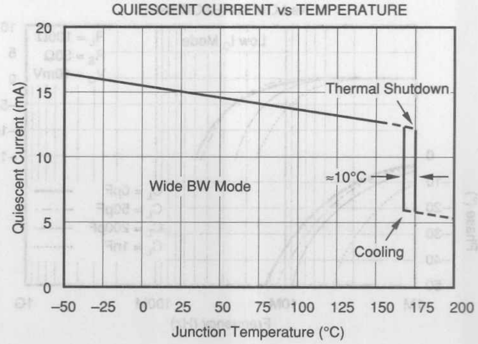
SHORT CIRCUIT CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



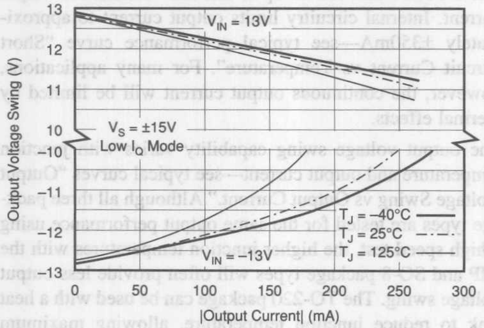
QUIESCENT CURRENT vs TEMPERATURE



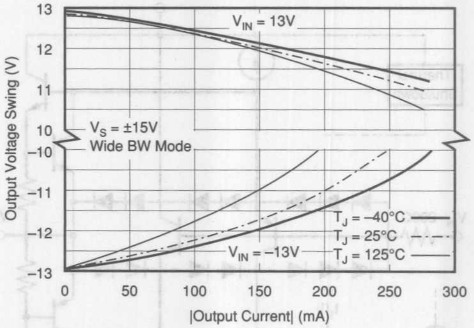
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm15V$ unless otherwise noted.

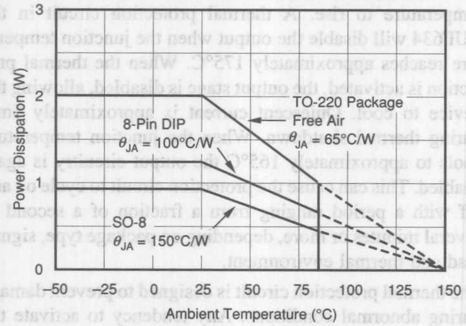
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



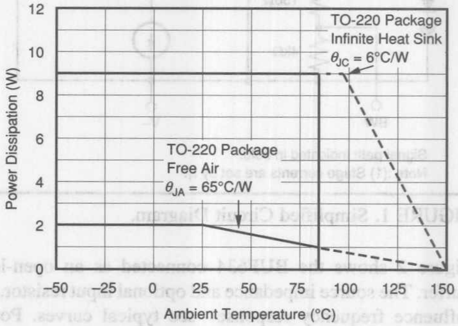
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



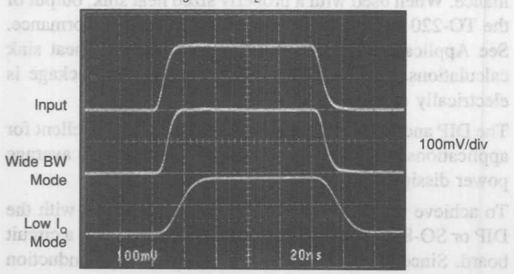
MAXIMUM POWER DISSIPATION vs TEMPERATURE



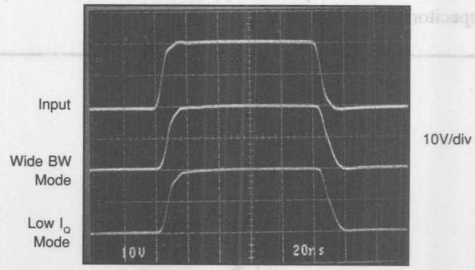
MAXIMUM POWER DISSIPATION vs TEMPERATURE



SMALL-SIGNAL RESPONSE
$R_s = 50\Omega$, $R_L = 100\Omega$



LARGE-SIGNAL RESPONSE
$R_s = 50\Omega$, $R_L = 100\Omega$



APPLICATION INFORMATION

Figure 1 is a simplified circuit diagram of the BUF634 showing its open-loop complementary follower design.

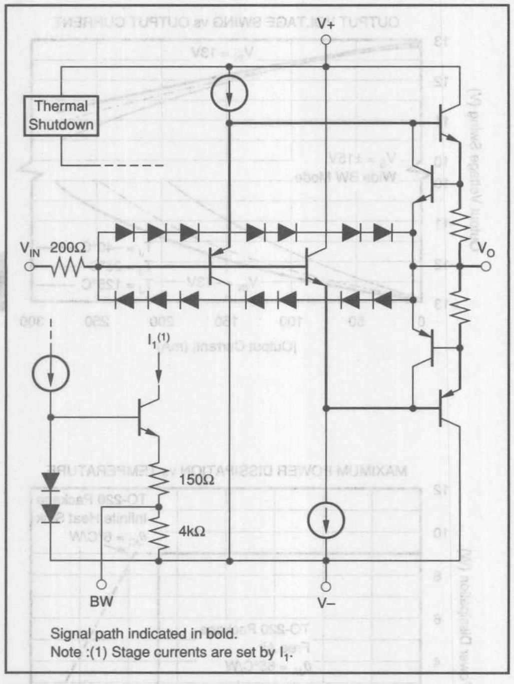


FIGURE 1. Simplified Circuit Diagram.

Figure 2 shows the BUF634 connected as an open-loop buffer. The source impedance and optional input resistor, R_S, influence frequency response—see typical curves. Power supplies should be bypassed with capacitors connected close to the device pins. Capacitor values as low as 0.1µF will assure stable operation in most applications, but high output current and fast output slewing can demand large current transients from the power supplies. Solid tantalum 10µF capacitors are recommended.

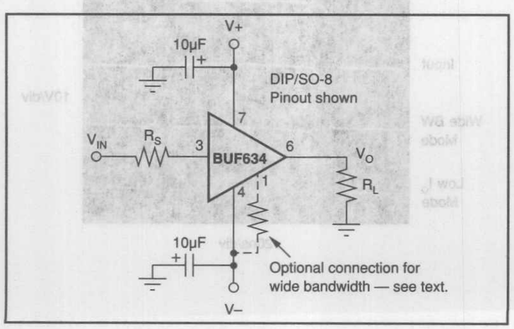


FIGURE 2. Buffer Connections.

High frequency open-loop applications may benefit from special bypassing and layout considerations—see "High Frequency Applications" at end of applications discussion.

OUTPUT CURRENT

The BUF634 can deliver up to ±250mA continuous output current. Internal circuitry limits output current to approximately ±350mA—see typical performance curve "Short Circuit Current vs Temperature". For many applications, however, the continuous output current will be limited by thermal effects.

The output voltage swing capability varies with junction temperature and output current—see typical curves "Output Voltage Swing vs Output Current." Although all three package types are tested for the same output performance using a high speed test, the higher junction temperatures with the DIP and SO-8 package types will often provide less output voltage swing. The TO-220 package can be used with a heat sink to reduce junction temperature, allowing maximum possible output swing.

THERMAL PROTECTION

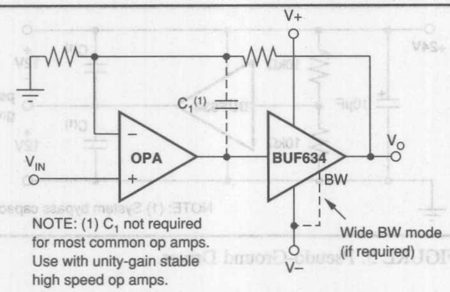
Power dissipated in the BUF634 will cause the junction temperature to rise. A thermal protection circuit in the BUF634 will disable the output when the junction temperature reaches approximately 175°C. When the thermal protection is activated, the output stage is disabled, allowing the device to cool. Quiescent current is approximately 6mA during thermal shutdown. When the junction temperature cools to approximately 165°C the output circuitry is again enabled. This can cause the protection circuit to cycle on and off with a period ranging from a fraction of a second to several minutes or more, depending on package type, signal, load and thermal environment.

The thermal protection circuit is designed to prevent damage during abnormal conditions. Any tendency to activate the thermal protection circuit during normal operation is a sign of an inadequate heat sink or excessive power dissipation for the package type.

The 5-pin TO-220 package provides the best thermal performance. When used with a properly sized heat sink, output of the TO-220 version is not limited by thermal performance. See Application Bulletin AB-037 for details on heat sink calculations. The mounting tab of the TO-220 package is electrically connected to the V– power supply.

The DIP and SO-8 surface-mount packages are excellent for applications requiring high output current with low average power dissipation.

To achieve the best possible thermal performance with the DIP or SO-8 packages, solder the device directly to a circuit board. Since much of the heat is dissipated by conduction through the package pins, sockets will degrade thermal performance. Use wide circuit board traces on all the device pins, including pins that are not connected. With the DIP package, use traces on both sides of the printed circuit board if possible.



OP AMP	RECOMMENDATIONS
OPA177, OPA1013 OPA111, OPA2111 OPA121	Use Low I_Q mode. G = 1 stable.
OPA27, OPA2107 OPA602, OPA404	Low I_Q mode is stable. Increasing C_L may cause excessive ringing or instability. Use Wide BW mode.
OPA627, OPA604 OPA2604	Use Wide BW mode, C_1 = 200pF. G = 1 stable.
OPA637, OPA37	Use Wide BW mode. These op amps are not G = 1 stable. Use in G > 4.

FIGURE 3. Boosting Op Amp Output Current.

POWER DISSIPATION

Power dissipation depends on power supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power supply voltage. Dissipation with AC signals is lower. Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered. The thermal protection should trigger more than 45°C above the maximum expected ambient condition of your application.

INPUT CHARACTERISTICS

Internal circuitry is protected with a diode clamp connected from the input to output of the BUF634—see Figure 1. If the output is unable to follow the input within approximately 3V (such as with an output short-circuit), the input will conduct increased current from the input source. This is limited by the internal 200Ω resistor. If the input source can be damaged by this increase in load current, an additional resistor can be connected in series with the input.

BANDWIDTH CONTROL PIN

The –3dB bandwidth of the BUF634 is approximately 30MHz in the low quiescent current mode (1.5mA typical). To select this mode, leave the bandwidth control pin open (no connection).

Bandwidth can be extended to approximately 180MHz by connecting the bandwidth control pin to V–. This increases the quiescent current to approximately 15mA. Intermediate bandwidths can be set by connecting a resistor in series with the bandwidth control pin—see typical curve "Quiescent Current vs Resistance" for resistor selection. Characteristics of the bandwidth control pin can be seen in the simplified circuit diagram, Figure 1.

The rated output current and slew rate are not affected by the bandwidth control, but the current limit value changes slightly. Output voltage swing is somewhat improved in the wide bandwidth mode. The increased quiescent current when in wide bandwidth mode produces greater power dissipation during low output current conditions. This quiescent power is equal to the total supply voltage, (V+)+|V–|, times the quiescent current.

BOOSTING OP AMP OUTPUT CURRENT

The BUF634 can be connected inside the feedback loop of most op amps to increase output current—see Figure 3. When connected inside the feedback loop, the BUF634's offset voltage and other errors are corrected by the feedback of the op amp.

To assure that the op amp remains stable, the BUF634's phase shift must remain small throughout the loop gain of the circuit. For a G=+1 op amp circuit, the BUF634 must contribute little additional phase shift (approximately 20° or less) at the unity-gain frequency of the op amp. Phase shift is affected by various operating conditions that may affect stability of the op amp—see typical Gain and Phase curves.

Most general-purpose or precision op amps remain unity-gain stable with the BUF634 connected inside the feedback loop as shown. Large capacitive loads may require the BUF634 to be connected for wide bandwidth for stable operation. High speed or fast-settling op amps generally require the wide bandwidth mode to remain stable and to assure good dynamic performance. To check for stability with an op amp, look for oscillations or excessive ringing on signal pulses with the intended load and worst case conditions that affect phase response of the buffer.

HIGH FREQUENCY APPLICATIONS

The BUF634's excellent bandwidth and fast slew rate make it useful in a variety of high frequency open-loop applications. When operated open-loop, circuit board layout and bypassing technique can affect dynamic performance.

For best results, use a ground plane type circuit board layout and bypass the power supplies with 0.1μF ceramic chip

ringing. Best response is usually achieved with a series input resistor of 25Ω to 200Ω, depending on the signal source. Response with some loads (especially capacitive) can be improved with a resistor of 10Ω to 150Ω in series with the output.

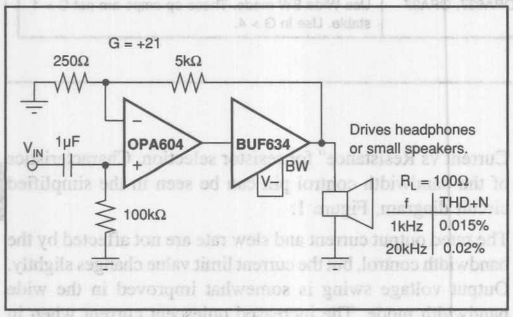


FIGURE 4. High Performance Headphone Driver.

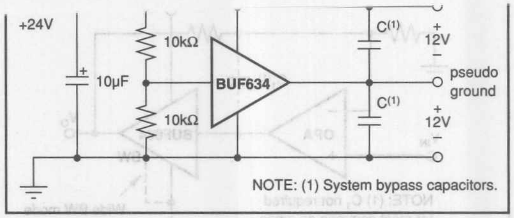


FIGURE 5. Pseudo-Ground Driver.

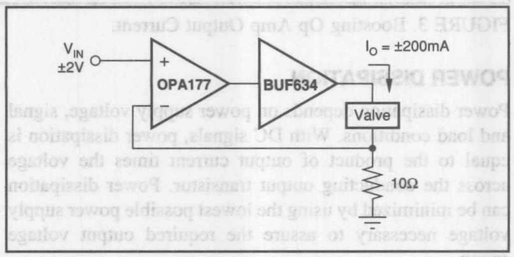


FIGURE 6. Current-Output Valve Driver.

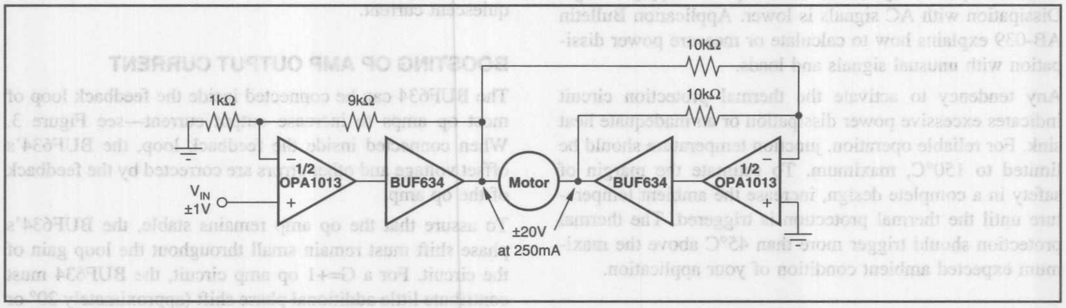


FIGURE 7. Bridge-Connected Motor Driver.

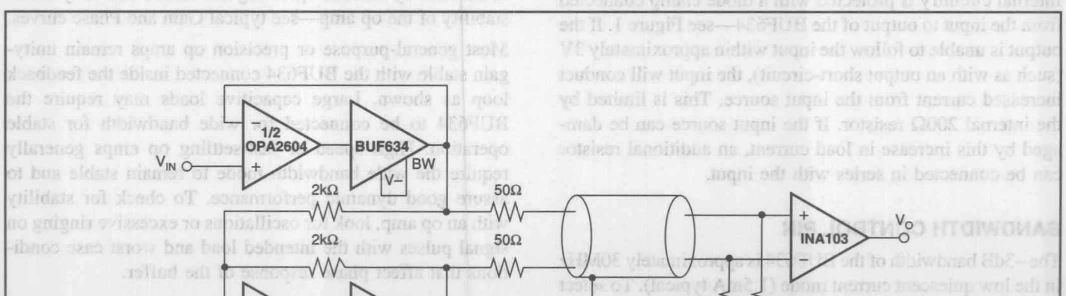
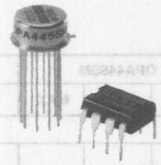


FIGURE 8. Differential Line Driver.

BURR - BROWN®

OPA445



High Voltage FET-Input OPERATIONAL AMPLIFIER

FEATURES

- WIDE POWER SUPPLY RANGE: ±10V to ±45V
- HIGH SLEW RATE: 10V/μs
- LOW INPUT BIAS CURRENT: 50pA max
- STANDARD-PINOUT TO-99 AND DIP PACKAGES

APPLICATIONS

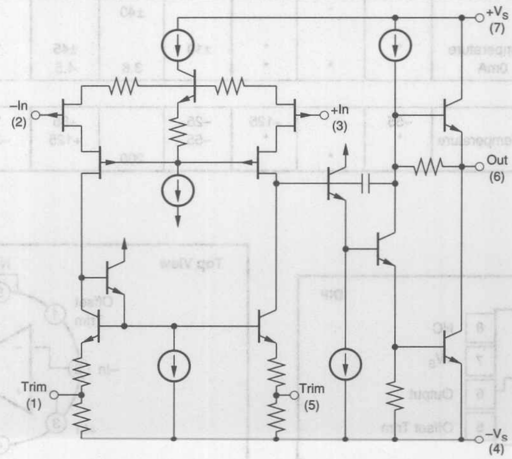
- TEST EQUIPMENT
- HIGH VOLTAGE REGULATORS
- POWER AMPLIFIERS
- DATA ACQUISITION
- SIGNAL CONDITIONING

DESCRIPTION

The OPA445 is a monolithic operational amplifier capable of operation from power supplies up to ±45V and output currents of 15mA. It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings.

The OPA445's high slew rate provides wide power-bandwidth response, which is often required for high voltage applications. FET input circuitry allows the use of high impedance feedback networks, thus minimizing their output loading effects. Laser trimming of the input circuitry yields low input offset voltage and drift.

The OPA445 is unity-gain stable and requires no external compensation components. It is available in both industrial (–25°C to +85°C) and military (–55°C to +125°C) temperature ranges.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

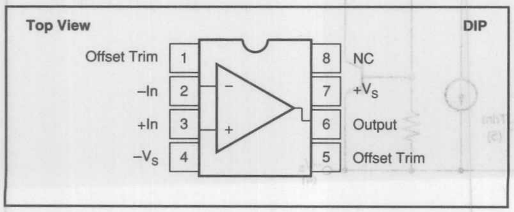
ELECTRICAL

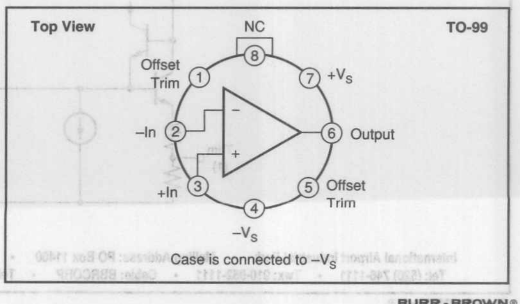
At $V_S = \pm 40°C$ and $T_A = +25°C$, unless otherwise specified.

PARAMETER	CONDITIONS	OPA445SM MIN	OPA445SM TYP	OPA445SM MAX	OPA445BM MIN	OPA445BM TYP	OPA445BM MAX	OPA445AP MIN	OPA445AP TYP	OPA445AP MAX	UNITS
INPUT											
OFFSET VOLTAGE											
Input Offset Voltage	$V_{CM} = 0V$		0.5	1.0		1.0	3.0		2.0	5.0	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		*			10			15		µV/°C
Supply Rejection	$V_S = \pm10V$ to $\pm50V$	*	*		80	110		*	*		dB
BIAS CURRENT											
Input Bias Current	$V_{CM} = 0V$		*	*		20	50		50	100	pA
Over Temperature				100			10			20	nA
OFFSET CURRENT											
Input Offset Current	$V_{CM} = 0V$		*	*		4	10		20	40	pA
Over Temperature				50			5			10	nA
IMPEDANCE											
Differential			*			$10^{13} \parallel 1$			*		Ω ‖ pF
Common-Mode			*			$10^{14} \parallel 3$			*		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		*			±35			*			V
Common-Mode Rejection	$V_{IN} = \pm30V$, Over Temp.	*	*		80	95		*	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L = 5k\Omega$	*	*		100	105		*	*		dB
Over Temperature		*			97			*			dB
FREQUENCY RESPONSE											
Gain Bandwidth	Small Signal		*			2			*		MHz
Full Power Response	35Vp-p, $R_L = 5k\Omega$	*	*		45	55		*	*		kHz
DYNAMIC RESPONSE											
Slew Rate	$V_O = \pm35V$, $R_L = 5k\Omega$	*	*		5	10		*	*		V/µs
Rise Time	$V_O = \pm200mV$		*			100			*		ns
Overshoot	$A_V = +1$, $Z_L = 5k\Omega \parallel 50pF$		*			30			*		%
OUTPUT											
Voltage Output, Over Temp.	$R_L = 5k\Omega$	*			±35			*			V
Current Output	$V_O = \pm28V$	*			±15			*			mA
Output Resistance	DC, Open Loop		*			220			*		Ω
Short Circuit Current			*			±26			*		mA
POWER SUPPLY											
Rated Voltage, $\pm V_S$			*			±40			*		V
Voltage Range, $\pm V_S$ Derated Performance	Over Temperature	*		*	±10		±45	*		*	V
Current, Quiescent	$I_O = 0mA$		*	*		3.8	4.5		*	*	mA
TEMPERATURE RANGE											
Specification		–55		+125	–25		+85	*		*	°C
Operating	Ambient Temperature	*		*	–55		+125	–25		+85	°C
θ Junction-Ambient			*			200			100		°C/W

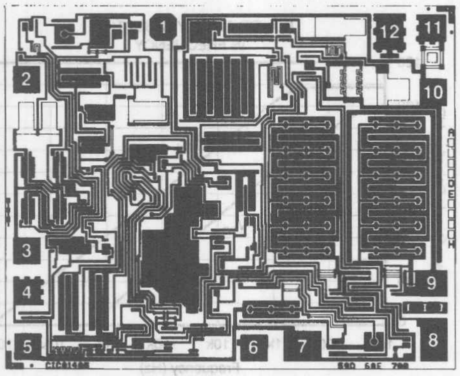
*Specifications same as OPA445BM.

CONNECTION DIAGRAMS





DICE INFORMATION



OPA445 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Trim	7	$-V_S$
2	–In	8	(Compensation)
3	+In	9	Output
4	NC	10	$+V_S$
5	$-V_S$	11	NC
6	Offset Trim	12	NC

Substrate Bias: Electrically connected to $-V_S$ supply.
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	88 x 72 ±5	2.24 x 1.83 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Chromium-Silver

ABSOLUTE MAXIMUM RATINGS

Power Supply	±50V
Internal Power Dissipation	680mW
Differential Input Voltage	±80V
Input Voltage Range	$\|\pm V_S\|$ –3V
Storage Temperature Range: M	–65°C to +150°C
P	–40°C to +85°C
Operating Temperature Range: M	–55°C to +125°C
P	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit to Ground (T_A = +25°C)	Continuous
Junction Temperature	+175°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA445AP	8-pin plastic DIP	–25°C to +85°C
OPA445BM	8-pin TO-99	–25°C to +85°C
OPA445SM	8-pin TO-99	–55°C to +125°C

PACKAGE INFORMATION

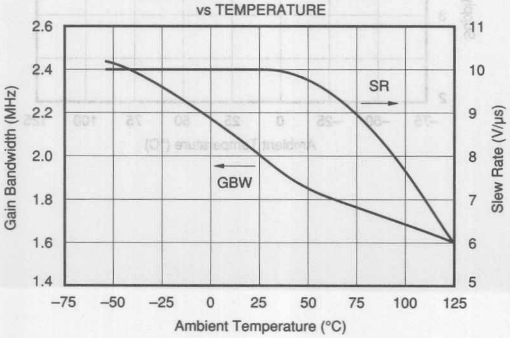
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA445AP	8-pin plastic DIP	006
OPA445BM	8-pin TO-99	001
OPA445SM	8-pin TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

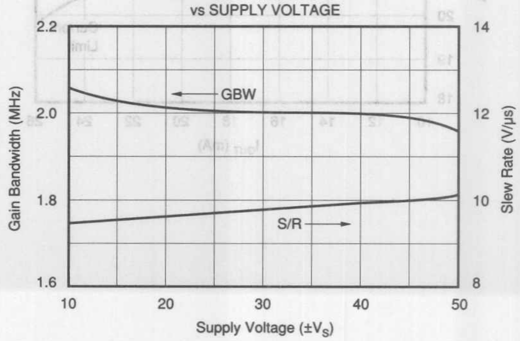
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±40VDC, unless otherwise noted.

GAIN BANDWIDTH AND SLEW RATE vs TEMPERATURE

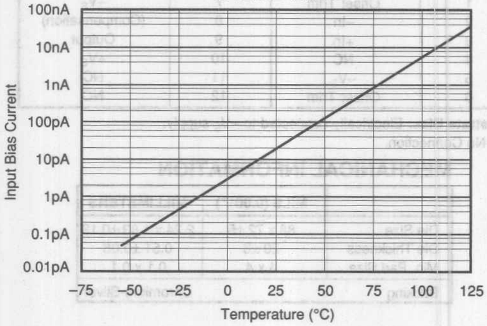


GAIN BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE

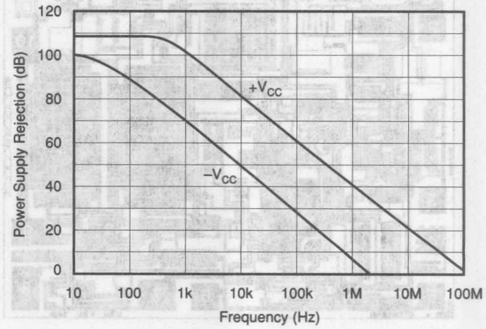


$T_A = +25°C$, $V_S = ±40VDC$, unless otherwise noted.

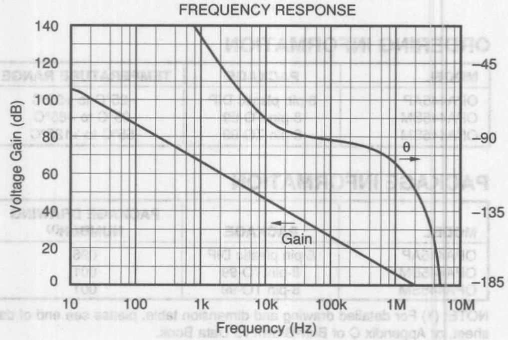
INPUT BIAS CURRENT
vs TEMPERATURE



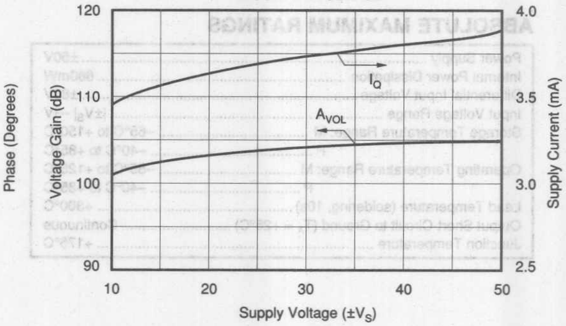
POWER SUPPLY REJECTION
vs FREQUENCY



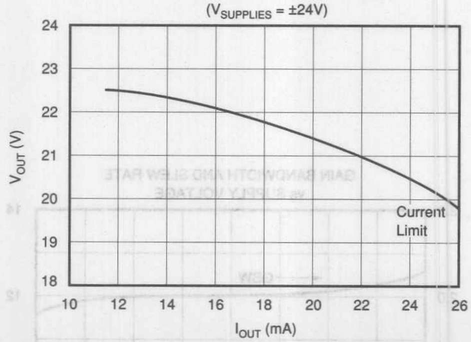
OPEN-LOOP
FREQUENCY RESPONSE



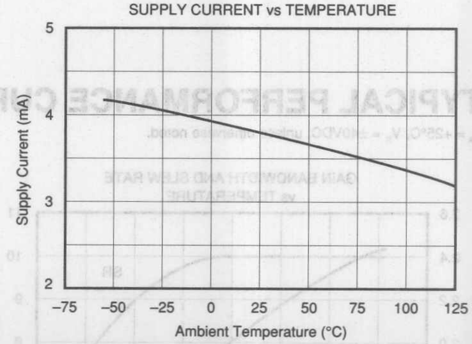
OPEN-LOOP GAIN AND SUPPLY CURRENT
vs SUPPLY VOLTAGE



OUTPUT VOLTAGE vs OUTPUT CURRENT
($V_{SUPPLIES} = ±24V$)

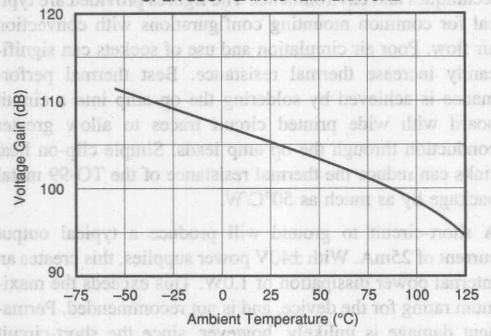


SUPPLY CURRENT vs TEMPERATURE

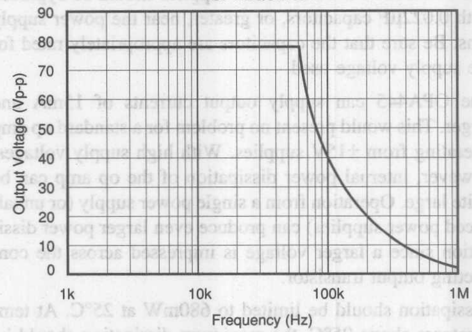


$T_A = +25°C$, $V_S = ±15VDC$ unless otherwise noted.

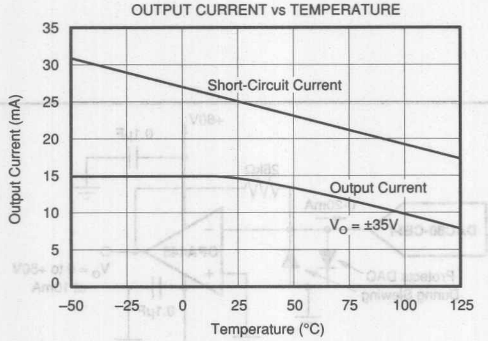
OPEN-LOOP GAIN vs TEMPERATURE



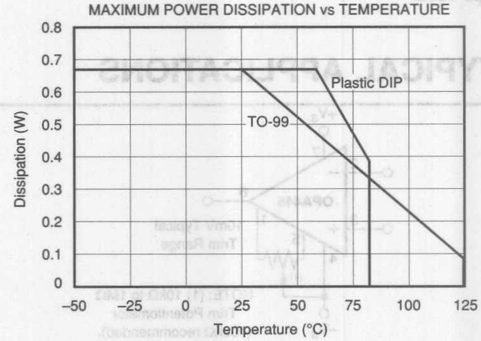
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



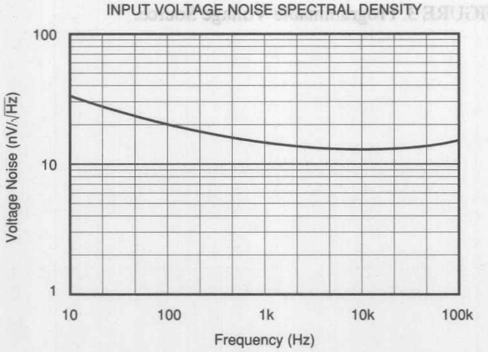
OUTPUT CURRENT vs TEMPERATURE



MAXIMUM POWER DISSIPATION vs TEMPERATURE



INPUT VOLTAGE NOISE SPECTRAL DENSITY



INSTALLATION AND OPERATING INSTRUCTIONS

The OPA445 may be operated from power supplies up to ±45V or a total of 90V. Power supplies should be bypassed with 0.022µF capacitors, or greater, near the power supply pins. Be sure that the capacitors are appropriately rated for the supply voltage used.

The OPA445 can supply output currents of 15mA and larger. This would present no problem for a standard op amp operating from ±15V supplies. With high supply voltages, however, internal power dissipation of the op amp can be quite large. Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation since a larger voltage is impressed across the conducting output transistor.

Dissipation should be limited to 680mW at 25°C. At temperatures above 25°C, the maximum dissipation should be derated according to the thermal resistance of the package type used.

Package thermal resistance, θ_{JC}, is affected by mounting techniques and environments. The figures provided are typical for common mounting configurations with convection air flow. Poor air circulation and use of sockets can significantly increase thermal resistance. Best thermal performance is achieved by soldering the op amp into a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Simple clip-on heat sinks can reduce the thermal resistance of the TO-99 metal package by as much as 50°C/W.

A short-circuit to ground will produce a typical output current of 25mA. With ±40V power supplies, this creates an internal power dissipation of 1.0W. This exceeds the maximum rating for the device, and is not recommended. Permanent damage is unlikely, however, since the short-circuit output current will diminish as the junction temperature rises.

TYPICAL APPLICATIONS

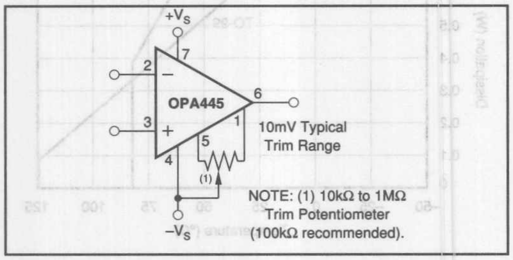


FIGURE 1. Offset Voltage Trim.

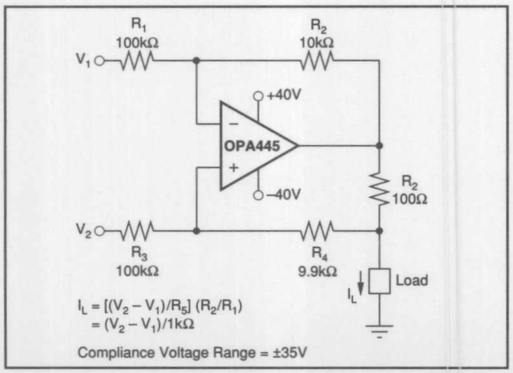


FIGURE 2. Voltage-to-Current Converter.

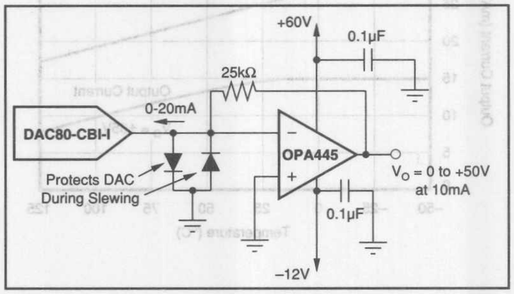


FIGURE 3. Programmable Voltage Source.

BURR - BROWN®

OPA501

High Current, High Power OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: ±10A Peak
- WIDE POWER SUPPLY RANGE: ±10 to ±40V
- LOW QUIESCENT CURRENT: 2.6mA
- ISOLATED CASE TO-3 PACKAGE

APPLICATIONS

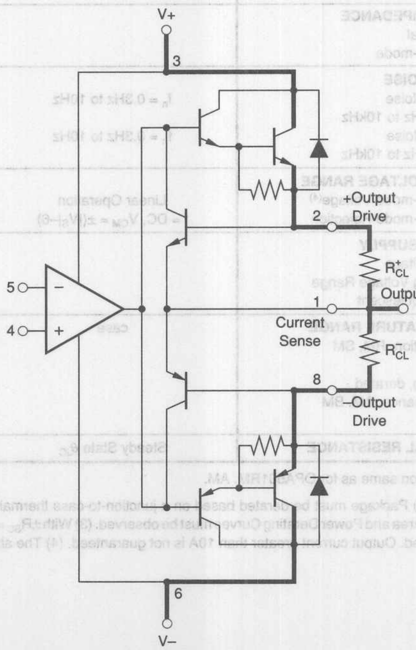
- MOTOR DRIVER
- SERVO AMPLIFIER
- VALVE ACTUATOR
- SYNCRO DRIVER
- PROGRAMMABLE POWER SUPPLY

DESCRIPTION

The OPA501 is a high output current operational amplifier. It can be used in virtually all common op amp circuits, yet is capable of output currents up to ±10A. Power supply voltages up to ±40V allow very high output power for driving motors or other electro-mechanical loads.

Safe operating area is fully specified, and user-set current limits provide protection for both the amplifier and load. The class-B (zero output stage bias) provides low quiescent current during small-signal conditions.

This rugged hybrid integrated circuit is packaged in a metal 8-pin TO-3 package. Both industrial and military temperature range models are available.



SPECIFICATIONS

ELECTRICAL

At $T_C = +25°C$, $V_S = ±28V$, (OPA501RM, AM); $V_S = ±34V$ (OPA501SM, BM) unless otherwise noted.

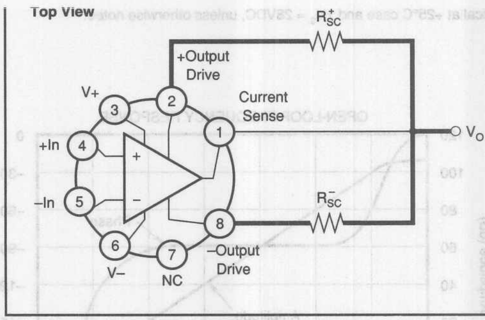
		OPA501RM, AM			OPA501SM, BM			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RATED OUTPUT(1, 2)								
Output Current	$R_L = 2\Omega$ (RM, AM)	±10			*			A
Continuous(3)	$R_L = 2.6\Omega$ (SM, BM)	±10			*			A
Output Voltage(3)	$I_O = 10A$ peak	±20	±23		±26	±29		V
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal		1			*		MHz
Full Power Bandwidth	$V_O = 40Vp\text{-}p$, $R_L = 8\Omega$	10	16		*	*		kHz
Slew Rate	$R_L = 5\Omega$ (RM, AM)	1.35			*			V/μs
	$R_L = 6.5\Omega$ (SM, BM)	1.35			*			v/μs
INPUT OFFSET VOLTAGE								
Initial Offset			±5	±10		±2	±5	mV
vs Temperature	–25°C < T < +85°C (AM, BM)		±10	±65				μV/°C
	–55°C < T < +125°C (RM, SM)					±10	±40	μV/°C
vs Supply Voltage			±35			*		μV/V
INPUT BIAS CURRENT								
Initial	$T_{CASE} = +25°C$		15	40		*	20	nA
vs Temperature			±0.05			*		nA/°C
vs Supply Voltage			±0.02			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	$T_{CASE} = +25°C$		±5	±10		±2	±3	nA
vs Temperature	–25°C < T < +85°C (AM, BM)		±0.01					nA/°C
	–55°C < T < +125°C (RM, SM)					±0.01		nA/°C
OPEN-LOOP GAIN, DC	$R_L = 5\Omega$ (RM, AM)	94	115					dB
$R_L = 6.5\Omega$ (SM, BM)					98	115		dB
INPUT IMPEDANCE								
Differential			10			*		MΩ
Common-mode			250			*		MΩ
INPUT NOISE								
Voltage Noise	$f_n = 0.3Hz$ to 10Hz		3			*		μVp-p
$f_n = 10Hz$ to 10kHz		5			*		μVrms	
Current Noise	$f_n = 0.3Hz$ to 10Hz		20			*		pAp-p
$f_n = 10Hz$ to 10kHz		4.5			*		pArms	
INPUT VOLTAGE RANGE								
Common-mode Voltage(4)	Linear Operation	$±(\lvert V_S\rvert–6)$	$±(\lvert V_S\rvert–3)$		*	*		V
Common-mode Rejection	f = DC, $V_{CM} = ±(\lvert V_S\rvert–6)$	70	110		80	*		dB
POWER SUPPLY								
Rated Voltage			±28			±34		V
Operating Voltage Range		±10		±36	*		±40	V
Current, quiescent			±2.6	±10		*	*	mA
TEMPERATURE RANGE	case							
Specification, RM, SM		–55		+125	*		*	°C
AM, BM		–25		+85	*		*	°C
Operating, derated performance, AM, BM		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
THERMAL RESISTANCE	Steady State θ_{JC}		2.0	2.2		*	*	°C/W

*Specification same as for OPA501RM, AM.

NOTES: (1) Package must be derated based on a junction-to-case thermal resistance of 2.2°C/W or a junction-to-ambient thermal resistance of 30°C/W. (2) Safe Operating Area and Power Derating Curves must be observed. (3) With $±R_{SC} = 0$. Peak output current is typically greater than 10A if duty cycle and pulse width limitations are observed. Output current greater than 10A is not guaranteed. (4) The absolute maximum voltage is 3V less than supply voltage.

Power Supply Voltage (V_S)	±40V
Power Dissipation at +25°C(1, 2)	79W
Differential Input Voltage	$\pm V_S - 3V$
Common-Mode Input Voltage	$\pm V_S$
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+200°C
Output Short-Circuit Duration(3)	Continuous

NOTES: (1) At case temperature of +25°C. Derate at 2.2°C/W above case temperature of +25°C. (2) Average dissipation. (3) Within safe operating area and with appropriate derating.



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA501AM	8-Pin Metal TO-3	–25°C to +85°C
OPA501BM	8-Pin Metal TO-3	–25°C to +85°C
OPA501RM	8-Pin Metal TO-3	–55°C to +125°C
OPA501SM	8-Pin Metal TO-3	–55°C to +125°C

PACKAGE INFORMATION

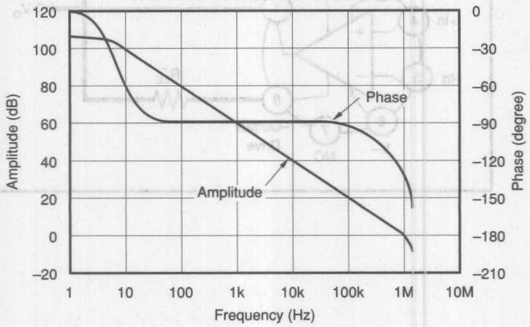
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA501AM	8-Pin Metal TO-3	030
OPA501BM	8-Pin Metal TO-3	030
OPA501RM	8-Pin Metal TO-3	030
OPA501SM	8-Pin Metal TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

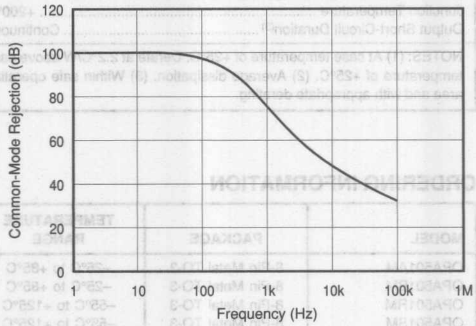
TYPICAL PERFORMANCE CURVES

Typical at +25°C case and $\pm V_S$ = 28VDC, unless otherwise noted.

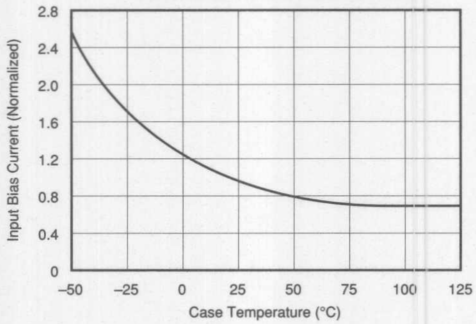
OPEN-LOOP FREQUENCY RESPONSE



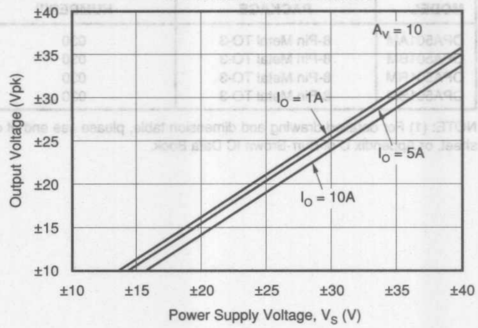
COMMON MODE REJECTION vs FREQUENCY



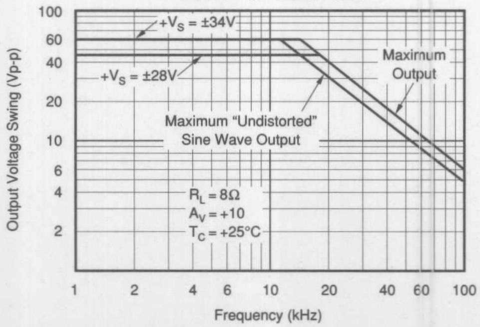
INPUT BIAS CURRENT vs TEMPERATURE



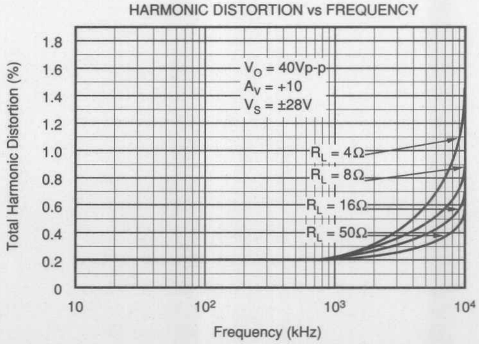
OUTPUT VOLTAGE SWING vs POWER SUPPLY VOLTAGE



FULL POWER RESPONSE



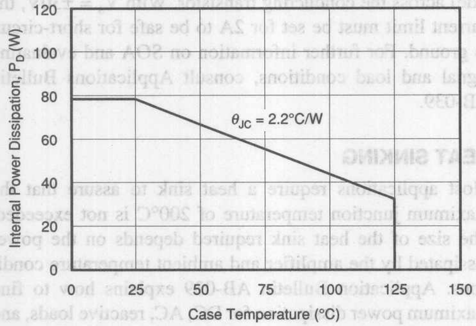
HARMONIC DISTORTION vs FREQUENCY



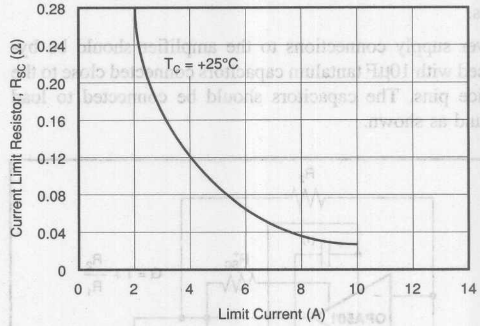
TYPICAL PERFORMANCE CURVES (CONT)

Typical at +25°C case and $\pm V_S$ = 28VDC, unless otherwise noted.

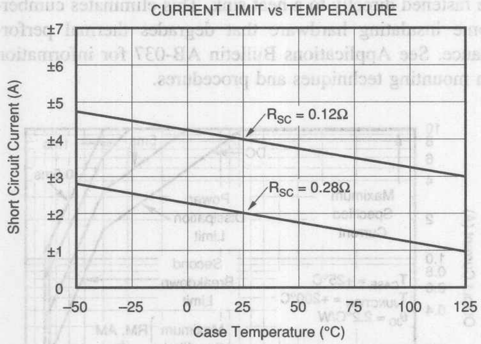
POWER DERATING CURVE



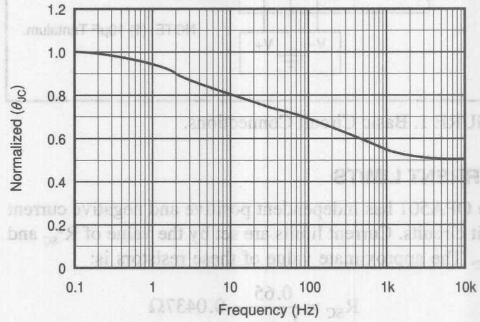
CURRENT LIMIT RESISTOR vs LIMIT CURRENT



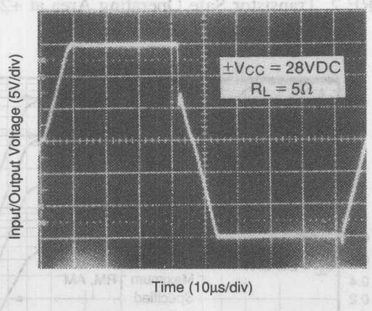
CURRENT LIMIT vs TEMPERATURE



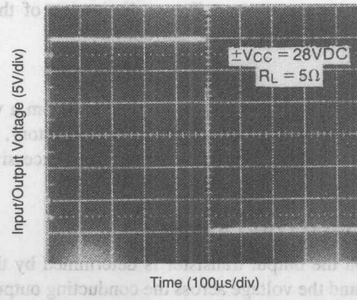
NORMALIZED THERMAL RESISTANCE vs FREQUENCY



PULSE RESPONSE, A_v = +1



PULSE RESPONSE, A_v = +1



Grounding techniques can greatly affect the performance of a power op amp. Figure 1 shows grounds connected so that load current does not flow through signal ground connections. Power supply and load connections should be physically separated from the amplifier input and signal connections.

Power supply connections to the amplifier should be bypassed with 10µF tantalum capacitors connected close to the device pins. The capacitors should be connected to load ground as shown.

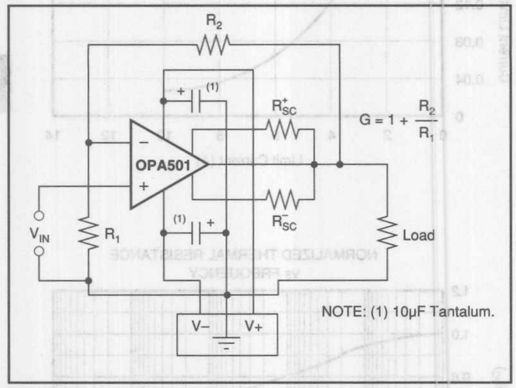


FIGURE 1. Basic Circuit Connections.

CURRENT LIMITS

The OPA501 has independent positive and negative current limit circuits. Current limits are set by the value of R^+_{SC} and R^-_{SC}. The approximate value of these resistors is:

$$R_{SC} = \frac{0.65}{I_{LIMIT}} - 0.0437\Omega$$

I_{LIMIT} is the desired maximum current at room temperature in Amperes and R_{SC} is in ohms. The current limit value decreases with increasing temperature—see typical performance curves. The current limit resistors conduct the full amplifier output current. Power dissipation of the current limit resistors at maximum current is:

$$P_{MAX} = (I_{LIMIT})^2 R_{SC}$$

The current limit resistors can be chosen from a variety of types. Most wire-wound types are satisfactory, although some physically large resistors may have excessive inductance which can cause instability.

SAFE OPERATING AREA

Stress on the output transistor is determined by the output current and the voltage across the conducting output transistor. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, V_{CE}. The Safe Operating Area (SOA), rent. SOA is reduced at high operating temperature—see Figure 3.

The safe output current decreases as V_{CE} increases. Output short-circuits are very demanding. A short-circuit to ground forces the full power supply voltage (positive or negative side) across the conducting transistor. With $V_S = \pm30V$, the current limit must be set for 2A to be safe for short-circuit to ground. For further information on SOA and evaluating signal and load conditions, consult Applications Bulletin AB-039.

HEAT SINKING

Most applications require a heat sink to assure that the maximum junction temperature of 200°C is not exceeded. The size of the heat sink required depends on the power dissipated by the amplifier and ambient temperature conditions. Application Bulletin AB-039 explains how to find maximum power dissipation for DC, AC, reactive loads, and other conditions. Applications Bulletin AB-038 shows how to determine heat sink requirements.

The case of the OPA501 is isolated from all circuitry and can be fastened directly to a heat sink. This eliminates cumbersome insulating hardware that degrades thermal performance. See Applications Bulletin AB-037 for information on mounting techniques and procedures.

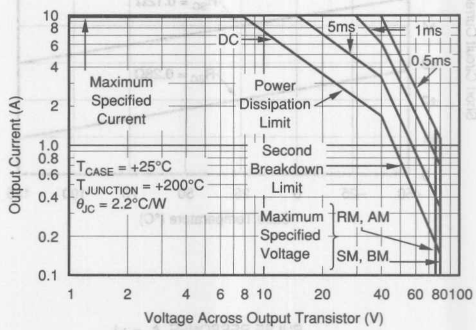


FIGURE 2. Transistor Safe Operating Area at +25°C Case Temperature.

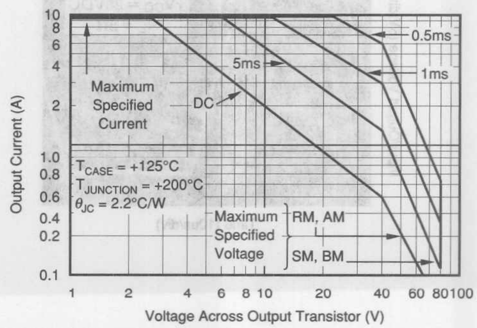
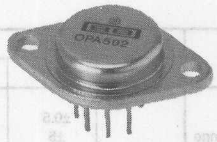


FIGURE 3. Transistor Safe Operating Area at +125°C Case Temperature.

BURR - BROWN®



OPA502

High Current, High Power OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: 10A
- WIDE POWER SUPPLY VOLTAGE: ±10V to ±45V
- USER-SET CURRENT LIMIT
- SLEW RATE: 10V/μs
- FET INPUT: I_B = 200pA max
- CLASS A/B OUTPUT STAGE
- QUIESCENT CURRENT: 25mA max
- HERMETIC TO-3 PACKAGE — ISOLATED CASE

APPLICATIONS

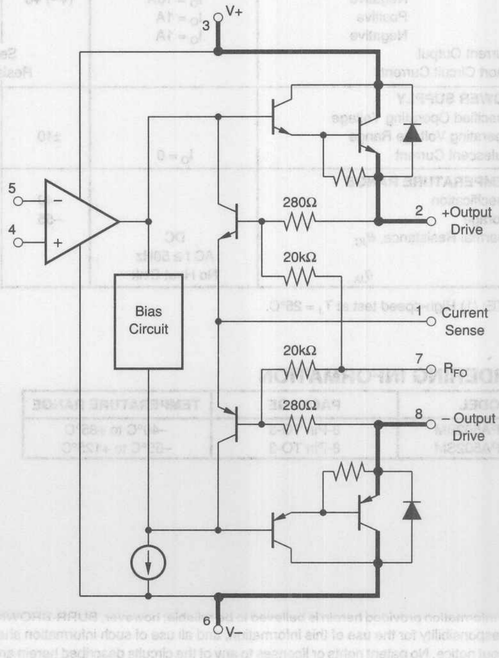
- MOTOR DRIVER
- SERVO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY
- ACTUATOR DRIVER
- AUDIO AMPLIFIER
- TEST EQUIPMENT

DESCRIPTION

The OPA502 is a high output current operational amplifier designed to drive a wide range of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from crossover distortion. Resistor-programmable current limits provide protection for both the amplifier and the load during abnormal operating conditions. An adjustable foldover current limit can also be used to protect against potentially damaging conditions.

The OPA502 employs a custom monolithic op amp/ driver circuit and rugged complementary output transistors, providing excellent DC and dynamic performance.

The industry-standard 8-pin TO-3 package is electrically isolated from all circuitry. This allows the OPA502 to be mounted directly to a heat sink without cumbersome insulating hardware which degrade thermal performance. The OPA502 is available in –40°C to +85°C and –55°C to +125°C temperature ranges.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, V_S = ±40V unless otherwise noted.

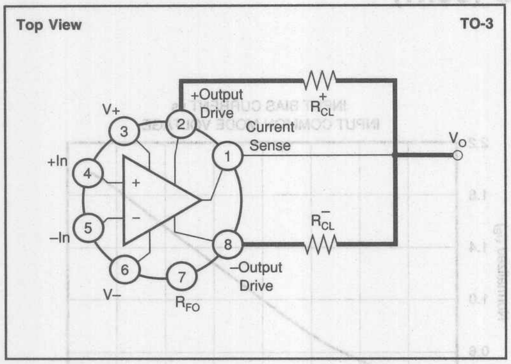
		OPA502BM			OPA502SM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE								
Input Offset Voltage			±0.5	±5		*	*	mV
vs Temperature	Specified Temp. Range		±5			*		μV/°C
vs Power Supply	V_S = ±10V to ±45V	74	92		*	*		dB
INPUT BIAS CURRENT(1)								
Input Bias Current	V_{CM} = 0V		12	200		*	*	pA
Input Offset Current	V_{CM} = 0V		±3			*		pA
NOISE								
Input Voltage Noise								
Noise Density,	f = 1kHz		25			*		$nV/\sqrt{Hz}$
Current Noise Density,	f = 1kHz		3			*		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE								
Common-Mode Input Range, Positive	Linear Operation	(V+) –5	(V+) –4		*	*		V
Negative	Linear Operation	(V–) +5	(V–) +4		*	*		V
Common-Mode Rejection	V_{CM} = ±35V	74	106		*	*		dB
INPUT IMPEDANCE								
Differential			10^{12} || 5			*		Ω || pF
Common-Mode			10^{12} || 4			*		Ω || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±34V, R_L = 6Ω	92	103		*	*		dB
FREQUENCY RESPONSE								
Gain-Bandwidth Product	G = +10, R_L = 50Ω		2.0			*		MHz
Slew Rate	68Vp-p, R_L = 6Ω	5	10		*	*		V/μs
Full-Power Bandwidth			See Typical Curves					
Total Harmonic Distortion	G = +3, f = 20kHz V_O = 20V, R_L = 8Ω		0.06			*		%
Capacitive Load			See Figure 6					
OUTPUT								
Voltage Output, Positive	I_O = 10A	(V+) –6	(V+)–3.5		*	*		V
Negative	I_O = 10A	(V–) +6	(V–) +3.6		*	*		V
Positive	I_O = 1A		(V+) –2.5			*		V
Negative	I_O = 1A		(V–) +3.1			*		V
Current Output			See SOA Curves					
Short Circuit Current			Resistor Programmed					
POWER SUPPLY								
Specified Operating Voltage			±40			*		V
Operating Voltage Range		±10		±45	*		*	V
Quiescent Current	I_O = 0		±20	±25		*	*	mA
TEMPERATURE RANGE								
Specification		–40		+85	–55		+125	°C
Storage		–55		+125	*		*	°C
Thermal Resistance, θ_{JC}	DC		1.25	1.4		*		°C/W
	AC f ≥ 50Hz		0.8	0.9		*		°C/W
θ_{JA}	No Heat Sink		30			*		°C/W

NOTE: (1) High-speed test at T_J = 25°C.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA502BM	8-Pin TO-3	–40°C to +85°C
OPA502SM	8-Pin TO-3	–55°C to +125°C

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	90V
Output Current	See SOA Curve
Input Voltage	(V–) –1V to (V+)+1V
Case Temperature, Operating	150°C
Junction Temperature	200°C

PACKAGE INFORMATION

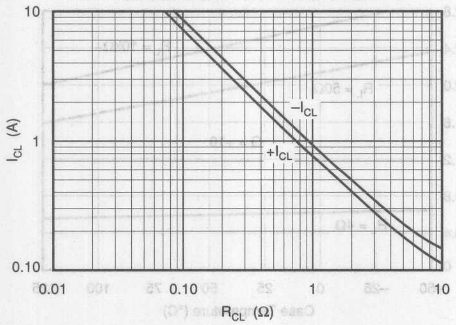
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[(1)]
OPA502BM	8-Pin TO-3	030
OPA502SM	8-Pin TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

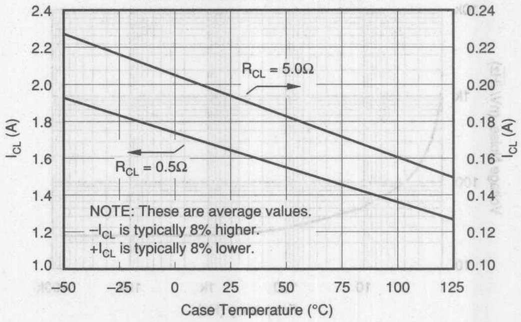
TYPICAL PERFORMANCE CURVES

T_{CASE} = +25°C, V_S = ±40V unless otherwise noted.

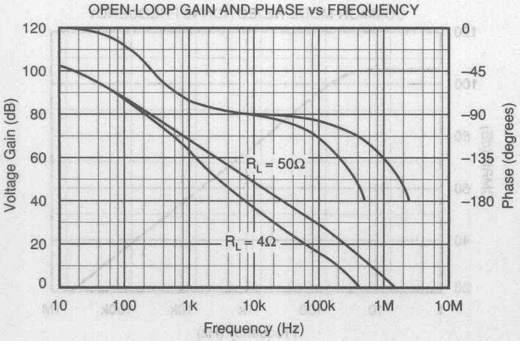
CURRENT LIMIT vs LIMIT RESISTOR



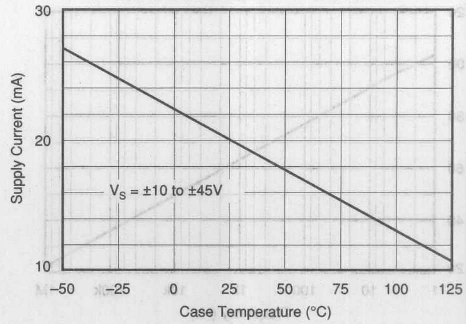
CURRENT LIMIT vs TEMPERATURE



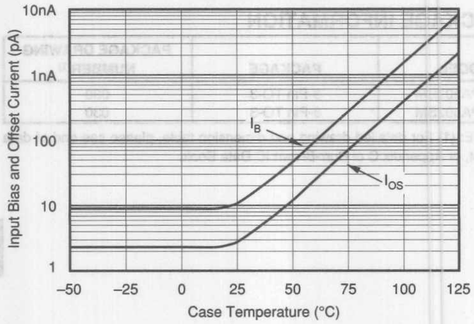
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



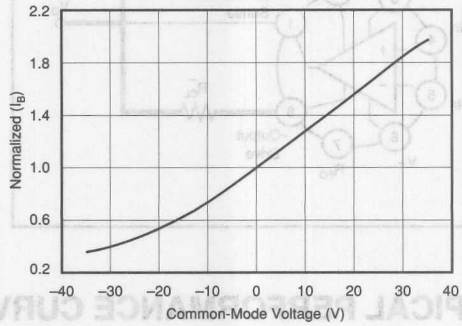
SUPPLY CURRENT vs TEMPERATURE



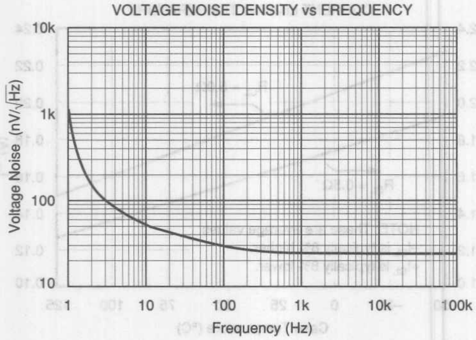
INPUT BIAS AND OFFSET CURRENTS
vs TEMPERATURE



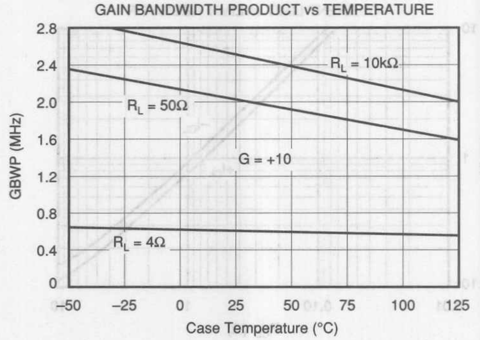
INPUT BIAS CURRENT vs
INPUT COMMON-MODE VOLTAGE



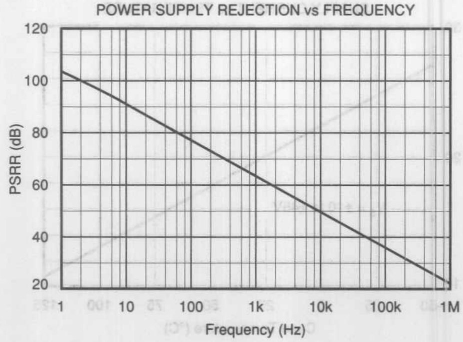
VOLTAGE NOISE DENSITY vs FREQUENCY



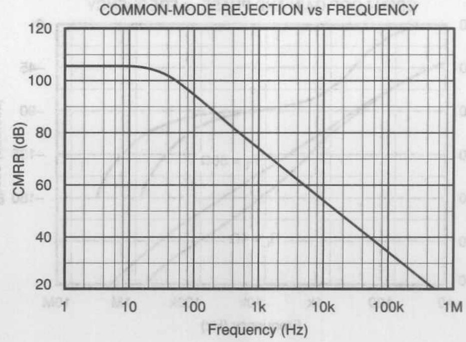
GAIN BANDWIDTH PRODUCT vs TEMPERATURE



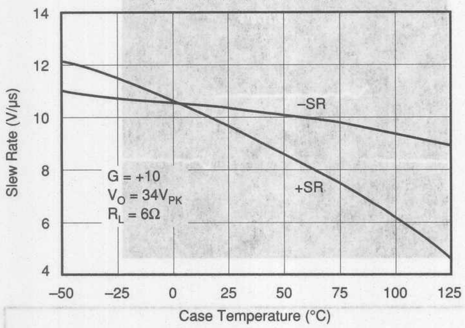
POWER SUPPLY REJECTION vs FREQUENCY



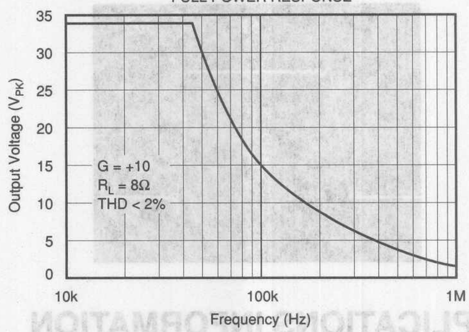
COMMON-MODE REJECTION vs FREQUENCY



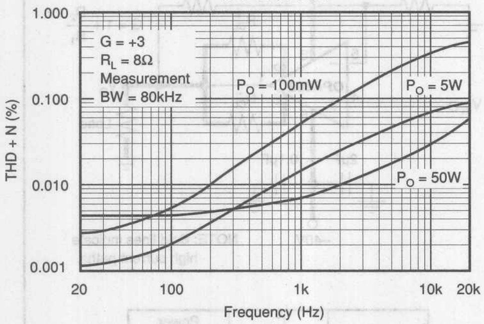
SLEW RATE vs TEMPERATURE



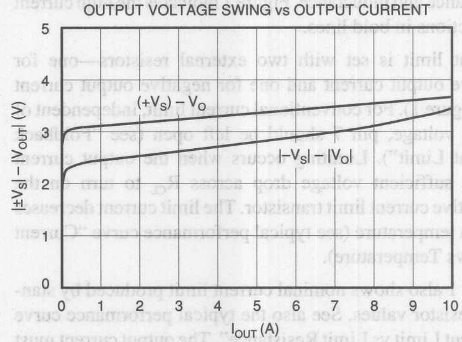
FULL POWER RESPONSE



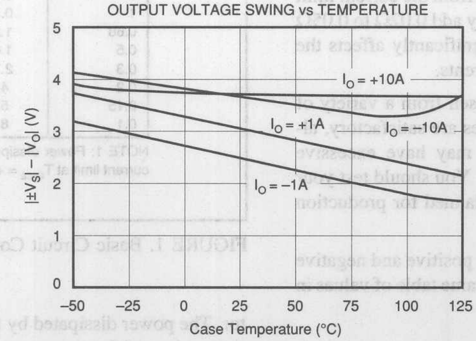
TOTAL HARMONIC DISTORTION AND NOISE vs FREQUENCY



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



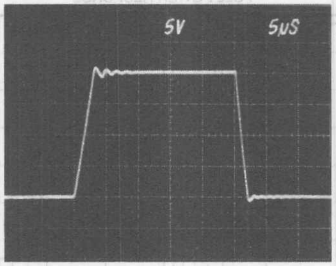
OUTPUT VOLTAGE SWING vs TEMPERATURE



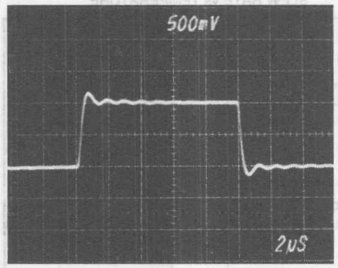
TYPICAL PERFORMANCE CURVES (CONT)

T_{CASE} = +25°C, V_S = ±40V unless otherwise noted.

LARGE SIGNAL RESPONSE
G = +3, R_L = 4Ω



SMALL SIGNAL RESPONSE
G = +3, C_L = 1000pF



APPLICATIONS INFORMATION

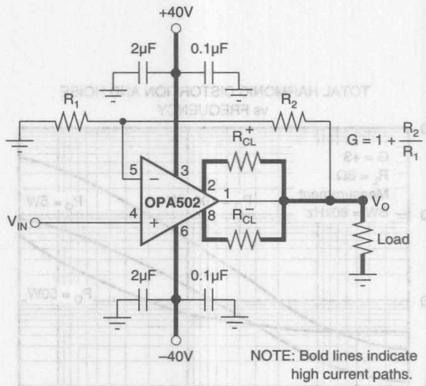
Power supply terminals should be bypassed with low series impedance capacitors such as ceramic or tantalum close to the device pins. Power supply wiring should have low series impedance and inductance. Figure 1 indicates the high current connections in bold lines.

Current limit is set with two external resistors—one for positive output current and one for negative output current (see Figure 1). For conventional current limit, independent of output voltage, pin 7 should be left open (see "Foldback Current Limit"). Limiting occurs when the output current causes sufficient voltage drop across R_{CL} to turn on the respective current limit transistor. The limit current decreases at high temperature (see typical performance curve "Current Limit vs Temperature).

Figure 1 also shows nominal current limit produced by standard resistor values. See also the typical performance curve "Current Limit vs Limit Resistance". The output current must flow through this resistor, so its power rating must be chosen accordingly. The table in Figure 1 shows the power dissipation of the current limit resistor during continuous current limit (room temperature). Connections from the current limit resistors to the device pins can typically add 0.02Ω to 0.05Ω to the effective value of R_{CL}. This significantly affects the current limit value for high output currents.

The current limit resistors can be chosen from a variety of types. Most common wire-wound types are satisfactory, although some physically large types may have excessive inductance which can cause problems. You should test your circuits with the exact resistor type planned for production use.

You can set different current limits for positive and negative current. Resistors are chosen with the same table of values in Figure 1.



R_{CL} (Ω)	I_{CL} at 25°C (A)	Power Dissipation[1] of R_{CL} (W)
10	0.11	0.12
5	0.19	0.18
2	0.44	0.39
1	0.78	0.61
0.68	1.22	1.0
0.5	1.65	1.4
0.3	2.73	2.2
0.2	4.0	3.2
0.15	5.4	4.4
0.1	8.1	6.6

NOTE 1: Power dissipation during continuous current limit at T_{CASE} = +25°C.

FIGURE 1. Basic Circuit Connections.

SAFE OPERATING AREA

Stress on the output transistors is determined by the output current and the voltage across the conducting output transistor. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, V_{CE}. The Safe Operating Area (SOA curve, Figure 2) shows the permissible range of voltage and current.

The safe output current decreases as V_{CE} increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage (V+ or V–) across the conducting transistor. With $V_S = \pm 40V$ the current limit must be set for 3A (25°C) to be safe for continuous short-circuit to ground. For further insight on SOA, consult AB-039.

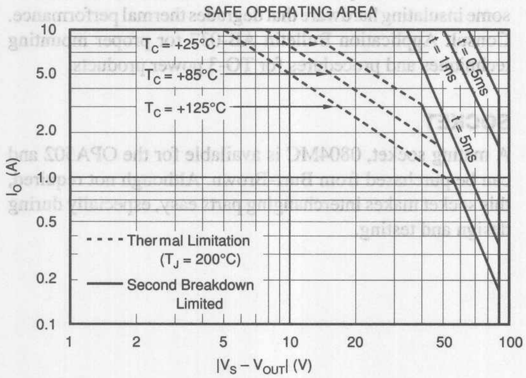


FIGURE 2. Safe Operating Area (SOA).

UNBALANCED POWER SUPPLIES

Some applications do not require equal positive and negative output voltage swing. The power supply voltages of the OPA502 do not need to be equal. Figure 3 shows a circuit designed for a positive output voltage and current. The –5V power supply voltage assures that the inputs of the OPA502 are operated within their linear common-mode range. The V+ power supply could range from 15V to 85V. The total voltage (V– to V+) can range from 20V to 90V.

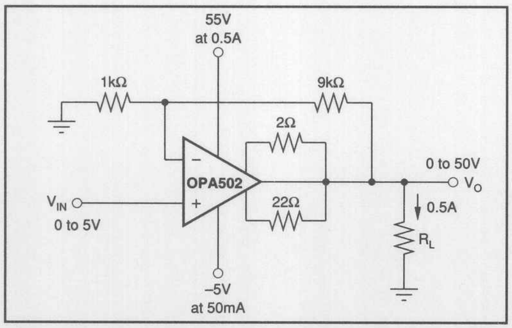


FIGURE 3. Unbalanced Power Supplies.

FOLDOVER CURRENT LIMIT

By connecting a resistor from pin 7 to ground, you can make the limit current vary with output voltage. The foldover limit circuit can be set to allow high output current when V_{CE} is low (high output voltage). Output current limits at a lower value under the more stressful condition when V_{CE} is high, (output voltage is low).

The behavior of this voltage-dependant current limit is described by the following equation.

$$I_{LIMIT} = \frac{0.81 + \left(\frac{0.28\,V_O}{R_{FO} + 20}\right)}{R_{CL}} + 0.03$$

where: V_O is the output voltage measured with respect to ground.

R_{FO} is the resistor connected from pin 7 to ground (in k ohms).

R_{CL} is the current limit resistor (in ohms).

The foldover limit circuitry can be set to allow large voltage and current to resistive loads, yet limit output current to a safe value with an output short circuit.

Reactive or EMF-generating loads can produce unexpected behavior with the foldover circuit driven into limiting. With a reactive load, peak output current occurs at low or zero output voltage. Compared to a resistive load, a reactive load with the same total impedance will be more likely to activate the foldover limit circuitry.

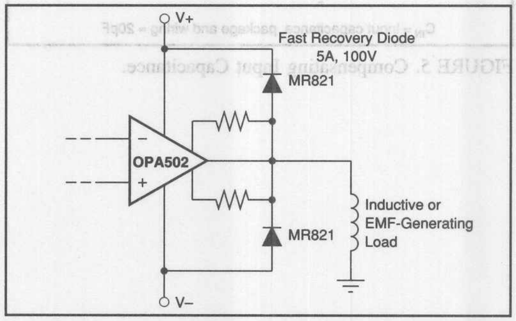


FIGURE 4. Diode Protection of Output.

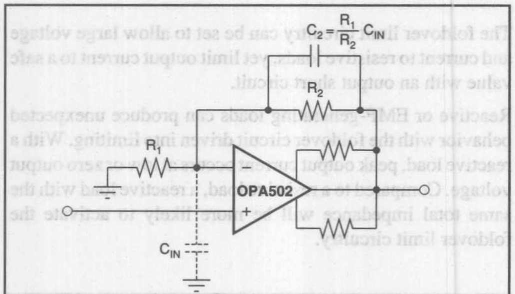
OUTPUT PROTECTION

The output stage of the OPA502 is protected by internal diode clamps to the power supply terminals. These internal diodes are similar to common silicon rectifier types and may not be fast enough for adequate protection. For loads that can deliver large reverse kickback current (greater than 5A) to the output, external fast-recovery clamp diodes are recommended (Figure 4). For these diodes (internal or external) to provide the intended protection, the power supplies must provide a low impedance to a reverse current.

pulse response ringing, and in severe cases, oscillations. A low value feedback capacitor can reduce or eliminate this effect by maintaining a constant feedback factor at high frequency (see Figure 5).

Depending on the load conditions, precautions may be required when using the OPA502 in low gains. Gains less than +3V/V or –2V/V may cause oscillations, particularly with capacitive loads. Figure 6 shows several circuits for low gain and capacitive loads.

Large value feedback capacitors used to limit the closed-loop bandwidth or form an integrator may also produce instability because the closed-loop gain approaches unity at high frequency.



C_{IN} = Input capacitance, package and wiring ≈ 20pF

FIGURE 5. Compensating Input Capacitance.

required depends on the power dissipated and on ambient conditions. Consult Application Bulletin AB-038 for information on determining heat sink requirements.

The case of the OPA502 is isolated from all circuitry and can be fastened directly to a heat sink. This eliminates cumbersome insulating hardware that degrades thermal performance. Consult Application Bulletin AB-037 for proper mounting techniques and procedures for TO-3 power products.

SOCKET

A mating socket, 0804MC is available for the OPA502 and can be purchased from Burr-Brown. Although not required, this socket makes interchanging parts easy, especially during design and testing.

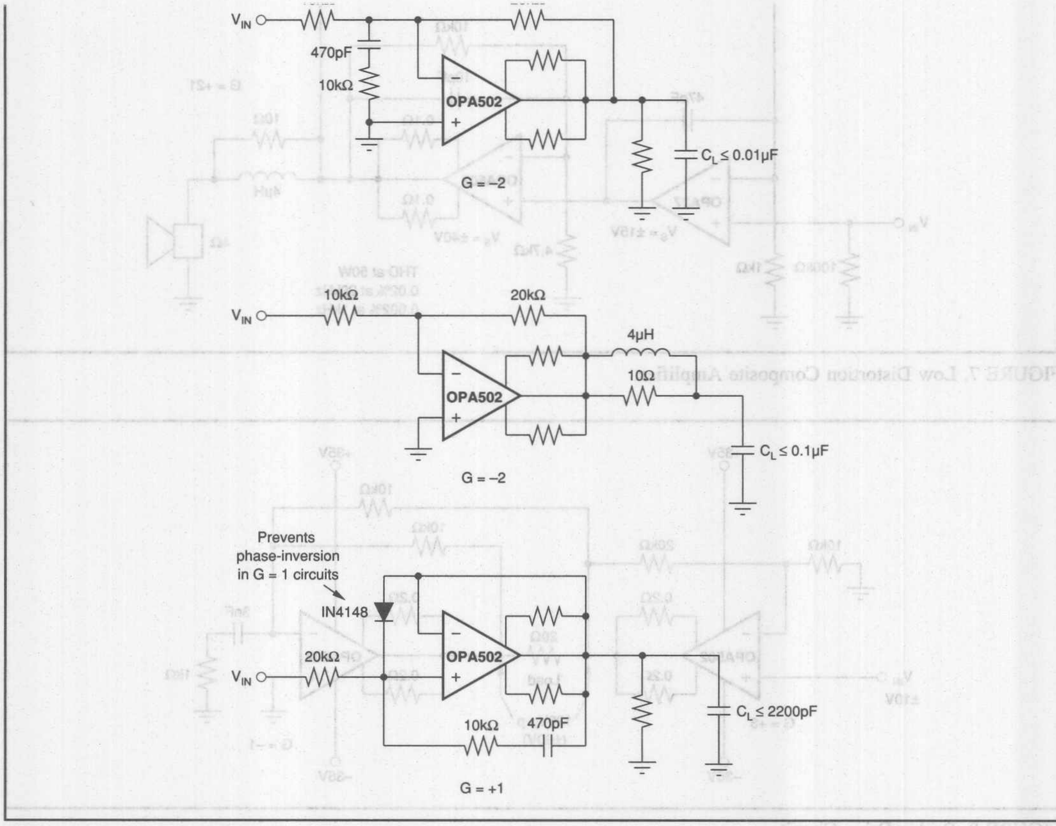


FIGURE 6. Compensation Circuits.

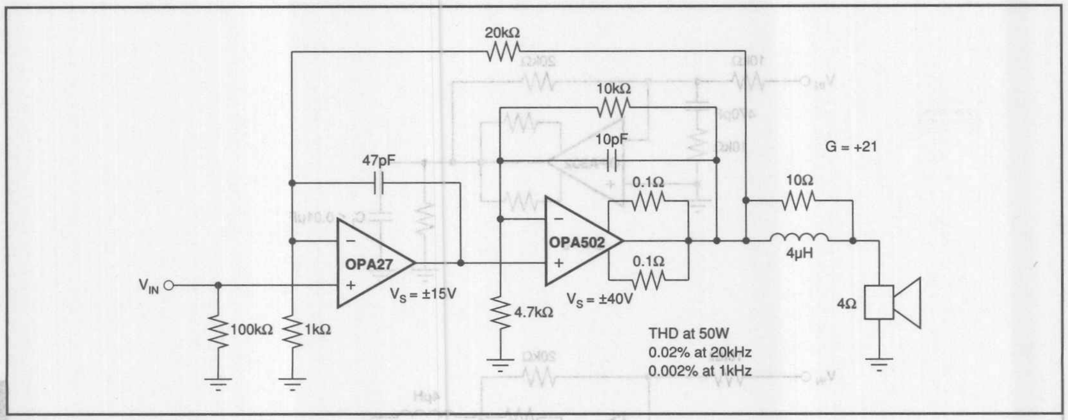


FIGURE 7. Low Distortion Composite Amplifier.

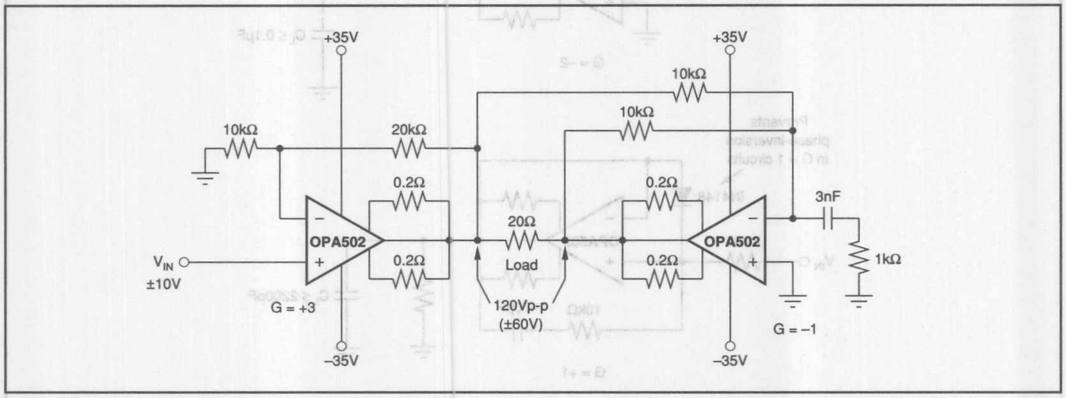


FIGURE 8. Bridge Drive Circuit.

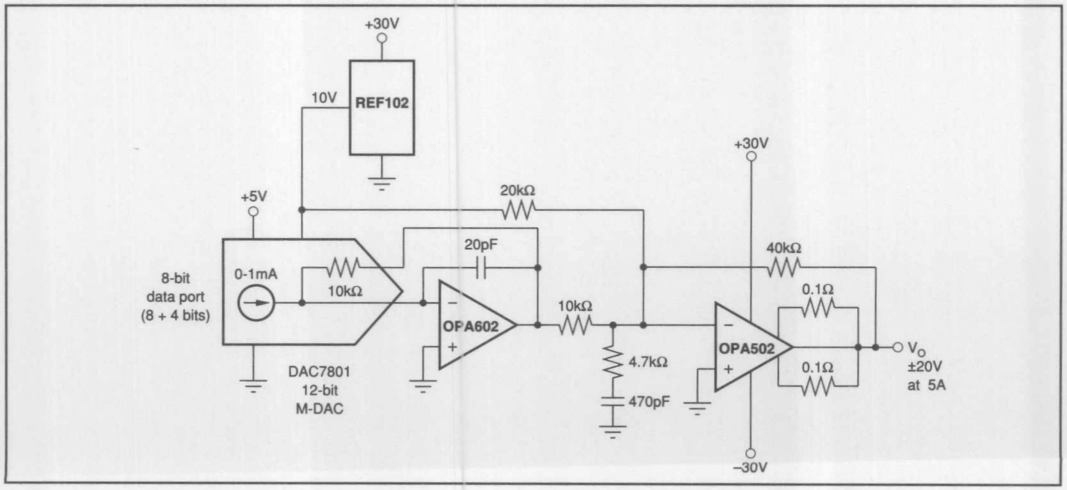
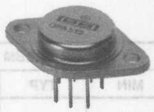


FIGURE 9. Digitally Programmable Power Supply.

BURR - BROWN®



OPA512

Very-High Current—High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE: ±10V to ±50V
- HIGH OUTPUT CURRENT: 15A Peak
- CLASS A/B OUTPUT STAGE: Low Distortion
- VOLTAGE-CURRENT LIMIT PROTECTION CIRCUIT
- SMALL TO-3 PACKAGE

APPLICATIONS

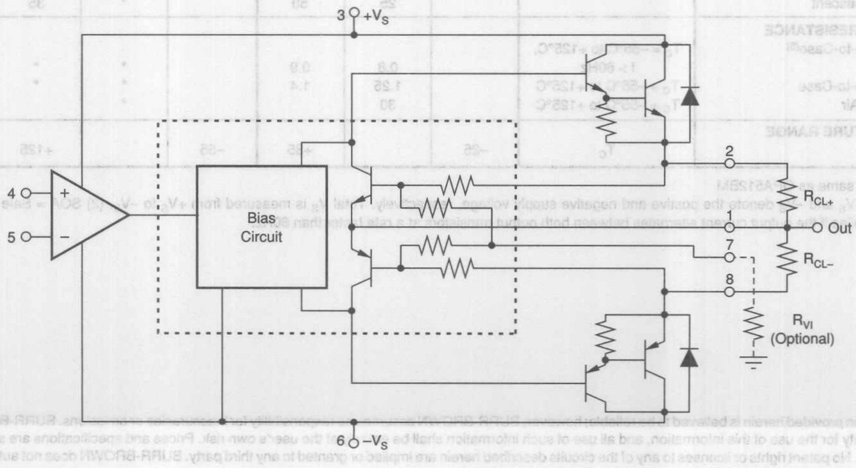
- SERVO AMPLIFIER
- MOTOR DRIVER
- SYNCRO EXCITATION
- AUDIO AMPLIFIER
- TEST PIN DRIVER

DESCRIPTION

The OPA512 is a high voltage, very-high current operational amplifier designed to drive a wide variety of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from cross-over distortion. User-set current limit circuitry provides protection to the amplifier and load in fault conditions. A resistor-programmable voltage-current limiter circuit may be used to further protect the amplifier from damaging conditions.

The OPA512 employs a laser-trimmed monolithic integrated circuit to bias the output transistors, providing excellent low-level signal fidelity and high output voltage swing. The reduced internal parts count made possible with this monolithic IC improves performance and reliability.

This hybrid integrated circuit is housed in a hermetic TO-3 package and all circuitry is electrically-isolated from the case. This allows direct mounting to a chassis or heat sink without cumbersome insulating hardware and provides optimum heat transfer.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At $T_C = +25°C$, and $V_S = ±40V$, unless otherwise noted.

		OPA512BM			OPA512SM			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT OFFSET VOLTAGE								
Initial Offset			±2	±6		±1	±3	mV
vs Temperature	Specified Temp. Range		±10	±65		*	±40	µV/°C
vs Supply Voltage			±30	±200		*	*	µV/V
vs Power			±20			*		µV/V
INPUT BIAS CURRENT								
Initial			12	30		10	20	nA
vs Temperature	Specified Temp. Range		±50	400		*	*	pA/°C
vs Supply Voltage			±10			*		pA/V
INPUT OFFSET CURRENT								
Initial			±12	±30		±5	±10	nA
vs Temperature	Specfied Temp. Range		±50			*		pA/°C
INPUT IMPEDANCE, DC			200			*		MΩ
INPUT CAPACITANCE			3			*		pF
VOLTAGE RANGE								
Common-Mode Voltage	Specified Temp. Range	$±(\|V_S\|-5)$	$±(\|V_S\|-3)$		*	*		V
Common-Mode Rejection	Specified Temp. Range	74	100		*	*		dB
GAIN								
Open-Loop Gain at 10Hz	1kΩ Load		110			*		dB
	Specified Temp. Range 8Ω Load	96	108		*	*		dB
Gain-Bandwidth Product, 1MHz	8Ω Load		4			*		MHz
Power Bandwidth	8Ω Load	13	20		*	*		kHz
Phase Margin	Specified Temp. Range 8Ω Load		20			*		Degrees
OUTPUT								
Voltage Swing (1)	BM at 10A, SM at 15A	$±(\|V_S\|-6)$			$±(\|V_S\|-7)$			V
	Specified Temp. Range $I_O = 80mA$	$±(\|V_S\|-5)$			*			V
	$I_O = 5A$	$±(\|V_S\|-5)$			*			V
Current, Peak		10			15			A
Settling Time to 0.1%	2V Step		2			*		µs
Slew Rate		2.5	4		*	*		V/µs
Capacitive Load	Specified Temp. Range G = 1			1.5			*	nF
	Specified Temp. Range G > 10			SOA(2)			*	
POWER SUPPLY								
Voltage	Specified Temp. Range	±10	±40	±45	*	*	±50	V
Current, Quiescent			25	50		*	35	mA
THERMAL RESISTANCE								
AC Junction-to-Case(3)	$T_C = -55°C$ to $+125°C$, f > 60Hz		0.8	0.9		*	*	°C/W
DC Junction-to-Case	$T_C = -55°C$ to $+125°C$		1.25	1.4		*	*	°C/W
Junction to Air	$T_C = -55°C$ to $+125°C$		30			*		°C/W
TEMPERATURE RANGE								
Specified	T_C	–25		+85	–55		+125	°C

*Specification same as OPA512BM.

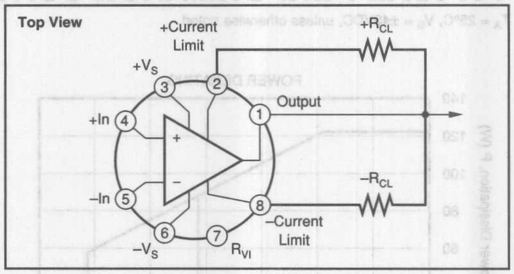
NOTES: (1) $+V_S$ and $-V_S$ denote the postive and negative supply voltage, respectively. Total V_S is measured from $+V_S$ to $-V_S$. (2) SOA = Safe Operating Area. (3) Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$	100V
Output Current: Source	15A
Sink	see SOA
Power Dissipation, Internal(1)	125W
Input Voltage: Differential	$\pm(\lvert V_S\rvert - 3V)$
Common-mode	$\pm V_S$
Temperature: Pins (soldering, 10s)	+300°C
Junction(1)	+200°C
Temperature Range: Storage(2)	–65°C to +150°C
Operating (Case)	–55°C to +125°C

NOTES: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. (2) OPA512BM, –55°C to +100°C.

CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA512BM	8-pin TO-3	–25°C to +85°C
OPA512SM	8-pin TO-3	–55°C to +125°C

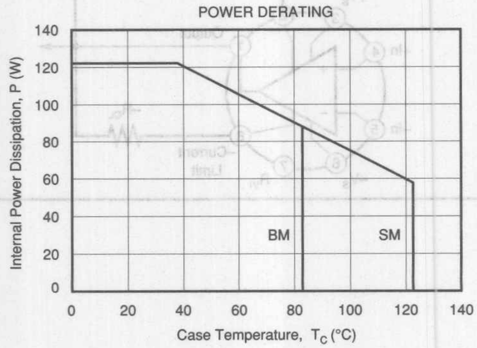
PACKAGE INFORMATION

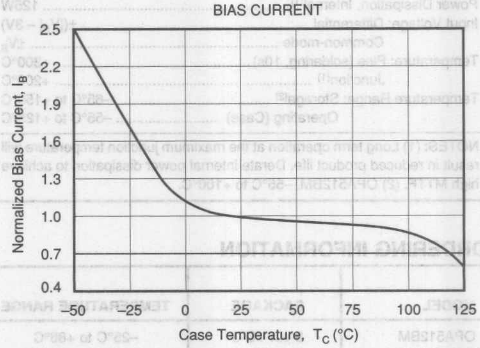
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA512BM	8-Pin TO-3	030
OPA512SM	8-Pin TO-3	030

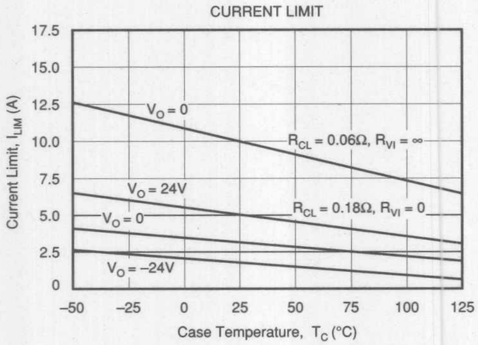
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

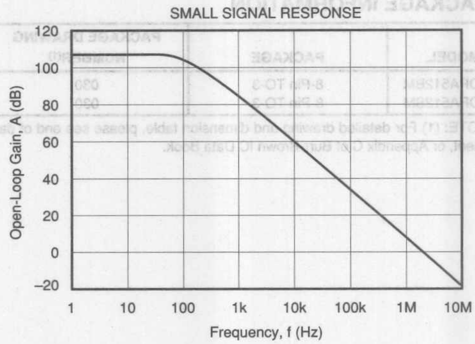
TYPICAL PERFORMANCE CURVES

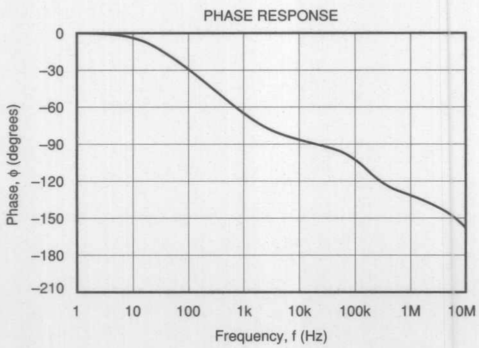
$T_A = 25°C$, $V_S = ±40VDC$, unless otherwise noted.

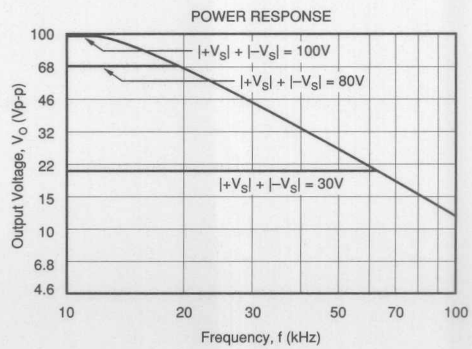






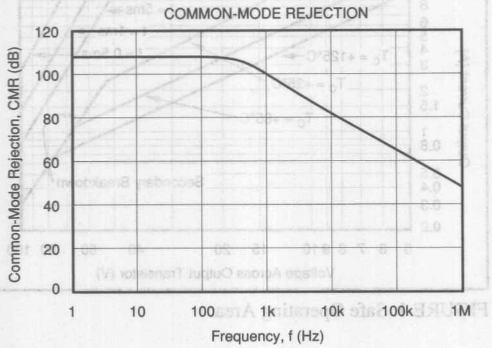


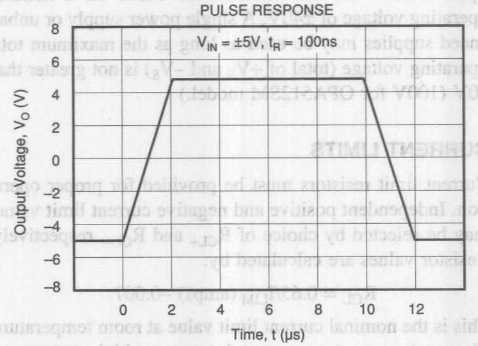


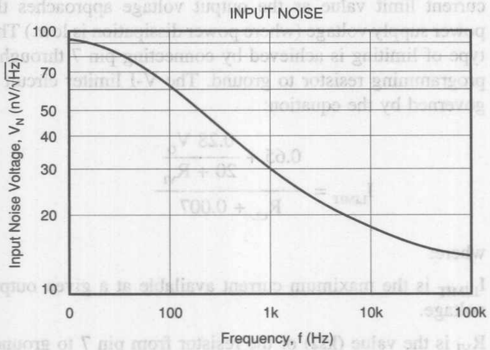


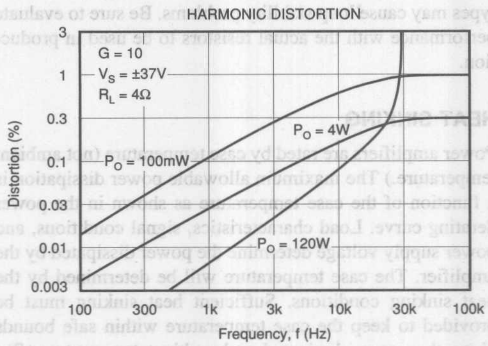
TYPICAL PERFORMANCE CURVES (CONT)

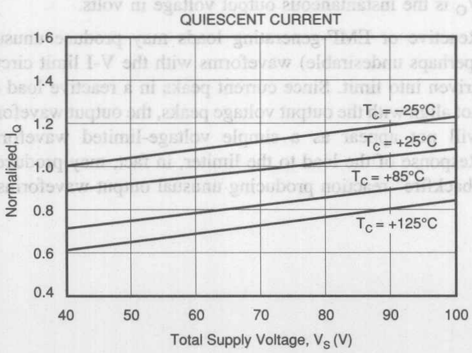
$T_A = 25°C$, $V_S = ±40VDC$, unless otherwise noted.

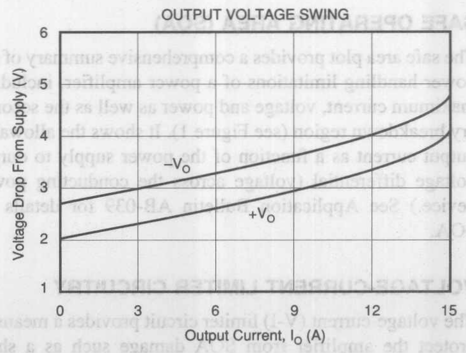












APPLICATIONS INFORMATION

POWER SUPPLIES

Specifications for the OPA512 are based on a nominal operating voltage of ±40V. A single power supply or unbalanced supplies may be used as long as the maximum total operating voltage (total of $+V_S$ and $-V_S$) is not greater than 90V (100V for OPA512SM model.)

CURRENT LIMITS

Current limit resistors must be provided for proper operation. Independent positive and negative current limit values may be selected by choice of R_{CL+} and R_{CL-}, respectively. Resistor values are calculated by:

$$R_{CL} = 0.65/I_{LIM} \text{ (amps)} - 0.007$$

This is the nominal current limit value at room temperature. The maximum output current decreases at high temperature as shown in the typical performance curve. Most wirewound resistors are satisfactory, but some highly inductive types may cause loop stability problems. Be sure to evaluate performance with the actual resistors to be used in production.

HEAT SINKING

Power amplifiers are rated by case temperature (not ambient temperature.) The maximum allowable power dissipation is a function of the case temperature as shown in the power derating curve. Load characteristics, signal conditions, and power supply voltage determine the power dissipated by the amplifier. The case temperature will be determined by the heat sinking conditions. Sufficient heat sinking must be provided to keep the case temperature within safe bounds given the power dissipated and ambient temperature. See Application Bulletin AB-038 for further details.

SAFE OPERATING AREA (SOA)

The safe area plot provides a comprehensive summary of the power handling limitations of a power amplifier, including maximum current, voltage and power as well as the secondary breakdown region (see Figure 1). It shows the allowable output current as a function of the power supply to output voltage differential (voltage across the conducting power device.) See Application Bulletin AB-039 for details on SOA.

VOLTAGE-CURRENT LIMITER CIRCUITRY

The voltage-current (V-I) limiter circuit provides a means to protect the amplifier from SOA damage such as a short circuit to ground, yet allows high output currents to flow

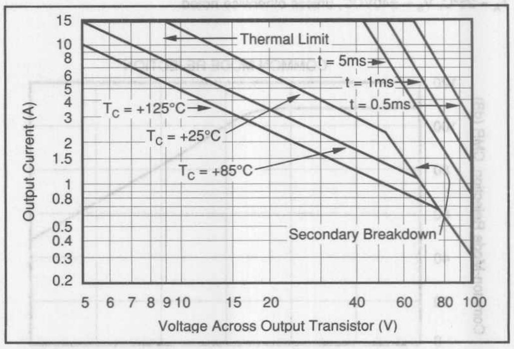


FIGURE 1. Safe Operating Area.

under normal load conditions. Sensing both the output current and the output voltage, this limiter circuit increases the current limit value as the output voltage approaches the power supply voltage (where power dissipation is low.) This type of limiting is achieved by connecting pin 7 through a programming resistor to ground. The V-I limiter circuit is governed by the equation:

$$I_{LIMIT} = \frac{0.65 + \dfrac{0.28\ V_O}{20 + R_{VI}}}{R_{CL} + 0.007}$$

where:

I_{LIMIT} is the maximum current available at a given output voltage.

R_{VI} is the value (kΩ) of the resistor from pin 7 to ground.

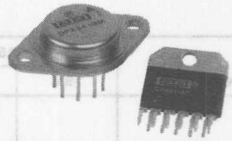
R_{CL} is the current limit resistor in ohms.

V_O is the instantaneous output voltage in volts.

Reactive or EMF-generating loads may produce unusual (perhaps undesirable) waveforms with the V-I limit circuit driven into limit. Since current peaks in a reactive load do not align with the output voltage peaks, the output waveform will not appear as a simple voltage-limited waveform. Response of the load to the limiter, in fact, may produce a "backfire" reaction producing unusual output waveforms.

BURR - BROWN®

OPA541



High Power Monolithic OPERATIONAL AMPLIFIER

FEATURES

- POWER SUPPLIES TO ±40V
- OUTPUT CURRENT TO 10A PEAK
- PROGRAMMABLE CURRENT LIMIT
- INDUSTRY-STANDARD PIN OUT
- FET INPUT
- TO-3 AND LOW-COST POWER PLASTIC PACKAGES

APPLICATIONS

- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCHRO EXCITATION
- AUDIO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY

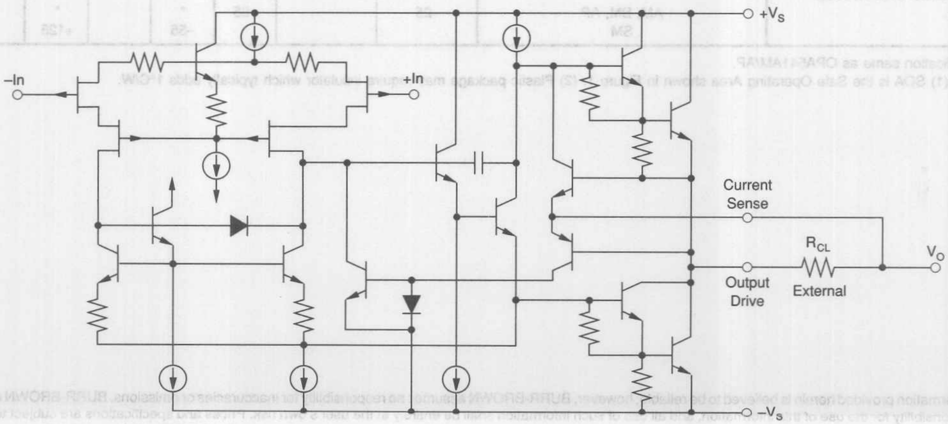
DESCRIPTION

The OPA541 is a power operational amplifier capable of operation from power supplies up to ±40V and delivering continuous output currents up to 5A. Internal current limit circuitry can be user-programmed with a single external resistor, protecting the amplifier and load from fault conditions. The OPA541 is fabricated using a proprietary bipolar/FET process.

Pinout is compatible with popular hybrid power amplifiers such as the OPA511, OPA512 and the 3573.

The OPA541 uses a single current-limit resistor to set both the positive and negative current limits. Applications currently using hybrid power amplifiers requiring two current-limit resistors need not be modified.

The OPA541 is available in an 11-pin power plastic package and an industry-standard 8-pin TO-3 hermetic package. The power plastic package has a copper-lead frame to maximize heat transfer. The TO-3 package is isolated from all circuitry, allowing it to be mounted directly to a heat sink without special insulators.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

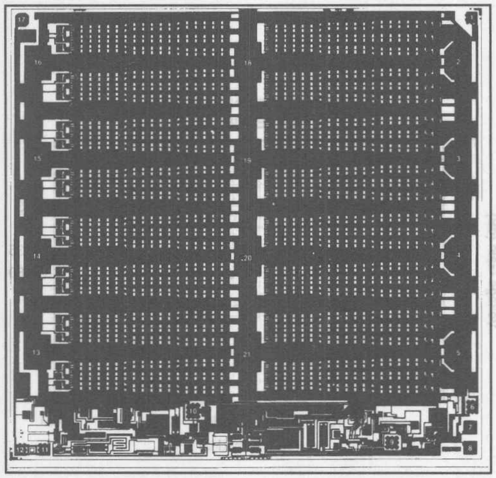
At T_C = +25°C and V_S = ±35VDC unless otherwise noted.

		OPA541AM/AP			OPA541BM/SM			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT OFFSET VOLTAGE								
V_{OS}			±2	±10		±0.1	±1	mV
vs Temperature	Specified Temperature Range		±20	±40		±15	±30	µV/°C
vs Supply Voltage	V_S = ±10V to ±V_{MAX}		±2.5	±10		*	*	µV/V
vs Power			±20	±60		*	*	µV/W
INPUT BIAS CURRENT								
I_B			4	50		*	*	pA
INPUT OFFSET CURRENT								
I_{OS}			±1	±30		*	*	pA
	Specified Temperature Range			5		*		nA
INPUT CHARACTERISTICS								
Common-Mode Voltage Range	Specified Temperature Range	±(|V_S| – 6)	±(|V_S| – 3)		*	*		V
Common-Mode Rejection	V_{CM} = (|±V_S| – 6V)	95	113		*	*		dB
Input Capacitance			5			*		pF
Input Impedance, DC			1			*		TΩ
GAIN CHARACTERISTICS								
Open Loop Gain at 10Hz	R_L = 6Ω	90	97		*	*		dB
Gain-Bandwidth Product			1.6			*		MHz
OUTPUT								
Voltage Swing	I_O = 5A, Continuous	±(|V_S| – 5.5)	±(|V_S| – 4.5)		*	*		V
	I_O = 2A	±(|V_S| – 4.5)	±(|V_S| – 3.6)		*	*		V
	I_O = 0.5A	±(|V_S| – 4)	±(|V_S| – 3.2)		*	*		V
Current, Peak		9	10		*	*		A
AC PERFORMANCE								
Slew Rate		6	10		*	*		V/µs
Power Bandwidth	R_L = 8Ω, V_O = 20Vrms	45	55		*	*		kHz
Settling Time to 0.1%	2V Step		2			*		µs
Capacitive Load	Specified Temperature Range, G = 1	3.3					*	nF
	Specified Temperature Range, G >10			SOA[1]			*	
Phase Margin	Specified Temperature Range, R_L = 8Ω		40			*		Degrees
POWER SUPPLY								
Power Supply Voltage, ±V_S	Specified Temperature Range	±10	±30	±35	*	±35	±40	V
Current, Quiescent			20	25		*	*	mA
THERMAL RESISTANCE								
θ_{JC} (Junction-to-Case)[2]	AC Output f > 60Hz		2.5					°C/W
θ_{JC}[2]	DC Output		3					°C/W
θ_{JA} (Junction-to-Ambient)	No Heat Sink		40					°C/W
OPA541AP (Plastic)			40					°C/W
TEMPERATURE RANGE								
T_{CASE}	AM, BM, AP	–25		+85	*		*	°C
	SM				–55		+125	°C

* Specification same as OPA541AM/AP.

NOTE: (1) SOA is the Safe Operating Area shown in Figure 1. (2) Plastic package may require insulator which typically adds 1°C/W.

DICE INFORMATION



OPA541 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	NC	11	NC
2	$-V_S$	12	Current Sense
3	$-V_S$	13	$+V_S$
4	$-V_S$	14	$+V_S$
5	$-V_S$	15	$+V_S$
6	NC	16	$+V_S$
7	–In	17	Current Sense
8	+In	18	Output Drive
9	NC	19	Output Drive
10	NC	20	Output Drive
		21	Output Drive

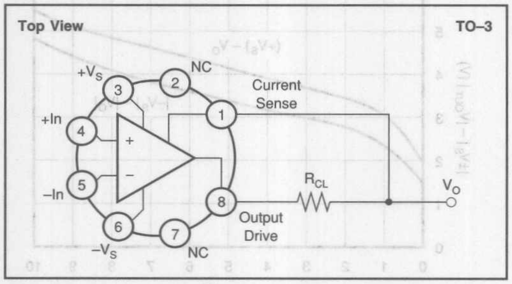
NOTE: For full output current capability, wire-bond all like connections of $+V_S$, $-V_S$ and Output Drive.

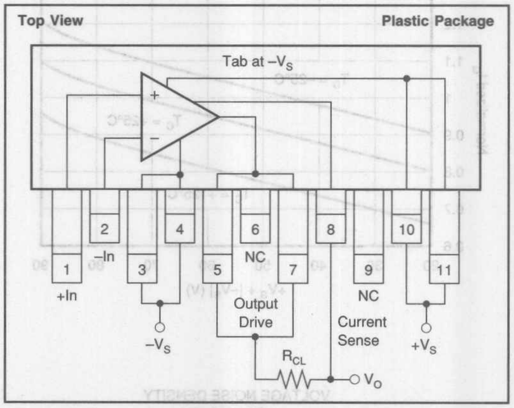
Substrate Bias: Electrically connected to $-V_S$ supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	213 x 205 ±5	5.41 x 5.21 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Chromium-Silver

CONNECTION DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 80V
Output Current .... see SOA
Power Dissipation, Internal[1] 125W
Input Voltage: Differential .... $\pm V_S$
Common-mode .... $\pm V_S$
Temperature: Pin solder, 10s .... +300°C
Junction[1] .... +150°C
Temperature Range:
AM, BM SM
Storage .... –65°C to +150°C
Operating (case) .... –55°C to +125°C
AP
Storage .... –40°C to +85°C
Operating (case) .... –25°C to +85°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

ORDERING INFORMATION

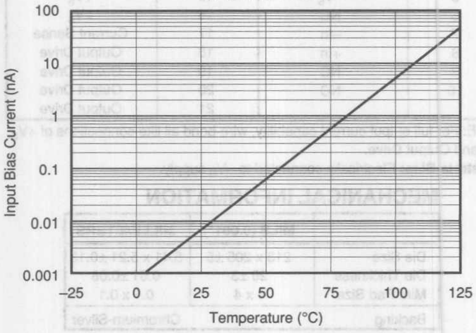
MODEL	PACKAGE	TEMPERATURE RANGE	CONTINUOUS CURRENT
OPA541AP	Power Plastic	–25°C to +85°C	5A at 25°C
OPA541AM	TO-3	–25°C to +85°C	5A at 25°C
OPA541BM	TO-3	–25°C to +85°C	5A at 25°C
OPA541SM	TO-3	–55°C to +125°C	5A at 25°C

PACKAGE INFORMATION

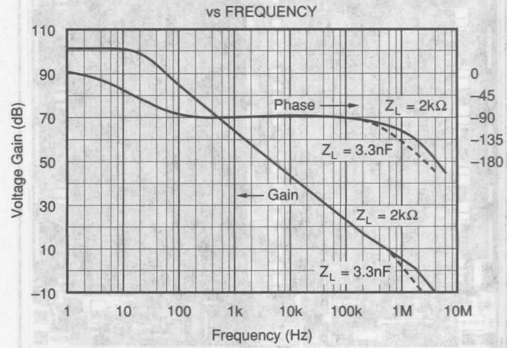
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA541AP	Power Plastic	242
OPA541AM	TO-3	030
OPA541BM	TO-3	030
OPA541SM	TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

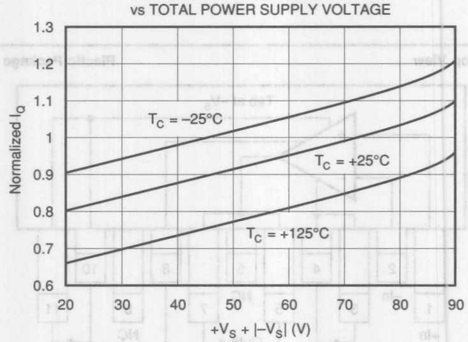
INPUT BIAS CURRENT
vs TEMPERATURE



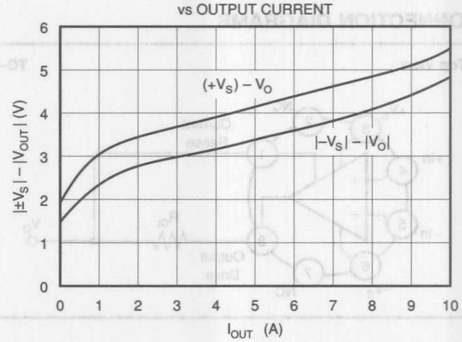
OPEN-LOOP GAIN AND PHASE
vs FREQUENCY



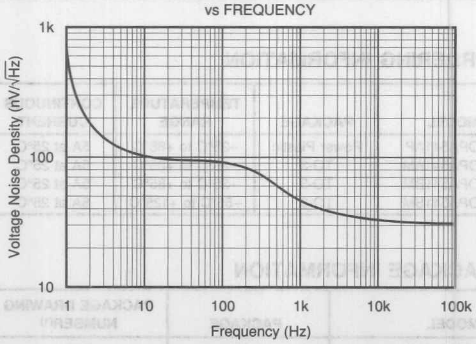
NORMALIZED QUIESCENT CURRENT
vs TOTAL POWER SUPPLY VOLTAGE



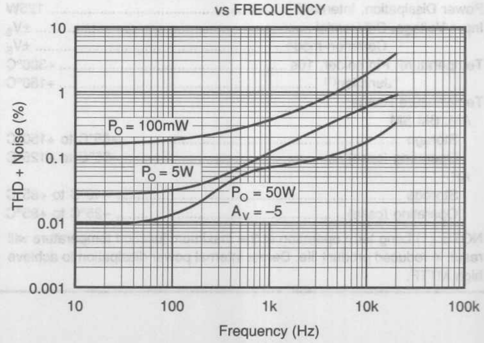
OUTPUT VOLTAGE SWING
vs OUTPUT CURRENT



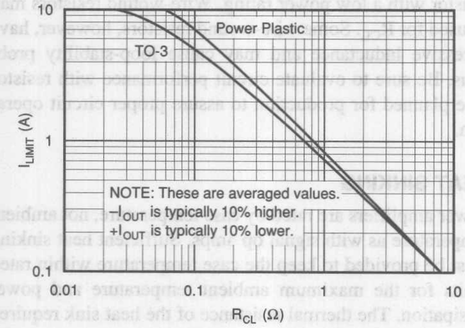
VOLTAGE NOISE DENSITY
vs FREQUENCY



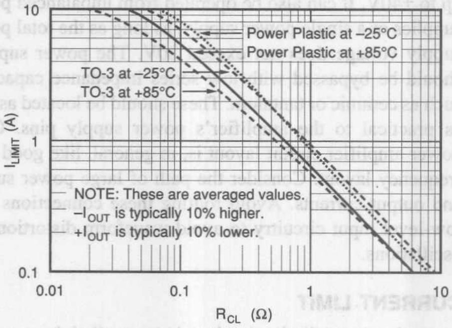
TOTAL HARMONIC DISTORTION + NOISE
vs FREQUENCY



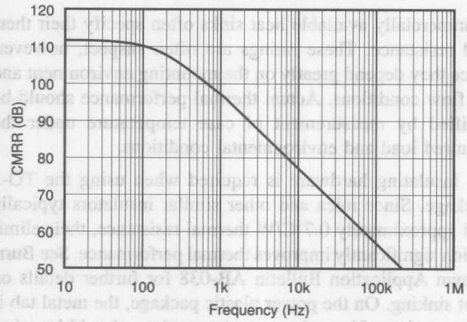
CURRENT LIMIT vs RESISTANCE LIMIT



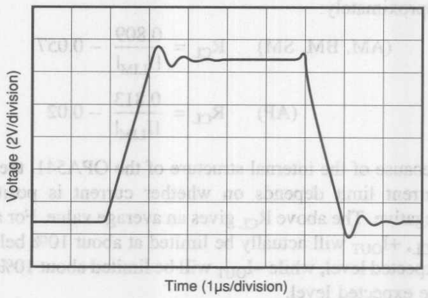
CURRENT LIMIT vs RESISTANCE LIMIT vs TEMPERATURE



COMMON-MODE REJECTION vs FREQUENCY



DYNAMIC RESPONSE



INSTALLATION INSTRUCTIONS

POWER SUPPLIES

The OPA541 is specified for operation from power supplies up to ±40V. It can also be operated from unbalanced power supplies or a single power supply, as long as the total power supply voltage does not exceed 80V. The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier's power supply pins. Good power amplifier circuit layout is, in general, like good high frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and oscillations.

CURRENT LIMIT

Internal current limit circuitry is controlled by a single external resistor, R_{CL}. Output load current flows through this external resistor. The current limit is activated when the voltage across this resistor is approximately a base-emitter turn-on voltage. The value of the current limit resistor is approximately:

$$\text{(AM, BM, SM)} \quad R_{CL} = \frac{0.809}{|I_{LIM}|} - 0.057$$

$$\text{(AP)} \quad R_{CL} = \frac{0.813}{|I_{LIM}|} - 0.02$$

Because of the internal structure of the OPA541, the actual current limit depends on whether current is positive or negative. The above R_{CL} gives an average value. For a given R_{CL}, $+I_{OUT}$ will actually be limited at about 10% below the expected level, while $-I_{OUT}$ will be limited about 10% above the expected level.

The current limit value decreases with increasing temperature due to the temperature coefficient of a base-emitter junction voltage. Similarly, the current limit value increases at low temperatures. Current limit versus resistor value and temperature effects are shown in the Typical Performance Curves. Approximate values for R_{CL} at other temperatures may be calculated by adjusting R_{CL} as follows:

$$\Delta R_{CL} = \frac{-2\text{mV}}{|I_{LIM}|} \times (T - 25)$$

The adjustable current limit can be set to provide protection from short circuits. The safe short-circuit current depends on power supply voltage. See the discussion on Safe Operating Area to determine the proper current limit value.

Since the full load current flows through R_{CL}, it must be selected for sufficient power dissipation. For a 5A current limit on the TO-3 package, the formula yields an R_{CL} of 0.105Ω (0.143Ω on the power plastic package due to different internal resistances). A continuous 5A through 0.105Ω would require an R_{CL} that can dissipate 2.625W.

Sinusoidal outputs create dissipation according to rms load current. For the same R_{CL}, AC peaks would still be limited to 5A, but rms current would be 3.5A, and a current limiting resistor with a lower power rating could be used. Some applications (such as voice amplification) are assured of signals with much lower duty cycles, allowing a current resistor with a low power rating. Wire-wound resistors may be used for R_{CL}. Some wire-wound resistors, however, have excessive inductance and may cause loop-stability problems. Be sure to evaluate circuit performance with resistor type planned for production to assure proper circuit operation.

HEAT SINKING

Power amplifiers are rated by case temperature, not ambient temperature as with signal op amps. Sufficient heat sinking must be provided to keep the case temperature within rated limits for the maximum ambient temperature and power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{HS} = \frac{T_{CASE} - T_{AMBIENT}}{P_D\ (\text{max})}$$

Commercially available heat sinks often specify their thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the TO-3 package. Since mica and other similar insulators typically add approximately 0.7°C/W thermal resistance, their elimination significantly improves thermal performance. See Burr-Brown Application Bulletin AB-038 for further details on heat sinking. On the power plastic package, the metal tab is connected to $-V_S$, and appropriate actions should be taken when mounting on a heat sink or chassis.

SAFE OPERATING AREA

The safe operating area (SOA) plot provides comprehensive information on the power handling abilities of the OPA541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

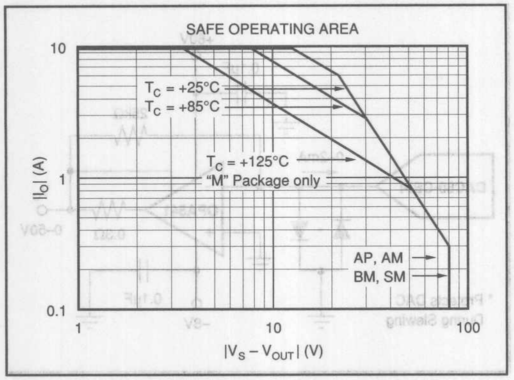


FIGURE 1. Safe Operating Area.

Short circuit protection requires evaluation of SOA. When the amplifier output is shorted to ground, the full power supply voltage is impressed across the conducting output transistor. The current limit must be set to a value which is safe for the power supply voltage used. For instance, with V_S ±35V, a short to ground would force 35V across the conducting power transistor. A current limit of 1.8A would be safe.

Reactive, or EMF-generating, loads such as DC motors can present difficult SOA requirements. With a purely reactive load, output voltage and load current are 90° out of phase. Thus, peak output current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Bulletin AB-039 for further information on evaluating SOA.

REPLACING HYBRID POWER AMPLIFIERS

The OPA541 can be used in applications currently using various hybrid power amplifiers, including the OPA501, OPA511, OPA512, and 3573. Of course, the application must be evaluated to assure that the output capability and other performance attributes of the OPA541 meet the necessary requirement. These hybrid power amplifiers use two current limit resistors to independently set the positive and negative current limit value. Since the OPA541 uses only one current limit resistor to set both the positive and negative current limit, only one resistor (see Figure 4) need be installed. If installed, the resistor connected to pin 2 (TO-3 package) is superfluous, but it does no harm.

Because one resistor carries the current previously carried by two, the resistor may require a higher power rating. Minor adjustments may be required in the resistor value to achieve the same current limit value. Often, however, the change in current limit value when changing models is small compared to its variation over temperature. Many applications can use the same current limit resistor.

APPLICATIONS CIRCUITS

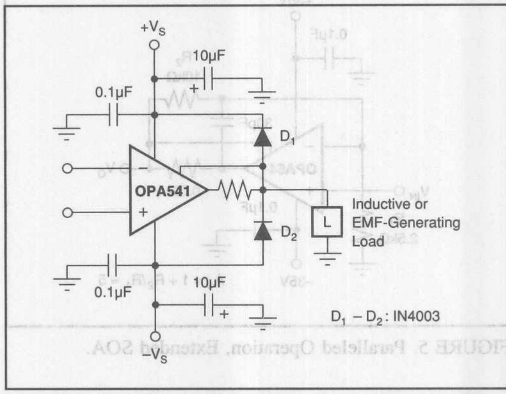


FIGURE 2. Clamping Output for EMF-Generating Loads.

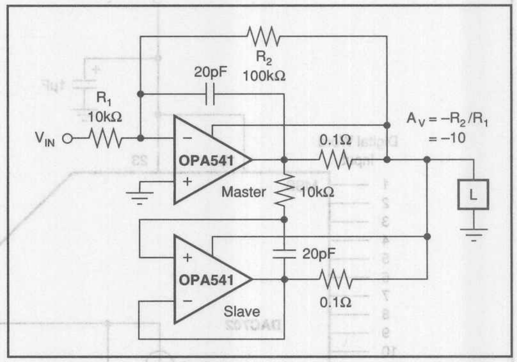


FIGURE 3. Isolating Capacitive Loads.

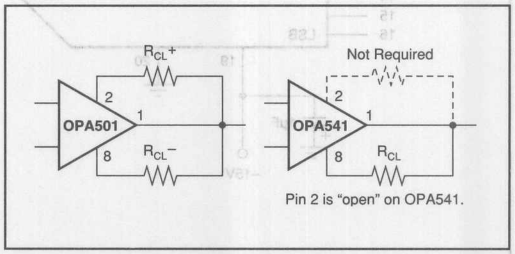


FIGURE 4. Replacing OPA501 with OPA541.

OPA541

3.2

POWER OPERATIONAL AMPLIFIERS

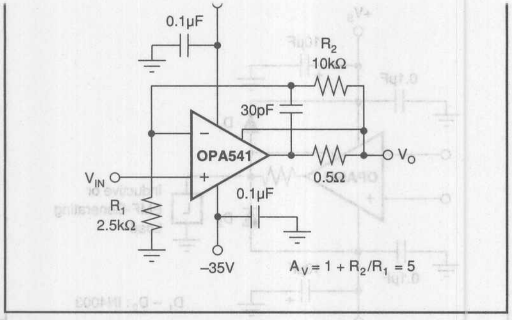


FIGURE 5. Paralleled Operation, Extended SOA.

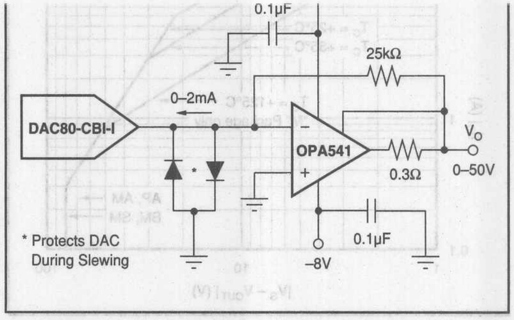


FIGURE 6. Programmable Voltage Source.

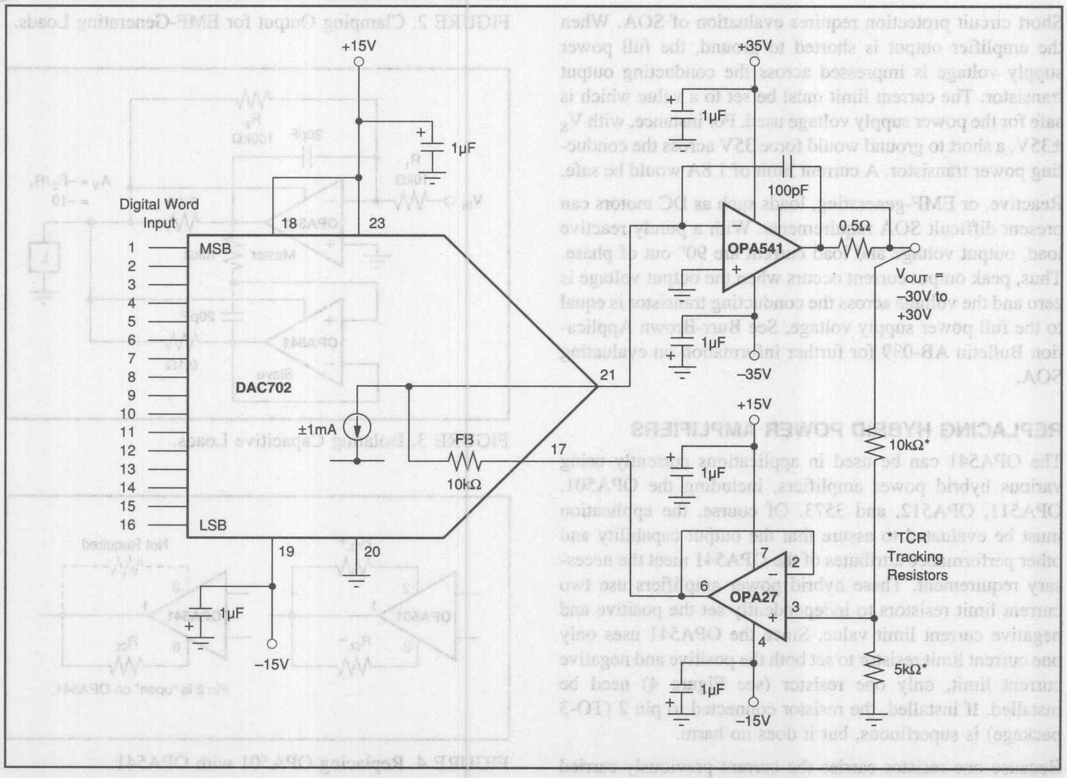
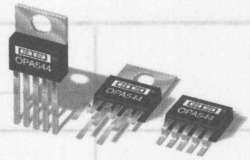


FIGURE 7. 16-Bit Programmable Voltage Source.



OPA544

High-Voltage, High-Current OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: 2A min
- WIDE POWER SUPPLY RANGE: ±10 to ±35V
- SLEW RATE: 8V/μs
- INTERNAL CURRENT LIMIT
- THERMAL SHUTDOWN PROTECTION
- FET INPUT: I_B = 100pA max
- 5-LEAD TO-220 PLASTIC PACKAGE
- 5-LEAD SURFACE MOUNT PACKAGE

APPLICATIONS

- MOTOR DRIVER
- PROGRAMMABLE POWER SUPPLY
- SERVO AMPLIFIER
- VALVES, ACTUATOR DRIVER
- MAGNETIC DEFLECTION COIL DRIVER
- AUDIO AMPLIFIER

DESCRIPTION

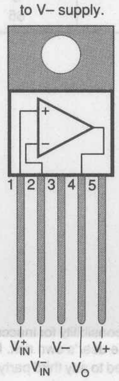
The OPA544 is a high-voltage/high-current operational amplifier suitable for driving a wide variety of high power loads. High performance FET op amp circuitry and high power output stage are combined on a single monolithic chip.

The OPA544 is protected by internal current limit and thermal shutdown circuits.

The OPA544 is available in industry-standard 5-lead TO-220 and 5-lead surface-mount power packages. Its copper tab allows easy mounting to a heat sink for excellent thermal performance. It is specified for operation over the extended industrial temperature range, –40°C to +85°C.

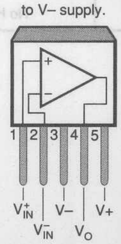
Tab is connected to V– supply.

5-Lead TO-220 and Stagger-Formed TO-220



Tab is connected to V– supply.

5-Lead Surface Mount



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

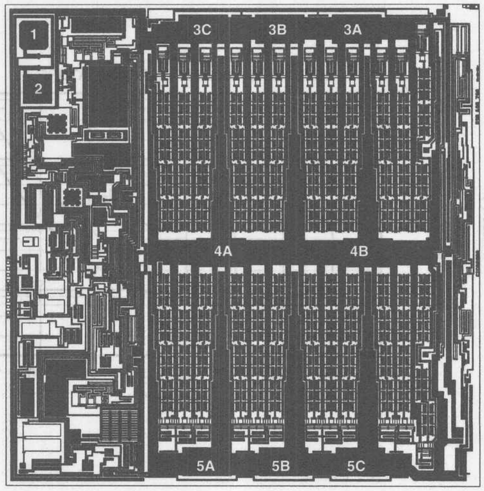
SPECIFICATIONS

T_{CASE} = +25°C, V_S = ±35V unless otherwise noted.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
		OPA544T OPA544T-1 OPA544F			
OFFSET VOLTAGE					
Input Offset Voltage			±1	±5	mV
vs Temperature	Specified Temperature Range		±10		µV/°C
vs Power Supply	V_S = ±10V to ±35V		±10	±100	µV/V
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		±15	±100	pA
vs Temperature			See Typical Curve		
Input Offset Current	V_{CM} = 0V		±10	±100	pA
NOISE					
Input Voltage Noise					
Noise Density, f = 1kHz			36		nV/√Hz
Current Noise Density, f = 1kHz			3		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range, Positive	Linear Operation	(V+) –6	(V+) –4		V
Negative	Linear Operation	(V–) +6	(V–) +4		V
Common-Mode Rejection	$V_{CM} = \pm V_S - 6V$	90	106		dB
INPUT IMPEDANCE					
Differential			10^{12} || 8		Ω || pF
Common-Mode			10^{12} || 10		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±30V, R_L = 1kΩ	90	103		dB
FREQUENCY RESPONSE					
Gain Bandwidth Product	R_L = 15Ω		1.4		MHz
Slew Rate	60Vp-p, R_L = 15Ω	5	8		V/µs
Full-Power Bandwidth			See Typical Curve		
Settling Time 0.1%	G = –10, 60V Step		25		µs
Total Harmonic Distortion			See Typical Curve		
OUTPUT					
Voltage Output, Positive	I_O = 2A	(V+) –5	(V+) –4.4		V
Negative	I_O = 2A	(V–) +5	(V–) +3.8		V
Positive	I_O = 0.5A	(V+) –4.2	(V+) –3.8		V
Negative	I_O = 0.5A	(V–) +4	(V–) +3.1		V
Current Output			See SOA Curves		
Short-Circuit Current			4		A
POWER SUPPLY					
Specified Operating Voltage			±35		V
Operating Voltage Range		±10		±35	V
Quiescent Current	I_O = 0		±12	±15	mA
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JC}	f > 50Hz		2.7		°C/W
Thermal Resistance, θ_{JC}	DC		3		°C/W
Thermal Resistance, θ_{JA}	No Heat Sink		65		°C/W

NOTES: (1) High-speed test at T_J = 25°C.

DICE INFORMATION



PAD	FUNCTION
1	+In
2	–In
3A, 3B, 3C	V–
4A, 4B	V_O
5A, 5B, 5C	V+

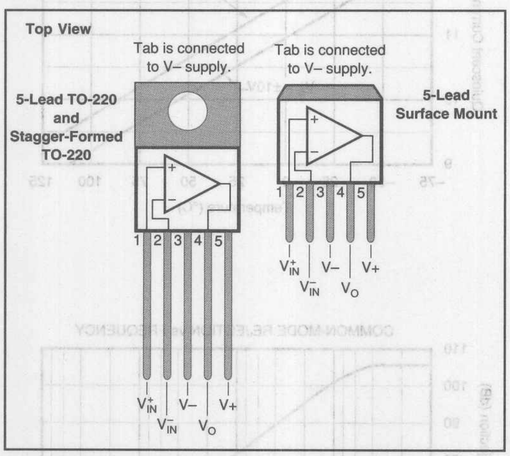
Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	159 x 162 ±5	4.04 x 4.11 ±0.13
Die Thickness	14 ±3	0.36 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Chromium-Silver

OPA544 DIE TOPOGRAPHY

CONNECTION DIAGRAMS



ORDERING/PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA544T	5-Lead TO-220	315
OPA544T-1	5-Lead Stagger-Formed TO-220	323
OPA544F	5-Lead Surface-Mount	325

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	70V
Output Current	See SOA Curve
Input Voltage	(V–) –0.7V to (V+) +0.7V
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering –10s)[1]	300°C

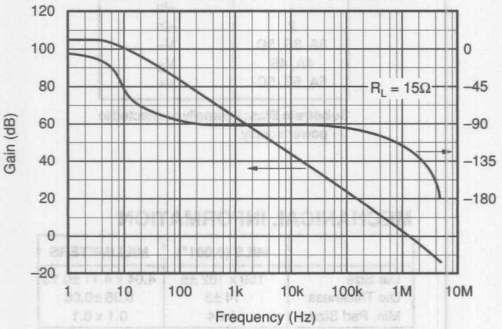
NOTE: (1) Vapor-phase or IR reflow techniques are recommended for soldering the OPA544F surface mount package. Wave soldering is not recommended due to excessive thermal shock and "shadowing" of nearby devices.

ELECTROSTATIC DISCHARGE SENSITIVITY

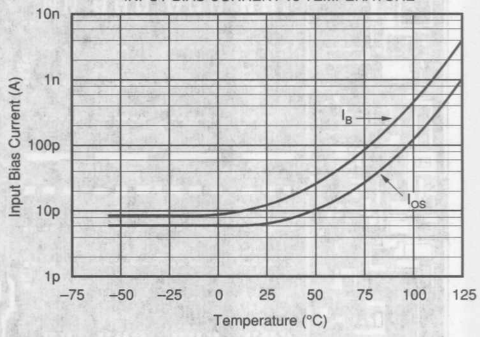
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

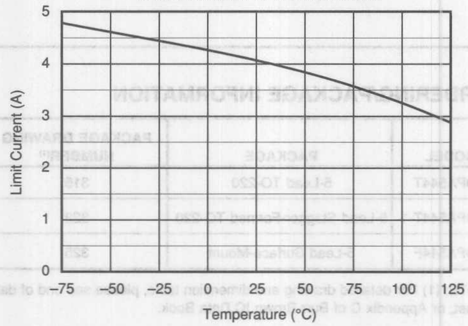
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



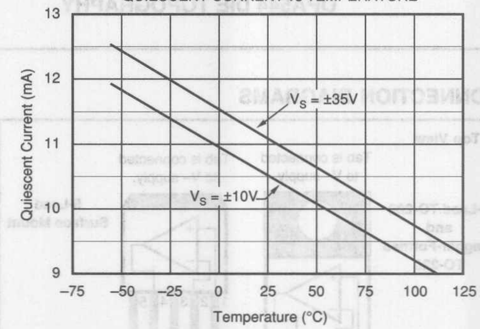
INPUT BIAS CURRENT vs TEMPERATURE



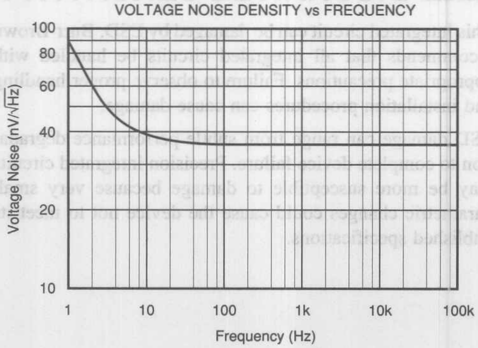
CURRENT LIMIT vs TEMPERATURE



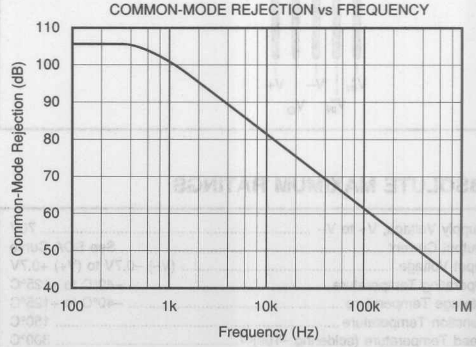
QUIESCENT CURRENT vs TEMPERATURE



VOLTAGE NOISE DENSITY vs FREQUENCY

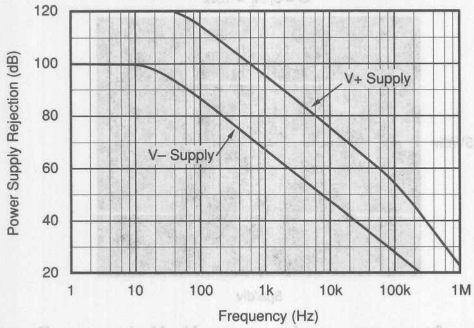


COMMON-MODE REJECTION vs FREQUENCY

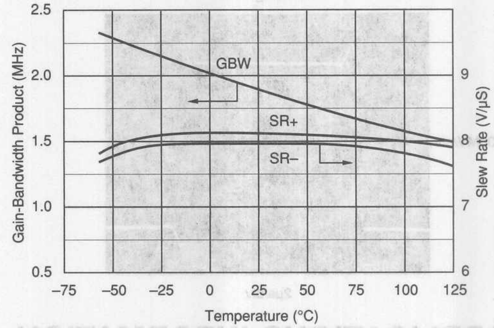


T_{CASE} = +25°C, V_S = ±35V unless otherwise noted.

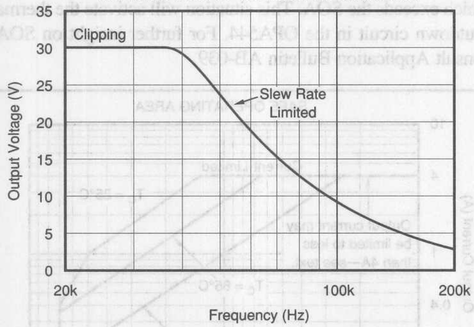
POWER SUPPLY REJECTION vs FREQUENCY



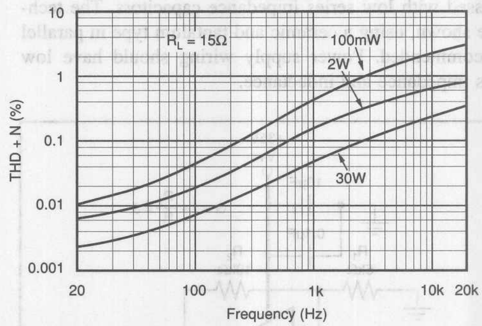
GAIN-BANDWIDTH PRODUCT AND SLEW RATE vs TEMPERATURE



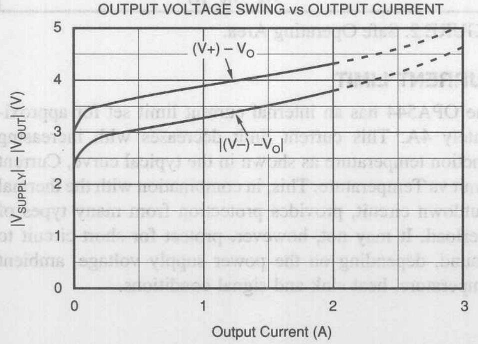
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



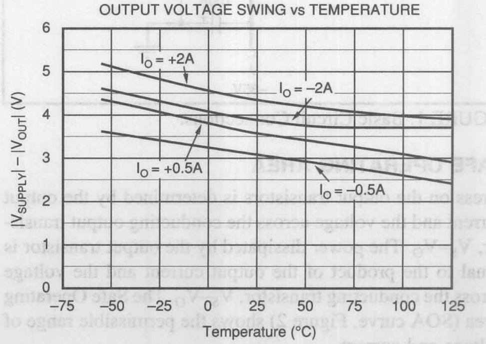
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

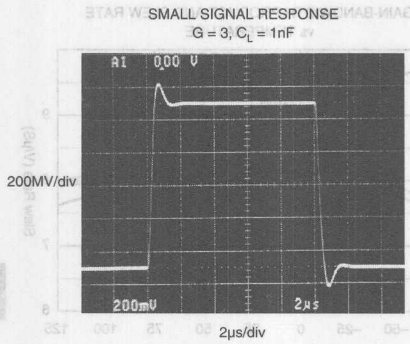


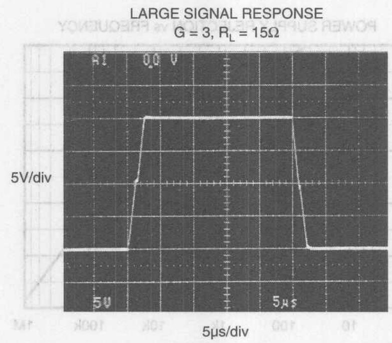
OUTPUT VOLTAGE SWING vs TEMPERATURE



TYPICAL PERFORMANCE CURVES (CONT)

T_{CASE} = +25°C, V_S = ±35V unless otherwise noted.





APPLICATIONS INFORMATION

Figure 1 shows the OPA544 connected as a basic non-inverting amplifier. The OPA544 can be used in virtually any op amp configuration. Power supply terminals should be bypassed with low series impedance capacitors. The technique shown, using a ceramic and tantalum type in parallel is recommended. Power supply wiring should have low series impedance and inductance.

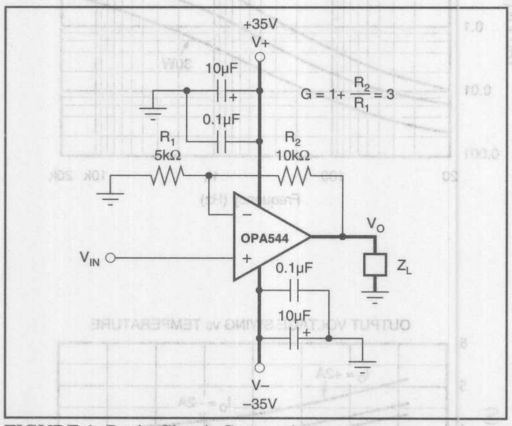


FIGURE 1. Basic Circuit Connections.

SAFE OPERATING AREA

Stress on the output transistors is determined by the output current and the voltage across the conducting output transistor, V_S–V_O. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, V_S–V_O. The Safe Operating Area (SOA curve, Figure 2) shows the permissible range of voltage and current.

The safe output current decreases as V_S–V_O increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage (V+ or V–) across the conducting transistor. With V_S = ±35V the safe output current is 1.5A (at 25°C). The short-circuit current is approximately 4A which exceeds the SOA. This situation will activate the thermal shutdown circuit in the OPA544. For further insight on SOA, consult Application Bulletin AB-039.

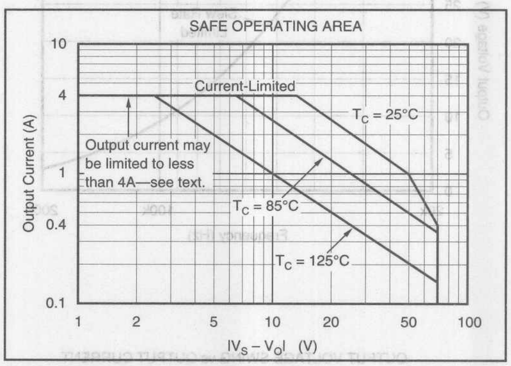


FIGURE 2. Safe Operating Area.

CURRENT LIMIT

The OPA544 has an internal current limit set for approximately 4A. This current limit decreases with increasing junction temperature as shown in the typical curve, Current Limit vs Temperature. This, in combination with the thermal shutdown circuit, provides protection from many types of overload. It may not, however, protect for short-circuit to ground, depending on the power supply voltage, ambient temperature, heat sink and signal conditions.

POWER DISSIPATION

Power dissipation depends on power supply, signal and load conditions. For dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

HEATSINKING

Most applications require a heat sink to assure that the maximum junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions. Consult Application Bulletin AB-038 for information on determining heat sink requirements.

The mounting tab of the surface-mount package version should be soldered to a circuit board copper area for good heat dissipation. Figure 3 shows typical thermal resistance from junction to ambient as a function of the copper area.

THERMAL PROTECTION

The OPA544 has thermal shutdown that protects the amplifier from damage. Any tendency to activate the thermal shutdown circuit during normal operation is indication of excessive power dissipation or an inadequate heat sink.

The thermal protection activates at a junction temperature of approximately 155°C. For reliable operation, junction temperature should be limited to 150°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection should trigger more than 25°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

Depending on load and signal conditions, the thermal protection circuit may produce a duty-cycle modulated output signal. This limits the dissipation in the amplifier, but the rapidly varying output waveform may be damaging to some loads. The thermal protection may behave differently depending on whether internal dissipation is produced by sourcing or sinking output current.

OUTPUT STAGE COMPENSATION

The complex load impedances common in power op amp applications can cause output stage instability. Figure 3 shows an output series R/C compensation network (1Ω in series with 0.01μF) which generally provides excellent stability. Some variation in circuit values may be required with certain loads.

UNBALANCED POWER SUPPLIES

Some applications do not require equal positive and negative output voltage swing. The power supply voltages of the OPA544 do not need to be equal. For example, a –6V negative power supply voltage assures that the inputs of the OPA544 are operated within their linear common-mode range, and that the output can swing to 0V. The V+ power supply could range from 15V to 65V. The total voltage (V– to V+) can range from 20V to 70V. With a 65V positive supply voltage, the device may not be protected from damage during short-circuits because of the larger V_{CE} during this condition.

OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies as shown in Figure 4. Fast-recovery rectifier diodes with a 4A or greater continuous rating are recommended.

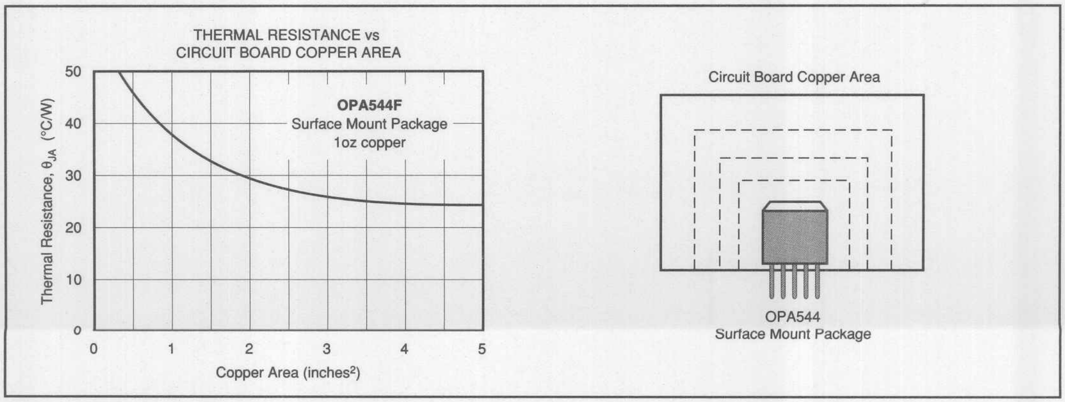


FIGURE 3. Thermal Resistance vs Circuit Board Copper Area.

POWER OPERATIONAL AMPLIFIERS OPA544 3.2

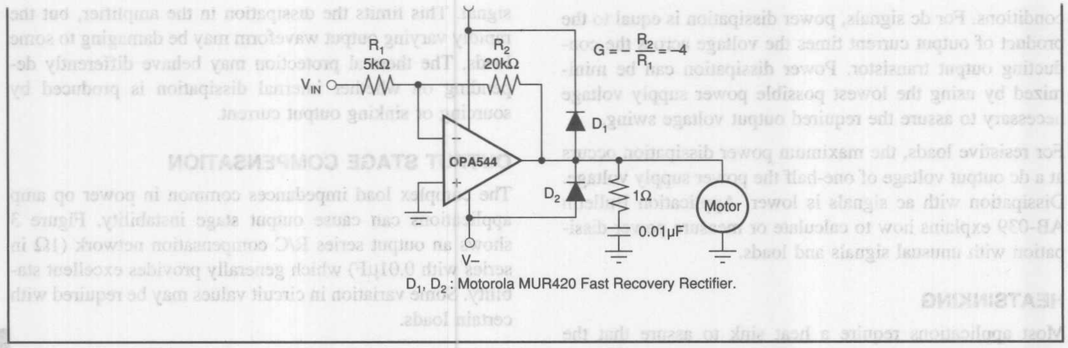


FIGURE 4. Motor Drive Circuit.

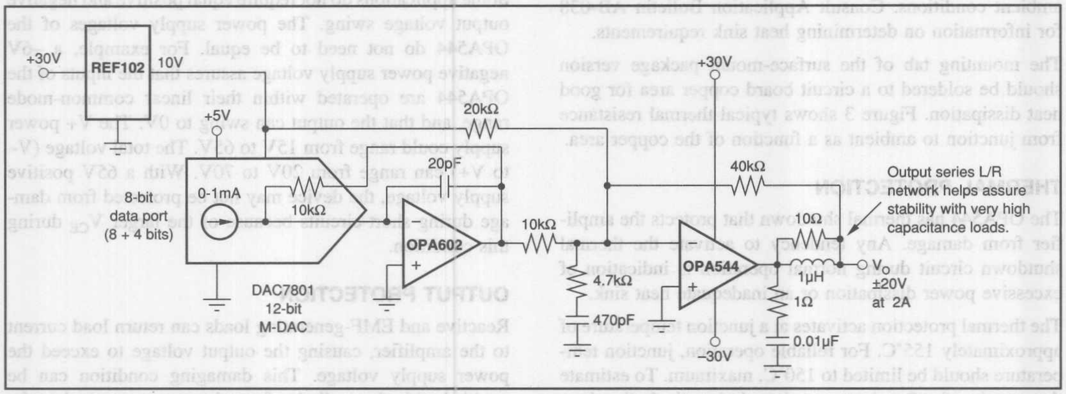
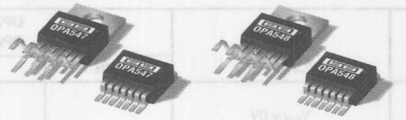


FIGURE 5. Digitally Programmable Power Supply.

BURR - BROWN®



OPA547
OPA548

PRELIMINARY INFORMATION SUBJECT TO CHANGE WITHOUT NOTICE

High-Voltage, High-Current OPERATIONAL AMPLIFIERS

FEATURES

- **WIDE SUPPLY RANGE**
  Single Supply: +8V to +70V
  Dual Supply: ±4V to ±35V
- **HIGH OUTPUT CURRENT**
  OPA547: 500mA
  OPA548: 3A
- **WIDE OUTPUT VOLTAGE SWING**
- **FULLY PROTECTED:**
  Thermal Shutdown
  Adjustable Current Limit
- **OUTPUT DISABLE CONTROL**
- **THERMAL SHUTDOWN INDICATOR**
- **HIGH SLEW RATE: 10V/µs**
- **LOW QUIESCENT CURRENT:**
  8mA OPA547
- **7-LEAD STAGGERED TO-220 and DDPAK SURFACE-MOUNT PLASTIC POWER PACKAGE**

APPLICATIONS

- **VALVE, ACTUATOR DRIVER**
- **SYNCHRO, SERVO DRIVER**
- **POWER SUPPLIES**
- **TEST EQUIPMENT**
- **TRANSDUCER EXCITATION**
- **AUDIO AMPLIFIER**

DESCRIPTION

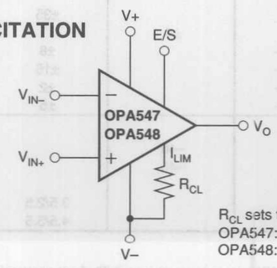
The OPA547 and OPA548 are low cost, high-voltage/high-current operational amplifiers ideal for driving a wide variety of loads. A single laser-trimmed monolithic integrated circuit provides excellent low-level signal accuracy and high output voltage swing.

The OPA547 and OPA548 can operate from either single or dual supplies for design flexibility. In single supply operation, the input common-mode range extends below ground.

The OPA547 and OPA548 are fully protected. Internal current limit and thermal shutdown circuits prevent damage from over-temperature conditions. Current limit is accurately set from 0 to 750mA (OPA547) and from 0 to 5A (OPA548) with a single low-power resistor, R_{CL}.

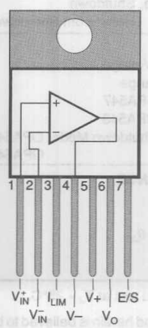
The Enable/Status (E/S) pin provides two functions: an input on this pin will disable the output stage and/or the output can be monitored to determine if the device is in thermal shutdown.

The OPA547 and OPA548 packages are an industry-standard 7-lead staggered TO-220 and a 7-lead DDPAK surface-mount plastic power package. The copper tab allows easy mounting to a heat sink or circuit board for excellent thermal performance. Both products are specified for operation over the extended industrial temperature range, –40°C to +85°C.



R_{CL} sets the current limit value
OPA547: 0 to 750mA
OPA548: 0 to 5A

7-Lead Stagger-Formed TO-220 and DDPAK Surface-Mount



Tab is connected to V– supply.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

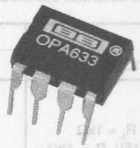
SPECIFICATIONS

T_{CASE} = +25°C, V_S = ±35V, unless otherwise noted.

PARAMETER	CONDITION	OPA547T, F OPA548T, F MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage	V_{CM} = 0V		±1	±5	mV
vs Temperature	Operating Temperature Range		±10		µV/°C
vs Power Supply	V_S = ±4V to ±35V		20	100	µV/V
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		100	500	nA
vs Temperature			0.5		nA/°C
Input Offset Current	V_{CM} = 0V		10	50	nA
INPUT VOLTAGE RANGE					
Common-Mode Input Range	Linear Operation	(V–)–0.1	(V–)–0.2/(V+)–2	(V+)–3	V
Common-Mode Rejection	V_{CM} = (V–)–0.1V to (V+)–3V	80	90		dB
OPEN-LOOP GAIN					
Open-Loop Voltage Gain, f = 10Hz	V_O = ±30V, R_L = 1kΩ	90	100		dB
f = 10Hz	V_O = ±30V, R_L = 60Ω		90		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product	R_L = 60Ω		1		MHz
Slew Rate	60Vp-p, R_L = 60Ω		10		V/µs
Settling Time: ±0.1%	G = –10, 60V Step		10		µs
Total Harmonic Distortion + Noise, f = 1kHz	R_L = 60Ω		0.05		%
OUTPUT: OPA547					
Voltage Output, Positive	I_O = 0.5A	(V+)–2.5	(V+)–2		V
Negative	I_O = 0.5A	(V–)+2	(V–)+1.5		V
Positive	I_O = 0.1A	(V+)–2	(V+)–1.5		V
Negative	I_O = 0.1A	(V–)+1	(V–)+0.7		V
Current Output, Continuous			±500		mA
Output Current Limit					
Current Limit Range			0 to ±750		mA
Current Limit Equation			I_{SC} = 5000•4.75/(31600Ω + R_{CL})		A
Current Limit	R_{CL} = 31.6kΩ	365	375	385	mA
Capacitive Load Drive (Stable Operation)	G = +1		1000		pF
OUTPUT: OPA548					
Voltage Output, Positive	I_O = 3A	(V+)–3.7	(V+)–3.3		V
Negative	I_O = 3A	(V–)+3.5	(V–)+3		V
Positive	I_O = 0.6A	(V+)–2.5	(V+)–2		V
Negative	I_O = 0.6A	(V–)+2	(V–)+1.5		V
Current Output, continuous			±3		A
Output Current Limit					
Current Limit Range			0 to ±5		A
Current Limit Equation			I_{SC} = 15000•4.75/(13750Ω + R_{CL})		A
Current Limit	R_{CL} = 14.8kΩ	2.4	2.5	2.6	A
Capacitive Load Drive (Stable Operation)	G = +1		1000		pF
ENABLE /STATUS (E/S) PIN					
Shutdown Input Mode					
$V_{E/S}$ High (output enabled)	E/S Pin Open or Pulled High	(V–)+2.4		V+	V
$V_{E/S}$ Low (output disabled)	E/S Pin Pulled Low	V–		(V–)+0.8	V
$I_{E/S}$ High (output enabled)	E/S Pin Open or Pulled High		0		µA
$I_{E/S}$ Low(output disabled)	E/S Pin Pulled Low		100		µA
Thermal Shutdown Status Output					
Normal Operation	Sourcing up to 20µA	(V–)+2.4	(V–)+3.3		V
Thermally Shutdown	Sinking up to 10µA		(V–)+0.2	(V–)+0.8	V
Junction Temperature, Shutdown			+160		°C
Reset from Shutdown			+140		°C
POWER SUPPLY					
Specified Operating Voltage			±35		V
Operating Voltage Range		±4		±35	V
Quiescent Current, OPA547	I_{LIM} Connected to V–		±8	±10	mA
OPA548	I_{LIM} Connected to V–		±15	±20	mA
Quiescent Current, Shutdown Mode, OPA547	I_{LIM} Connected to V–		±2		mA
OPA548	I_{LIM} Connected to V–		±5		mA
TEMPERATURE RANGE					
Specified Range		–40		+85	°C
Operating Range		–40		+125	°C
Thermal Resistance, θ_{JC}					
f > 50Hz	(OPA547/OPA548)		3.5/2.5		°C/W
DC	(OPA547/OPA548)		4.5/3.5		°C/W

NOTES: (1) High-speed test at T_J = 25°C.

BURR-BROWN®



OPA633

High Speed BUFFER AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 260MHz
- HIGH SLEW RATE: 2500V/µs
- HIGH OUTPUT CURRENT: 100mA
- LOW OFFSET VOLTAGE: 1.5mV
- REPLACES HA-5033
- IMPROVED PERFORMANCE/PRICE: LH0033, LTC1010, H0S200

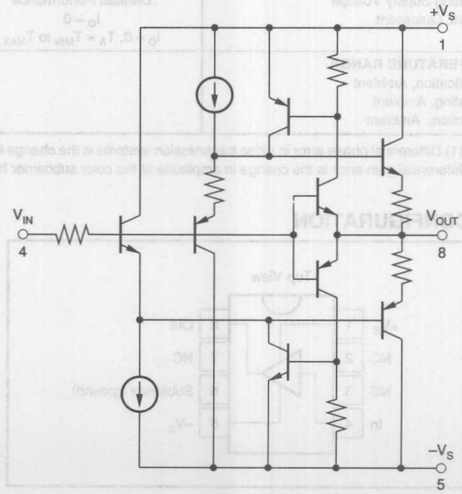
APPLICATIONS

- OP AMP CURRENT BOOSTER
- VIDEO BUFFER
- LINE DRIVER
- A/D CONVERTER INPUT BUFFER

DESCRIPTION

The OPA633 is a monolithic unity-gain buffer amplifier featuring very wide bandwidth and high slew rate. A dielectric isolation process incorporating both NPN and PNP high frequency transistors achieves performance unattainable with conventional integrated circuit technology. Laser trimming provides low input offset voltage.

High output current capability allows the OPA633 to drive 50Ω and 75Ω lines, making it ideal for RF, IF and video applications. Low phase shift allows the OPA633 to be used inside amplifier feedback loops. OPA633 is available in a low cost plastic DIP package specified for 0°C to +75°C operation.

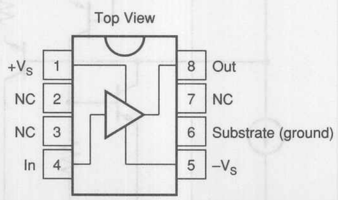


International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PARAMETER	CONDITIONS	OPA633KP MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE					
Small Signal Bandwidth			260		MHz
Full Power Bandwidth	V_O = 1Vrms, R_L = 1kΩ		40		MHz
Slew Rate	V_O = 10V, V_S = ±15V, R_L = 1kΩ	1000	2500		V/µs
Rise Time, 10% to 90%	V_O = 500mV		2.5		ns
Propagation Delay			1		ns
Overshoot			10		%
Settling Time, 0.1%			50		ns
Differential Phase Error (1)			0.1		Degrees
Differential Gain Error (1)			0.1		%
Total Harmonic Distortion	V_O = 1Vrms, R_L = 1kΩ, f = 100kHz		0.005		%
	V_O = 1Vrms, R_L = 100Ω, f = 100kHz		0.02		%
OUTPUT CHARACTERISTICS					
Voltage	T_A = T_{MIN} to T_{MAX}	±8	±10		V
	R_L = 1kΩ, V_S = ±15V	±11	±13		V
Current		±80	±100		mA
Resistance			5		Ω
TRANSFER CHARACTERISTICS					
Gain		0.93	0.95		V/V
	R_L = 1kΩ		0.99		V/V
	T_A = T_{MIN} to T_{MAX}	0.92	0.95		V/V
INPUT					
Offset Voltage	T_A = +25°C		±5	±15	mV
	T_A = T_{MIN} to T_{MAX}		±6	±25	mV
vs Temperature			±33		µV/°C
vs Supply	T_A = T_{MIN} to T_{MAX}	54	72		dB
Bias Current	T_A = +25°C		±15	±35	µA
	T_A = T_{MIN} to T_{MAX}		±20	±50	µA
Noise Voltage	10Hz to 1MHz		20		µVp-p
Resistance			1.5		MΩ
Capacitance			1.6		pF
POWER SUPPLY					
Rated Supply Voltage	Specified Performance		±12		V
Operating Supply Voltage	Derated Performance	±5		±16	V
Current, Quiescent	I_O = 0		21	25	mA
	I_O = 0, T_A = T_{MIN} to T_{MAX}		21	30	mA
TEMPERATURE RANGE					
Specification, Ambient		0		+75	°C
Operating, Ambient		-25		+85	°C
θ Junction, Ambient			90		°C/W

NOTE: (1) Differential phase error in video transmission systems is the change in phase of a color subcarrier resulting from a change in picture signal from blanked to white. Differential gain error is the change in amplitude at the color subcarrier frequency resulting from a change in picture signal from blanked to white.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply, $\pm V_S$	±20V
Input Voltage V_{IN}	$+V_S$ + 2V to $-V_S$ – 2V
Output Current (peak)	±200mA
Internal Power Dissipation (25°C)	1.95W
Junction Temperature	200°C
Storage Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	300°C

PACKAGE INFORMATION

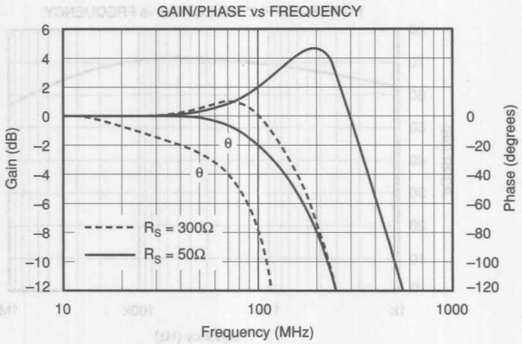
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA633KP	8-Pin Plastic DIP	006

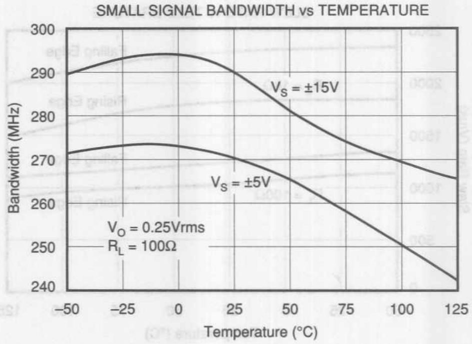
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

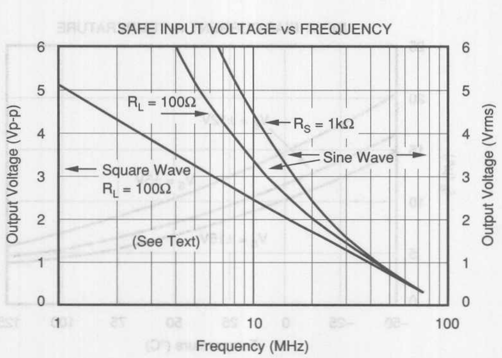
ORDERING INFORMATION

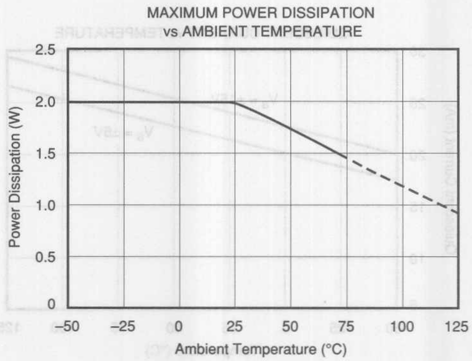
MODEL	PACKAGE	TEMPERATURE RANGE
OPA633KP	8-Pin Plastic DIP	0°C to +75°C

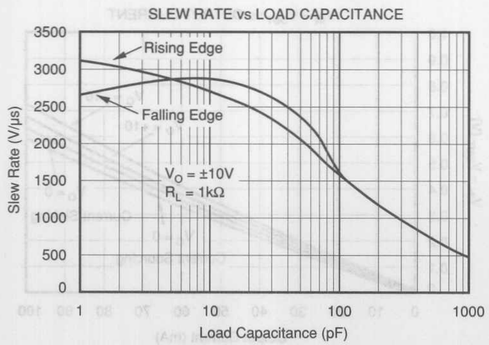
At +25°C, V_S = ±12V, R_S = 50Ω, R_L = 100Ω, and C_L = 10pF, unless otherwise specified.

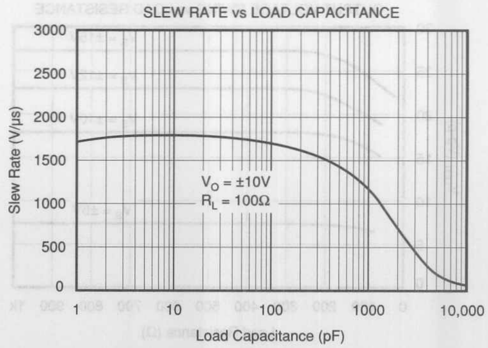












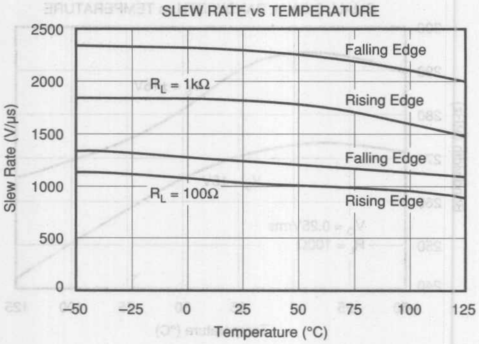
OPA633

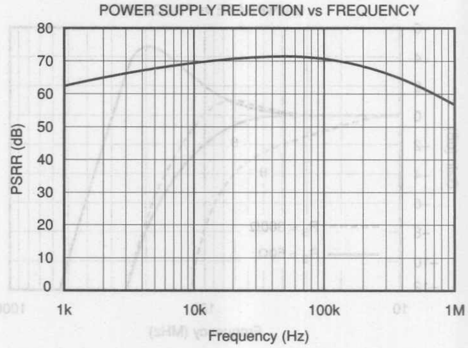
3.2

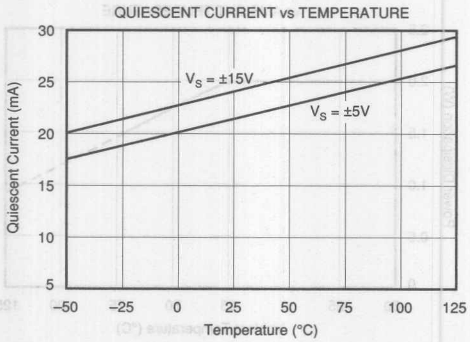
POWER OPERATIONAL AMPLIFIERS

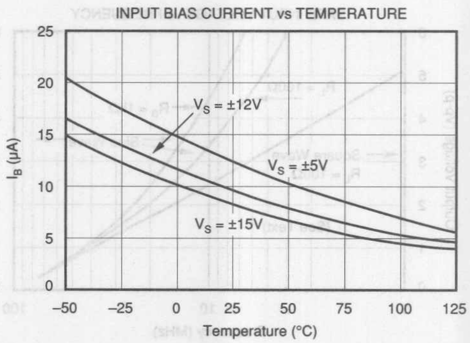
TYPICAL PERFORMANCE CURVES (CONT)

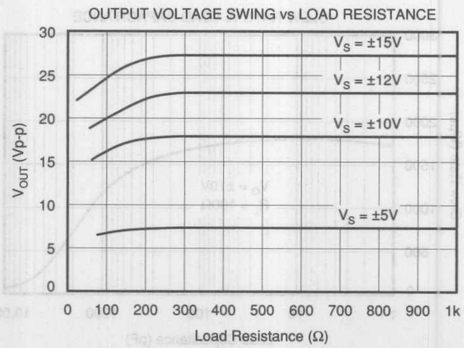
At +25°C, V_S = ±12V, R_S = 50Ω, R_L = 100Ω, and C_L = 10pF, unless otherwise specified.

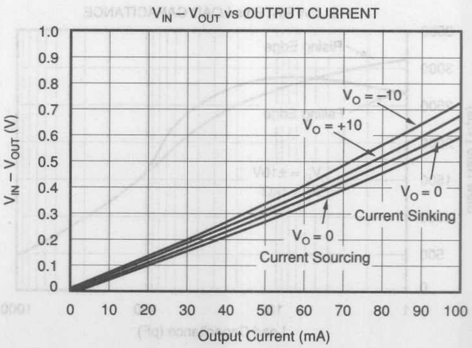








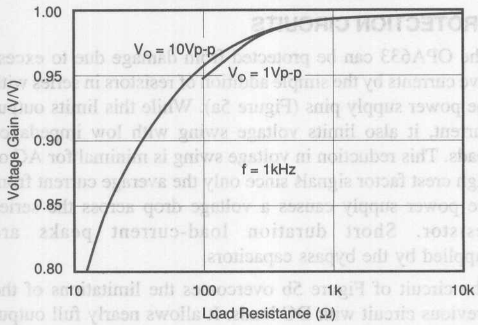




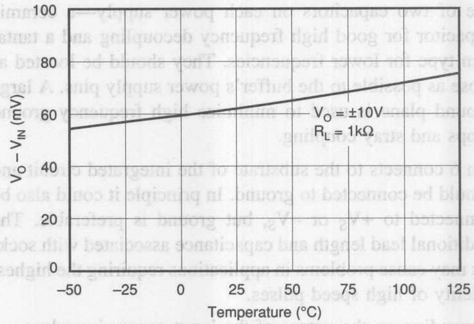
TYPICAL PERFORMANCE CURVES (CONT)

At +25°C, $V_S = \pm12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, and $C_L = 10pF$, unless otherwise specified.

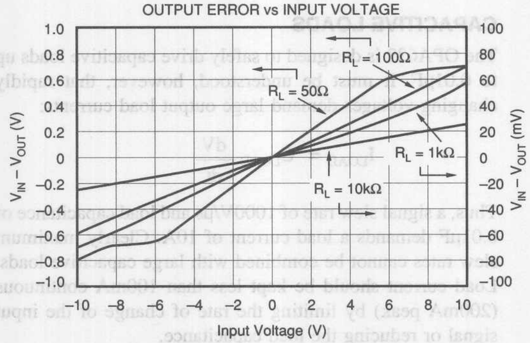
VOLTAGE GAIN vs LOAD RESISTANCE



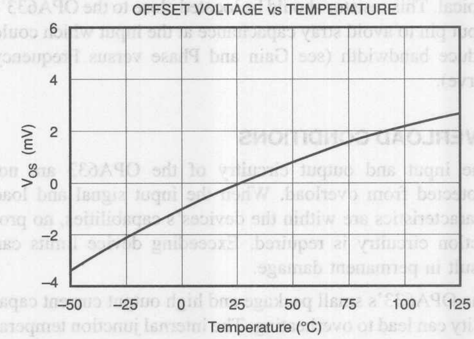
GAIN ERROR vs TEMPERATURE



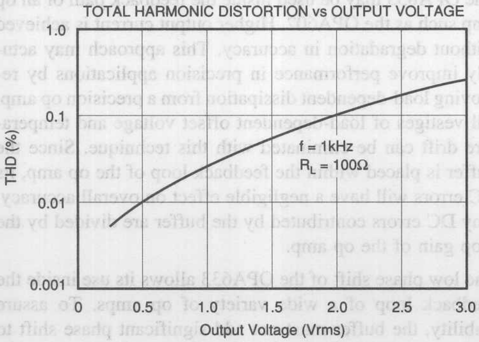
OUTPUT ERROR vs INPUT VOLTAGE



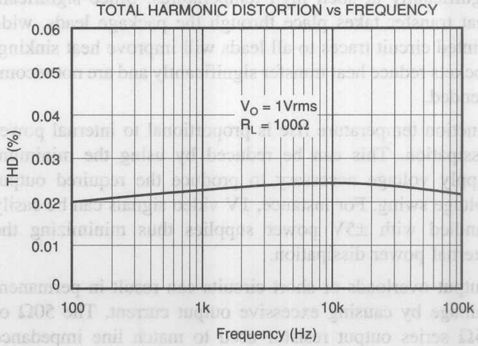
OFFSET VOLTAGE vs TEMPERATURE



TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION vs FREQUENCY



As with any high frequency circuitry, good circuit layout technique must be used to achieve optimum performance. Power supply connections must be bypassed with high frequency capacitors. Many applications benefit from the use of two capacitors on each power supply—a ceramic capacitor for good high frequency decoupling and a tantalum type for lower frequencies. They should be located as close as possible to the buffer's power supply pins. A large ground plane is used to minimize high frequency ground drops and stray coupling.

Pin 6 connects to the substrate of the integrated circuit and should be connected to ground. In principle it could also be connected to $+V_S$ or $-V_S$, but ground is preferable. The additional lead length and capacitance associated with sockets may cause problems in applications requiring the highest fidelity of high speed pulses.

Depending on the nature of the input source impedance, a series input resistor may be required for best stability. This behavior is influenced somewhat by the load impedance (including any reactive effects). A value of 50Ω to 200Ω is typical. This resistor should be located close to the OPA633's input pin to avoid stray capacitance at the input which could reduce bandwidth (see Gain and Phase versus Frequency curve).

OVERLOAD CONDITIONS

The input and output circuitry of the OPA633 are not protected from overload. When the input signal and load characteristics are within the devices's capabilities, no protection circuitry is required. Exceeding device limits can result in permanent damage.

The OPA633's small package and high output current capability can lead to overheating. The internal junction temperature should not be allowed to exceed 150°C. Although failure is unlikely to occur until junction temperature exceeds 200°C, reliability of the part will be degraded significantly at such high temperatures. Since significant heat transfer takes place through the package leads, wide printed circuit traces to all leads will improve heat sinking. Sockets reduce heat transfer significantly and are not recommended.

Junction temperature rise is proportional to internal power dissipation. This can be reduced by using the minimum supply voltage necessary to produce the required output voltage swing. For instance, 1V video signals can be easily handled with ±5V power supplies thus minimizing the internal power dissipation.

Output overloads or short circuits can result in permanent damage by causing excessive output current. The 50Ω or 75Ω series output resistor used to match line impedance will, in most cases, provide adequate protection. When this resistor is not used, the device can be protected by limiting the power supply current. See "Protection Circuits."

Excessive input levels at high frequency can cause increased internal dissipation and permanent damage. See the safe most cases, by the op amp. When high frequency inputs can exceed safe levels, the device must be protected by limiting the power supply current.

PROTECTION CIRCUITS

The OPA633 can be protected from damage due to excessive currents by the simple addition of resistors in series with the power supply pins (Figure 5a). While this limits output current, it also limits voltage swing with low impedance loads. This reduction in voltage swing is minimal for AC or high crest factor signals since only the average current from the power supply causes a voltage drop across the series resistor. Short duration load-current peaks are supplied by the bypass capacitors.

The circuit of Figure 5b overcomes the limitations of the previous circuit with DC loads. It allows nearly full output voltage swing up to its current limit of approximately 140mA. Both circuits require good high frequency capacitors (e.g., tantalum) to bypass the buffer's power supply connections.

CAPACITIVE LOADS

The OPA633 is designed to safely drive capacitive loads up to 0.01μF. It must be understood, however, that rapidly changing voltages demand large output load currents:

$$I_{LOAD} = C_{LOAD}\frac{dV}{dt}$$

Thus, a signal slew rate of 1000V/μs and load capacitance of 0.01μF demands a load current of 10A. Clearly maximum slew rates cannot be combined with large capacitive loads. Load current should be kept less than 100mA continuous (200mA peak) by limiting the rate of change of the input signal or reducing the load capacitance.

USE INSIDE A FEEDBACK LOOP

The OPA633 may be used inside the feedback path of an op amp such as the OPA602. Higher output current is achieved without degradation in accuracy. This approach may actually improve performance in precision applications by removing load-dependent dissipation from a precision op amp. All vestiges of load-dependent offset voltage and temperature drift can be eliminated with this technique. Since the buffer is placed within the feedback loop of the op amp, its DC errors will have a negligible effect on overall accuracy. Any DC errors contributed by the buffer are divided by the loop gain of the op amp.

The low phase shift of the OPA633 allows its use inside the feedback loop of a wide variety of op amps. To assure stability, the buffer must not add significant phase shift to the loop at the gain crossing frequency of the circuit—the frequency at which the open loop gain of the op amp is equal to the closed loop gain of the application. The OPA633 has a typical phase shift of less than 10° up to 70MHz, thus making it useful even with wideband op amps.

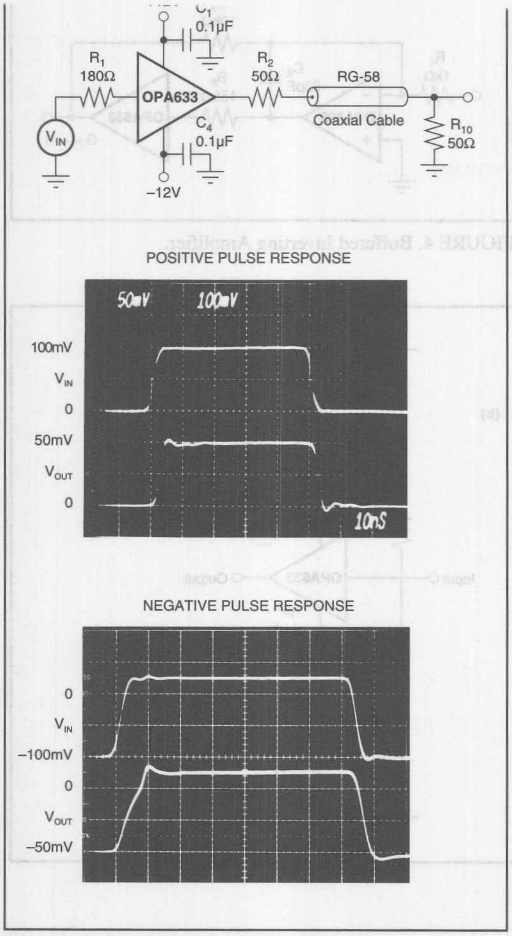


FIGURE 1. Coaxial Cable Driver Circuit.

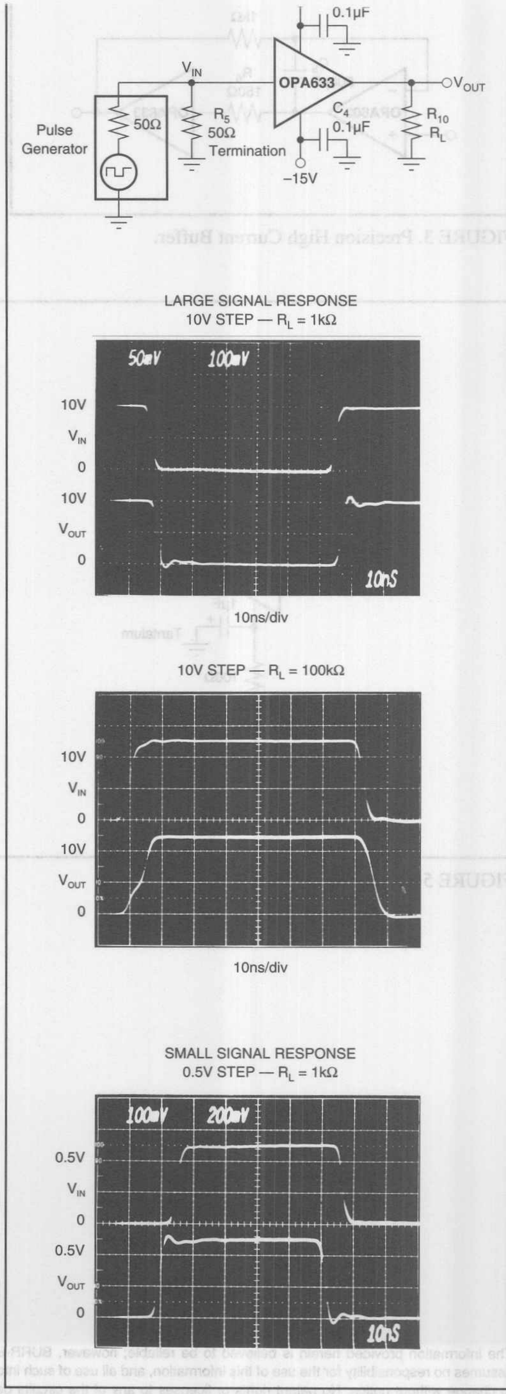


FIGURE 2. Dynamic Response Test Circuit.

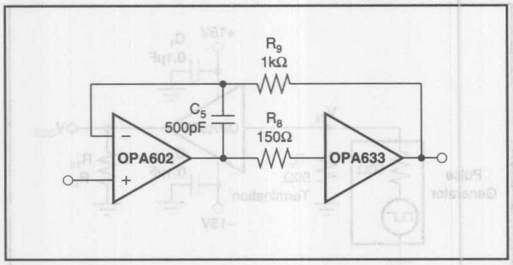


FIGURE 3. Precision High Current Buffer.

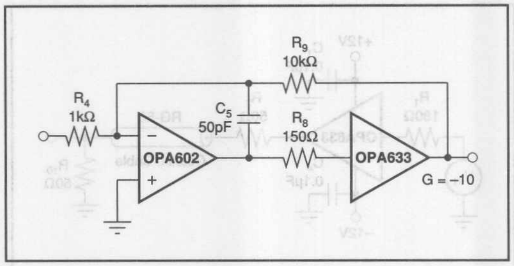
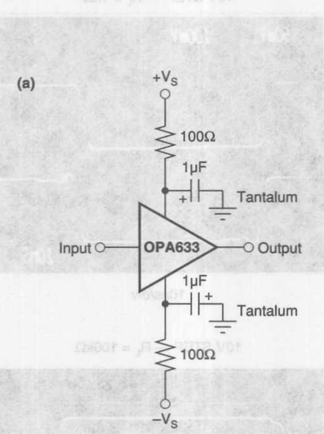


FIGURE 4. Buffered Inverting Amplifier.



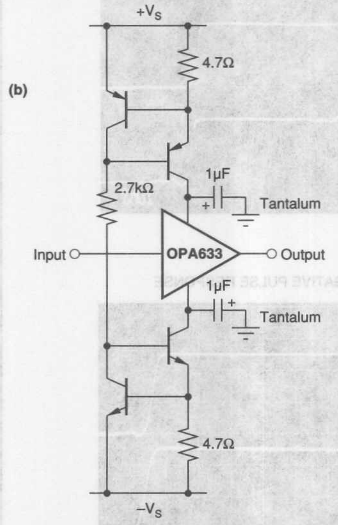
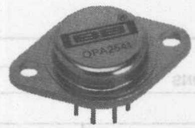


FIGURE 5. Output Protection Circuits.

BURR - BROWN®



OPA2541

Dual High Power OPERATIONAL AMPLIFIER

FEATURES

- OUTPUT CURRENTS TO 5A
- POWER SUPPLIES TO ±40V
- FET INPUT
- ELECTRICALLY ISOLATED CASE

APPLICATIONS

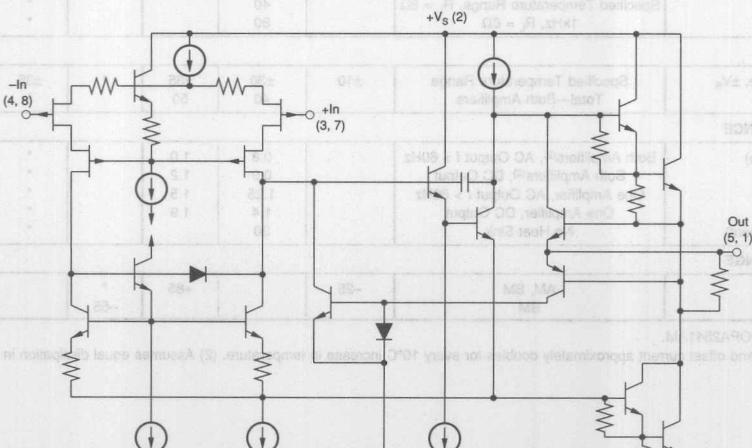
- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCRO/RESOLVER EXCITATION
- VOICE COIL DRIVER
- BRIDGE AMPLIFIER
- PROGRAMMABLE POWER SUPPLY
- AUDIO AMPLIFIER

DESCRIPTION

The OPA2541 is a dual power operational amplifier capable of operation from power supplies up to ±40V and output currents of 5A continuous. With two monolithic power amplifiers in a single package it provides unequaled functional density.

The industry-standard 8-pin TO-3 package is isolated from all internal circuitry allowing it to be mounted directly to a heat sink without insulators which degrade thermal performance. Internal circuitry limits output current to approximately 6A.

The OPA2541 is available in both industrial and military temperature range versions.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At T_C = +25°C and V_S = ±35VDC, unless otherwise noted.

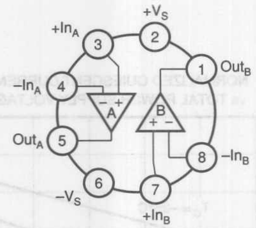
		OPA2541AM			OPA2541BM, SM			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT OFFSET VOLTAGE								
V_{OS}			±2	±10		±0.25	±1	mV
vs Temperature	Specified Temperature Range		±20	±40		±15	±30	μV/°C
vs Supply Voltage	V_S = ±10V to $\pm V_{MAX}$		±2.5	±10		*	*	μV/V
vs Power			±20	±60		*	*	μV/W
INPUT BIAS CURRENT								
I_B			15	50		*	*	pA
	Specified Temperature Range		Note 1			*		
INPUT OFFSET CURRENT								
I_{OS}			±5	±30		*	*	pA
	Specified Temperature Range		Note 1			*		
INPUT CHARACTERISTICS								
Common-Mode Voltage Range	Specified Temperature Range	$\pm(\lvert V_S\rvert -6)$	$\pm(\lvert V_S\rvert -3)$		*	*		V
Common-Mode Rejection	$V_{CM} = (\lvert\pm V_S\rvert -6V)$	95	106		*	*		dB
Input Capacitance			5			*		pF
Input Impedance, DC			1			*		$10^{12}\Omega$
GAIN CHARACTERISTICS								
Open Loop Gain at 10Hz	R_L = 6Ω	90	96		*	*		dB
Gain-Bandwidth Product			1.6			*		MHz
OUTPUT								
Voltage Swing	I_O = 5A	$\pm(\lvert V_S\rvert -5.5)$	$\pm(\lvert V_S\rvert -4.5)$		*	*		V
	I_O = 2A	$\pm(\lvert V_S\rvert -4.5)$	$\pm(\lvert V_S\rvert -3.6)$		*	*		V
	I_O = 0.5A	$\pm(\lvert V_S\rvert -4)$	$\pm(\lvert V_S\rvert -3.2)$		*	*		V
Current, Continuous	+25°C	5	7.0		*	*		A
	+85°C	4	5.0		*	*		A
	+125°C (SM grade only)				3	3.5		A
AC PERFORMANCE								
Slew Rate		6	8		*	*		V/μs
Power Bandwidth	R_L = 8Ω, V_O = 20Vrms	45	55		*	*		kHz
Settling Time to 0.1%	2V Step		2			*		μs
Capacitive Load	Specified Temperature Range, G = 1			3.3			*	nF
	Specified Temperature Range, G >10			SOA			*	
Phase Margin	Specified Temperature Range, R_L = 8Ω		40			*		Degrees
Channel Separation	1kHz, R_L = 6Ω		80			*		dB
POWER SUPPLY								
Power Supply Voltage, $\pm V_S$	Specified Temperature Range	±10	±30	±35	*	±35	±40	V
Current, Quiescent	Total—Both Amplifiers		40	50		*	*	mA
THERMAL RESISTANCE								
θ_{JC}, (Junction-to-Case)	Both Amplifiers(2), AC Output f > 60Hz		0.8	1.0		*	*	°C/W
θ_{JC}	Both Amplifiers(2), DC Output		0.9	1.2		*	*	°C/W
θ_{JC}	One Amplifier, AC Output f > 60Hz		1.25	1.5		*	*	°C/W
θ_{JC}	One Amplifier, DC Output		1.4	1.9		*	*	°C/W
θ_{JA}, (Junction-to-Ambient)	No Heat Sink		30			*		°C/W
TEMPERATURE RANGE								
Case	AM, BM	–25		+85	*		*	°C
	SM				–55		+125	°C

*Specification same as OPA2541AM.

NOTES: (1) Input bias and offset current approximately doubles for every 10°C increase in temperature. (2) Assumes equal dissipation in both amplifiers.

Output Current	see SOA
Power Dissipation, Internal(1)	125W
Input Voltage: Differential	$\pm V_S$
Common-mode	$\pm V_S$
Temperature: Pin Solder, 10s	+300°C
Junction(1)	+150°C
Temperature Range:	
Storage	–65°C to +150°C
Operating (Case)	–55°C to +125°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA2541AM	TO-3	030
OPA2541BM	TO-3	030
OPA2541SM	TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

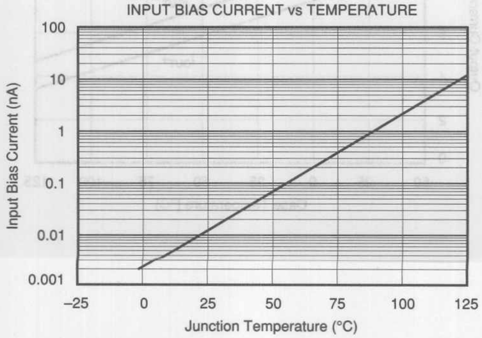
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA2541AM	TO-3	–25°C to +85°C
OPA2541BM	TO-3	–25°C to +85°C
OPA2541SM	TO-3	–55°C to +125°C

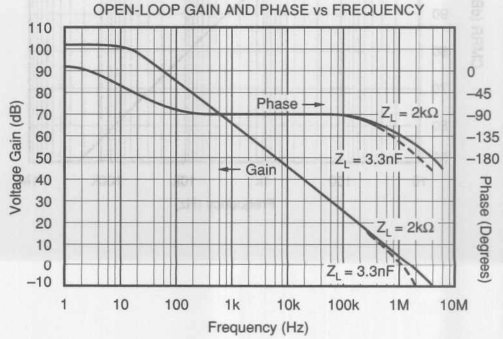
TYPICAL PERFORMANCE CURVES

T_A = +25°C and V_S = ±35VDC, unless otherwise noted.

INPUT BIAS CURRENT vs TEMPERATURE

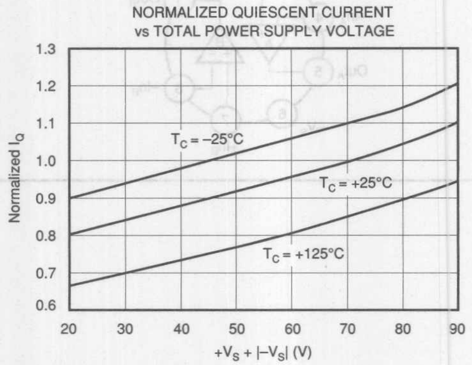


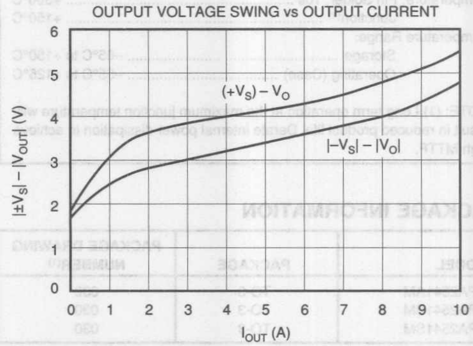
OPEN-LOOP GAIN AND PHASE vs FREQUENCY

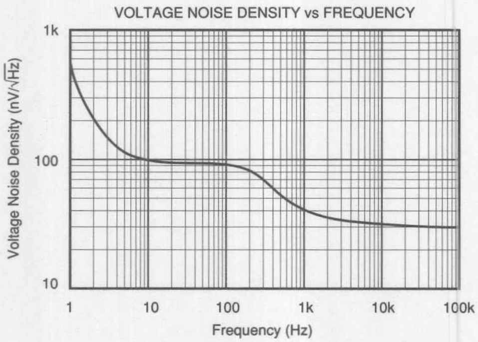


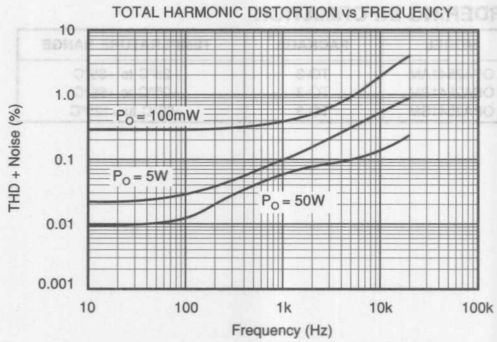
TYPICAL PERFORMANCE CURVES (CONT)

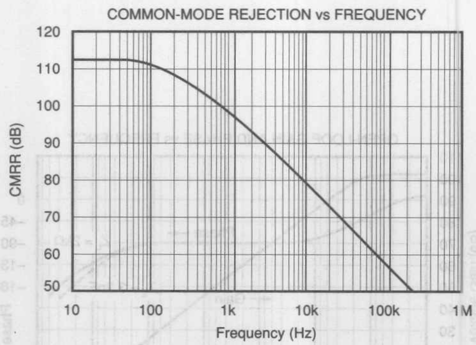
$T_A = +25°C$ and $V_S = ±35VDC$, unless otherwise noted.

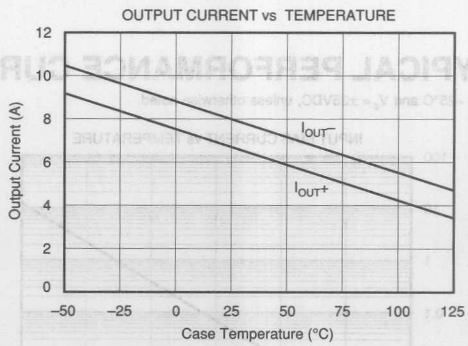








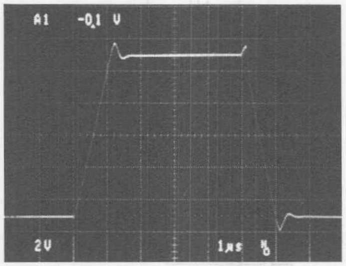




TYPICAL PERFORMANCE CURVES (CONT)

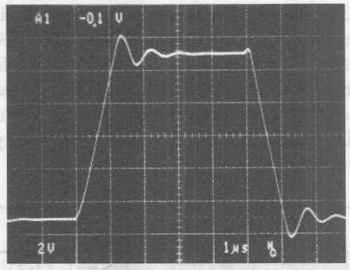
T_A = +25°C and V_S = ±35VDC, unless otherwise noted.

DYNAMIC RESPONSE



$Z_{LOAD} = \infty$, V_S = ±35V, A_V = +1

DYNAMIC RESPONSE



Z_{LOAD} = 4700pF, V_S = ±35V, A_V = +1

INSTALLATION INSTRUCTIONS

POWER SUPPLIES

The OPA2541 is specified for operation from power supplies up to ±40V. It can also be operated from an unbalanced or a single power supply so long as the total power supply voltage does not exceed 80V (70V for "AM" grade). The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier's power supply pins. Good power amplifier circuit layout is, in general, like good high-frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and instability.

Signal dependent load current can modulate the power supply voltage with inadequate power supply bypassing. This can affect both amplifiers' outputs. Since the second amplifier's signal may not be related to the first, this will degrade the inherent channel separation of the OPA2541.

HEAT SINKING

Most applications will require a heat sink to prevent junction temperatures from exceeding the 150°C maximum rating. The type of heat sink required will depend on the output signals, power dissipation of each amplifier, and ambient temperature. The thermal resistance from junction-to-case, θ_{JC}, depends on how the power dissipation is distributed on the amplifier die.

DC output concentrates the power dissipation in one output transistor. AC output distributes the power dissipation equally between the two output transistors and therefore has lower thermal resistance. Similarly, the power dissipation may be all in one amplifier (worst case) or equally distributed between the two amplifiers (best case). Thermal resistances are provided for each of these possibilities. The case-to-junction temperature rise is the product of the power dissipation (total of both amplifiers) times the appropriate thermal resistance—

$$\Delta T_{JC} = (P_D \text{ total})\ (\theta_{JC}).$$

Sufficient heat sinking must be provided to keep the case temperature within safe limits for the maximum ambient temperature and power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{HS} = (150°C - \Delta T_{JC} - T_A)/P_D.$$

Commercially available heat sinks usually specify thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the OPA2541. Since mica and other similar insulators typically add 0.7°C/W thermal resistance, this is a significant advantage. See Burr-Brown Application Bulletin AB-037 for further details on heat sinking.

SAFE OPERATING AREA

The Safe Operating Area (SOA) curve provides comprehensive information on the power handling abilities of the OPA2541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

shorted to ground, the full power supply voltage is impressed across the conducting output transistor. For instance, with $V_S = \pm35V$, a short circuit to ground would impress 35V across the conducting power transistor. The maximum safe output current at this voltage is 1.8A, so the internal current limit would not protect the amplifier. The unit-to-unit variation and temperature dependence of the internal current limit suggest that it be used to handle abnormal conditions and not activated in commonly encountered circuit operation.

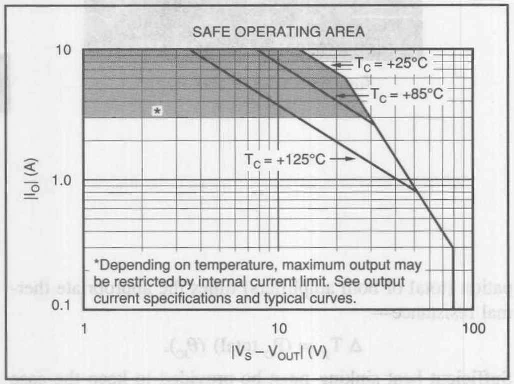


FIGURE 1. Safe Operating Area.

Reactive, or EMF generating loads such as DC motors can present demanding SOA requirements. With a purely reactive load, output voltage current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Bulletin AB-039 for further information on evaluating SOA.

Applications with inductive or EMF-generating loads which can produce "kick back" voltage surges to the amplifiers should include clamp diodes from the output terminals to the power supplies. These diodes should be chosen to limit the peak amplifier output voltage surges to less than 2V beyond the power supply rail voltage. Common 1A rated rectifier diodes will suffice in most applications.

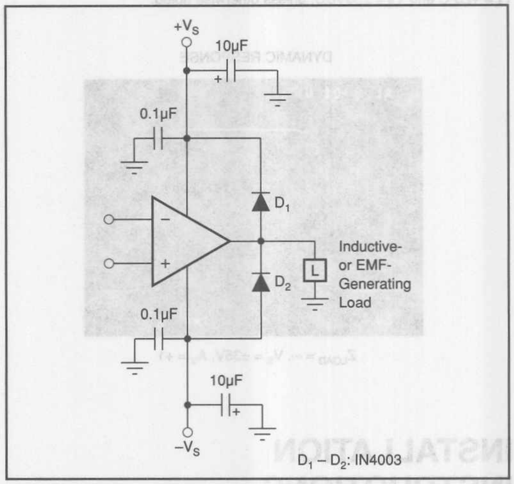


FIGURE 2. Clamping Output for EMF-Generating Loads.

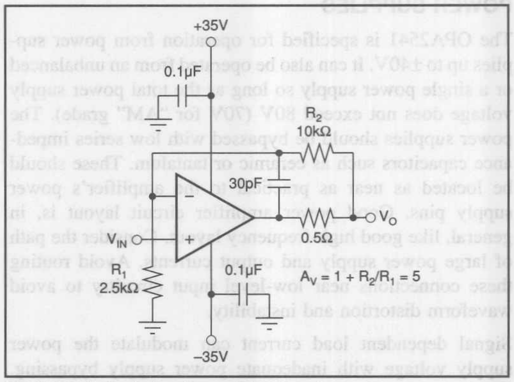


FIGURE 3. Isolating Capacitive Loads.

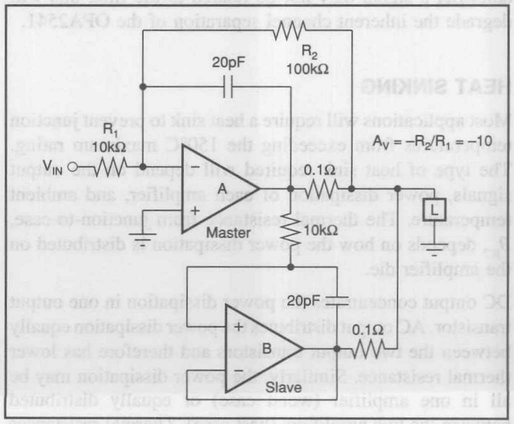


FIGURE 4. Paralleled Operation, Extended SOA.

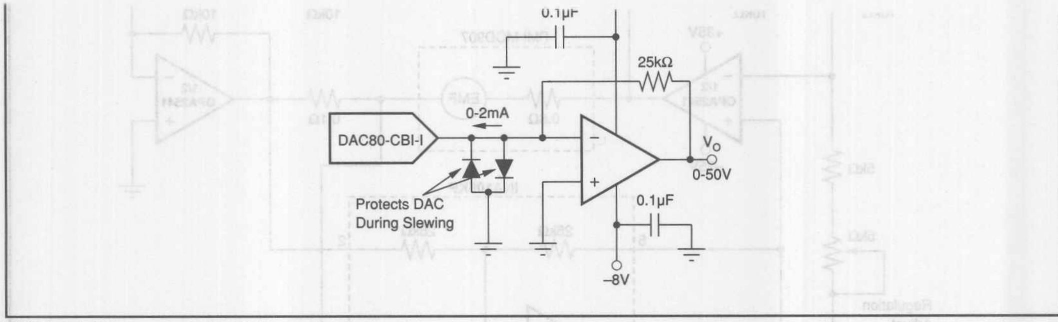


FIGURE 5. Programmable Voltage Source.

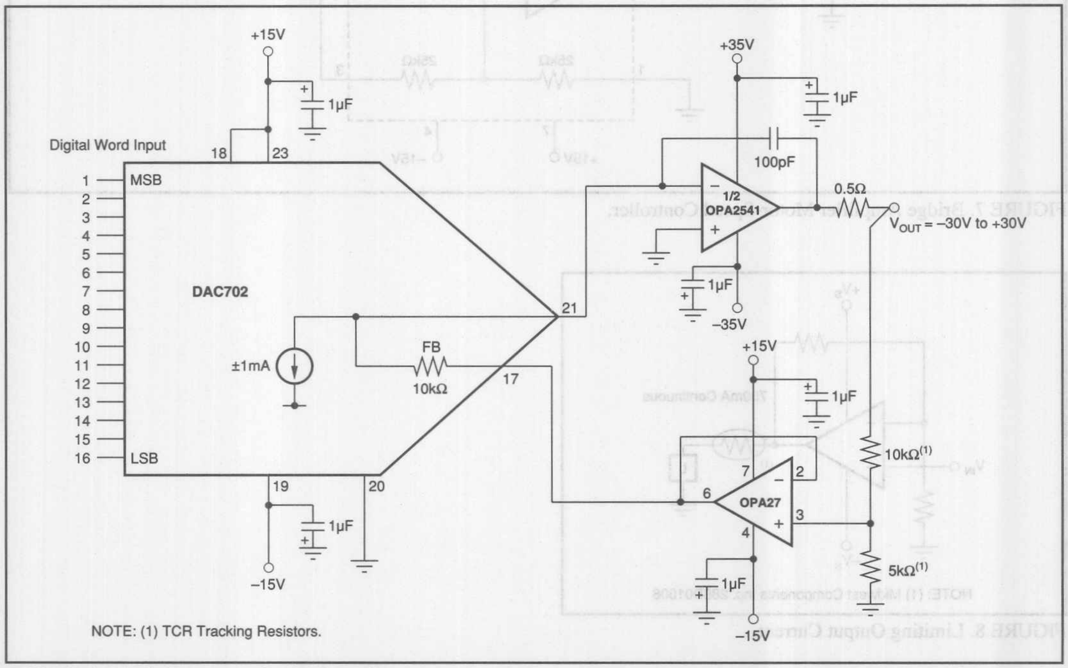


FIGURE 6. 16-Bit Programmable Voltage Source.

OPA2541

3.2

POWER OPERATIONAL AMPLIFIERS

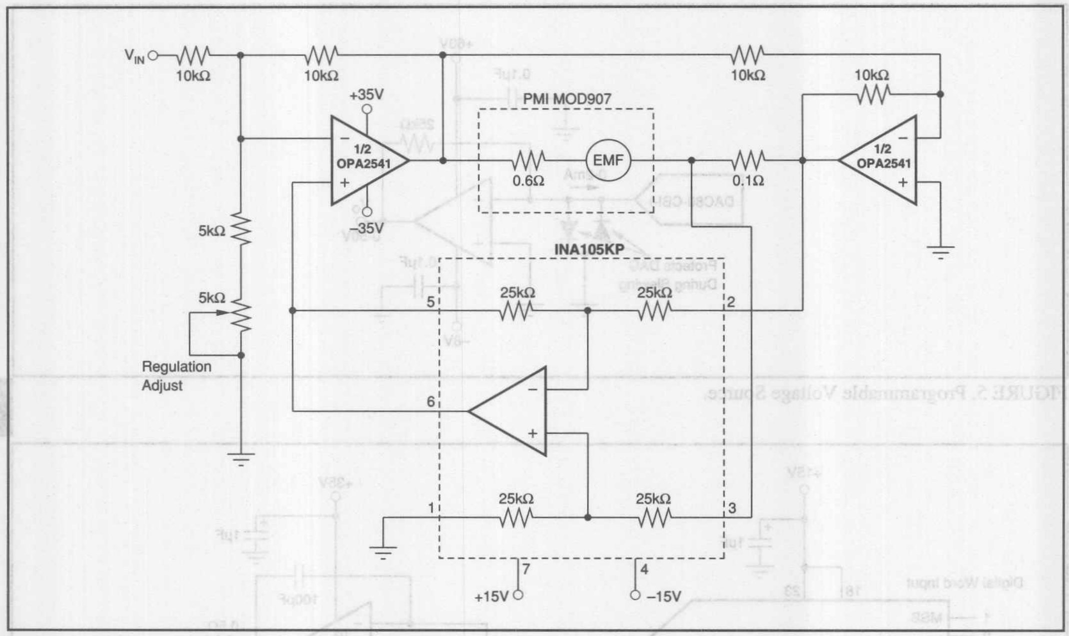


FIGURE 7. Bridge Amplifier Motor-Speed Controller.

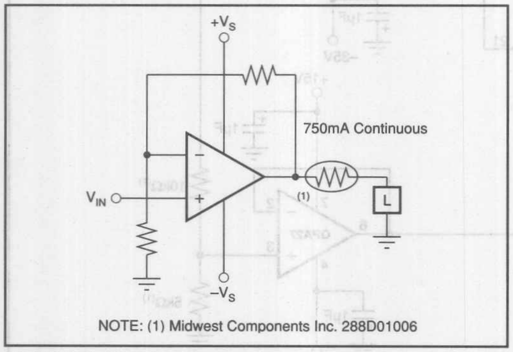
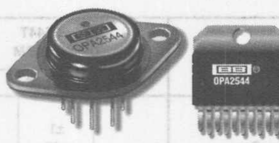


FIGURE 8. Limiting Output Current.

BURR - BROWN®



OPA2544

High-Voltage, High-Current DUAL OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: 2A min
- WIDE POWER SUPPLY RANGE: ±10V to ±35V
- SLEW RATE: 8V/µs
- INTERNAL CURRENT LIMIT
- THERMAL SHUTDOWN PROTECTION
- FET INPUT: I_B = 50pA max
- 8-PIN HERMETIC TO-3 AND 11-LEAD PLASTIC PACKAGES

APPLICATIONS

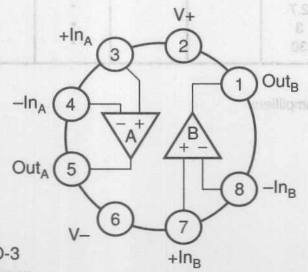
- MOTOR DRIVER
- PROGRAMMABLE POWER SUPPLY
- SERVO AMPLIFIER
- VALVES, ACTUATOR DRIVER
- MAGNETIC DEFLECTION COIL DRIVER
- AUDIO AMPLIFIER

DESCRIPTION

The OPA2544 is a dual high-voltage/high-current operational amplifier suitable for driving a wide variety of high power loads. It provides 2A output current and power supply voltage range extends to ±35V.

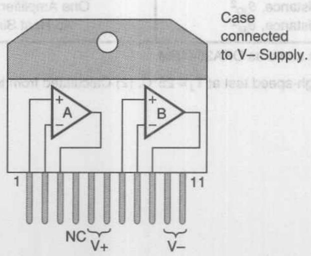
The OPA2544 integrates two high performance FET op amps with high power output stages on a single monolithic chip. Internal current limit and thermal shutdown protect the amplifier and load from damage.

The OPA2544 is available in a hermetic 8-pin metal TO-3, and 11-lead plastic packages. Models are available in –40°C to +85°C, and –55°C to +125°C temperature ranges.



TO-3 Package Electrically Isolated

Top View



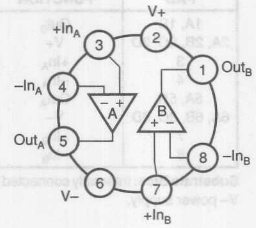
International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At T_{CASE} = +25°C and V_S = ±35V, unless otherwise noted.

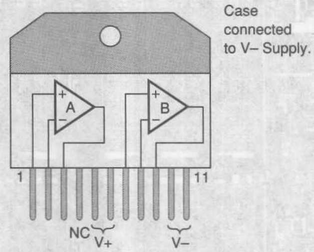
		OPA2544T OPA2544BM			OPA2544SM			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE								
Input Offset Voltage			±1	±5		*	*	mV
vs Temperature	Specified Temp. Range		±10			*		μV/°C
vs Power Supply	V_S = ±10V to ±35V		±10	±100		*	*	μV/V
INPUT BIAS CURRENT(1)								
Input Bias Current	V_{CM} = 0V		±15	±50		*	*	pA
vs Temperature			Doubles every 10°C			*		
Input Offset Current	V_{CM} = 0V		±10	±50		*	*	pA
NOISE								
Input Voltage Noise								
Noise Density, f = 1kHz			36			*		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz			3			*		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE								
Common-Mode Input Range								
Positive	Linear Operation	(V+) –6	(V+) –4		*	*		V
Negative	Linear Operation	(V–) +6	(V–) +4		*	*		V
Common-Mode Rejection	$V_{CM} = \pm V_S$-6V	90	106		*	*		dB
INPUT IMPEDANCE								
Differential			10^{12} || 8			*		Ω || pF
Common-Mode			10^{12} || 10			*		Ω || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±30V, R_L = 15Ω	90	103		*	*		dB
FREQUENCY RESPONSE								
Gain-Bandwidth Product	R_L = 15Ω		1.4			*		MHz
Slew Rate	60Vp-p, R_L = 15Ω	5	8		*	*		V/μs
Full-Power Bandwidth			See Typical Curve			*		
Settling Time 0.1%	G = –10, 60V Step		25			*		μs
Total Harmonic Distortion			See Typical Curve			*		
OUTPUT								
Voltage Output: Positive	I_O = 2A	(V+) –5	(V+) –4.4		*	*		V
Negative	I_O = 2A	(V–) +5	(V–) +3.8		*	*		V
Positive	I_O = 0.5A	(V+) –4.2	(V+) –3.8		*	*		V
Negative	I_O = 0.5A	(V–) +4	(V–) +3.1		*	*		V
Current Output			See SOA Curves			*		
Short-Circuit Current			±4			*		A
POWER SUPPLY								
Specified Operating Voltage			±35			*		V
Operating Voltage Range		±10		±35	*		*	V
Quiescent Current (total)	I_O = 0		±22	±30		*	*	mA
TEMPERATURE RANGE								
Operating Range		–40		+85	–55		+125	°C
Storage, Metal TO-3 Package		–65		+125	*		*	°C
Plastic Package		–40		+125				°C
Thermal Resistance, θ_{JC}[2]	Both Amplifiers, f > 50Hz		2			*		°C/W
Thermal Resistance, θ_{JC}[2]	Both Amplifiers, DC		2.5			*		°C/W
Thermal Resistance, θ_{JC}[2]	One Amplifier, f > 50Hz		2.7			*		°C/W
Thermal Resistance, θ_{JC}[2]	One Amplifier, DC		3			*		°C/W
Thermal Resistance, θ_{JA}[2]	No Heat Sink		30			*		°C/W

* Specifications same as OPA2544BM.

NOTES: (1) High-speed test at T_J = 25°C. (2) Calculated from total power dissipation of both amplifiers.



Case is electrically isolated.



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA2544T	11-Lead Plastic	–40°C to +85°C
OPA2544BM	8-Pin Metal TO-3	–40°C to +85°C
OPA2544SM	8-Pin Metal TO-3	–55°C to +125°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA2544T	11-Lead Plastic	242
OPA2544BM	8-Pin Metal TO-3	030
OPA2544SM	8-Pin Metal TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

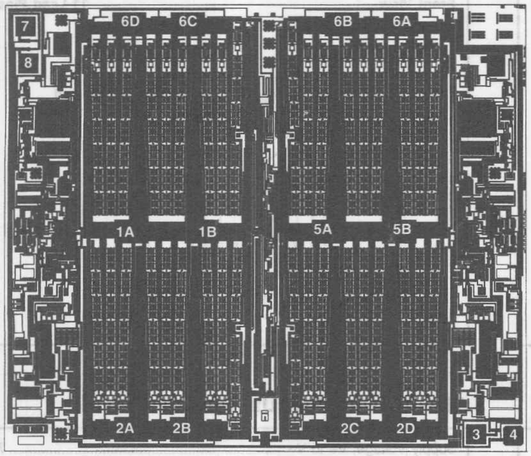
Supply Voltage, V+ to V–	70V
Output Current	See SOA Curve
Input Voltage	(V–) –0.7V to (V+) +0.7V
Operating Temperature	–55°C to +125°C
Storage Temperature, Metal TO-3 Package	–55°C to +125°C
Plastic Package	–40°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, –10s)	300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DICE INFORMATION



OPA2544 DIE TOPOGRAPHY

PAD	FUNCTION
1A, 1B	Out_B
2A, 2B, 2C, 2D	V+
3	$+In_A$
4	$-In_A$
5A, 5B	Out_A
6A, 6B, 6C, 6D	V–
7	$+In_B$
8	$-In_B$

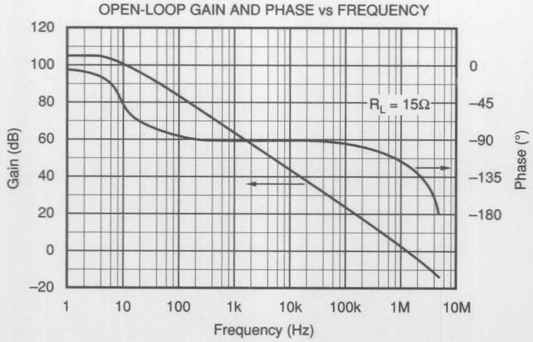
Substrate Bias: Internally connected to V– power supply.

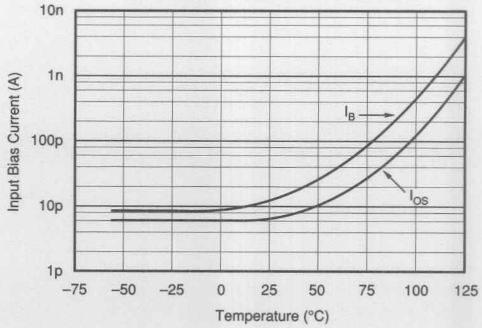
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	218 x 252 ±5	8.58 x 9.92 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Chromium-Silver

TYPICAL PERFORMANCE CURVES

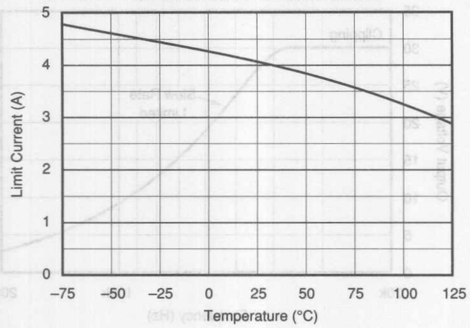
T_{CASE} = +25°C, V_S = ±35V unless otherwise noted.



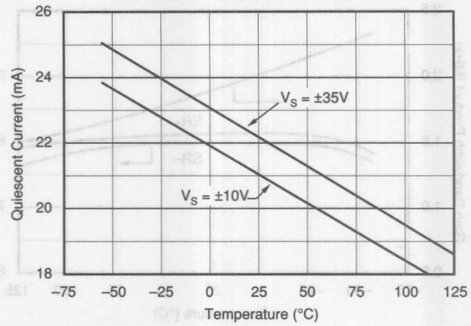


TYPICAL PERFORMANCE CURVES (CONT)

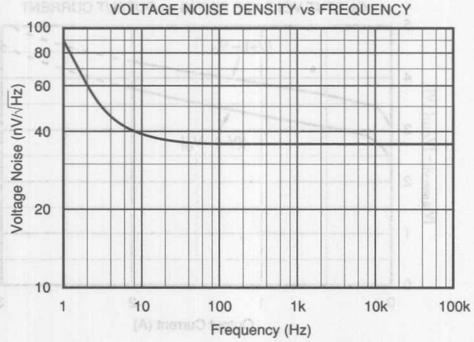
At T_{CASE} = +25°C and V_S = ±35V, unless otherwise noted.



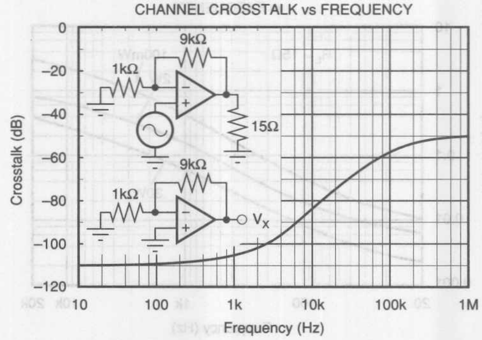
CURRENT LIMIT vs TEMPERATURE



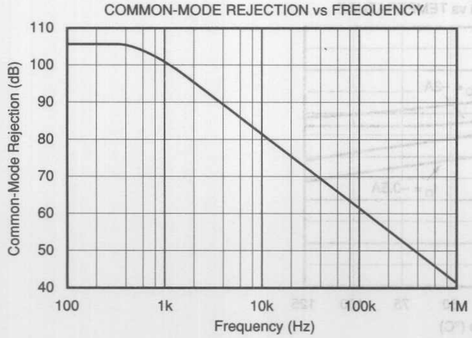
QUIESCENT CURRENT vs TEMPERATURE



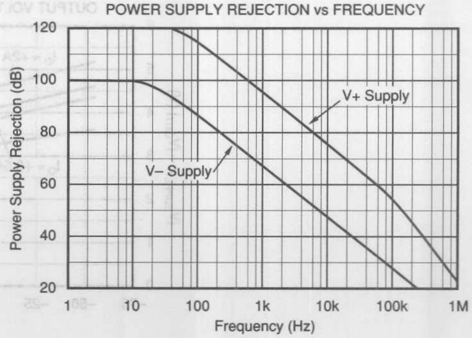
VOLTAGE NOISE DENSITY vs FREQUENCY



CHANNEL CROSSTALK vs FREQUENCY



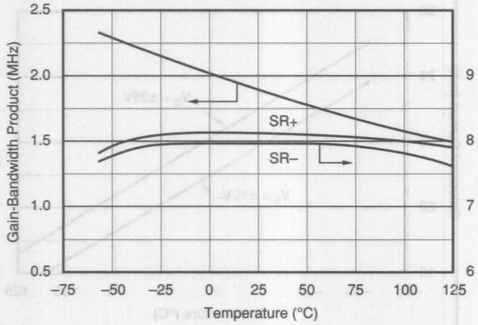
COMMON-MODE REJECTION vs FREQUENCY



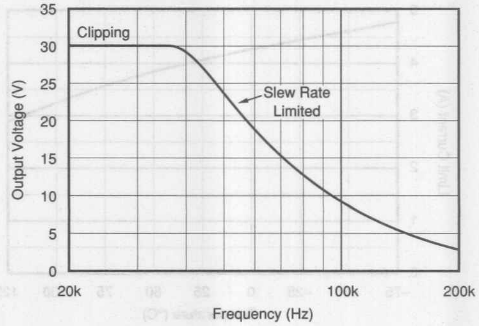
POWER SUPPLY REJECTION vs FREQUENCY

At T_{CASE} = +25°C and V_S = ±35V, unless otherwise noted.

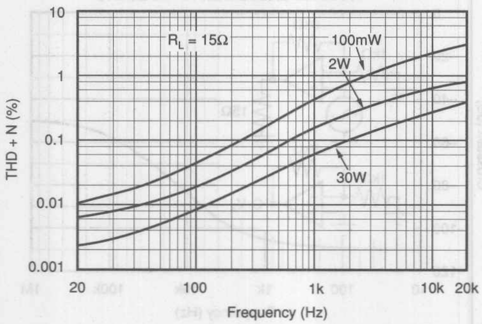
GAIN-BANDWIDTH PRODUCT AND SLEW RATE vs TEMPERATURE



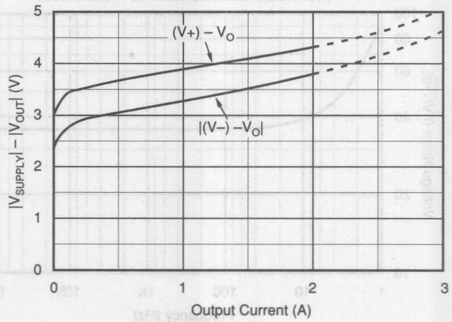
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



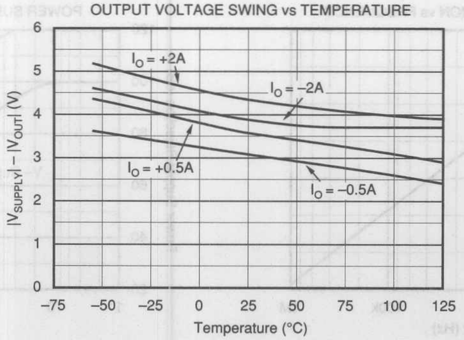
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



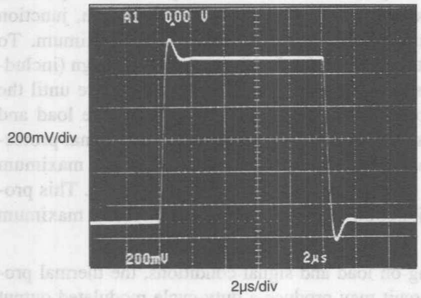
OUTPUT VOLTAGE SWING vs TEMPERATURE



At T_{CASE} = +25°C and V_S = ±35V, unless otherwise noted.

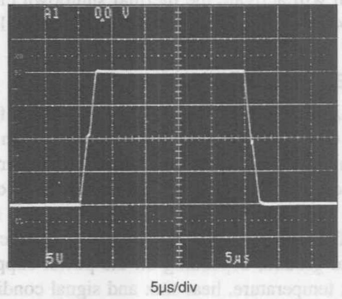
SMALL SIGNAL RESPONSE

G = 3, C_L = 1nF



LARGE SIGNAL RESPONSE

G = 3, R_L = 15Ω



APPLICATIONS INFORMATION

Figure 1 shows the OPA2544 connected as a basic non-inverting amplifier. The OPA2544 can be used in virtually any op amp configuration. Power supply terminals should be bypassed with low series impedance capacitors. The technique shown, using a ceramic and tantalum type in parallel, is recommended. Power supply wiring should have low series impedance and inductance.

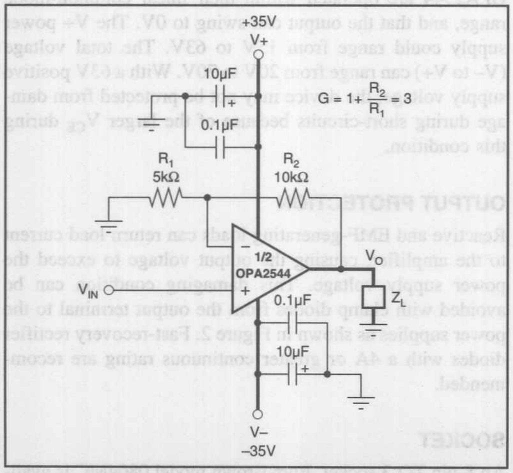


FIGURE 1. Basic Circuit Connections.

SAFE OPERATING AREA

Stress on the output transistors is determined by the output current and the voltage across the conducting output transistor, V_{CE}. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, V_{CE}. The Safe Operating Area (SOA curve, Figure 2) shows the permissible range of voltage and current.

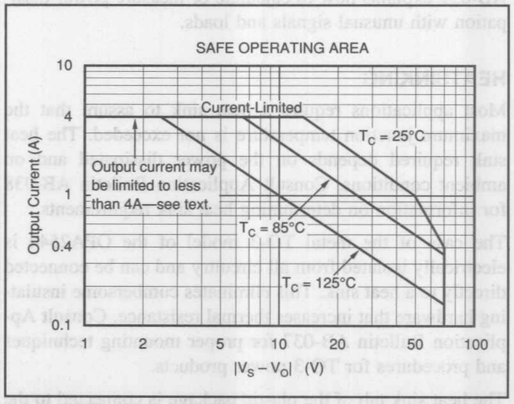


FIGURE 2. Safe Operating Area.

The safe output current decreases as V_{CE} increases. Output short-circuit is a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage (V+ or V–) across the conducting transistor. With $V_S = \pm35V$ the safe output current is 1.5A (at 25°C). The short-circuit current is approximately 4A which exceeds the SOA. This situation will activate the thermal shutdown circuit in the OPA2544. For further insight on SOA, consult AB-039.

CURRENT LIMIT

The OPA2544 has an internal current limit set for approximately 4A. This current limit decreases with increasing junction temperature as shown in the typical curve, Current Limit versus Temperature. This, in combination with the thermal shutdown circuit, provides protection from many types of overload. It may not, however, protect for short-circuit to ground, depending on the power supply voltage, ambient temperature, heat sink and signal conditions.

POWER DISSIPATION

Power dissipation depends on power supply, signal and load conditions. For DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power supply voltage. Dissipation with AC signals is lower. Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

HEATSINKING

Most applications require a heat sink to assure that the maximum junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions. Consult Application Bulletin AB-038 for information on determining heat sink requirements.

The case of the metal TO-3 model of the OPA2544 is electrically isolated from all circuitry and can be connected directly to a heat sink. This eliminates cumbersome insulating hardware that increases thermal resistance. Consult Application Bulletin AB-037 for proper mounting techniques and procedures for TO-3 power products.

The heat sink tab of the plastic package is connected to the V– power supply terminal. Lowest thermal resistance can be achieved by mounting the tab directly to a heat sink. If the heat sink cannot be electrically "hot" at V– power supply potential, insulating hardware must be used.

THERMAL PROTECTION

The OPA2544 has thermal shutdown that protects the amplifier from damage. Any tendency to activate the thermal shutdown circuit during normal operation is indication of excessive power dissipation or an inadequate heat sink.

The thermal protection activates at a junction temperature of approximately 155°C. For reliable operation, junction temperature should be limited to 150°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection should trigger more than 25°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

Depending on load and signal conditions, the thermal protection circuit may produce a duty-cycle modulated output signal. This limits the dissipation in the amplifier, but the rapidly varying output waveform may be damaging to some loads. The thermal protection may behave differently depending on whether internal dissipation is produced by sourcing or sinking output current.

UNBALANCED POWER SUPPLIES

Some applications do not require equal positive and negative output voltage swing. The power supply voltages of the OPA2544 do not need to be equal. For example, a –7V negative power supply voltage assures that the inputs of the OPA2544 are operated within their linear common-mode range, and that the output can swing to 0V. The V+ power supply could range from 15V to 63V. The total voltage (V– to V+) can range from 20V to 70V. With a 63V positive supply voltage, the device may not be protected from damage during short-circuits because of the larger V_{CE} during this condition.

OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies as shown in Figure 2. Fast-recovery rectifier diodes with a 4A or greater continuous rating are recommended.

SOCKET

An 8-pin TO-3 socket, Burr-Brown model 0804MC is available. Although not required, this socket makes mounting and interchanging parts easy, especially during design and testing.

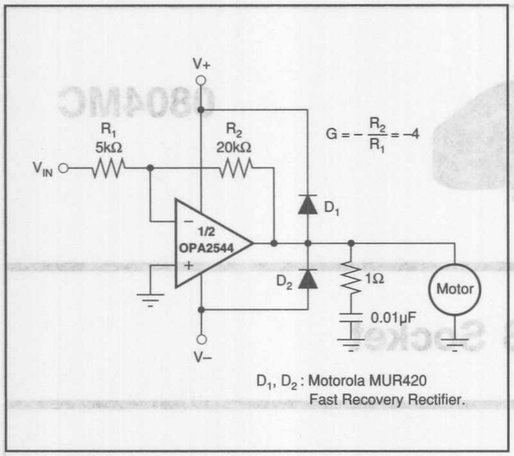


FIGURE 3. Motor Drive Circuit.

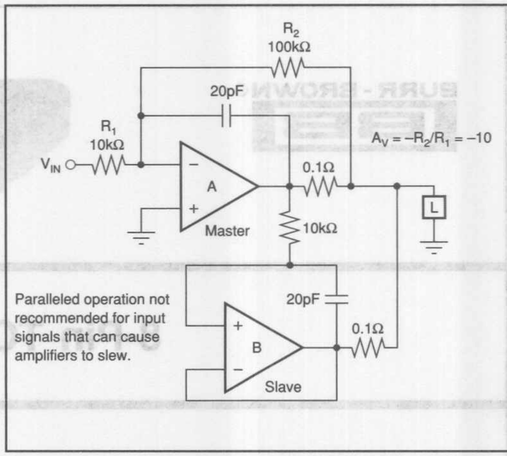


FIGURE 5. Paralleled Operation, Extended SOA.

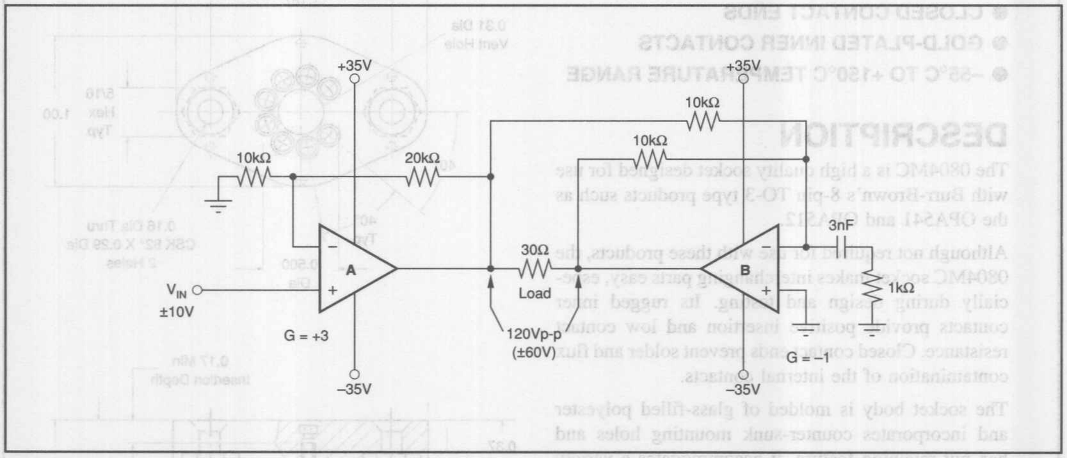
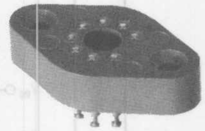


FIGURE 4. Bridge Drive Circuit.

BURR - BROWN®



0804MC

8-Pin TO-3 Socket

FEATURES

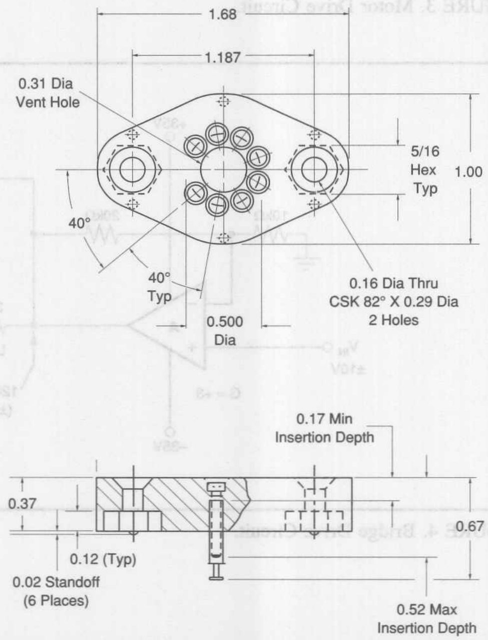
- LOW CONTACT RESISTANCE
- CLOSED CONTACT ENDS
- GOLD-PLATED INNER CONTACTS
- –55°C TO +150°C TEMPERATURE RANGE

DESCRIPTION

The 0804MC is a high quality socket designed for use with Burr-Brown's 8-pin TO-3 type products such as the OPA541 and OPA512.

Although not required for use with these products, the 0804MC socket makes interchanging parts easy, especially during design and testing. Its rugged inner contacts provide positive insertion and low contact resistance. Closed contact ends prevent solder and flux contamination of the internal contacts.

The socket body is molded of glass-filled polyester and incorporates counter-sunk mounting holes and hex-nut retaining feature. It accommodates a variety of mounting hardware and mechanical designs.



Contact Resistance: 0.02Ω Typ

Outer Contact: Brass
200µ inch Tin over 100µ inch Nickel Plate

Inner Contact: BeCu
30µ inch Gold over 50µ inch Nickel Plate

Socket Body: Glass-Filled Polyester, 94 V-0 rating

Operating Temperature Range: –55°C to +150°C

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

BURR - BROWN®

High Voltage, High Current OPERATIONAL AMPLIFIER

FEATURES

- WIDE POWER SUPPLY VOLTAGE: ±70V to ±150V
- OUTPUT CURRENT TO 75mA
- SLEW RATE: 30V/μs
- FET INPUT: I_B = 20pA max
- THERMAL SHUT-DOWN PROTECTION
- HERMETIC TO-3 PACKAGE, ISOLATED CASE

APPLICATIONS

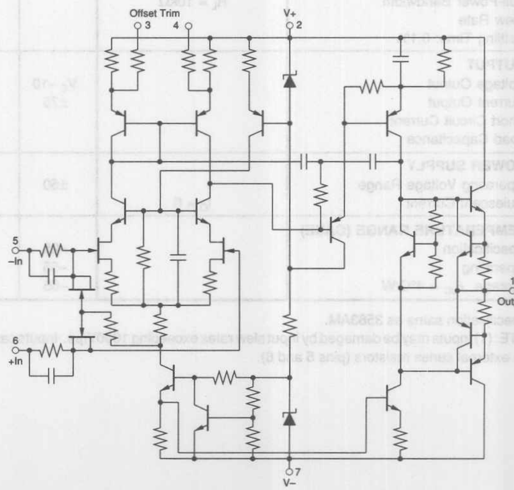
- PROGRAMMABLE POWER SUPPLY
- PIEZO-ELECTRIC TRANSDUCER DRIVER
- HIGH VOLTAGE CURRENT SOURCE

DESCRIPTION

The 3583 is a high voltage, high speed hybrid operational amplifier designed for a wide variety of programmable power supply and transducer driver applications.

The 3583 operates over a wide power supply range (±50V to ±150V) and provides outputs up to 75mA. Laser-trimmed FET input circuitry provides low offset voltage (3mV max) and low input bias current (20pA max). Thermal shut-down circuitry protects internal circuitry from excessive power dissipation.

Commercial and industrial temperature range models are available. The 3583's hermetic 8-pin TO-3 package is electrically isolated from all internal circuitry.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

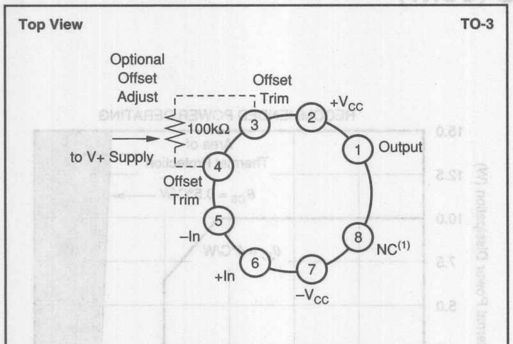
T_{CASE} = +25°C, V_S = ±150V, unless otherwise noted.

PARAMETER	CONDITIONS	3583AM MIN	3583AM TYP	3583AM MAX	3583JM MIN	3583JM TYP	3583JM MAX	UNITS
OFFSET VOLTAGE								
Input Offset Voltage				±3			*	mV
vs Temperature	Specified Temp. Range			±23			*	µV/°C
vs Power Supply			20			*		µV/V
vs Time			50			*		µV/month
INPUT BIAS CURRENT(1)								
Input Bias Current	V_{CM} = 0V			−20			*	pA
vs Temperature			Doubles Every 10°C			*		
vs Power Supply			0.2			*		pA/V
Input Offset Current	V_{CM} = 0V			±20			*	pA
vs Temperature			Doubles Every 10°C			*		
vs Power Supply			0.2			*		pA/V
NOISE								
Voltage, 0.01Hz to 10Hz			5			*		µVp-p
10Hz to 1kHz			1.7			*		µVrms
Current, 0.01Hz to 10Hz			0.3			*		pAp-p
INPUT VOLTAGE RANGE								
Max Safe Differential Input			(V+) + |V−|			*		
Max Safe Common-Mode Input			V− to V+			*		
Common-Mode Input Range	Linear Operation		V_S −10			*		V
Common-Mode Rejection			110			*		dB
INPUT IMPEDANCE								
Differential			10^{11} || 10			*		Ω || pF
Common-Mode			10^{11}			*		Ω || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	No Load, DC		118			*		dB
Open-Loop Voltage Gain	Rated Load, DC	94	105		*	*		dB
FREQUENCY RESPONSE								
Unity-Gain Bandwidth	Small-Signal		5			*		MHz
Full-Power Bandwidth	R_L = 10kΩ		60			*		kHz
Slew Rate			30			*		V/µs
Settling Time: 0.1%			12			*		µs
OUTPUT								
Voltage Output		V_S −10			*			V
Current Output		±75			*			mA
Short Circuit Current			±100			*		mA
Load Capacitance				10			*	nF
POWER SUPPLY								
Operating Voltage Range		±50		±150	*		*	V
Quiescent Current	I_O = 0			±8.5			*	mA
TEMPERATURE RANGE (CASE)								
Specification		−25		+85	0		+70	°C
Operating		−55		+125	*		*	°C
Storage θ_{JC} = 4°C/W		−55		+125	*		*	°C

* Specification same as 3583AM.

NOTE: (1) Inputs may be damaged by input slew rates exceeding 1000V/µs. Inputs can be protected from signals exceeding 1000V/µs by limiting input current to 150mA with external series resistors (pins 5 and 6).

CONNECTION DIAGRAM



NOTE: (1) No internal connection.
Optional socket available: 804MC

PACKAGING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
3583AM	8-Pin TO 3	030
3583JM	8-Pin TO 3	030

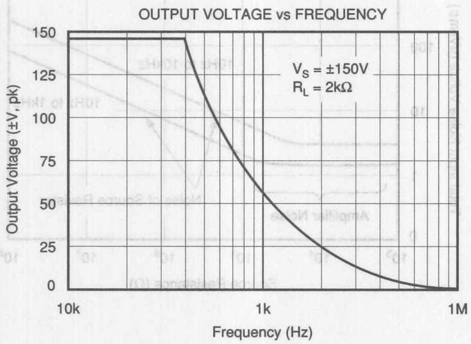
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

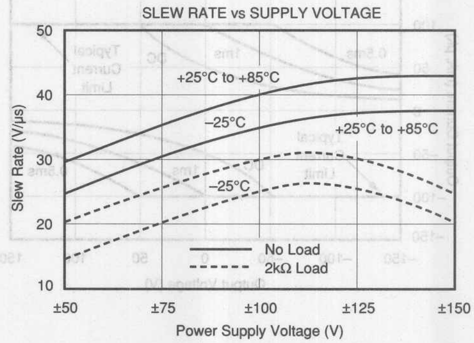
ORDERING INFORMATION

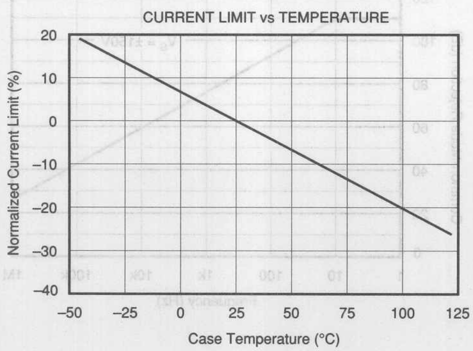
MODEL	PACKAGE	TEMPERATURE RANGE
3583AM	8-Pin TO-3	–25°C to +85°C
3583JM	8-Pin TO-3	0°C to +70°C

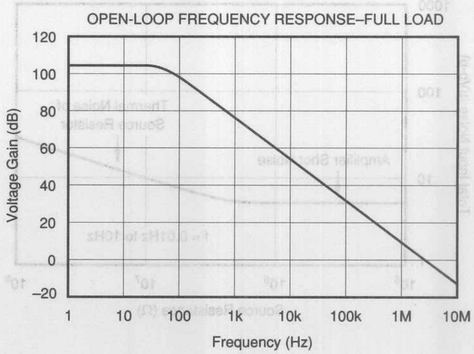
TYPICAL PERFORMANCE CURVES

T_{CASE} = +25°C, $\pm V_{CC}$ = 150VDC, unless otherwise noted.



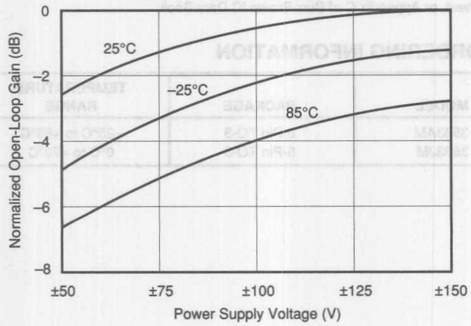




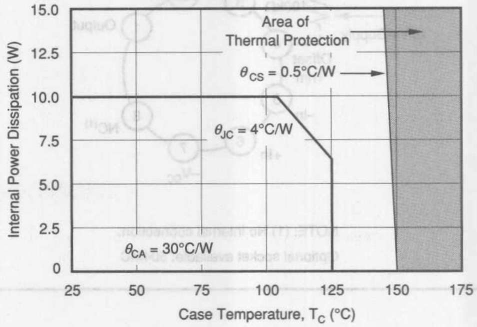


T_{CASE} = +25°C, $\pm V_{CC}$ = 150VDC, unless otherwise noted.

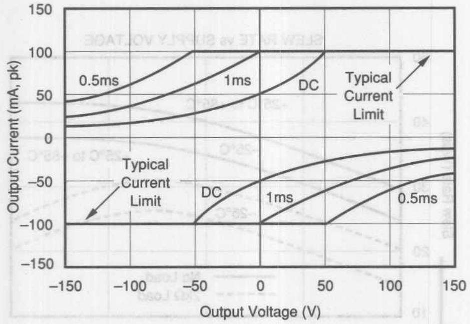
OPEN-LOOP GAIN vs SUPPLY VOLTAGE AT FULL LOAD



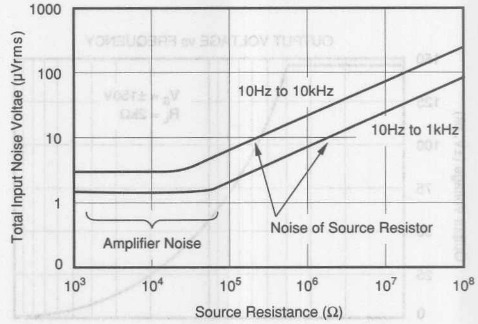
RECOMMENDED POWER DERATING



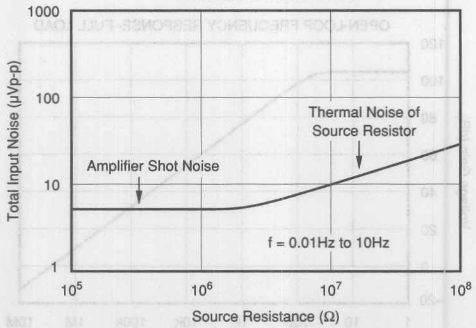
SAFE OPERATING AREA



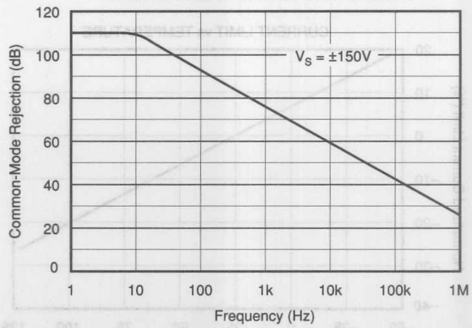
TOTAL INPUT NOISE VOLTAGE vs SOURCE RESISTANCE



TOTAL LOW FREQUENCY INPUT NOISE vs SOURCE RESISTANCE

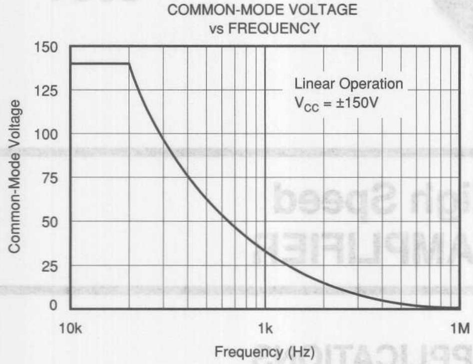


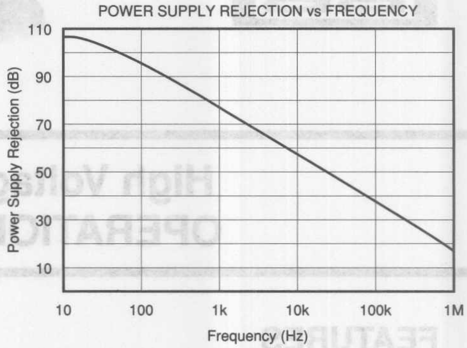
COMMON-MODE REJECTION vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

T_{CASE} = +25°C, ±V_{CC} = 150VDC, unless otherwise noted.





APPLICATION INFORMATION

Figure 1 shows the basic connections required to operate the 3583. Power supply bypass capacitors should be connected close to the device pins. Be sure that these capacitors have an adequate voltage rating.

Input offset voltage and drift of the 3583 are laser-trimmed. Many applications require no external offset trimming. Figure 1 also shows connection of an optional offset trim potentiometer connected to pins 3 and 4.

FET input circuitry reduces the input bias current of the 3583 to less than 20pA at room temperature. Input bias current remains nearly constant throughout the full common-mode range. Input bias current approximately doubles for each 10°C increase in case temperature above 25°C. Heat sinking can help minimize this effect by reducing the case temperature.

Input circuitry of the 3583 is protected with series limiting resistors and input clamp diodes. The inputs can withstand the full rated supply voltage of ±150V (common-mode or differential).

THERMAL PROTECTION

The 3583 has internal thermal shut-down circuitry that activates at a case temperature of approximately 150°C or higher. As this circuitry is activated, the output current drive is reduced. As the case temperature returns to less than the activation temperature, operation will return to normal. A heat sink may be required depending on load and signal conditions.

Note that a 75mA output may not be safe for all output voltages—see typical performance curve "Safe Operating Area". Applications such as current sources where output voltage may be low (or the opposite polarity of the output current) can overstress the output stage.

The thermal shut-down circuit will normally protect the amplifier during a short-circuit to ground. It will not protect against short-circuit to one of the power supplies. The typical performance curve "Safe Operating Area" shows that the large stress occurring during this high voltage condition may cause damage if it exceeds 5ms duration. The thermal protection circuitry will not activate fast enough to protect the device from short-circuits to one of the power supplies.

The package case of the 3583 is electrically isolated from all circuitry. No special insulating hardware is required. Although not absolutely required, it is recommended that the case be connected to ground.

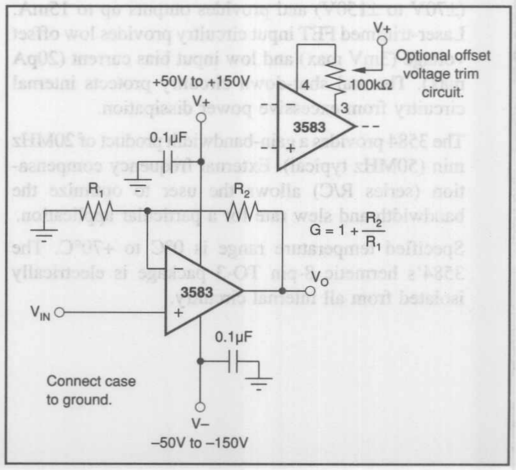
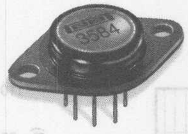


FIGURE 1. Basic Circuit Connections.

BURR - BROWN®



3584

High Voltage, High Speed OPERATIONAL AMPLIFIER

FEATURES

- WIDE POWER SUPPLY VOLTAGE: ±70V to ±150V
- GAIN-BANDWIDTH PRODUCT: 50MHz
- SLEW RATE: 150V/µs
- FET INPUT: I_B = 20pA max
- THERMAL SHUT-DOWN PROTECTION
- HERMETIC TO-3 PACKAGE, ISOLATED CASE

APPLICATIONS

- PROGRAMABLE POWER SUPPLY
- PIEZO-ELECTRIC TRANSDUCER DRIVER
- ELECTROSTATIC TRANSDUCER DRIVER
- CRT DEFLECTION

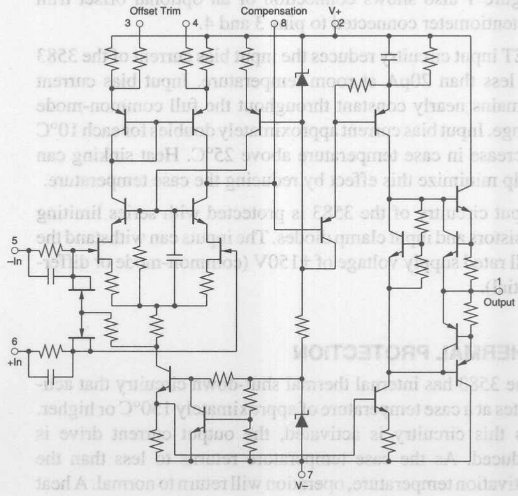
DESCRIPTION

The 3584 is a high voltage, high speed hybrid operational amplifier designed for a wide variety of programmable power supply and transducer driver applications.

The 3584 operates over a wide power supply range (±70V to ±150V) and provides outputs up to 15mA. Laser-trimmed FET input circuitry provides low offset voltage (3mV max) and low input bias current (20pA max). Thermal shut-down circuitry protects internal circuitry from excessive power dissipation.

The 3584 provides a gain-bandwidth product of 20MHz min (50MHz typical). External frequency compensation (series R/C) allows the user to optimize the bandwidth and slew rate for a particular application.

Specified temperature range is 0°C to +70°C. The 3584's hermetic 8-pin TO-3 package is electrically isolated from all internal circuitry.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-376B

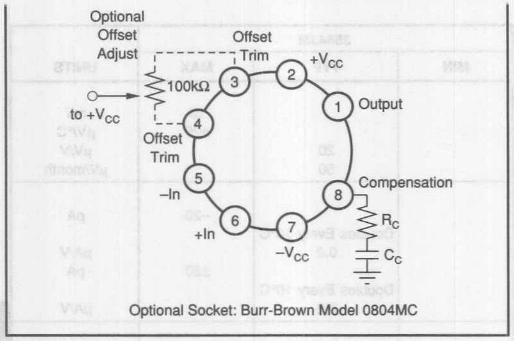
SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, V_S = ±150V, unless otherwise noted.

PARAMETER	CONDITIONS	3584JM MIN	3584JM TYP	3584JM MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage				±3	mV
vs Temperature	Specified Temperature Range			±25	µV/°C
vs Power Supply			20		µV/V
vs Time			50		µV/month
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V			−20	pA
vs Temperature			Doubles Every 10°C		
vs Power Supply			0.2		pA/V
Input Offset Current	V_{CM} = 0V			±20	pA
vs Temperature			Doubles Every 10°C		
vs Power Supply			0.2		pA/V
NOISE					
Voltage, 0.01Hz to 10Hz			5		µVp-p
10Hz to 1kHz			1.7		µVrms
Current, 0.01Hz to 10Hz			0.3		pAp-p
INPUT VOLTAGE RANGE					
Maximum Safe Differential Input			(V+) + |V−|		
Maximum Safe Common-Mode Input			V− to V+		
Common-Mode Input Range	Linear Operation		V_S − 10		V
Common-Mode Rejection			110		dB
INPUT IMPEDANCE					
Differential			10^{11}||10		Ω || pF
Common-Mode			10^{11}		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	No Load, DC		120		dB
Open-Loop Voltage Gain	Rated Load, DC	100			dB
FREQUENCY RESPONSE					
Unity-Gain Bandwidth	Small-Signal		7		MHz
Gain-Bandwidth Product	f = 1kHz, G = 100	20			MHz
Full-Power Bandwidth	G = 100		135		kHz
Slew Rate	G = 100		150		V/µs
Settling Time: 0.1%	G = 100		12		µs
OUTPUT					
Voltage Output		V_S - 5			V
Current Output		±15			mA
Short Circuit Current			±25		mA
Load Capacitance (Maximum)			10		nF
POWER SUPPLY					
Operating Voltage Range		±70		±150	V
Quiescent Current	I_O = 0			±6.5	mA
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		−55		+125	°C
Storage		−55		+150	°C

NOTE: (1) Inputs may be damaged by input slew rates exceeding 1000V/µs. Inputs can be protected from signals exceeding 1000V/µs by limiting input current to 150mA with external series resistors (pins 5 and 6).



3584JM	8-Pin TO-3	0°C to +70°C

PACKAGE INFORMATION

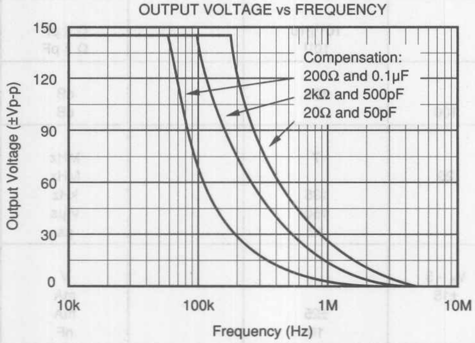
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
3584JM	8-Pin TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

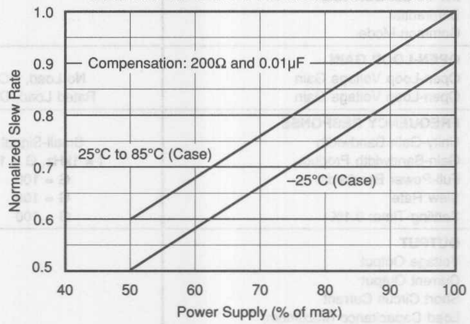
TYPICAL PERFORMANCE CURVES

T_{CASE} = +25°C, V_S = ±150V, unless otherwise noted.

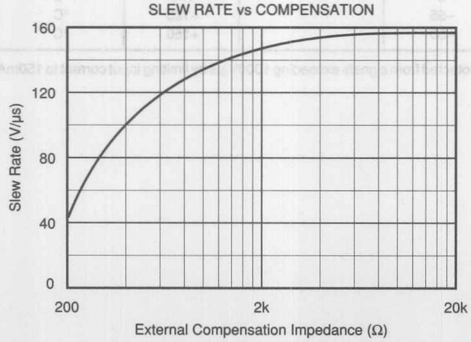
OUTPUT VOLTAGE vs FREQUENCY



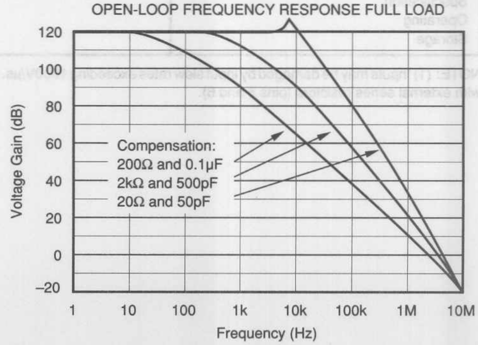
SLEW RATE vs SUPPLY VOLTAGE AT FULL LOAD



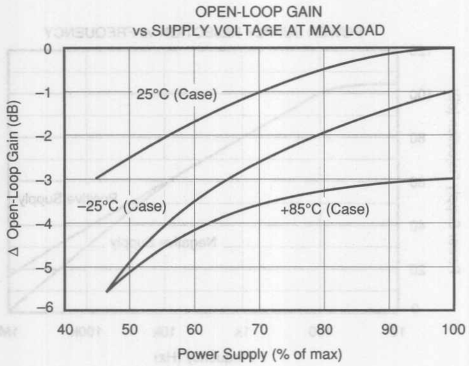
SLEW RATE vs COMPENSATION

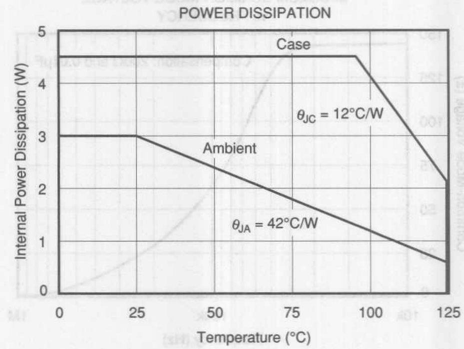


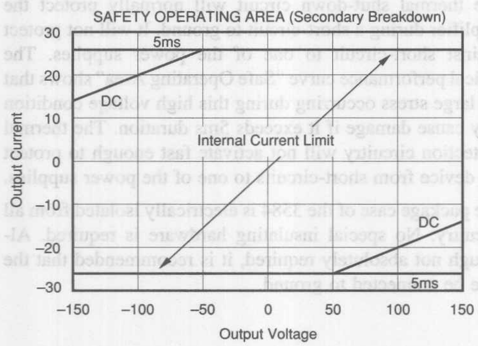
OPEN-LOOP FREQUENCY RESPONSE FULL LOAD

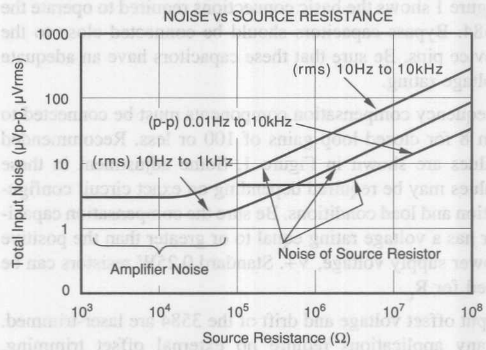


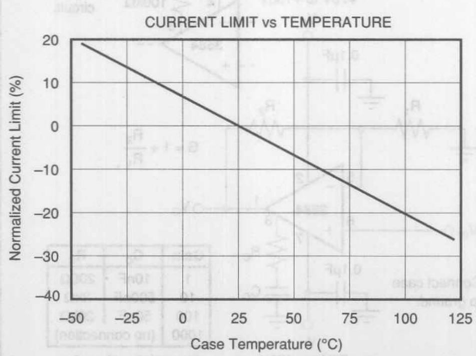
T_{CASE} = +25°C, V_S = ±150V, unless otherwise noted.

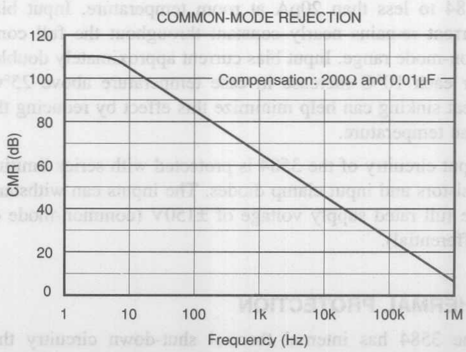






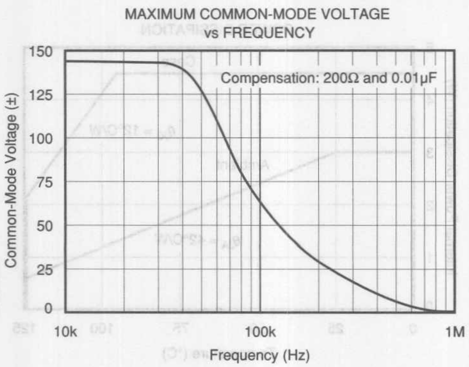


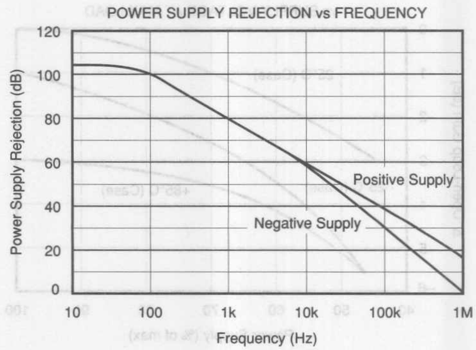




TYPICAL PERFORMANCE CURVES (CONT)

T_{CASE} = +25°C, V_S = ±150V, unless otherwise noted.





APPLICATION INFORMATION

Figure 1 shows the basic connections required to operate the 3584. Bypass capacitors should be connected close to the device pins. Be sure that these capacitors have an adequate voltage rating.

Frequency compensation components must be connected to pin 8 for closed-loop gains of 100 or less. Recommended values are shown in Figure 1. Some adjustment in these values may be required depending on exact circuit configuration and load conditions. Be sure the compensation capacitor has a voltage rating equal to or greater than the positive power supply voltage, V+. Standard 0.25W resistors can be used for R_C.

Input offset voltage and drift of the 3584 are laser-trimmed. Many applications require no external offset trimming. Figure 1 shows connection of an optional offset trim potentiometer which connects to pins 3 and 4.

FET input circuitry reduces the input bias current of the 3584 to less than 20pA at room temperature. Input bias current remains nearly constant throughout the full common-mode range. Input bias current approximately doubles for each 10°C increase in case temperature above 25°C. Heat sinking can help minimize this effect by reducing the case temperature.

Input circuitry of the 3584 is protected with series limiting resistors and input clamp diodes. The inputs can withstand the full rated supply voltage of ±150V (common-mode or differential).

THERMAL PROTECTION

The 3584 has internal thermal shut-down circuitry that activates at a case temperature of approximately 150°C or higher. As this circuitry is activated, the output current drive is reduced. As the case temperature returns to less than the activation temperature, operation will return to normal.

The thermal shut-down circuit will normally protect the amplifier during a short-circuit to ground. It will not protect against short-circuit to one of the power supplies. The typical performance curve "Safe Operating Area" shows that the large stress occurring during this high voltage condition may cause damage if it exceeds 5ms duration. The thermal protection circuitry will not activate fast enough to protect the device from short-circuits to one of the power supplies.

The package case of the 3584 is electrically isolated from all circuitry. No special insulating hardware is required. Although not absolutely required, it is recommended that the case be connected to ground.

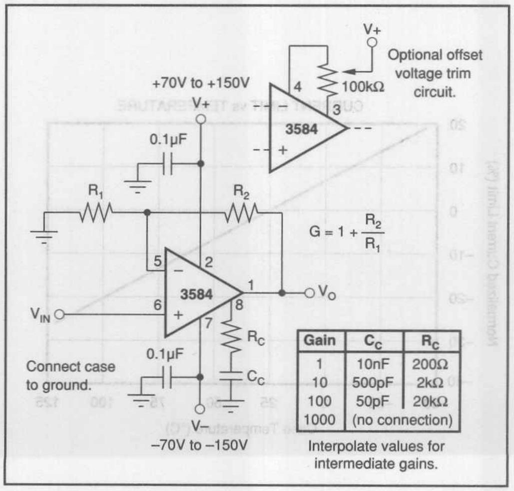


FIGURE 1. Basic Circuit Connections.

4 Instrumentation Amplifiers

Instrumentation amplifiers (IAs) are much more than just precise op amps. They are closed loop amplifiers with built-in precision feedback components. Knowledgeable designers use IAs to extract low-level signals from system errors and noise.

Instrumentation amplifiers can amplify signals in the presence of large common-mode signals. They are ideal for use with all sensor types such as strain gages, load cells, thermocouples, RTDs, current shunts, chemical sensors, and physiological probes. They also make excellent universal input amplifiers for data acquisition systems.

Programmable gain amplifiers are ideal for systems that must connect to a variety of sources with varying signal levels. Products include programmable-gain IAs and op amps.

Choose from the industry's widest selection, including:

INA105, INA106—Simple G=1 and G=10 difference amplifiers... incredibly versatile circuit elements.

INA114, INA118—The industry's most versatile and accurate 8-pin IAs. INA118 features low-power operation.

INA111—High-speed, FET-input IAs using a current-feedback architecture.

INA116—Electrometer IA with ultra-low 3fA input bias current. Its 3-op amp design provides an ultra-high impedance differential input, and allows gain setting from 1 to 1000 by connecting a single external resistor.

INA103—Ultra-low $1nV/\sqrt{Hz}$ noise makes this IA ideal for microphones, bridges or other low impedance sources.

INA117—A difference amplifier with ±200V common-mode voltage range.

INA128 and INA141—Low power, general purpose IAs offering excellent accuracy and wide bandwidth, even at high gain (200kHz at G=100). INA128 gain can be set from 1 to 10,000 using a single external resistor. INA141, a fixed-gain version, uses simple pin connections to set an accurate gain of 10 or 100V/V without external resistors.

INA2128, INA2141—Industry's first dual instrumentation amplifiers—two complete IAs on a single monolithic chip. Both provide excellent accuracy and wide bandwidth at high gain (200kHz at G=100).

PGA204, PGA205—Programmable gain IAs great for data acquisition systems that connect to a variety of sources or needing exceptional dynamic range.

PGA206, PGA207—These are complete 3-op amp IAs with digitally selected gains. PGA206 provides gains of 1, 2, 4 and 8V/V, while PGA207 has gains of 1, 2, 5 and 10V/V. Fast settling time of 3.5μs to 0.01% (all gains) allows fast polling of many channels.

ALD1000—A new, monolithic programmable voltage-to-current or voltage-to-voltage analog line driver circuit. Both current and voltage sensing can be performed simultaneously: current sensing is achieved through an external resistor, while voltage sensing is performed directly across the load.

XTR101, XTR103, XTR104—4-20mA current loop transmitters with built-in IAs for RTDs or bridges.

XTR501—A high current 1W bridge driver and programmable 4-20mA current transmitter designed for sensors requiring up to 600mA of sensor current.

Other popular products provide special features and performance. Use our detailed selection guide to locate the IA for your application.

Instrumentation Amplifiers

INSTRUMENTATION AMPLIFIERS

INSTRUMENTATION AMPLIFIERS (3 Op Amp Topology)

PRECISION (Linearity Error at G = 100, max)
- INA114 (±0.002%)
- INA115 (±0.002%)
- INA118 (±0.002%)
- INA131 (±0.002%)
- INA101 (±0.003%)

LOW NOISE (Noise at 1kHz, typ)
- INA103 (1nV/√Hz)
- INA2128 (8nV/√Hz, Dual)
- **INA128 (8nV/√Hz)**
- **INA2141 (8nV/√Hz, Dual)**
- **INA141 (8nV/√Hz)**
- INA111 (10nV/√Hz)
- INA118 (10nV/√Hz)
- INA114 (11nV/√Hz)
- INA110 (13nV/√Hz)

LOW POWER (V_S, min, I_Q, max)
- INA118 (±1.35, 350µA)
- **INA141 (±2.25, 650µA)**
- **INA128 (±2.25, 750µA)**
- **INA2128 (±2.25, 1.3mA, Dual)**
- **INA2141 (±2.25, 1.3mA, Dual)**
- INA102 (±3.5, 750µA)

FAST SETTLING (Settling Time to 0.01% Accuracy, G = 10, typ)
- INA111 (2µs)
- INA110 (3µs)
- INA103 (3.5µs)

LOW BIAS CURRENT (I_B, max)
- INA111 (20pA)
- ***INA116 (25fA)***
- INA110 (50pA)

FIXED GAIN (Gains)
- INA131 (100)
- **INA141 (10, 100)**
- **INA2141 (10, 100, Dual)**

PROGRAMMABLE GAIN AMPLIFIERS

DIFFERENTIAL INPUT

DC Precision (Gains)
- PGA204 (G = 1, 10, 100, 1000)
- PGA200 (G = 1, 10, 100, 1000)
- PGA205 (G = 1, 2, 4, 8)
- 3606 (G = 1, 2, 4, ...1024)

Fast Settling (Gains)
- PGA202 (G = 1, 10, 100, 1000)
- PGA206 (G = 1, 2, 4, 8)
- PGA207 (G = 1, 2, 5, 10)
- PGA203 (G = 1, 2, 4, 8)

SINGLE-ENDED INPUT
- PGA103 (G = 1, 10, 100)
- PGA102 (G = 1, 10, 100)
- PGA100 (G = 1, 2, 4, ...128)

4-20mA CURRENT TRANSMITTERS/ RECEIVERS

TRANSMITTERS (Input, Output)
- XTR101 (RTD, TC, Bridge, 2 Wire)
- XTR103 (RTD, 2 Wire)
- XTR104 (Bridge, 2 Wire)
- XTR110 (0-10V, 3 Wire)
- XTR501 (Bridge, 3 Wire)

PROGRAMMABLE I/V TRANSMITTER
- **ALD1000 (±10V or 4-20mA)**

RECEIVE
- RCV420 (4-

DIFFERE AMPLIFI (Gain)
- INA105 (G = 1
- 3627 (G = 1
- INA106 (G = 1
- INA117 (±200

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELO

Some specifications have been estimated for comp purposes. Refer to data sheets for guaranteed spec

INSTRUMENTATION AMPLIFI

Product	Gains Available	Gain Error(2) max (%)	Gain Drift(2) max ± (ppm/°C)	Non Linearity(2) max (%)	CMR(1,2) min (dB)	Offset Voltage Drift max (μV/°C)	Small Signal Bandwidth(2) typ (kHz)	Package	Description
INA101	1-1k(3)	0.1	110	±0.003	106	±0.25+10/G	25	CDIP, PDIP, SOIC, TO-100	25μV Offset, 13nV/√Hz, High CMR INA
	1, 10, 100, 1000	0.15	15	±0.020	90	±0.25+5/G	3	CDIP, PDIP, SOIC	Low Power: 7V, 750μA
INA103	1-1k(3)	0.1	25	±0.004	110	±0.25+5/G	800	CDIP, PDIP, SOIC	1nV/√Hz Noise, 0.0009% THD+N
INA104	1-1k(3)	0.15	55	±0.002	106	±0.25+10/G	25	MDIP	High Accuracy, Internal 4th Op Amp
INA110	1, 10, 100, 200, 500	0.1	20	±0.010	106	±0.25+5/G	450	CDIP, PDIP, SOIC	FET-Input, 3μs t_S, 50pA I_B
INA111	1-10k(3)	0.5	110	±0.005	106	±5±100/G	450	PDIP, SOIC	FET-Input, 4μs t_S, 20pA I_B, 8-pin DIP
INA114	1-10k(3)	0.5	110	±0.002	110	±0.25+5/G	10	PDIP, SOIC	Accurate, Low cost, 8-pin DIP
INA115	1-10k(3)	0.5	110	±0.002	110	±0.25+5/G	10	SOIC	INA114 with additional pin-outs.
INA116	**1-1000**	**0.5**	**110**	**±0.005**	**86**	**±0.25+20/G***	**70**	**PDIP, SOIC**	**Electrometer input (10fA), Guard Driv**
INA118	1-10k(3)	0.5	110	±0.002	107	±0.25+5/G	100	PDIP, SOIC	Low Power: ±1.35V, 350μA. 8-pin DIP
INA120	1, 10, 100, 1000	0.2	30	±0.010	106	±0.25+10/G	20	PDIP	Low Offset and Drift, High CMR
INA128	**1-10k(3)**	**0.5**	**100**	**±0.002**	**120**	**±0.5±20/G**	**200**	**PDIP, SOIC**	**Low Power, 600μA, 8-pin DIP, SO-8**
INA131	100	0.024	10	±0.002	110	±0.25	70	PDIP, SOIC	G = 100, 8 pin DIP, Ultra Low Gain Erro
INA141	**10,100**	**0.075**	**10**	**±0.002**	**117**	**±0.5**	**200**	**PDIP, SOIC**	**Low Power, 600μA**
INA2128	**1-10k(3)**	**0.5**	**100**	**±0.002**	**120**	**±0.5+20/G**	**200**	**PDIP, SOIC**	**Worlds first Dual IA, High Accuracy**
INA2141	**10, 100**	**0.075**	**10**	**±0.002**	**117**	**±0.5**	**200**	**PDIP, SOIC**	**Dual IA, 2 Fixed Gains, Low gain erro**

NOTES: (1) DC to 60Hz, balanced source impedance. (2) G = 100. (3) Set with external resistor. (4) G = 50. (5) G = 0.5. (6) G = 1.

DIGITALLY PROGRAMMABLE GAIN AMPLIFI

Product	Digitally Selected Gains(2)	Gain Error(2) max (%)	Gain Drift(2) max (ppm/°C)	Non Linearity Error(2) max (%)	CMR(1,2) min (dB)	Offset Voltage Drift ± max (μV/°C)	Small Signal Bandwidth(2) typ (kHz)	Package	Description
PGA100	1, 2, 4, ... *128*	0.02	10	0.005	NA	6*	40	CDIP	8 Multiplexed S-E(3) inputs, 8 Binary gains. Still Avai
PGA102	1, 10, *100*	0.025	20	0.01	NA	3	250	CDIP, PDIP	3 S-E(3) inputs. Gain control per channel.
PGA103	1, 10, *100*	0.2	30*	0.01	NA	2*	250	PDIP, SOIC	8-pin, low cost. 1 S-E input. < 3 mA Iq.
PGA200	1, 10, *100*, 1000	0.02	10	0.003	106	0.4	30	CDIP, PDIP	IA(3) Input. Precision hybrid. Still Available.
PGA202	1, 10, *100*, 1000	0.15	60	0.012	92	13	1000	CDIP, PDIP	FET IA(3) Input. 3μs t_S, constant GBW.
PGA203	1, 2, 4, *8*	0.15	15	0.012	86	27	1000	CDIP, PDIP	FET IA(3) Input. 3μs t_S, constant GBW.
PGA204	1, 10, *100*, 1000	0.024	10	0.002	110	0.25	10	PDIP, SOIC	IA(3) Input, DC precision. ±40V protection.
PGA205	1, 2, 4, *8*	0.024	10	0.002	96	0.26	80	PDIP, SOIC	IA(3) Input, DC precision. ±40V protection.
PGA206	1, 2, 4, *8*	0.05	10	0.002	95	2*	600	PDIP, SOIC	IA(3) Input. Fast: t_S = 3.5μs, SR = 25V/μs.
PGA207	1, 2, 5, *10*	0.05	10	0.002	95	2*	600	PDIP, SOIC	IA(3) Input. Fast: t_S = 3.5μs, SR = 25V/μs.
3606	1, 2, 4, ... *1024*	0.02	10	0.01	110	5	10	CDIP	Precision Hybrid, 2^9 Binary Gains.

NOTES: (1) DC to 60Hz, balanced source impedance. (2) Listed specifications apply for gain values in italics from "Digitally Selected Gains" column. (3) S-E: Single-Ended input. IA: Instrumentation Amplifier inputs (differentia impedance).

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMI

Some specifications have been estimated for comparis purposes. Refer to data sheets for guaranteed specific:

4-20mA TRANSMITTERS/RECEIVERS

Product	Supply Voltage Range (V)	Span Error (Unadj) max (%)	Non-Linearity max (%)	CMR 60Hz typ (dB)	Offset Voltage Drift max (µV/°C)	Output Zero Error ± max	Full Scale Output Error max	Package	Description
RCV420	–5/11.4 to ±18	—	0.002	94	—	1.25mV	2.5mV	CDIP, PDIP	Precision 4-20mA current loop receiver.
XTR101	11.6 to 40	5	0.01	100	0.75	6µA	30µA	CDIP, PDIP, SOIC	2 Wire transmitter, selectable in/out ranges.
XTR103	9 to 40	1	0.01	100	2.5	50µA	50µA	PDIP, SOIC	2 Wire, RTD excitation/linearization.
XTR104	9 to 40	1	0.01	100	2.5	50µA	50µA	PDIP, SOIC	2 Wire, Bridge excitation/linearization.
XTR110	13.5 to 40	0.2	0.005	—	—	16µA	32µA	CDIP, PDIP, SOIC	3 Wire transmitter, selectable in/out ranges.
XTR501	11.4 to 30	2.5(1)	0.025	85	50*	100µA	—	DIP	1W bridge excitation for low Z sensors.

NOTE: (1) Gain = 1.

PROGRAMMABLE I/V TRANSMITTERS

Product	Current Output	Span error max (5)	Voltage Output	Non Linearity max (%)	Voltage Frequency Response G = 1 (kHz)	Supply Voltage	Package	Description
ALD1000	**4-20mA**	**1**	**±10V**	**0.05**	**100***	**V_S- = –15V** **V_S+ = +24V**	**SOIC**	**Programmable voltage-to-current or voltage-to-voltage analog driver circuit.**

DIFFERENCE AMPLIFIERS

Product	Gain (V/V)	Gain Error max (%)	Gain Drift* max (ppm/°C)	Non Linearity max (%)	CMR(1) DC min (dB)	Offset Voltage Drift max (µV/°C)	Small Signal Bandwidth typ (kHz)	Package	Description
INA105	1	0.010	5	±0.001	86	10	1000	TO-99, DIP, SOIC	High Accuracy, Cost Effective
INA106	10	0.025	4*	±0.001	86	0.2*	5000	DIP, SOIC	High Accuracy, Cost Effective
INA117	1	0.020	10	±0.001	86	20	200	TO-99, DIP	±200VDC Common Mode, ±500VDC (V_{CM} and V_{DIFF}) Protected Input
3627	1	0.010	5	±0.001	100	20	800	TO-99	High Accuracy, High CMR (Still Available)

NOTE: (1) DC to 60Hz, balanced source impedance.

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

BURR - BROWN®

ALD1000

Precision Programmable CURRENT/VOLTAGE TRANSMITTER

FEATURES

- SWITCHABLE OUTPUT ±10V OR 4-20mA
- DRIVES 1000Ω ‖ 1µF AT 20mA
- VOLTAGE AND CURRENT SENSE
- GROUND NOISE SUPPRESSION
- ERROR DETECTION FLAG
- OUTPUT DISABLE
- ACCURACY: 0.05% max
- WIDE SUPPLY RANGE: ±11V TO +24/–15V

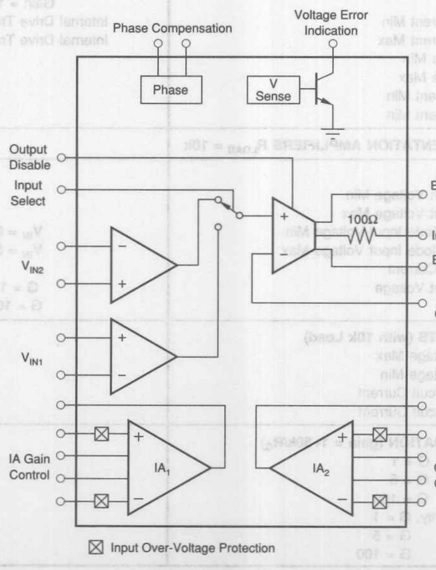
APPLICATIONS

- PROGRAMMABLE CONTROLLERS
- STANDARDIZED OUTPUTS FOR TERMINATION PANELS
- INDUSTRIAL PROCESS CONTROL
- PROGRAMMABLE CURRENT SOURCE
- MOTOR CONTROL SYSTEMS
- PC AND VME BASED INSTRUMENTATION
- CONDITIONER FOR STANDARD SENSOR OUTPUTS
- TEST EQUIPMENT PIN DRIVER

DESCRIPTION

This product is a monolithic programmable voltage-to-current or voltage-to-voltage analog line driver circuit. It can convert a ±10V input into either an output voltage or current with remote sensing. It provides drive for external transistors to boost output current to greater than ±25mA levels.

Current and voltage sensing can be performed simultaneously. Current sensing is achieved through a single external sense resistor. Voltage sensing is performed directly across the load. The logic inputs provide for both output disable and switching between constant current or constant voltage output functions. An open collector output provides an error flag for open circuit loads. The output disable function allows full control of the output even during power-on and power-off sequencing. The instrumentation amplifiers are designed to insure that load noise is not circulated within the control loop.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PARAMETER	CONDITIONS	ALD1000U MIN	TYP	MAX	UNITS
TRANSMITTER					
SWOP INPUTS					
Linear Range Min	Internal Drive Transistors			–10	V
Linear Range Max	5mA Load	10			V
Input Bias Current			50		pA
XTR OUTPUT					
Positive Overvoltage Sense			19.5		V
Negative Overvoltage Sense	Internal Drive Transistors		–10.5		V
Positive Overcurrent Sense			+25		mA
Negative Overcurrent Sense			–15		mA
LOGIC INPUTS					
Logic Low				0.8	V
Logic High		4.0	2.6		V
LOGIC OUTPUTS					
Logic High	5V Logic Supply	4.0			V
Logic Low	with 10k pull-up resistor			0.8	V
OUTPUT—VOLTAGE MODE (Gain = 1 unless otherwise specified)					
Span Error			0.5	1	%
Span Drift			50		ppm/°C of FS
Linear Range Min	0.1% of FS		–10		
Linear Range Max	0.1% of FS	10			
Output Current Min	Internal Drive Transistors			–5	mA
Output Current Max	Internal Drive Transistors	5			mA
Short-Circuit Current	Internal Drive Transistors		25		mA
Short-Circuit Current	Internal Drive Transistors		–15		mA
Non-Linearity			0.005	0.05	%
Initial Offset Voltage—RTI			2		mV
Offset Voltage vs Temperature			20		µV/°C
OUTPUT—CURRENT MODE (Gain = 5 with 50Ω shunt resistor unless otherwise specified)					
Span Error			5		%
Span Drift	Gain = 1(1)		50		ppm/°C of FS
Output Current Min	Internal Drive Transistors(2)			–5	mA
Output Current Max	Internal Drive Transistors(2)	5			mA
Compliance Min		–10			V
Compliance Max			15		V
Offset Current Min			–25		µA
Offset Current Min		25			µA
INSTRUMENTATION AMPLIFIERS R_{LOAD} = 10k					
IA INPUTS					
Linear Input Voltage Min				–10	V
Linear Input Voltage Max		20			V
Common-Mode Input Voltage Min	$V_{IN} = 0$			–10	V
Common-Mode Input Voltage Max	$V_{IN} = 0$	20			V
Input Bias Current			100		nA
Initial Offset Voltage	G = 1	–500		500	µV
CMRR	G = 10	80	100		
IA OUTPUTS (with 10k Load)					
Output Voltage Max		20			V
Output Voltage Min				–10	V
+ Short Circuit Current			5		mA
– Short Circuit Current			–12		mA
GAIN EQUATION (gain = 1+50k/R_G)					
Gain Error, G = 1				0.3	%±FS
G = 5				0.6	%±FS
G = 100				0.8	%±FS
Non-Linearity, G = 1				0.004	%±FS
G = 5				0.008	%±FS
G = 100				0.02	%±FS

SPECIFICATIONS (CONT)

At $+V_S$ = 24V, $-V_S$ = 15V, T_{AMB} = 25°C, and 2N2222, 2N2907 external transistors, unless otherwise noted.

PARAMETER	CONDITIONS	ALD1000U MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE					
G = 1			700		kHz
G = 5			400		kHz
G = 100			50		kHz
Slew Rate	V_O = ±10V, G = 10		4		V/µS
SETTLING TIME, 0.01%					
G = 1			20		µS
G = 5			20		µS
G = 100			30		µS
POWER SUPPLY					
Quiescent Current	Internal Drive Transistors		5		mA
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–65		+150	°C

NOTES: (1) Gain drift depends on tempco of 50K factor on gain equation when gain is greater than 1. (2) External Drive capacity varies with configuration. See Application Note.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (±V_S)	+25V, –18V
IA Inputs	±40V
SWOP Inputs	±V_S
Logic Inputs	$+V_S$, $-V_S$ + 0.5V
Junction Temperature	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-to-Ground at 25°C	Continuous

ORDERING INFORMATION

MODEL	PACKAGE
ALD1000U	28-Pin SOIC

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ALD1000U	28-Pin SOIC	217

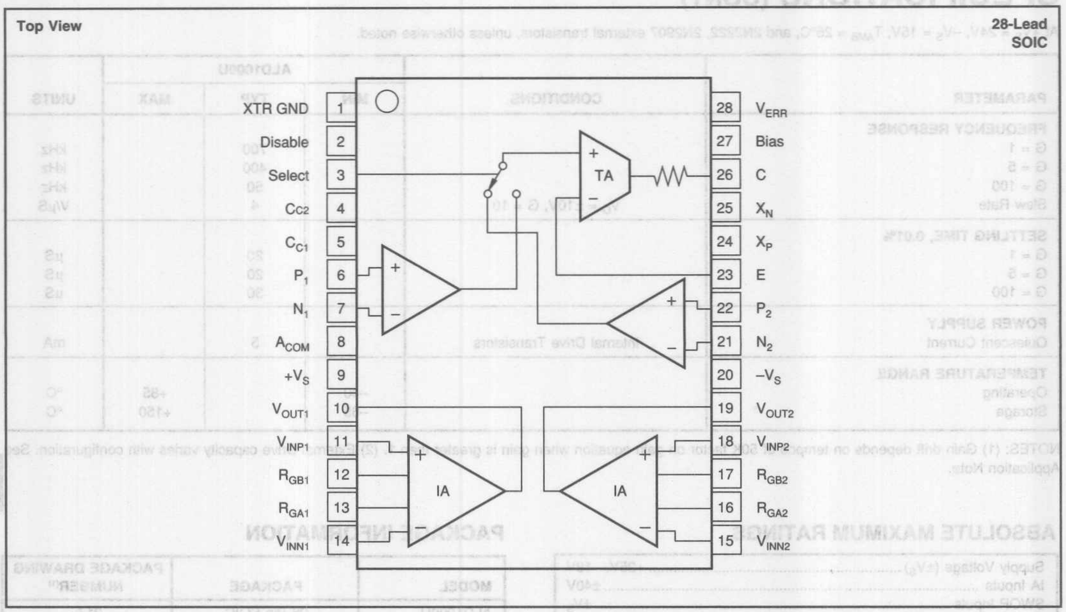
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION



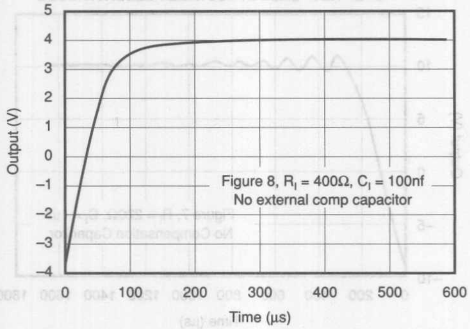
PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	XTR GND	Power ground pin.
2	Disable	A 5V signal puts the internal drive in a high impedance state and limits the external drive capacity.
3	Select	Selects the SWOP amp input. A 5V signal selects inputs N1 and P1.
4	C_{C2}	C_{C1} and C_{C2} are for the external compensation capacitor.
5	C_{C1}	C_{C1} and C_{C2} are for the external compensation capacitor.
6	P_1	Non-inverting input to the XTR SWOP amp 1.
7	N_1	Inverting input to the XTR SWOP amp 1.
8	A_{COM}	Signal ground for the instrumentation amplifiers.
9	$+V_S$	Positive power supply voltage.
10	V_{OUT1}	Output of the instrumentation amplifier 1.
11	V_{INP1}	Non-inverting input to instrumentation amplifier 1.
12	R_{GB1}	Gain set resistor for instrumentation amplifier 1.
13	R_{GA1}	Gain set resistor for instrumentation amplifier 1.
14	V_{INN1}	Inverting input of instrumentation amplifier 1.
15	V_{INN2}	Inverting input of instrumentation amplifier 2.
16	R_{GA2}	Gain set resistor for instrumentation amplifier 2.
17	R_{GB2}	Gain set resistor for instrumentation amplifier 2.
18	V_{INP2}	Non-inverting input to instrumentation amplifier 2.
19	V_{OUT2}	Output of the instrumentation amplifier 2.
20	$-V_S$	Negative power supply voltage.
21	N_2	Inverting input to the XTR SWOP amp 2.
22	P_2	Non-inverting input to the XTR SWOP amp 2.
23	E	Inverting input (emitter) of the output transconductance amplifier.
24	X_P	Base drive for an external, PNP, driver transistor (optional).
25	X_N	Base drive for an external, NPN, driver transistor (optional).
26	C	Output (collector) of the output transconductance amplifier.
27	Bias	Open collector output indicating an internal overcurrent condition.
28	V_{ERR}	Open collector output indicating an overvoltage condition.

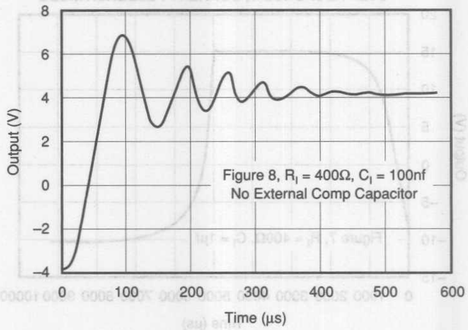
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$; $+V_S = 24V$, $-V_S = -15V$ unless otherwise noted.

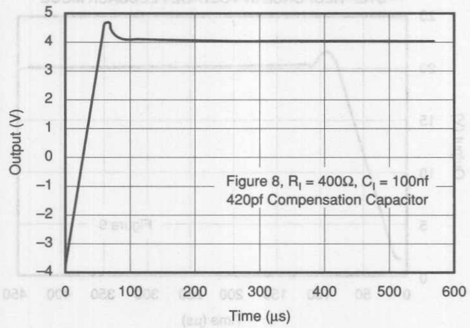
STEP RESPONSE IN THE CURRENT FEEDBACK MODE



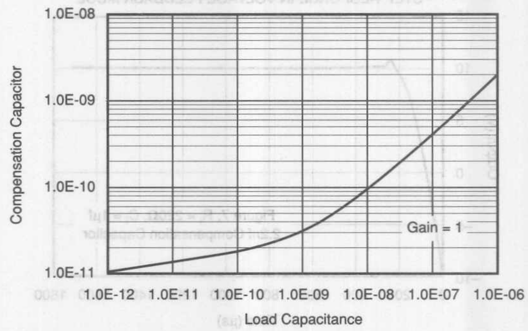
STEP RESPONSE IN VOLTAGE FEEDBACK



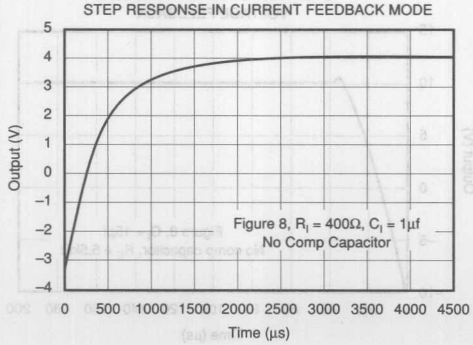
STEP RESPONSE IN VOLTAGE FEEDBACK



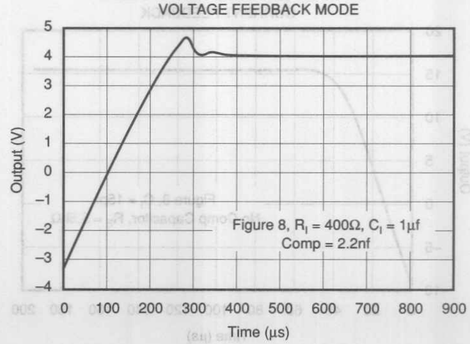
COMPENSATION CAPACITOR vs LOAD CAPACITANCE

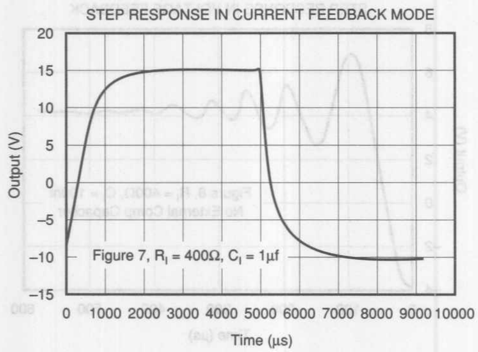


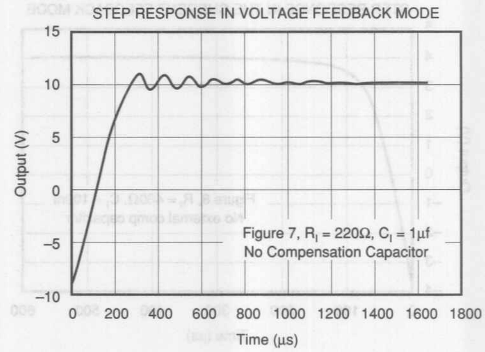
STEP RESPONSE IN CURRENT FEEDBACK MODE

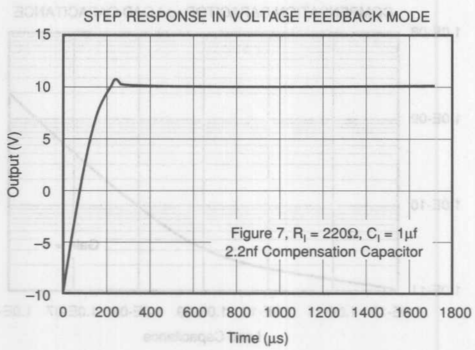


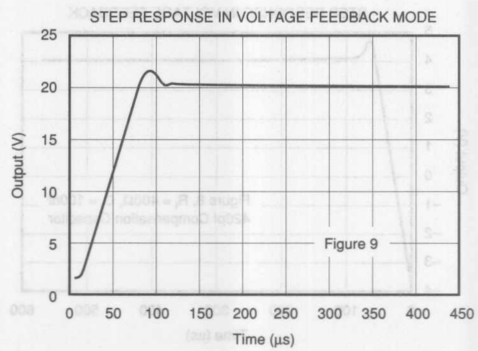
STEP RESPONSE LOAD IN THE VOLTAGE FEEDBACK MODE

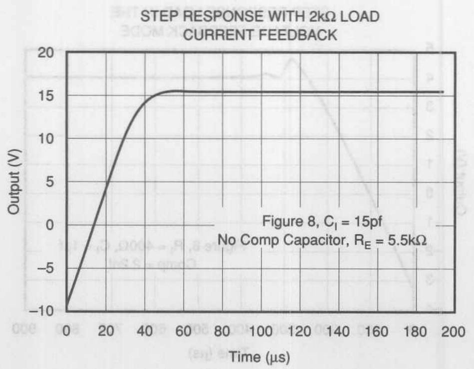


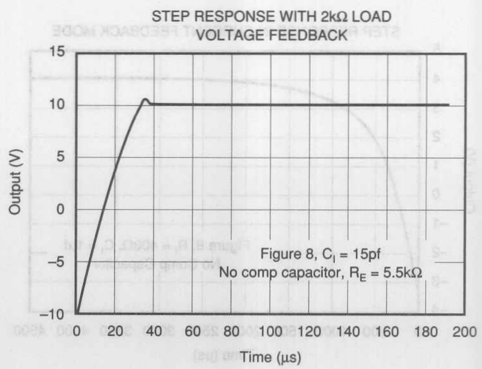

STEP RESPONSE IN CURRENT FEEDBACK MODE
Output (V)
Time (µs)
Figure 7, $R_I = 400\Omega$, $C_I = 1\mu f$


STEP RESPONSE IN VOLTAGE FEEDBACK MODE
Output (V)
Time (µs)
Figure 7, $R_I = 220\Omega$, $C_I = 1\mu f$
No Compensation Capacitor


STEP RESPONSE IN VOLTAGE FEEDBACK MODE
Output (V)
Time (µs)
Figure 7, $R_I = 220\Omega$, $C_I = 1\mu f$
2.2nf Compensation Capacitor

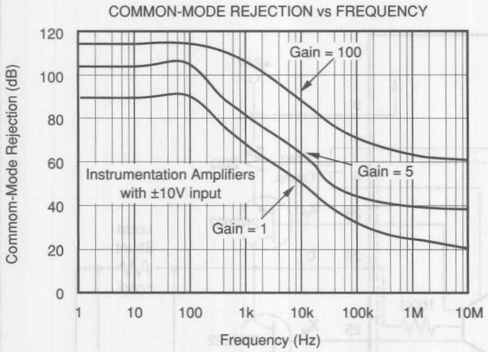

STEP RESPONSE IN VOLTAGE FEEDBACK MODE
Output (V)
Time (µs)
Figure 9

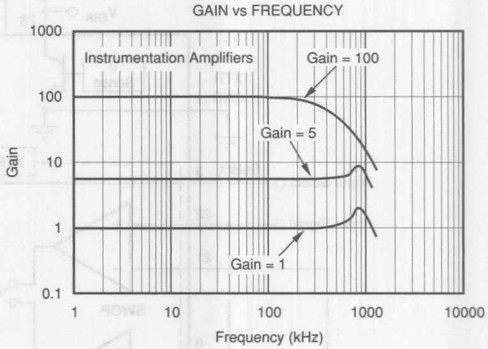

STEP RESPONSE WITH 2kΩ LOAD
CURRENT FEEDBACK
Output (V)
Time (µs)
Figure 8, $C_I = 15pf$
No Comp Capacitor, $R_E = 5.5k\Omega$

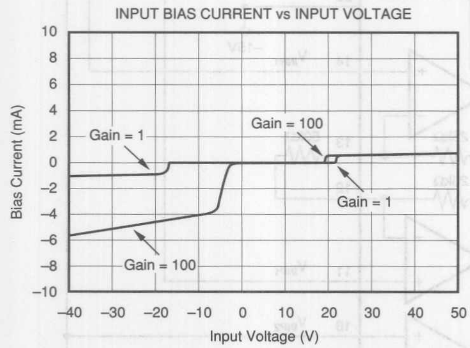

STEP RESPONSE WITH 2kΩ LOAD
VOLTAGE FEEDBACK
Output (V)
Time (µs)
Figure 8, $C_I = 15pf$
No comp capacitor, $R_E = 5.5k\Omega$

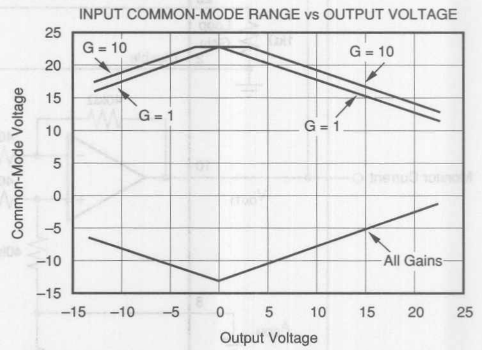
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$; $+V_S = +24V$, $-V_S = -15V$ unless otherwise noted.









BASIC OPERATION

ALD1000 FUNCTIONAL BLOCKS

The typical ALD1000 control loop comprises three primary functional blocks (see Figure 1): the current transmitter (XTR), the load, and the instrumentation amplifier (IA). The XTR can be further viewed as divided into the switchable input operational amplifier (SWOP amp), and the voltage to current, transconductance amplifier (TA). Each of these blocks plays a role in the dynamic performance of the control loop, particularly in terms of loop stability with reactive loads.

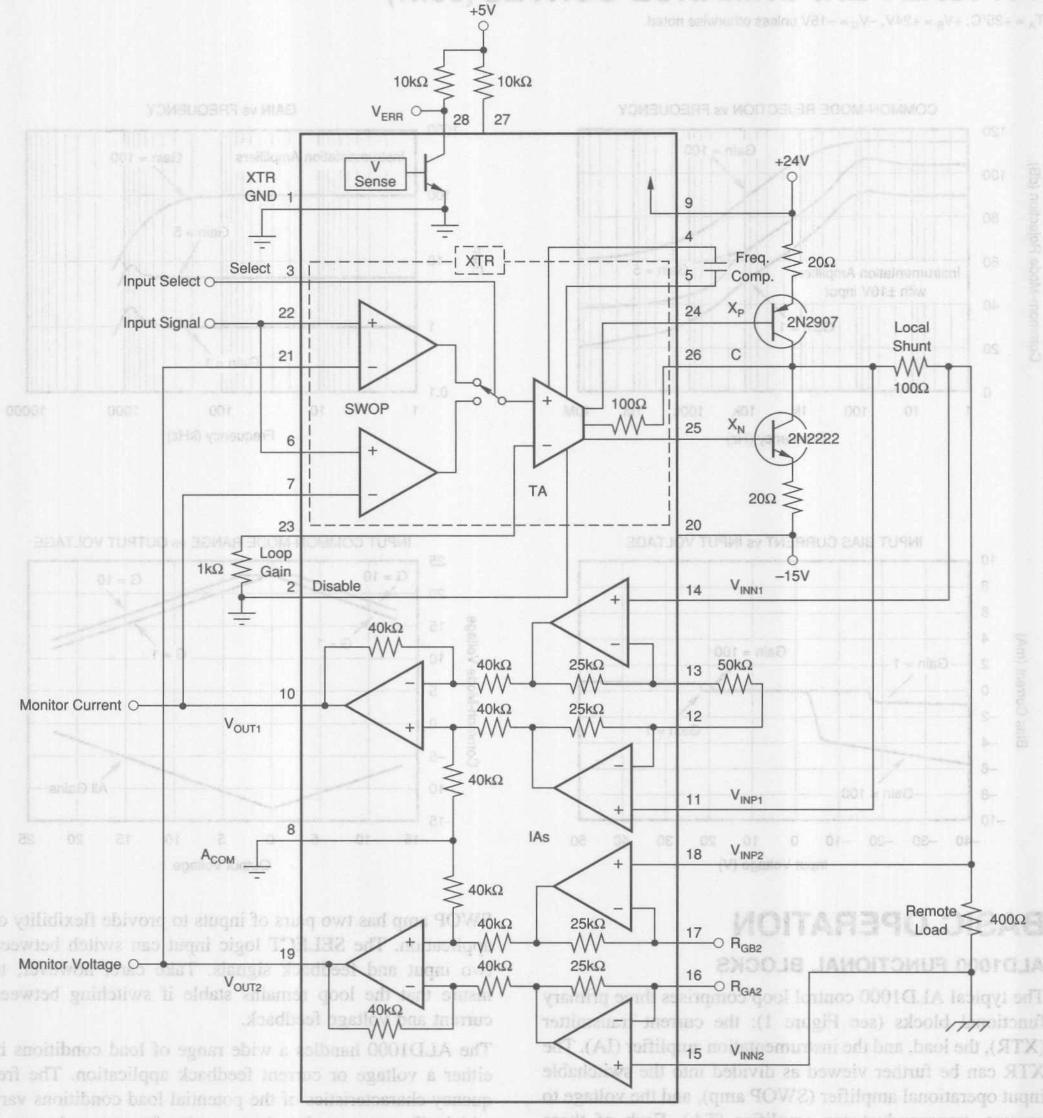
THE CURRENT TRANSMITTER (XTR)

The XTR produces the forward gain necessary for error amplification. It also controls the frequency response which must be adjusted to balance the trade-off between step response and stability when driving reactive loads.

Within the XTR the SWOP amp serves as the input stage. It amplifies the error between the input and output signals to produce a precise signal to the TA to drive the load. The SWOP amp has two pairs of inputs to provide flexibility of application. The SELECT logic input can switch between two input and feedback signals. Take care, however, to insure that the loop remains stable if switching between current and voltage feedback.

The ALD1000 handles a wide range of load conditions in either a voltage or current feedback application. The frequency characteristics of the potential load conditions vary widely. To accommodate these varying frequency characteristics the XTR includes a compensation network. It consists of a simple resistor divider network which forms a single pole, high pass, RC filter when a compensation capacitor is connected externally.

The transconductance amplifier converts the output voltage of the SWOP amp into an output current to drive the load. Whether used in a current feedback or a voltage feedback loop, the ALD1000 transmitter should be viewed as a source of current not voltage. In a voltage loop, the output current is converted to a feedback voltage by the load. In a current loop the output current is converted to a feedback voltage by the shunt resistor. The external, XTR gain resistor, tied to E (Pin 23, Figure 1), sets the voltage to current ratio.



V_{IN}	I_{OUT}	V_{OUT}	SELECT	DISABLE
0-2	0-10mA		1	0
0-10	0-50mA		1	0
0.8-4	4-20mA		1	0
2-10	10-50mA		1	0
0-5		0-5V	0	0
0-10		0-10V	0	0
±5		±5V	0	0
±10		±10V	0	0
X	OFF	OFF	X	1

FIGURE 1.

THE INSTRUMENTATION AMPLIFIERS (IA)

The ALD1000 includes two, general purpose, uncommitted, 3-op amp, instrumentation amplifiers (see Figure 1). The two IAs are connected to the common power supply and operate at full supply voltage. They share the same analog common reference. Otherwise they are configured independently for maximum flexibility.

The instrumentation amplifier senses the feedback signal, reduces any common-mode component, and scales it to the level required.

A more comprehensive discussion of the instrumentation amplifiers follows in a later section.

ALD1000 LOGIC

The logic inputs used for the SWOP amp select and the XTR disable functions are simple, differential pair comparators as shown in Figure 2.

The logic outputs are open collector NPN transistors with their emitters at ground (pin 1).

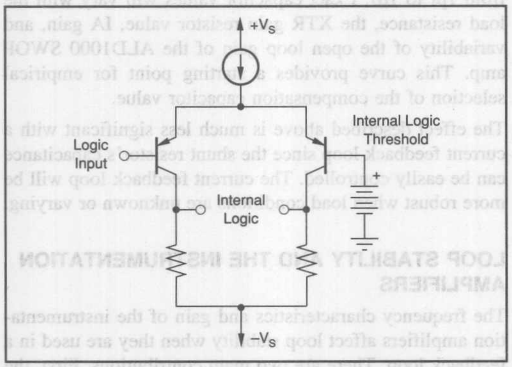


FIGURE 2. Simplified Diagram of the Internal ALD1000 Logic Input Circuitry.

VOLTAGE ERROR INDICATION

The V_{ERR} error signal at pin 28 triggers when the voltage at C (pin 26) exceeds the Positive Overvoltage Sense or the Negative Overvoltage Sense (see SPECIFICATIONS) internal thresholds. When external transistors are used without connecting them to C, as shown in Figure 7, the load voltage cannot be detected. The logic signal will generally trigger to an error state (low). However, consider it indeterminate under these conditions.

INSTRUMENTATION AMPLIFIERS

SETTING THE GAIN

The IA gain is set by connecting a single, external resistor, Rg in Figure 3, between the gain set pins.

$$G = 1 + \frac{50k\Omega}{R_G}$$

INPUT PROTECTION

The inputs of the ALD1000 instrumentation amplifiers are individually protected against over-voltage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1ma to 5ma. Refer to the typical performance curve "Input Bias Current vs Input Voltage." The inputs are protected even if the power supplies are disconnected or turned off.

IA INPUT OVERLOAD AND INPUT COMMON-MODE RANGE

The linear voltage range of the input circuitry of the ALD1000 instrumentation amplifiers is from approximately 0.6V below the positive supply to 1V above the negative supply. However, the output swing of the input amplifiers

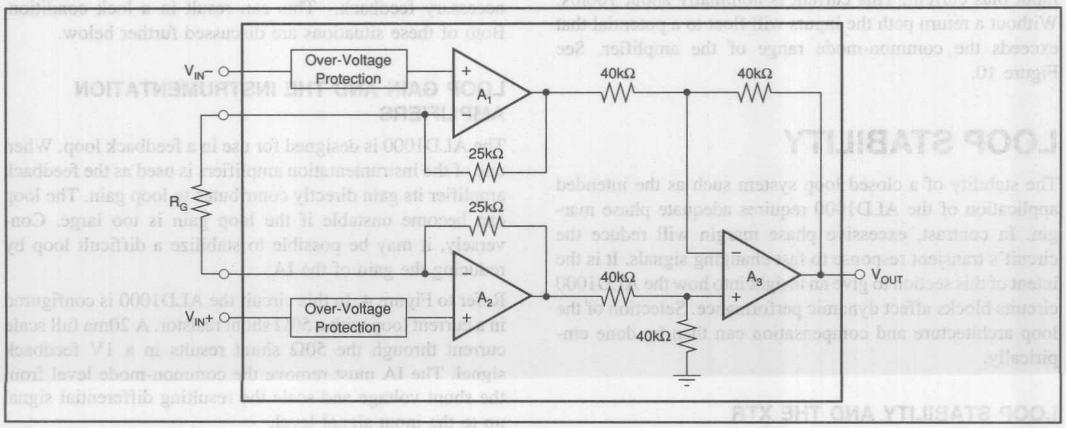


FIGURE 3. Simplified Schematic of the Instrumentation Amplifiers. Resistor RG Controls the Gain.

range relates to the output voltage of the complete amplifier. This behavior also depends in supply voltage—see performance curve "Input Common-Mode Range vs Output Voltage."

The combination of a significant differential signal and a high common-mode voltage as occurs in the current feedback configuration reduces the common-mode range. Exceeding the common-mode range results in a reduced IA output voltage. When this occurs the feedback loop can no longer balance. The forward gain of the ALD1000 amplifies this false error signal, the output voltage tries to increase, and this holds the IA in an overloaded condition.

The ALD1000 applies two defenses against this problem. First, there is a 100Ω resistor in series with the transmitter output. This resistor, which primarily provides protection from over-voltage damage to the output terminal, acts to limit the output swing under high current conditions. Second, the ALD1000's error detection circuitry signals when the transmitter output voltage exceeds rating. This serves to detect a potential lock condition.

Limiting the transmitter's output swing to within the instrumentation amplifier's input range allows the loop to recover without reducing the input signal should a transient voltage level exceed the common-mode input range. However, the common-mode range of the instrumentation amplifiers varies with application specific factors. Lock-up can occur. The application designer must provide defenses against this condition where it is warranted.

USING THE INSTRUMENTATION AMPLIFIERS WITH A FLOATING SIGNAL SOURCE

The input impedance of the ALD1000 instrumentation amplifiers are very high—about $10^6\Omega$. Within a feedback loop, as shown in the examples, this characteristic acts to minimize errors caused by loading of the feedback signal. However, if used as an amplifier for a thermocouple, microphone, or other isolated signal source a path is needed for the input bias current. This current is nominally about 100nA. Without a return path the inputs will float to a potential that exceeds the common-mode range of the amplifier. See Figure 10.

LOOP STABILITY

The stability of a closed loop system such as the intended application of the ALD1000 requires adequate phase margin. In contrast, excessive phase margin will reduce the circuit's transient response to fast changing signals. It is the intent of this section to give an insight into how the ALD1000 circuits blocks affect dynamic performance. Selection of the loop architecture and compensation can then be done empirically.

LOOP STABILITY AND THE XTR

There are two critical parameters that must be controlled to margin which defines dynamic performance.

Loop gain is the product of the forward voltage to current ratio, the load impedance, and the IA gain. The input error voltage is converted to an output current. The output current is converted to a feedback voltage by the load impedance. The feedback voltage is gained up by the feedback IA. All three blocks affect loop stability.

The XTR gain resistor, which is connected to the E pin of the ALD1000, adjusts the voltage to current relationship. Increasing this resistor decreases loop gain. This, in turn, increases phase margin and slows step response. This resistor will typically be between 250Ω and 2500Ω.

In a voltage feedback loop the frequency at which the loop gain starts to roll off decreases with increasing capacitance. It is necessary to compensate for the loss of bandwidth caused by load capacitance. The compensation network provides this capability. Typical performance curve "Compensation Capacitor vs Load Capacitance" illustrates typical compensation capacitor values for load capacitance varying from 1pf to 1µf. Exact capacitor values will vary with the load resistance, the XTR gain resistor value, IA gain, and variability of the open loop gain of the ALD1000 SWOP amp. This curve provides a starting point for empirical selection of the compensation capacitor value.

The effect described above is much less significant with a current feedback loop since the shunt resistor's capacitance can be easily controlled. The current feedback loop will be more robust when load conditions are unknown or varying.

LOOP STABILITY AND THE INSTRUMENTATION AMPLIFIERS

The frequency characteristics and gain of the instrumentation amplifiers affect loop stability when they are used in a feedback loop. There are two main contributions. First, the IA gain directly multiplies loop gain. As a result high IA gains reduce phase margin. Second, when the input exceeds the IA range the IA output can no longer provide the necessary feedback. This can result in a lock condition. Both of these situations are discussed further below.

LOOP GAIN AND THE INSTRUMENTATION AMPLIFIERS

The ALD1000 is designed for use in a feedback loop. When one of the instrumentation amplifiers is used as the feedback amplifier its gain directly contributes to loop gain. The loop can become unstable if the loop gain is too large. Conversely, it may be possible to stabilize a difficult loop by reducing the gain of the IA.

Refer to Figure 4. In this circuit the ALD1000 is configured in a current loop with a 50Ω shunt resistor. A 20ma full scale current through the 50Ω shunt results in a 1V feedback signal. The IA must remove the common-mode level from the shunt voltage and scale the resulting differential signal up to the input signal level.

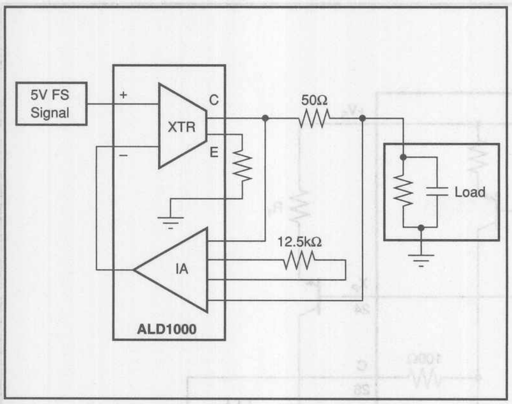


FIGURE 4. Simplified Block Diagram of a 20ma Current Loop. The IA is in a Gain of 5 to Match the 1V Full Scale Shunt Signal to the 5V Full Scale Input Signal.

Here the input signal affects loop stability. A 10V full scale input signal would require an IA gain of 10. A lower input signal, 5V as shown in Figure 4, allows the IA gain to be reduced to 5. This results in a lower loop gain and increased phase margin.

Note that it is possible to reduce the IA gain to less than 1 by using a voltage divider at the IA output.

VOLTAGE FEEDBACK AND THE INSTRUMENTATION AMPLIFIERS

The instrumentation amplifiers can be used for remote sensing in a voltage feedback loop as illustrated in Figure 5. Here the instrumentation amplifier tends to reject small ground potential differences between the source and load. The voltage loop, however, is more sensitive to reactive load impedance than the current loop. The ALD1000 emitter resistor and compensation capacitor need to be selected for the specific load conditions. Voltage feedback may not be appropriate for variable load conditions.

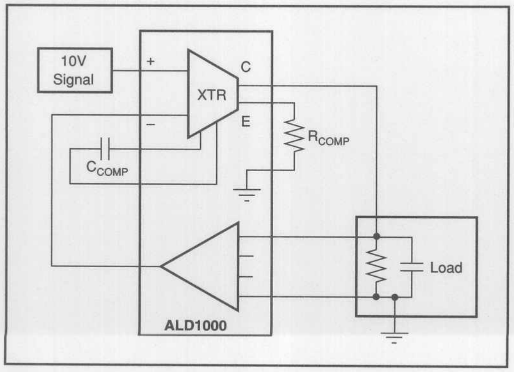


FIGURE 5. Simplified Block Diagram of the ALD1000 in Voltage Feedback.

USING THE ALD1000 WITH EXTERNAL DRIVE TRANSISTORS

Power dissipated by the internal driver stage affects the built-in instrumentation amplifiers compromising their accuracy. External transistors reduce the internal power dissapation.

The external transistors are configured as current sources. A PNP transistor delivers positive current. An NPN supplies the negative drive. Either or both can be used. For example a 4ma to 20ma current loop may only require a PNP transistor since negative current drive is not required. See Figure 9.

Degeneration resistors are required (refer to R_1 and R_2 in Figure 6). The value of the degeneration resistors will affect stability, load sharing with the internal driver devices, and the current limit value. These issues are covered in more detail below.

EXTERNAL TRANSISTORS AND THE CURRENT LIMIT VALUE

The ALD1000 contains circuitry to prevent damage to the internal components due to excess current. When using the internal driver stage by itself, current to the load is limited to about 20ma at room temperature. When using external drivers, the current limit depends, approximately, on the load sharing ratio between the internal and external transistors. Figure 6 illustrates the circuit relationship between the current limit circuitry and external drive transistors.

THE DEGENERATION RESISTORS

The degeneration resistors, R_1 and R_2 in Figure 6, control the load sharing between the internal and external transistors. Choose the resistor values by measuring load current, current through the external transistor, and calculating the current being supplied by the internal drive.

LOOP STABILITY AND THE DEGENERATION RESISTORS

Loop stability depends on loop gain. Because the degeneration resistors affect the voltage to current ratio of the loop the value of these resistors also affect loop gain and thus stability. Smaller resistor values will increase loop gain. It may be necessary to compensate for this by adjusting the value of the XTR gain resistor connected to the E Pin, R_4 in Figure 6.

EXTERNAL TRANSISTORS AND OUTPUT VOLTAGE SWING

The output voltage swing must be limited within the input range of the instrumentation amplifiers. The 100Ω resistor shown in Figure 6 limits output swing under high current conditions. Resistor R_3 performs this function with external transistors. R_3 must be sized to limit output swing, at the expected full load, within the input range of the instrumentation amplifiers. Refer to the section on the instrumentation amplifiers for further information.

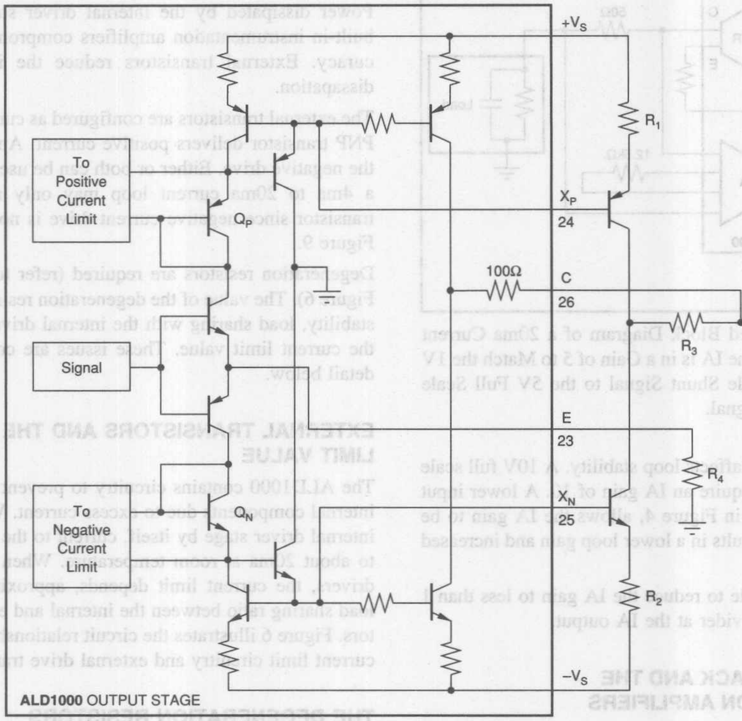


FIGURE 6. Simplified Schematic Showing the Use of External Drive Transistors. R_1 and R_2 Provide Degeneration that Affects the Current Limit and Loop Stability. R_4 Controls the Transconductance Amplifier Gain Affecting Loop Stability and Transient Response. See the Text.

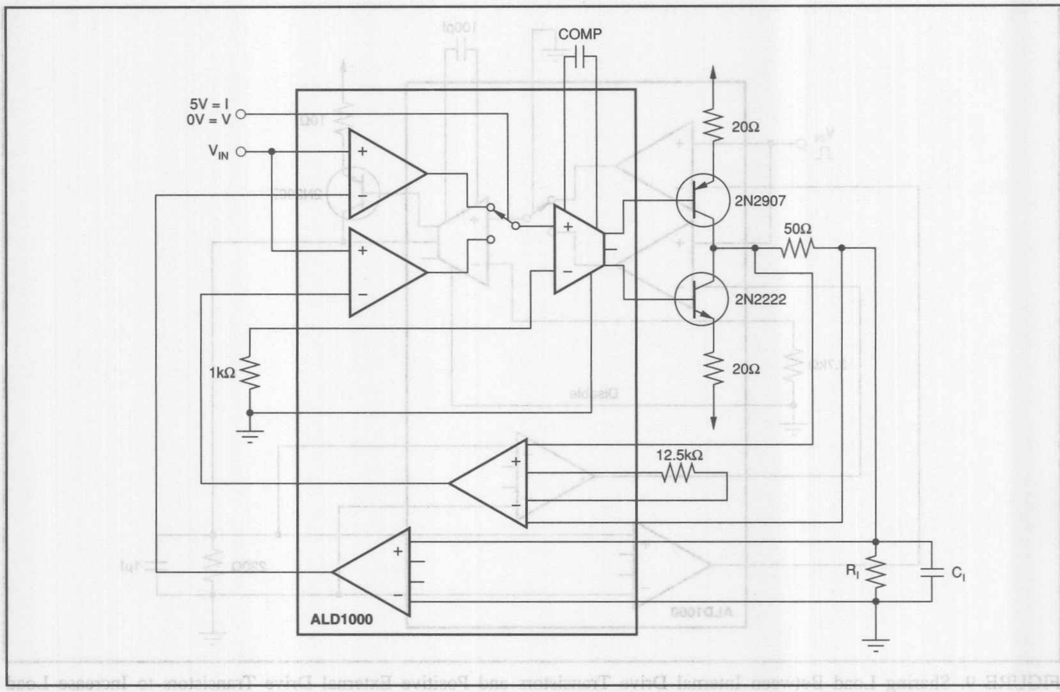


FIGURE 7. Using External Transistors Without Internal Drive. Note that an Overvoltage Condition Can Not Be Detected.

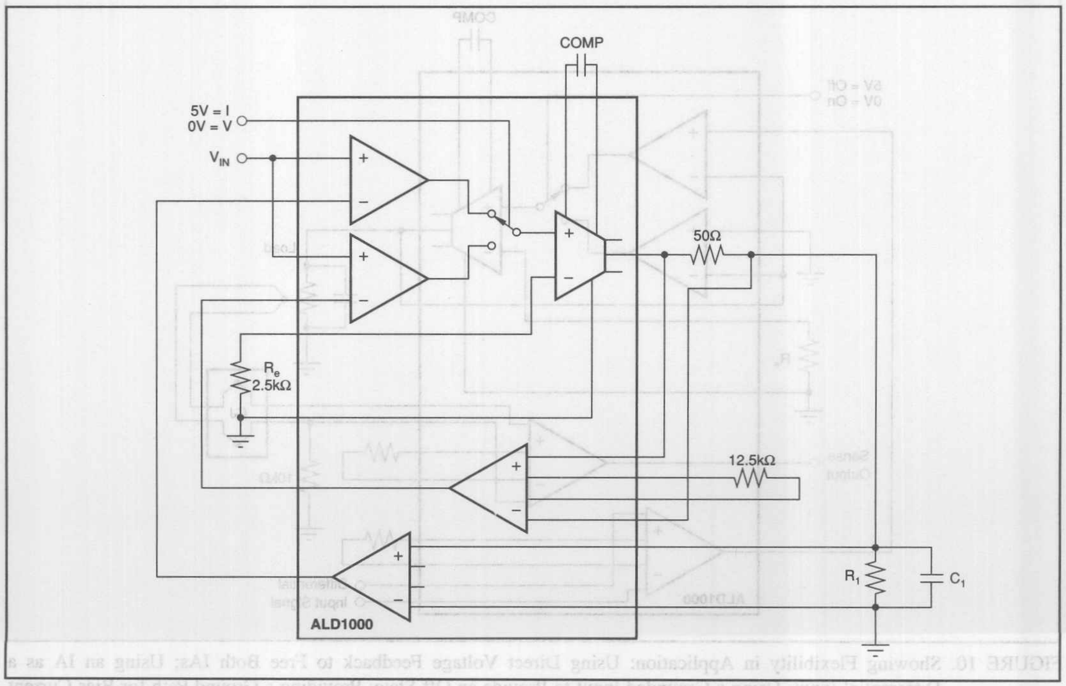


FIGURE 8.Using Internal Drive Transistors.

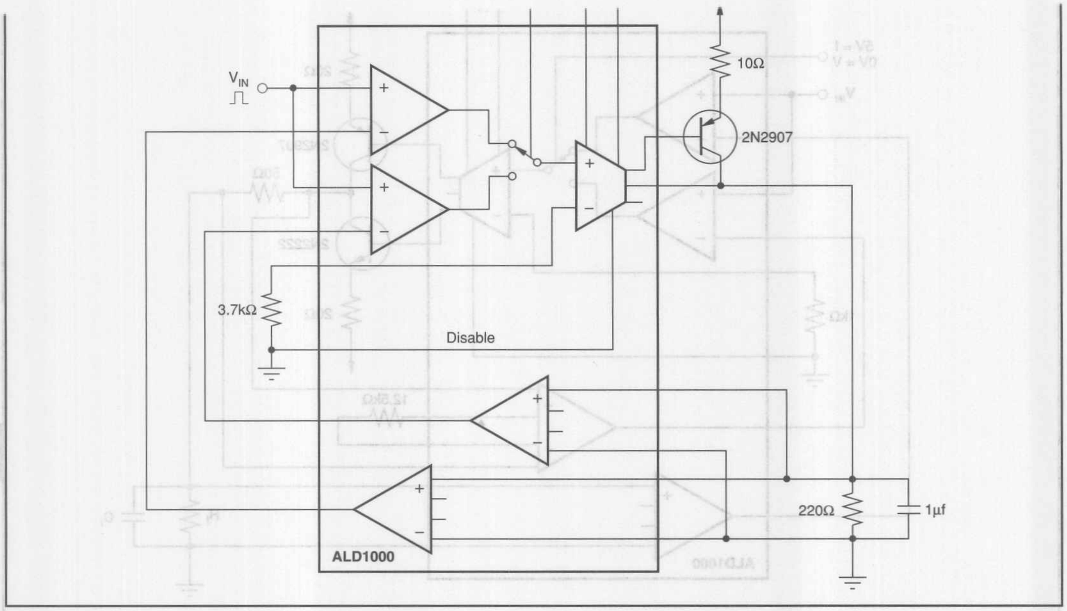


FIGURE 9. Sharing Load Between Internal Drive Transistors and Positive External Drive Transistors to Increase Load Capacity. A Similiar Configuration is Possible with the Negative External Drive Transistor.

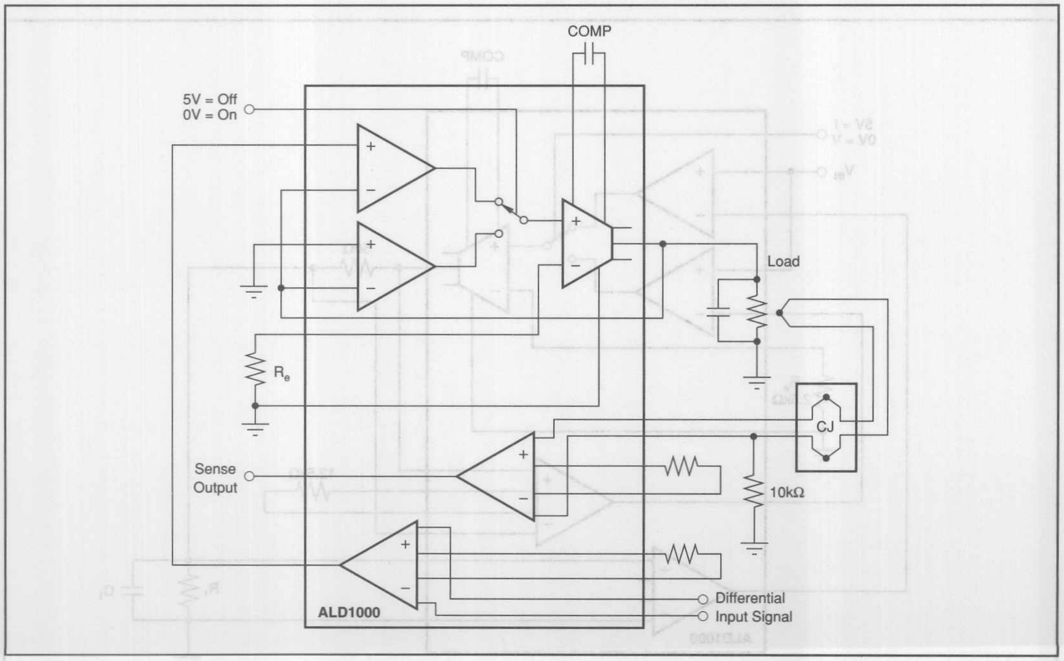
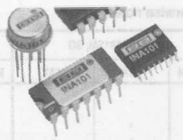


FIGURE 10. Showing Flexibility in Application: Using Direct Voltage Feedback to Free Both IAs; Using an IA as a Differential Input; Using a Grounded Input to Provide an Off State; Providing a Ground Path for Bias Current With a Thermocouple.



INA101

ABRIDGED DATA SHEET

For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 10454

High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- LOW DRIFT: 0.25μV/°C max
- LOW OFFSET VOLTAGE: 25μV max
- LOW NONLINEARITY: 0.002%
- LOW NOISE: 13nV/$\sqrt{\text{Hz}}$
- HIGH CMR: 106dB AT 60Hz
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$
- 14-PIN PLASTIC, CERAMIC DIP, SOL-16, AND TO-100 PACKAGES

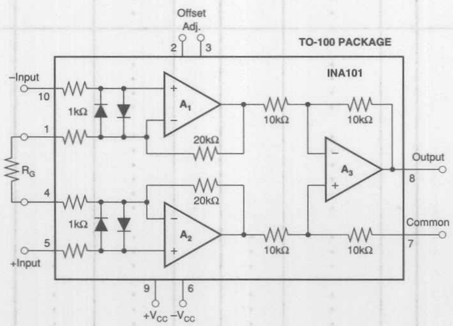
APPLICATIONS

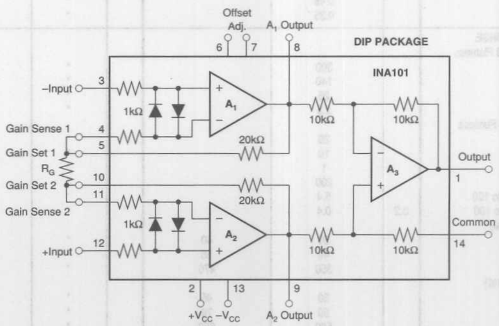
- STRAIN GAGES
- THERMOCOUPLES
- RTDs
- REMOTE TRANSDUCERS
- LOW-LEVEL SIGNALS
- MEDICAL INSTRUMENTATION

DESCRIPTION

The INA101 is a high accuracy instrumentation amplifier designed for low-level signal amplification and general purpose data acquisition. Three precision op amps and laser-trimmed metal film resistors are integrated on a single monolithic integrated circuit.

The INA101 is packaged in TO-100 metal, 14-pin plastic and ceramic DIP, and SOL-16 surface-mount packages. Commercial, industrial and military temperature range models are available.





International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

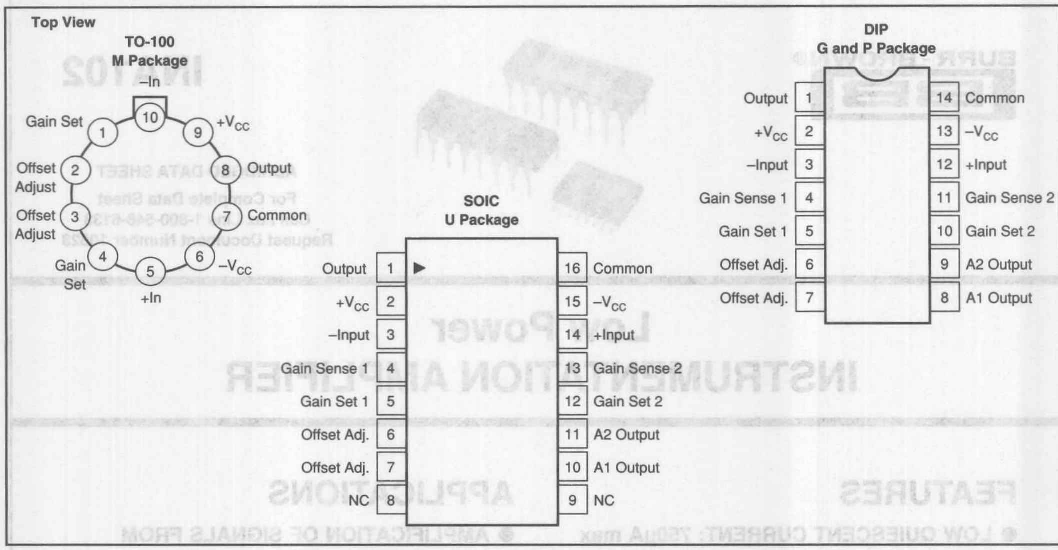
At +25°C with ±15VDC power supply and in circuit of Figure 1 unless otherwise noted.

	INA101AM, AG			INA101SM, SG			INA101CM, CG			INA101HP, KU			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN													
Range of Gain	1		1000	*		*	*		*	*		*	V/V
Gain Equation		$G = 1 + (40k/R_G)$			*			*			*		V/V
Error from Equation, DC(1)		±(0.04 + 0.00016G −0.02/G)	±(0.1 + 0.0003G −0.05/G)		*	*		*	*		±(0.1 + 0.00015G) −0.05/G	±(0.3 + 0.0002G) −0.10/G	%
Gain Temp. Coefficient(3)													
G = 1		2	5		*	*		*	*		*	*	ppm/°C
G = 10		20	100		*	*		10	*		*	*	ppm/°C
G = 100		22	110		*	*		11	*		*	*	ppm/°C
G = 1000		22	110		*	*		11	*		*	*	ppm/°C
Nonlinearity, DC(2)		$\pm(0.002 + 10^{-5}G)$	$\pm(0.005 + 2 \times 10^{-5}G)$		$\pm(0.001 + 10^{-5}G)$	$\pm(0.002 + 10^{-5}G)$		$\pm(0.001 + 10^{-5}G)$	$\pm(0.002 + 10^{-5}G)$		*	*	% of p-p FS
RATED OUTPUT													
Voltage	±10	±12.5		*	*		*	*		*	*		V
Current	±5	±10		*	*		*	*		*	*		mA
Output Impedance		0.2			*			*			*		Ω
Capacitive Load		1000			*			*			*		pF
INPUT OFFSET VOLTAGE													
Initial Offset at +25°C		±(25 + 200/G)	±(50 + 400/G)		±10+ 100/G)	±(25 +200/G)		±(10+ 100/G)	±(25 + 200/G)		±(125 + 450/G)	±(250 + 900/G)	µV
vs Temperature			±(2 + 20/G)			±(0.75 + 10/G)			±(0.25 + 10/G)		±(2 + 20/G)		µV/°C
vs Supply		±(1 + 20/G)			*			*			*		µV/V
vs Time		±(1 + 20/G)			*			*			*		µV/mo
INPUT BIAS CURRENT													
Initial Bias Current (each input)		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.2			*			*					nA/°C
vs Supply		±0.1			*			*					nA/V
Initial Offset Current		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.5											nA/°C
INPUT IMPEDANCE													
Differential		$10^{10} \parallel 3$			*			*			*		Ω ∥ pF
Common-mode		$10^{10} \parallel 3$			*			*			*		Ω ∥ pF
INPUT VOLTAGE RANGE													
Range, Linear Response	±10	±12		*	*		*	*		*	*		V
CMR with 1kΩ Source Imbalance													
DC to 60Hz, G = 1	80	90		*	*		*	*		65	85		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		90	95		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		100	105		dB
INPUT NOISE													
Input Voltage Noise													
f_B = 0.01Hz to 10Hz		0.8			*			*			*		µV, p-p
Density, G = 1000													
f_O = 10Hz		18			*			*			*		nV/√Hz
f_O = 100Hz		15			*			*			*		nV/√Hz
f_O = 1kHz		13			*			*			*		nV/√Hz
Input Current Noise													
f_B = 0.01Hz to 10Hz		50			*			*			*		pA, p-p
Density													
f_O = 10Hz		0.8			*			*			*		pA/√Hz
f_O = 100Hz		0.46			*			*			*		pA/√Hz
f_O = 1kHz		0.35			*			*			*		pA/√Hz
DYNAMIC RESPONSE													
Small Signal, ±3dB Flatness													
G = 1		300			*			*			*		kHz
G = 10		140			*			*			*		kHz
G = 100		25			*			*			*		kHz
G = 1000		2.5			*			*			*		kHz
Small Signal, ±1% Flatness													
G = 1		20			*			*			*		kHz
G = 10		10			*			*			*		kHz
G = 100		1			*			*			*		kHz
G = 1000		200			*			*			*		Hz
Full Power, G = 1 to 100		6.4			*			*			*		kHz
Slew Rate, G = 1 to 100	0.2	0.4		*	*		*	*		*	*		V/µs
Settling Time (0.1%)													
G = 1		30	40		*	*		*	*		*	*	µs
G = 100		40	55		*	*		*	*		*	*	µs
G = 1000		350	470		*	*		*	*		*	*	µs
Settling Time (0.01%)													
G = 1		30	45		*	*		*	*		*	*	µs
G = 100		50	70		*	*		*	*		*	*	µs
G = 1000		500	650		*	*		*	*		*	*	µs
POWER SUPPLY													
Rated Voltage		±15			*			*			*		V
Voltage Range	±5		±20	*		*	*		*	*		*	V
Current, Quiescent(2)		±6.7	±8.5		*	*		*	*		*	*	mA
TEMPERATURE RANGE(5)													
Specification	−25		+85	−55		+125	*		*	0		+70	°C
Operation	−55		+125	*		*	*		*	−25		+85	°C
Storage	−65		+150	*		*	*		*	−40		+85	°C

* Specifications same as for INA101AM, AG.

NOTES: (1) Typically the tolerance of R_G will be the major source of gain error. (2) Nonlinearity is the maximum peak deviation from the best straight-line as a percentage of peak-to-peak full scale output. (3) Not including the TCR of R_G. (4) Adjustable to zero at any one gain. (5) θ_{JC} output stage = 113°C/W, θ_{JC} quiescent circuitry = 19°C/W, θ_{CA} = 83°C/W.

PIN CONFIGURATIONS



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA101AM	10-Pin Metal TO-100	−25°C to +85°C
INA101CM	10-Pin Metal TO-100	−25°C to +85°C
INA101AG	14-Pin Ceramic DIP	−25°C to +85°C
INA101CG	14-Pin Ceramic DIP	−25°C to +85°C
INA101HP	14-Pin Plastic DIP	0°C to +70°C
INA101KU	SOL-16 Surface-Mount	0°C to +70°C
INA101SG	14-Pin Ceramic DIP	−55°C to +125°C
INA101SM	10-Pin Metal TO-100	−55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Power Dissipation	600mW
Input Voltage Range	$\pm V_{CC}$
Output Short Circuit (to ground)	Continuous
Operating Temperature M, G Package	−55°C to +125°C
P, U Package	−25°C to +85°C
Storage Temperature M, G Package	−65°C to +150°C
P, U Package	−40°C to +85°C
Lead Temperature (soldering, 10s) M, G, P Package	+300°C
Lead Temperature (wave soldering, 3s) U Package	+260°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA101AM	10-Pin Metal TO-100	007
INA101CM	10-Pin Metal TO-100	007
INA101AG	14-Pin Ceramic DIP	169
INA101CG	14-Pin Ceramic DIP	169
INA101HP	14-Pin Plastic DIP	010
INA101KU	SOL-16 Surface-Mount	211
INA101SG	14-Pin Ceramic DIP	169
INA101SM	10-Pin Metal TO-100	007

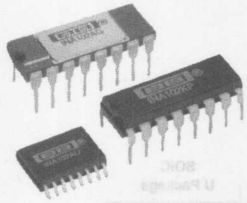
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR - BROWN®



INA102

ABRIDGED DATA SHEET

For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 10523

Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 750μA max
- INTERNAL GAINS: 1, 10, 100, 1000
- LOW GAIN DRIFT: 5ppm/°C max
- HIGH CMR: 90dB min
- LOW OFFSET VOLTAGE DRIFT: 2μV/°C max
- LOW OFFSET VOLTAGE: 100μV max
- LOW NONLINEARITY: 0.01% max
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$

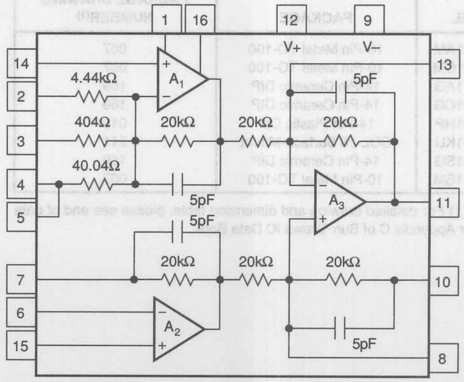
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  Strain Gages (Weigh Scale Applications)
  Thermocouples
  Bridge Transducers
- REMOTE TRANSDUCER AMPLIFIER
- LOW-LEVEL SIGNAL AMPLIFIER
- MEDICAL INSTRUMENTATION
- MULTICHANNEL SYSTEMS
- BATTERY POWERED EQUIPMENT

DESCRIPTION

The INA102 is a high-accuracy monolithic instrumentation amplifier designed for signal conditioning applications where low quiescent power is desired. On-chip thin-film resistors provide excellent temperature and stability performance. State-of-the-art laser-trimming technology insures high gain accuracy and common-mode rejection while avoiding expensive external components. These features make the INA102 ideally suited for battery-powered and high-volume applications.

The INA102 is also convenient to use. A gain of 1, 10, 100, or 1000 may be selected by simply strapping the appropriate pins together. A gain drift of 5ppm/°C in low gains can then be achieved without external adjustment. When higher-than-specified CMR is required, CMR can be trimmed using the pins provided. In addition, balanced filtering can be accomplished in the output stage.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

		INA102AG			INA102CG			INA102KP/INA102AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
GAIN											
Range of Gain		1		1000	*		*	*		*	V/V
Gain Equation, External, ±20%			$G = 1 + (40k/R_G)$[1]				*			*	V/V
Error, DC: G = 1	T_A = +25°C			0.1			0.05			0.15	%
G = 10	T_A = +25°C			0.1			0.05			0.35	%
G = 100	T_A = +25°C			0.25			0.15			0.4	%
G = 1000	T_A = +25°C			0.75			0.5			0.9	%
G = 1	$T_A = T_{MIN}$ to T_{MAX}			0.16			0.08			0.21	%
G = 10	$T_A = T_{MIN}$ to T_{MAX}			0.19			0.11			0.44	%
G = 100	$T_A = T_{MIN}$ to T_{MAX}			0.37			0.21			0.52	%
G = 1000	$T_A = T_{MIN}$ to T_{MAX}			0.93			0.62			1.08	%
Gain Temp. Coefficient											
G = 1				10			5			*	ppm/°C
G = 10				15			10			*	ppm/°C
G = 100				20			15			*	ppm/°C
G = 1000				30			20			*	ppm/°C
Nonlinearity, DC											
G = 1	T_A = +25°C			0.03			0.01			*	% of FS
G = 10	T_A = +25°C			0.03			0.01			*	% of FS
G = 100	T_A = +25°C			0.05			0.02			*	% of FS
G = 1000	T_A = +25°C			0.1			0.05			*	% of FS
G = 1	$T_A = T_{MIN}$ to T_{MAX}			0.045			0.015			*	% of FS
G = 10	$T_A = T_{MIN}$ to T_{MAX}			0.045			0.015			*	% of FS
G = 100	$T_A = T_{MIN}$ to T_{MAX}			0.075			0.03			*	% of FS
G = 1000	$T_A = T_{MIN}$ to T_{MAX}			0.15			0.1			*	% of FS
RATED OUTPUT											
Voltage	R_L = 10kΩ	$\pm(\lvert V_{CC}\rvert - 2.5)$			*			*			V
Current		±1			*			*			mA
Short Circuit Current[2]			2			*			*		mA
Output Impedance, G = 1000			0.1			*			*		Ω
INPUT											
OFFSET VOLTAGE											
Initial Offset[3]	T_A = +25°C			±300 ±300/G			±100 ±200/G			*	µV
INA102AU										±500 ±300/G	µV
vs Temperature				±5 ±10/G			±2 ±5/G			*	µV/°C
vs Supply				±40 ±50/G			±10 ±20/G			*	µV/V
vs Time			±(20 + 30/G)			*			*		µV/mo
BIAS CURRENT											
Initial Bias Current											
(Each Input)	$T_A = T_{MIN}$ to T_{MAX}		25	50		6	30		*	*	nA
vs Temperature			±0.1			*			*		nA/°C
vs Supply			±0.1			*			*		nA/V
Initial Offset Current	$T_A = T_{MIN}$ to T_{MAX}		±2.5	±15		±2.5	±10		*	*	nA
vs Temperature			±0.1			*			*		nA/°C
IMPEDANCE											
Differential			$10^{10} \parallel 2$			*			*		Ω ∥ pF
Common-Mode			$10^{10} \parallel 2$			*			*		Ω ∥ pF
VOLTAGE RANGE											
Range, Linear Response	$T_A = T_{MIN}$ to T_{MAX}	$\pm(\lvert V_{CC}\rvert - 4.5)$			*			*			V
CMR With 1kΩ Source Imbalance											
G = 1	DC to 60Hz	80	94		90	*		75	*		dB
G = 10	DC to 60Hz	80	100		90	*		*	*		dB
G = 10 to 1000	DC to 60Hz	80	100		90	*		*	*		dB
NOISE											
Input Voltage Noise											
f_B = 0.01Hz to 10Hz			1			*			*		µVp-p
Density, G = 1000: f_O = 10Hz			30			*			*		nV/√Hz
f_O = 100Hz			25			*			*		nV/√Hz
f_O = 1kHz			25			*			*		nV/√Hz
Input Current Noise											
f_B = 0.01Hz to 10Hz			25			*			*		pAp-p
Density: f_O = 10Hz			0.3			*			*		pA/√Hz
f_O = 100Hz			0.2			*			*		pA/√Hz
f_O = 1kHz			0.15			*			*		pA/√Hz

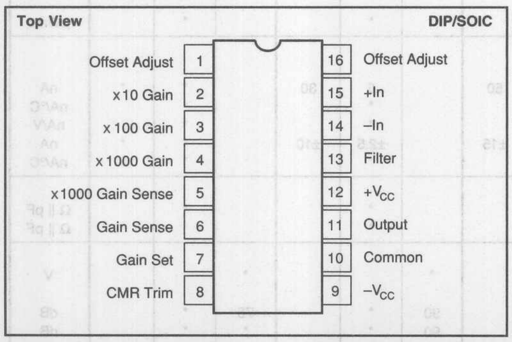
ELECTRICAL (CONT)

PARAMETER	CONDITIONS	INA102AG			INA102CG			INA102KP/INA102AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE											
Small Signal, ±3dB Flatness	V_{OUT} = 0.1Vrms										
G = 1			300			*			*		kHz
G = 10			30			*			*		kHz
G = 100			3			*			*		kHz
G = 1000			0.3			*			*		kHz
Small Signal, ±1% Flatness	V_{OUT} = 0.1Vrms										
G = 1			30			*			*		kHz
G = 10			3			*			*		kHz
G = 100			0.3			*			*		kHz
G = 1000			0.03			*			*		kHz
Full Power, G = 1 to 100	V_{OUT} = 10V, R_L = 10kΩ	1.7	2.5		*	*		*	*		kHz
Slew Rate, G = 1 to 100	V_{OUT} = 10V, R_L = 10kΩ	0.1	0.15		*	*		*	*		V/µs
Settling Time	R_L = 10kΩ, C_L = 100pF										
0.1%: G = 1	10V Step		50			*			*		µs
G = 100			360			*			*		µs
G = 1000			3300			*			*		µs
0.01%: G = 1	10V Step		60			*			*		µs
G = 100			500			*			*		µs
G = 1000			4500			*			*		µs
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±3.5		±18	*		*	*		*	V
Quiescent Current	V_O = 0V, T_A = T_{MIN} to T_{MAX}		±500	±750		*	*		*	*	µA
TEMPERATURE RANGE											
Specification		–25		+85	*		*	0		+70	°C
INA102AU								**–25**		**+85**	°C
Operation	R_L > 50kΩ[(2)]	–25		+85	*		*	–25		+85	°C
Storage		–65		+150	*		*	–55		+125	°C

*Specification same as for INA102AG.

NOTES: (1) The internal gain set resistors have an absolute tolerance of ±20%; however, their tracking is 50ppm/°C. R_G will add to the gain error if gains other than 1, 10, 100, or 1000 are set externally. (2) At high temperature, output drive current is limited. An external buffer can be used if required. (3) Adjustable to zero.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply .... ±18V
Input Voltage Range .... $\pm V_{CC}$
Operating Temperature Range .... –25°C to +85°C
Storage Temperature Range: Ceramic .... –65°C to +150°C
Plastic, SOIC .... –55°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
Output Short Circuit Duration .... Continuous to Ground

PACKAGE INFORMATION

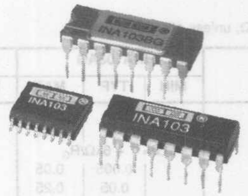
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[(1)]
INA102AG	16-Pin Ceramic DIP	109
INA102CG	16-Pin Ceramic DIP	109
INA102KP	16-Pin Plastic DIP	180
INA102AU	16-Pin SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA102AG	16-Pin Ceramic DIP	–25°C to +85°C
INA102CG	16-Pin Ceramic DIP	–25°C to +85°C
INA102KP	16-Pin Plastic DIP	0°C to +70°C
INA102AU	16-Pin Plastic SOIC	–25°C to +85°C

BURR - BROWN®



INA103

Low Noise, Low Distortion INSTRUMENTATION AMPLIFIER

FEATURES

- LOW NOISE: $1nV/\sqrt{Hz}$
- LOW THD+N: 0.0009% at 1kHz, G = 100
- HIGH GBW: 100MHz at G = 1000
- WIDE SUPPLY RANGE: ±9V to ±25V
- HIGH CMRR: >110dB
- BUILT-IN GAIN SETTING RESISTORS: G = 1, 100
- UPGRADES AD625

APPLICATIONS

- HIGH QUALITY MICROPHONE PREAMPS (REPLACES TRANSFORMERS)
- MOVING-COIL PREAMPLIFIERS
- DIFFERENTIAL RECEIVERS
- AMPLIFICATION OF SIGNALS FROM:
  Strain Gages (Weigh Scale Applications)
  Thermocouples
  Bridge Transducers

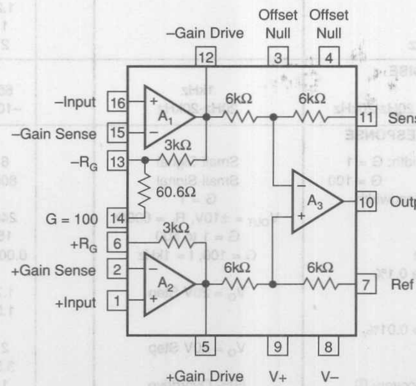
DESCRIPTION

The INA103 is a very low noise, low distortion monolithic instrumentation amplifier. Its current-feedback circuitry achieves very wide bandwidth and excellent dynamic response. It is ideal for low-level audio signals such as balanced low-impedance microphones. The INA103 provides near-theoretical limit noise performance for 200Ω source impedances. Many industrial applications also benefit from its low noise and wide bandwidth.

Unique distortion cancellation circuitry reduces distortion to extremely low levels, even in high gain. Its balanced input, low noise and low distortion provide superior performance compared to transformer-coupled microphone amplifiers used in professional audio equipment.

The INA103's wide supply voltage (±9 to ±25V) and high output current drive allow its use in high-level audio stages as well. A copper lead frame in the plastic DIP assures excellent thermal performance.

The INA103 is available in 16-pin plastic DIP, 16-pin ceramic DIP and SOL-16 surface-mount packages. Commercial and industrial temperature range models are available.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

All specifications at $T_A = +25°C$, $V_S = ±15V$ and $R_L = 2kΩ$, unless otherwise noted.

PARAMETER	CONDITIONS	INA103AG MIN	INA103AG TYP	INA103AG MAX	INA103BG MIN	INA103BG TYP	INA103BG MAX	INA103KP, KU MIN	INA103KP, KU TYP	INA103KP, KU MAX	UNITS
GAIN											
Range of Gain		1		1000	*		*	*		*	V/V
Gain Equation (1)			$G = 1 + 6kΩ/R_G$			*			*		V/V
Gain Error, DC G = 1	±10V Output		0.005	0.05		0.003	0.01		*	*	%
G = 100			0.05	0.25		0.04	0.1		0.07	*	%
Equation			0.5			0.1			*		%
Gain Temp. Co. G = 1	±10V Output		10			*			*		ppm/°C
G = 100			25			*			*		ppm/°C
Equation			25			*			*		ppm/°C
Nonlinearity, DC G = 1	±10V Output		0.0003	0.01		0.0002	0.002		*	*	% of FS(2)
G = 100			0.0006	0.01		0.0006	0.004		*	*	% of FS
OUTPUT											
Voltage, $R_L = 600Ω$	$T_A = T_{MIN}$ to T_{MAX}	±11.5	±12		*	*		*	*		V
$R_L = 600Ω$	$V_S = ±25$, $T_A = 25°C$	±20	±21		*	*		*	*		V
Current	$T_A = T_{MIN}$ to T_{MAX}	±40			*			*			mA
Short Circuit Current			±70			*			*		mA
Capacitive Load Stability			10			*			*		nF
INPUT OFFSET VOLTAGE											
Initial Offset RTI (3)			(20 + 700/G)	(100 + 5000/G)		(20 + 320/G)	(50 + 2000/G)		(30 + 1200/G)		μV
(KU Grade)										(250+ 5000/G)	μV
vs Temp G = 1 to 1000	$T_A = T_{MIN}$ to T_{MAX}		1 + 20/G			0.75 + 10/G			1 + 20/G		μV/°C
G = 1000	$T_A = T_{MIN}$ to T_{MAX}		1	2		*	*				μV/°C
vs Supply	±9V to ±25V		0.2 + 8/G	4 + 60/G		*	2 + 30/G		*	*	μV/V
INPUT BIAS CURRENT											
Initial Bias Current			2.5	12		*	8		*	*	μA
vs Temp	$T_A = T_{MIN}$ to T_{MAX}		15			*	40 (4)		*		nA/°C
Initial Offset Current			0.04	1		0.03	0.5		*	*	μA
vs Temp	$T_A = T_{MIN}$ to T_{MAX}		0.5			*	2.5 (4)		*		nA/°C
INPUT IMPEDANCE											
Differential Mode			60 || 2			*			*		MΩ || pF
Common-Mode			60 || 5			*			*		MΩ || pF
INPUT VOLTAGE RANGE											
Common-Mode Range (5)		±11	±12		*	*		*	*		V
CMR											
G = 1	DC to 60Hz	72	86		80	91		*	*		dB
G = 100	DC to 60Hz	100	125		110	129		*	*		dB
INPUT NOISE											
Voltage (6)	$R_S = 0Ω$										
10Hz			2			*			*		nV/√Hz
100Hz			1.2			*			*		nV/√Hz
1kHz			1			*	1.4 (4)		*		nV/√Hz
Current, 1kHz			2			*			*		pA/√Hz
OUTPUT NOISE											
Voltage	1kHz		65			*			*		nV/√Hz
A Weighted, 20Hz-20kHz	20Hz-20kHz		–100			*			*		dBu
DYNAMIC RESPONSE											
–3dB Bandwidth: G = 1	Small Signal		6			*			*		MHz
G = 100	Small Signal		800			*			*		kHz
Full Power Bandwidth	G = 1 $V_{OUT} = ±10V$, $R_L = 600Ω$		240			*			*		kHz
Slew Rate	G = 1 to 500		15			*			*		V/μs
THD + Noise	G = 100, f = 1kHz		0.0009			*			*		%
Settling TIme 0.1%											
G = 1	$V_O = 20V$ Step		1.7			*			*		μs
G = 100			1.5			*			*		μs
Settling Time 0.01%											
G = 1	$V_O = 20V$ Step		2			*			*		μs
G = 100			3.5			*			*		μs
Overload Recovery (7)	50% Overdrive		1			*			*		μs

*Same specification as INA103AG.

NOTES: (1) Gains other than 1 and 100 can be set by adding an external resistor, R_G between pins 2 and 15. Gain accuracy is a function of R_G. (2) FS = Full Scale. (3) Adjustable to zero. (4) Guaranteed by design. (5) $V_O = 0V$, see Typical Curves for V_{CM} vs V_O. (6) $V_{NOISE\ RTI} = \sqrt{V^2_{N\ INPUT} + (V_{N\ OUTPUT}/Gain)^2 + 4KTR_G}$. See Typical Curves. (7) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

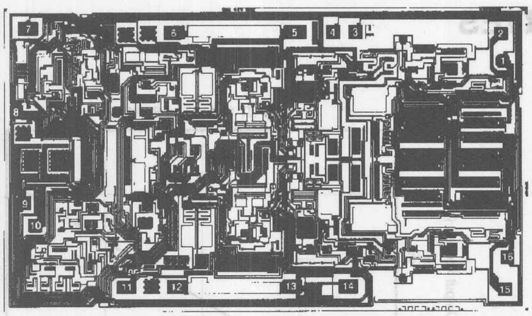
SPECIFICATIONS (CONT)

ELECTRICAL

All specifications at T_A = +25°C, V_S = ±15V and R_L = 2kΩ, unless otherwise noted.

		INA103AG			INA103BG			INA103KP, KU			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±9		±25	*		*	*		*	V
Quiescent Current			9	12.5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		–25		+85	*		*	0		+70	°C
Operation		–55		+125	*		*	–40		+85	°C
Storage		–65		+150	*		*	–40		+100	°C
Thermal Resistance, θ_{JA}			100			*			*		°C/W

DICE INFORMATION



INA103 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	+Input	9	V+
2	+Gain Sense	10	Output
3	+Offset Null	11	Sense
4	–Offset Null	12	–Gain Drive
5	+Gain Drive	13	$-R_G$
6	$+R_G$	14	G = 100
7	Ref	15	– Gain Sense
8	V–	16	–Input

Substrate Bias: Electrically connected to V– supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	194 x 115 ±5	4.93 x 2.92 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Chromium-Silver

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA103AG	Ceramic DIP	109
INA103BG	Ceramic DIP	109
INA103KP	Plastic DIP	180
INA103KU	SOL-16	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

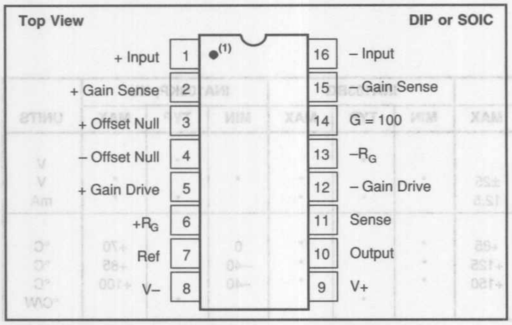
MODEL	PACKAGE	TEMP RANGE
INA103AG	Ceramic DIP	–25°C to +85°C
INA103BG	Ceramic DIP	–25°C to +85°C
INA103KP	Plastic DIP	0°C to +70°C
INA103KU	*SOL-16*	*0°C to +70°C*

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION



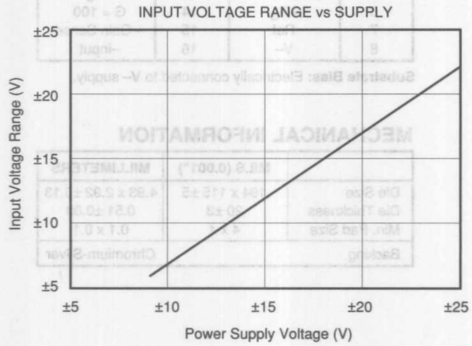
NOTE: (1) Pin 1 Marking—SOL-16 Package

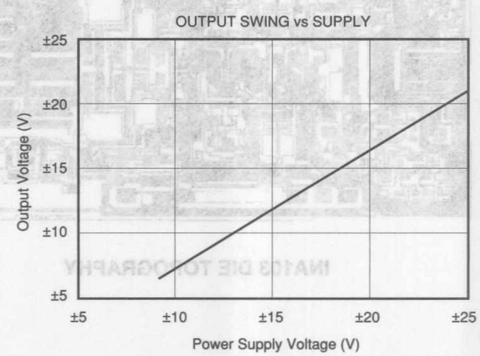
ABSOLUTE MAXIMUM RATINGS

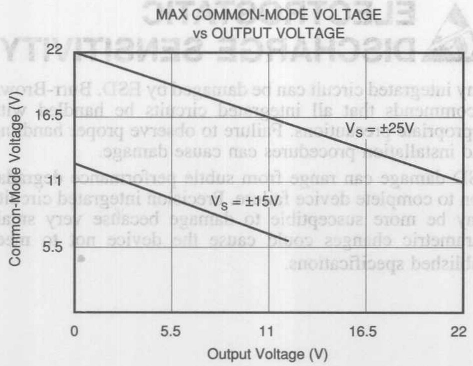
Power Supply Voltage	±25V
Input Voltage Range, Continuous	$\pm V_S$
Operating Temperature Range:	
P, U Package	–40°C to +85°C
G Package	–55°C to +125°C
Storage Temperature Range:	
P, U Package	–40°C to +100°C
G Package	–65°C to +150°C
Junction Temperature:	
P, U Package	+125°C
G Package	+150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common	Continuous

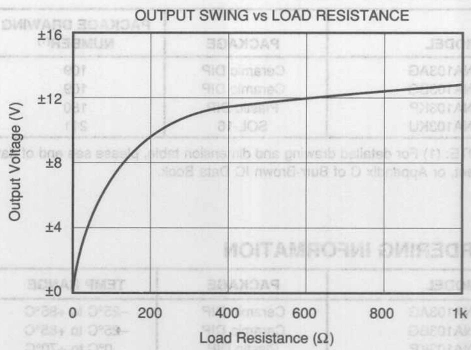
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V unless otherwise noted.



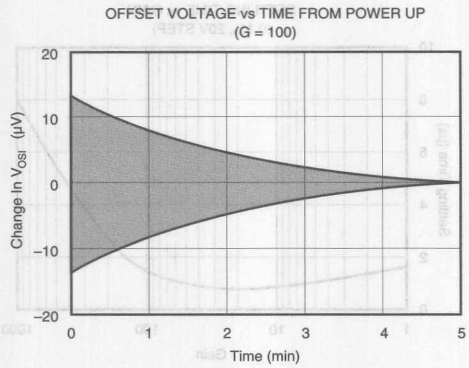


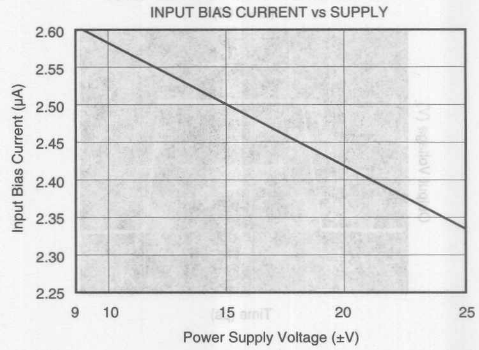


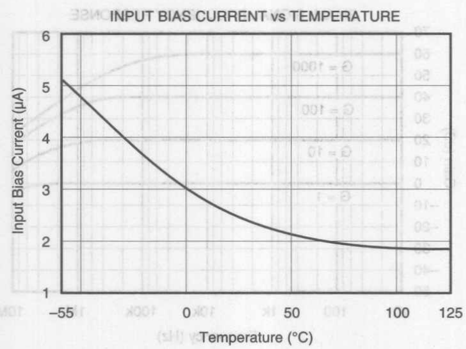


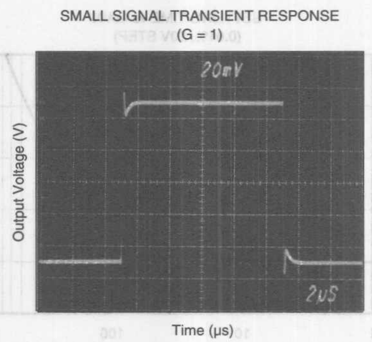
TYPICAL PERFORMANCE CURVES (CONT)

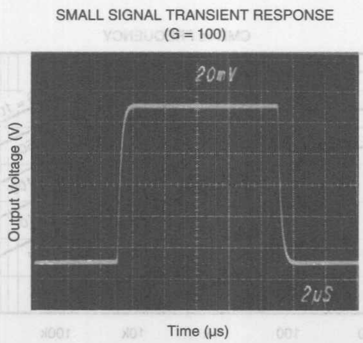
At $T_A = +25°C$, $V_S = \pm15V$ unless otherwise noted.

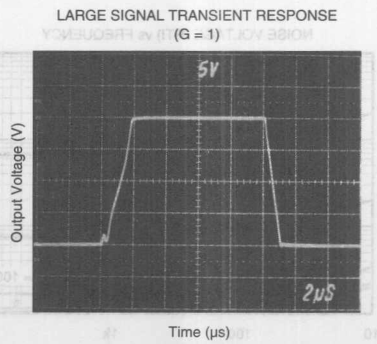












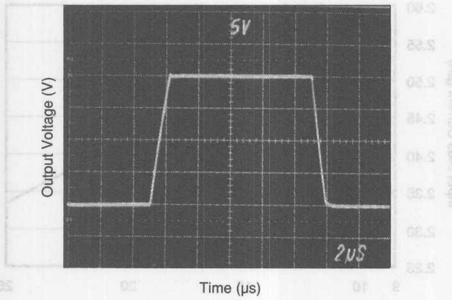
INA103

4

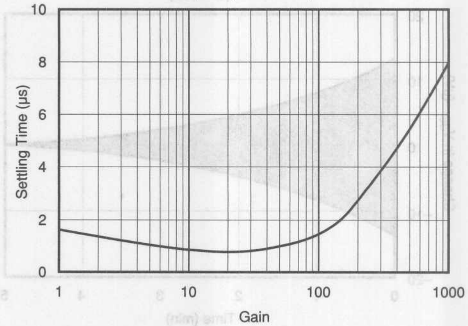
INSTRUMENTATION AMPLIFIERS

At $T_A = +25°C$, $V_S = \pm15V$ unless otherwise noted.

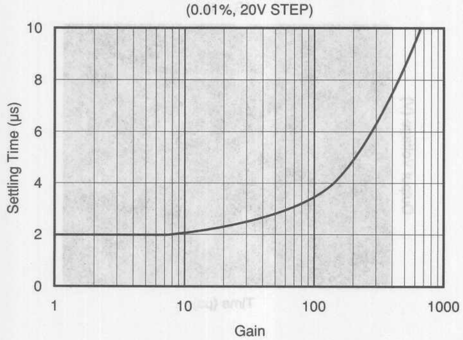
LARGE SIGNAL TRANSIENT RESPONSE
(G = 100)



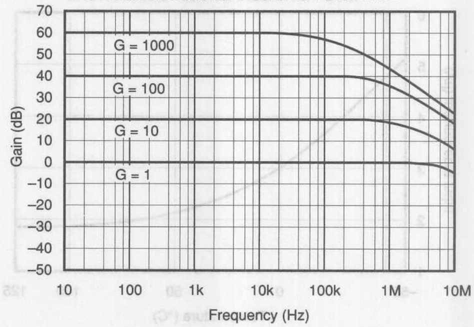
SETTLING TIME vs GAIN
(0.1%, 20V STEP)



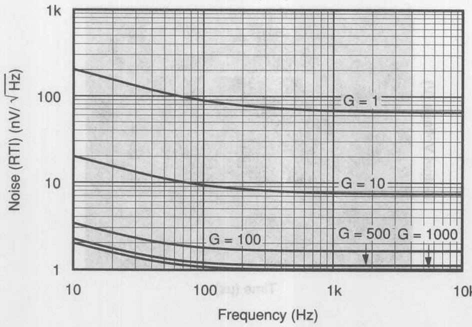
SETTLING TIME vs GAIN
(0.01%, 20V STEP)



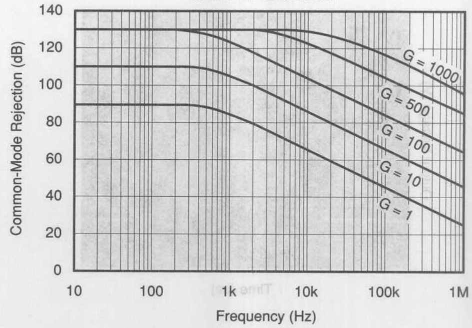
SMALL-SIGNAL FREQUENCY RESPONSE



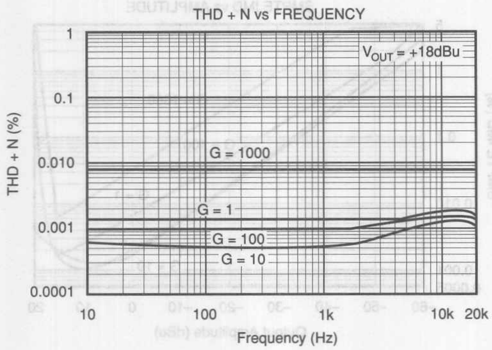
NOISE VOLTAGE (RTI) vs FREQUENCY

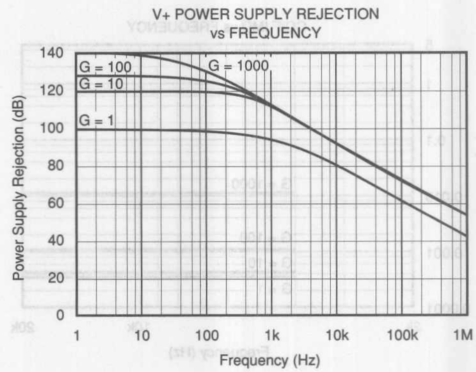


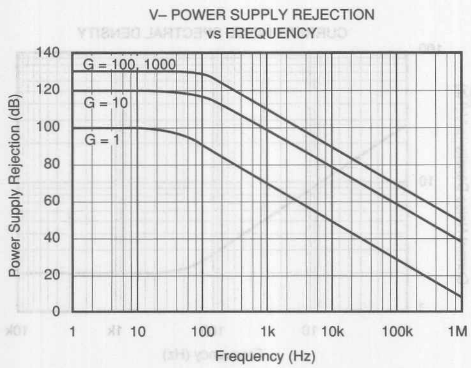
CMR vs FREQUENCY

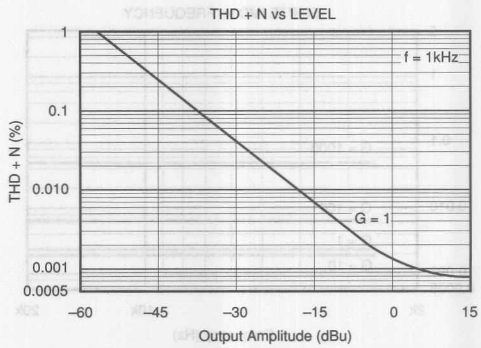


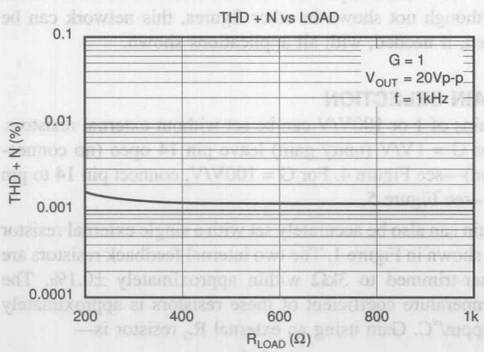
At T_A = +25°C, V_S = ±15V unless otherwise noted.

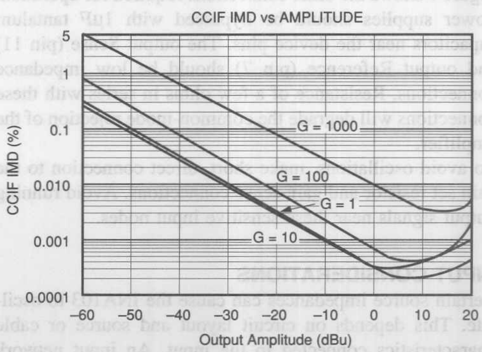






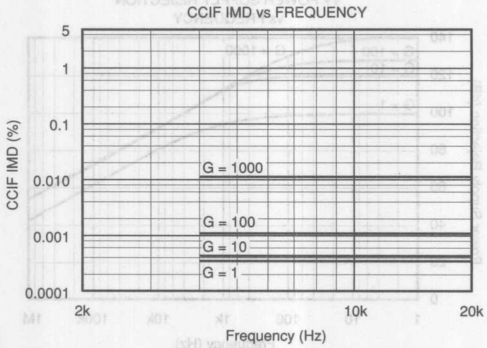


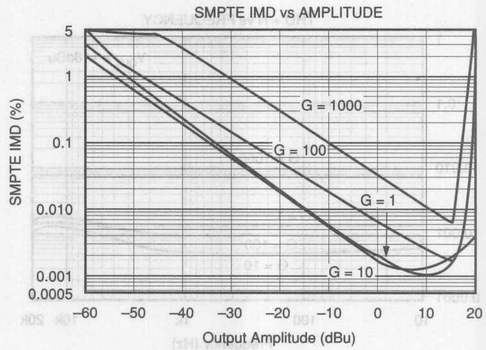


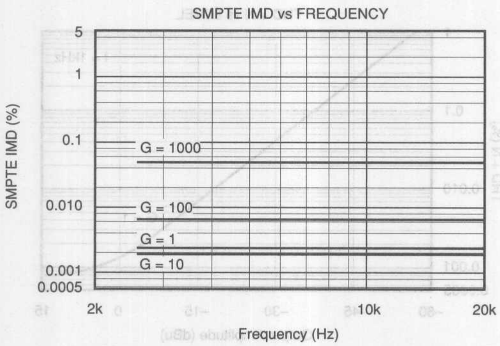


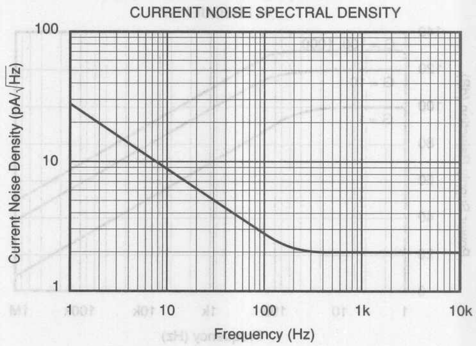
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = ±15V$ unless otherwise noted.









APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation. Power supplies should be bypassed with 1µF tantalum capacitors near the device pins. The output Sense (pin 11) and output Reference (pin 7) should be low impedance connections. Resistance of a few ohms in series with these connections will degrade the common-mode rejection of the amplifier.

To avoid oscillations, make short, direct connection to the gain set resistor and gain sense connections. Avoid running output signals near these sensitive input nodes.

INPUT CONSIDERATIONS

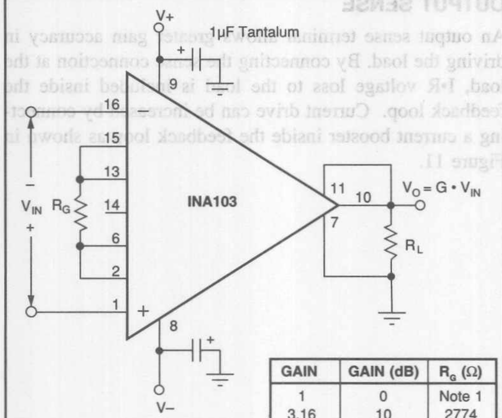
Certain source impedances can cause the INA103 to oscillate. This depends on circuit layout and source or cable characteristics connected to the input. An input network consisting of a small inductor and resistor (Figure 2) can greatly reduce the tendancy to oscillate. This is especially useful if various input sources are connected to the INA103. Although not shown in other figures, this network can be used, if needed, with all applications shown.

GAIN SELECTION

Gains of 1 or 100V/V can be set without external resistors. For G = 1V/V (unity gain) leave pin 14 open (no connection)—see Figure 4. For G = 100V/V, connect pin 14 to pin 6—see Figure 5.

Gain can also be accurately set with a single external resistor as shown in Figure 1. The two internal feedback resistors are laser-trimmed to 3kΩ within approximately ±0.1%. The temperature coefficient of these resistors is approximately 50ppm/°C. Gain using an external R_G resistor is—

$$G = 1 + \frac{6k\Omega}{R_G}$$



GAIN	GAIN (dB)	R_G (Ω)
1	0	Note 1
3.16	10	2774
10	20	667
31.6	30	196
100	40	60.6[2]
316	50	19
1000	60	6

NOTES: (1) No R_G required for G = 1. See gain-set connections in Figure 4. (2) R_G for G = 100 is internal. See gain-set connection in Figure 5.

FIGURE 1. Basic Circuit Configuration.

Accuracy and TCR of the external R_G will also contribute to gain error and temperature drift. These effects can be directly inferred from the gain equation.

Connections available on A_1 and A_2 allow external resistors to be substituted for the internal 3kΩ feedback resistors. A precision resistor network can be used for very accurate and stable gains. To preserve the low noise of the INA103, the value of external feedback resistors should be kept low. Increasing the feedback resistors to 20kΩ would increase noise of the INA103 to approximately 1.5nV/√Hz. Due to the current-feedback input circuitry, bandwidth would also be reduced.

NOISE PERFORMANCE

The INA103 provides very low noise with low source impedance. Its 1nV/√Hz voltage noise delivers near theoretical noise performance with a source impedance of 200Ω.

Relatively high input stage current is used to achieve this low noise. This results in relatively high input bias current and input current noise. As a result, the INA103 may not provide best noise performance with source impedances greater than 10kΩ. For source impedance greater than 10kΩ, consider the INA114 (excellent for precise DC applications), or the INA111 FET-input IA for high speed applications.

OFFSET ADJUSTMENT

Offset voltage of the INA103 has two components: input stage offset voltage is produced by A_1 and A_2; and, output stage offset is produced by A_3. Both input and output stage offset are laser trimmed and may not need adjustment in many applications.

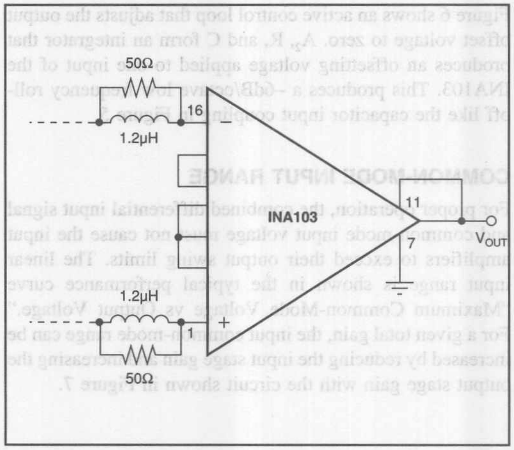


FIGURE 2. Input Stabilization Network.

Offset voltage can be trimmed with the optional circuit shown in Figure 3. This offset trim circuit primarily adjusts the output stage offset, but also has a small effect on input stage offset. For a 1mV adjustment of the output voltage, the input stage offset is adjusted approximately 1µV. Use this adjustment to null the INA103's offset voltage with zero differential input voltage. Do not use this adjustment to null offset produced by a sensor, or offset produced by subsequent stages, since this will increase temperature drift.

To offset the output voltage without affecting drift, use the circuit shown in Figure 4. The voltage applied to pin 7 is summed at the output. The op amp connected as a buffer provides a low impedance at pin 7 to assure good common-mode rejection.

Figure 5 shows a method to trim offset voltage in AC-coupled applications. A nearly constant and equal input bias current of approximately 2.5µA flows into both input terminals. A variable input trim voltage is created by adjusting the balance of the two input bias return resistances through which the input bias currents must flow.

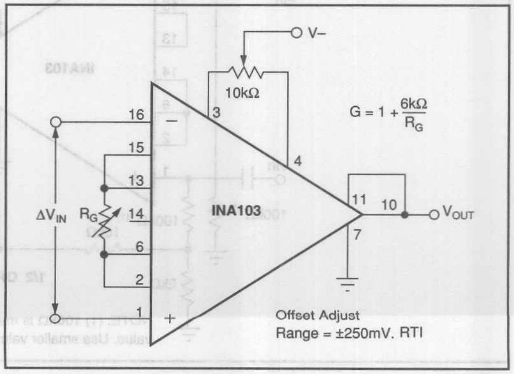


FIGURE 3. Offset Adjustment Circuit.

offset voltage to zero. A_2, R, and C form an integrator that produces an offsetting voltage applied to one input of the INA103. This produces a –6dB/octave low frequency roll-off like the capacitor input coupling in Figure 5.

COMMON-MODE INPUT RANGE

For proper operation, the combined differential input signal and common-mode input voltage must not cause the input amplifiers to exceed their output swing limits. The linear input range is shown in the typical performance curve "Maximum Common-Mode Voltage vs Output Voltage." For a given total gain, the input common-mode range can be increased by reducing the input stage gain and increasing the output stage gain with the circuit shown in Figure 7.

An output sense terminal allows greater gain accuracy in driving the load. By connecting the sense connection at the load, I•R voltage loss to the load is included inside the feedback loop. Current drive can be increased by connecting a current booster inside the feedback loop as shown in Figure 11.

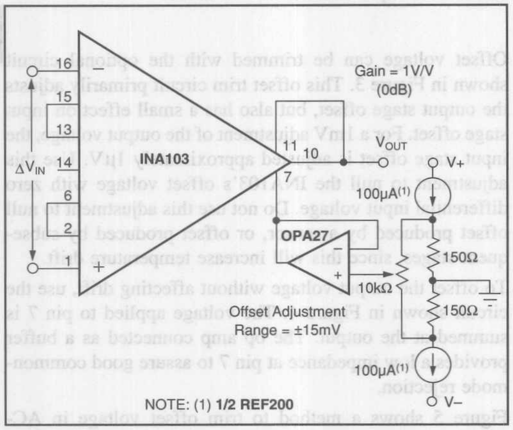


FIGURE 4. Output Offsetting.

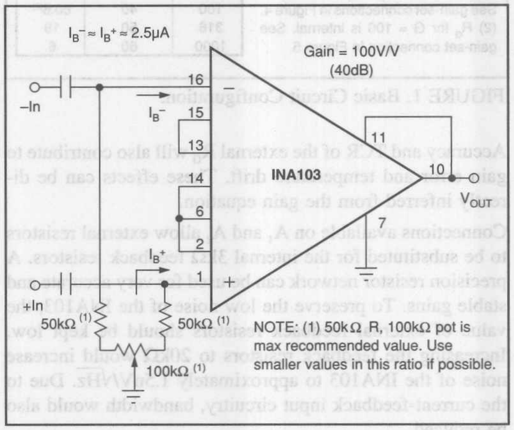


FIGURE 5. Input Offset Adjustment for AC-Coupled Inputs.

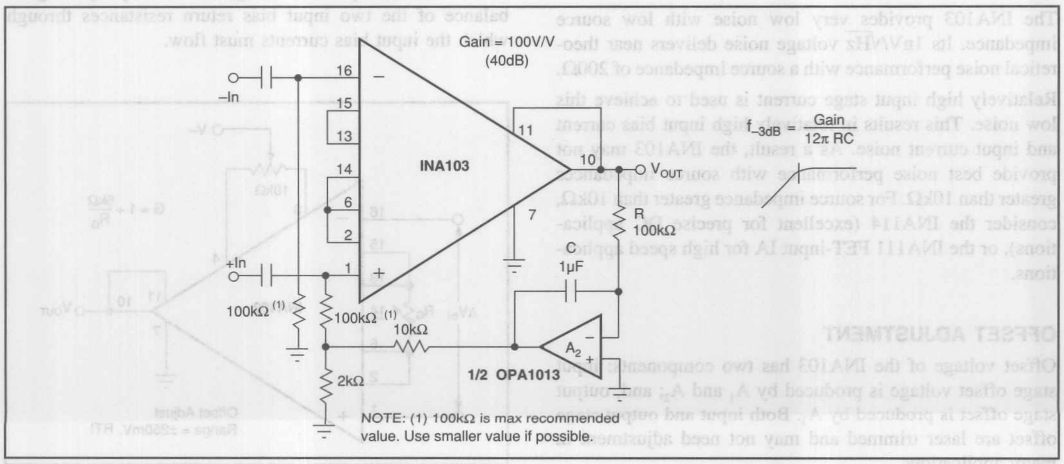
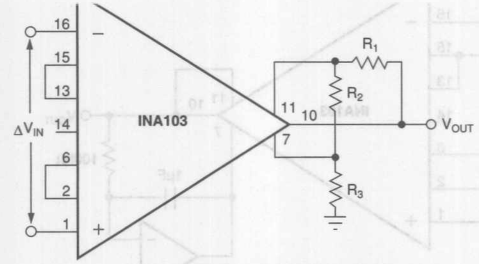


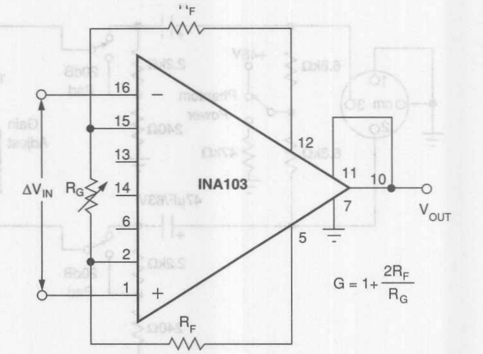
FIGURE 6. Automatic DC Restoration.



Output Stage Gain = $\frac{(R_2 \parallel 12k) + R_1 + R_3}{(R_2 \parallel 12k)}$

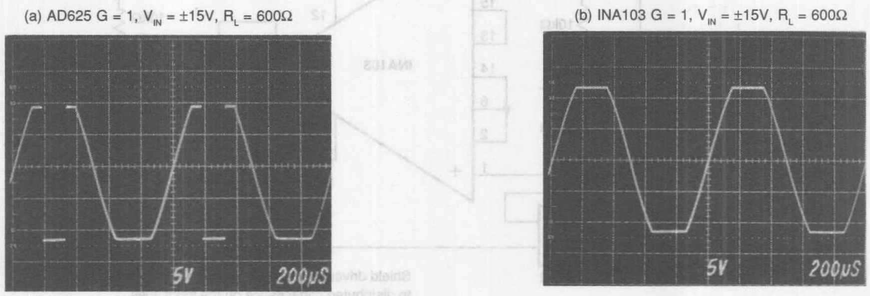
OUTPUT STAGE GAIN	R_1 and R_3 (kΩ)	R_2 (Ω)
2	1k	2.4k
5	1.2k	632Ω
10	1.2k	273Ω

FIGURE 7. Gain Adjustment of Output Stage.



R_F > 10kΩ can increase noise and reduce bandwidth—see text.
NOTE: AD625 equivalent pinout.

FIGURE 8. Use of External Resistors for Gain Set.



A common problem with many IC op amps and instrumentation amplifiers is shown in (a). Here, the amplifier's input is driven beyond its linear common-mode range, forcing the output of the amplifier into the supply rails. The output then "folds back", i.e., a more positive input voltage now causes the output of the amplifier to go negative. The INA103 has protection circuitry to prevent fold-back, and as shown in (b), limits cleanly.

FIGURE 9. INA103 Overload Condition Performance.

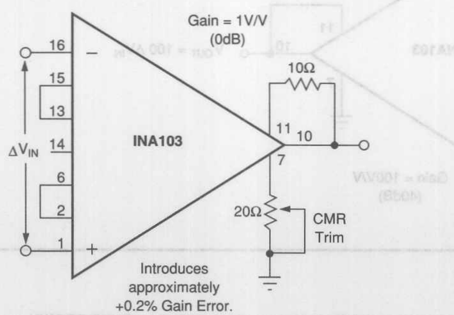


FIGURE 10. Optional Circuit for Externally Trimming CMR.

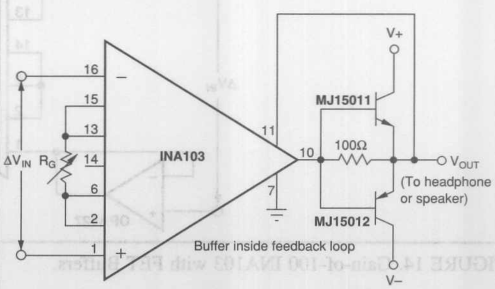


FIGURE 11. Increasing Output Circuit Drive.

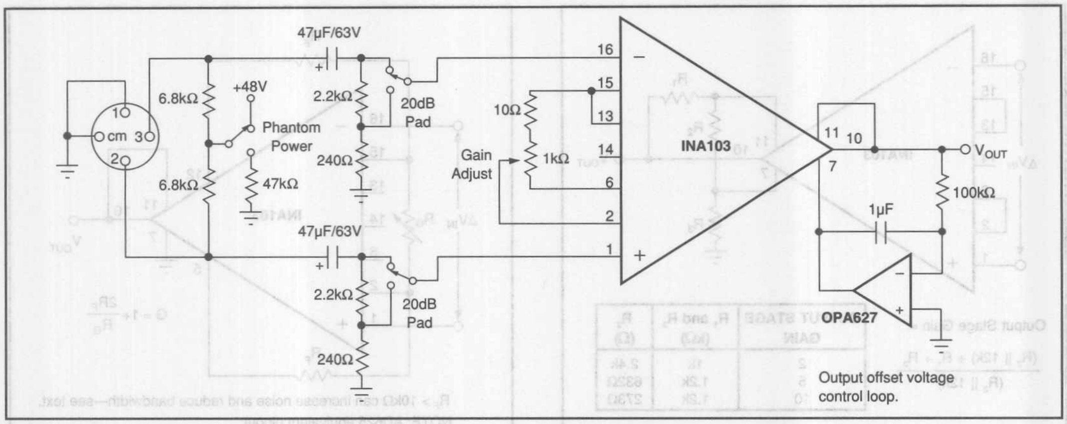


FIGURE 12. Microphone Preamplifier with Provision for Phantom Power Microphones.

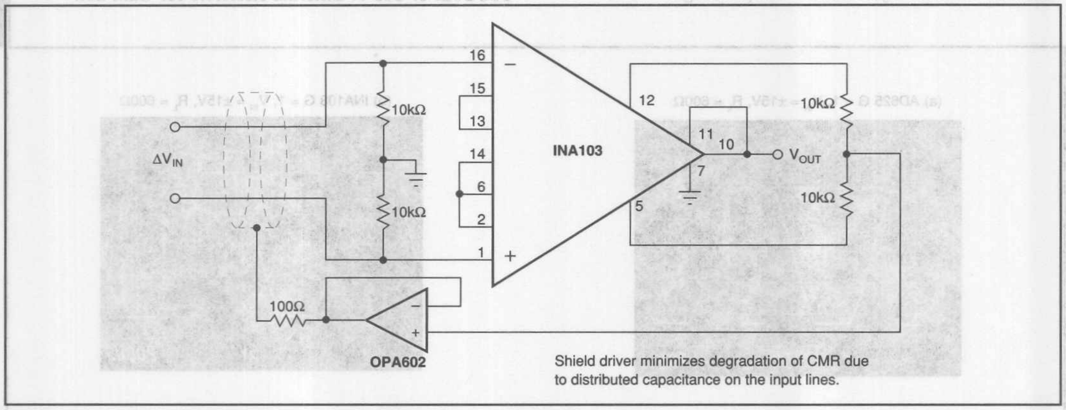


FIGURE 13. Instrumentation Amplifier with Shield Driver.

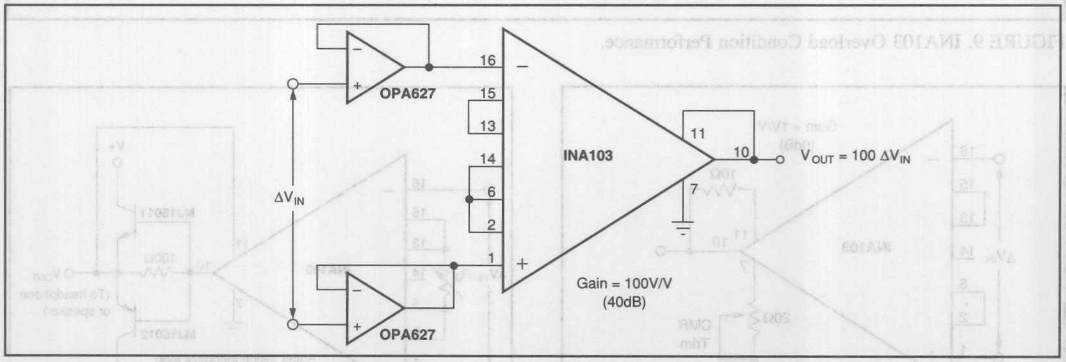
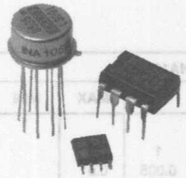


FIGURE 14. Gain-of-100 INA103 with FET Buffers.

BURR - BROWN®



INA105

Precision Unity Gain DIFFERENTIAL AMPLIFIER

FEATURES

- CMR 86dB min OVER TEMPERATURE
- GAIN ERROR: 0.01% max
- NONLINEARITY: 0.001% max
- NO EXTERNAL ADJUSTMENTS REQUIRED
- EASY TO USE
- COMPLETE SOLUTION
- HIGHLY VERSATILE
- LOW COST
- PLASTIC DIP, TO-99 HERMETIC METAL, AND SO-8 SOIC PACKAGES

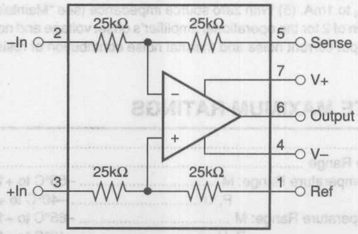
APPLICATIONS

- DIFFERENTIAL AMPLIFIER
- INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- GAIN-OF-1/2 AMPLIFIER
- NONINVERTING GAIN-OF-2 AMPLIFIER
- AVERAGE VALUE AMPLIFIER
- ABSOLUTE VALUE AMPLIFIER
- SUMMING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT RECEIVER WITH COMPLIANCE TO RAILS
- 4mA TO 20mA TRANSMITTER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ALL-PASS FILTERS

DESCRIPTION

The INA105 is a monolithic Gain = 1 differential amplifier consisting of a precision op amp and on-chip metal film resistors. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature.

The differential amplifier is the foundation of many commonly used circuits. The INA105 provides this precision circuit function without using an expensive precision resistor network. The INA105 is available in 8-pin plastic DIP, SO-8 surface-mount and TO-99 metal packages.



ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	INA105AM MIN	INA105AM TYP	INA105AM MAX	INA105BM MIN	INA105BM TYP	INA105BM MAX	INA105KP, KU MIN	INA105KP, KU TYP	INA105KP, KU MAX	UNITS
GAIN											
Initial(1)			1			*			*		V/V
Error			0.005	0.01		*	*		0.01	0.025	%
vs Temperature			1	5		*	*		*	*	ppm/°C
Nonlinearity(2)			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, –5mA	10	12		*	*		*	*		V
Rated Current	V_O = 10V	+20, –5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To Common		+40/–10			*			*		mA
Capacitive Load	Stable Operation		1000			*			*		pF
INPUT											
Impedance(3)	Differential		50			*			*		kΩ
	Common-Mode		50			*			*		kΩ
Voltage Range(4)	Differential	±10			*			*			V
	Common-Mode	±20			*			*			V
Common-Mode Rejection(5)	$T_A = T_{MIN}$ to T_{MAX}	80	90		86	100		72	*		dB
OFFSET VOLTAGE	RTO(6), (7)										
Initial			50	250		*	*		*	500	µV
vs Temperature			5	20		5	10		*	*	µV/°C
vs Supply	$\pm V_S$ = 6V to 18V		1	25		*	15		*	*	µV/V
vs Time			20			*			*		µV/mo
OUTPUT NOISE VOLTAGE	RTO(6), (8)										
f_B = 0.01Hz to 10Hz			2.4			*			*		µVp-p
f_O = 10kHz			60			*			*		nV/√Hz
DYNAMIC RESPONSE											
Small Signal Bandwidth	–3dB		1			*			*		MHz
Full Power Bandwidth	V_O = 20Vp-p	30	50		*	*		*	*		kHz
Slew Rate		2	3		*	*		*	*		V/µs
Settling Time: 0.1%	V_O = 10V Step		4			*			*		µs
0.01%	V_O = 10V Step		5			*			*		µs
0.01%	V_{CM} = 10V Step, V_{DIFF} = 0V		1.5			*			*		µs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated Performance	±5		±18	*		*	*		*	V
Quiescent Current	V_O = 0V		±1.5	±2		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		–40		+85	*		*	*		*	°C
Operation		–55		+125	*		*	–40		+85	°C
Storage		–65		+150	*		*	–40		+125	°C

* Specification same as for INA105AM.

NOTES: (1) Connected as difference amplifier (see Figure 4). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) 25kΩ resistors are ratio matched but have ±20% absolute value. (4) Maximum input voltage without protection is 10V more than either ±15V supply (±25V). Limit I_{IN} to 1mA. (5) With zero source impedance (see "Maintaining CMR" section). (6) Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifier's offset voltage and noise voltage. (7) Includes effects of amplifier's input bias and offset currents. (8) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

ABSOLUTE MAXIMUM RATINGS

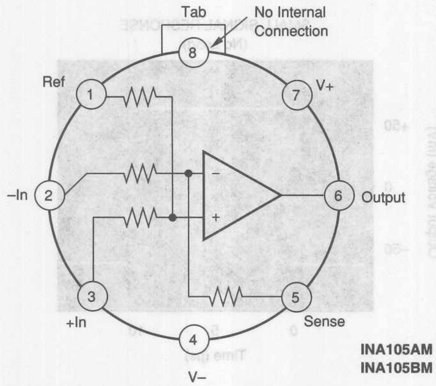
Supply	±18V
Input Voltage Range	$\pm V_S$
Operating Temperature Range: M	–55°C to +125°C
P, U	–40°C to +85°C
Storage Temperature Range: M	–65°C to +150°C
P, U	–40°C to +125°C
Lead Temperature (soldering, 10s) M, P	+300°C
Wave Soldering (3s, max) U	+260°C
Output Short Circuit to Common	Continuous

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA105AM	TO-99 Metal	001
INA105BM	TO-99 Metal	001
INA105KP	8-Pin Plastic DIP	006
INA105KU	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

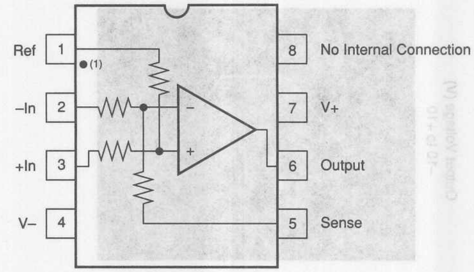
Top View **TO-99**



INA105AM
INA105BM

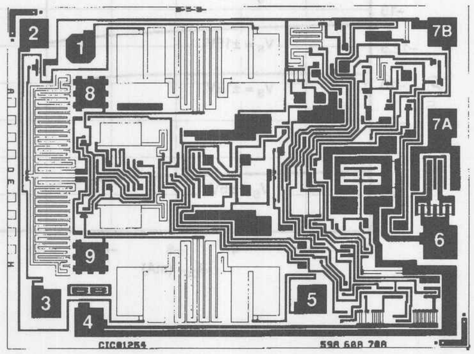
Case internally connected to V–. Make no connection.

Top View **DIP/SOIC**



NOTE: (1) Performance grade identifier box for small outline surface mount. Blank indicates K grade. Part is marked INA105U.

DICE INFORMATION



INA105 DIE TOPOGRAPHY

PAD	FUNCTION
1	Reference
2	–In
3	+In
4	V–
5	Sense
6	Output
7A	V+ (Connect Both)
7B	V+ (Connect Both)
8	(Op Amp +In)
9	(Op Amp –In)

Substrate Bias: Electrically connected to V– supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	83 x 63 ±5	2.11 x 1.60 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

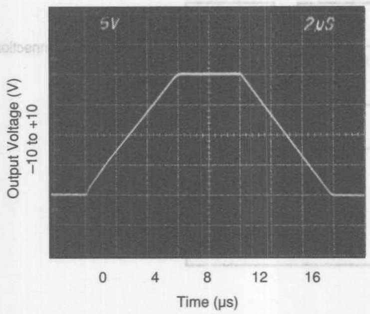
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE
INA105AM	TO-99 Metal	–40°C to +85°C
INA105BM	TO-99 Metal	–40°C to +85°C
INA105KP	8-Pin Plastic DIP	–40°C to +85°C
INA105KU	8-Pin SOIC	–40°C to +85°C

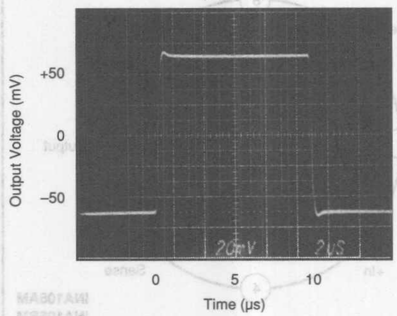
TYPICAL PERFORMANCE CURVES

$T_A = 25°C$, $V_S = \pm15V$ unless otherwise noted.

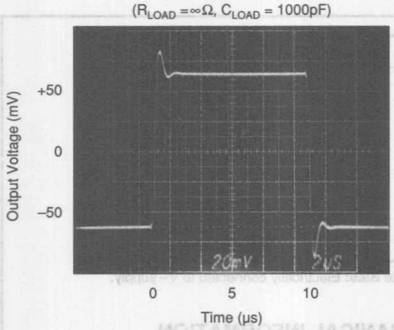
STEP RESPONSE



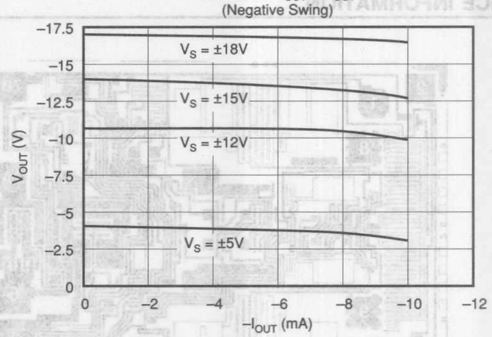
SMALL SIGNAL RESPONSE (No Load)



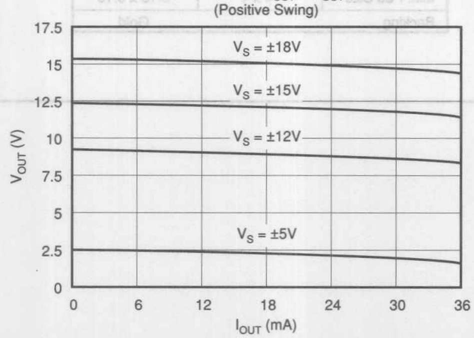
SMALL SIGNAL RESPONSE ($R_{LOAD} = \infty\Omega$, C_{LOAD} = 1000pF)



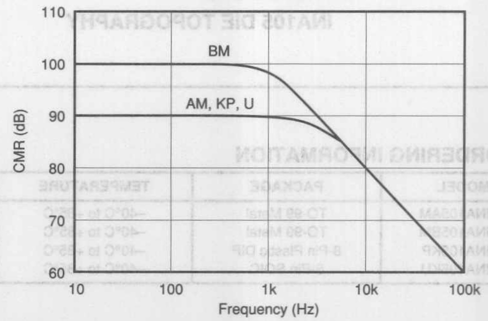
MAXIMUM V_{OUT} vs I_{OUT} (Negative Swing)



MAXIMUM V_{OUT} vs I_{OUT} (Positive Swing)

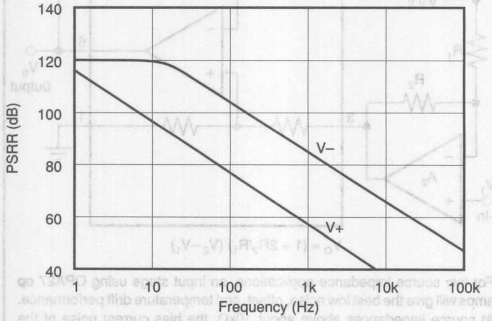


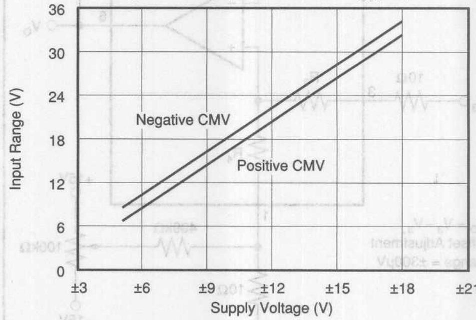
CMR vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = 25°C$, $V_S = \pm15V$ unless otherwise noted.





ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA105. Power supply bypass capacitors should be connected close to the device pins.

The differential input signal is connected to pins 2 and 3 as shown. The source impedances connected to the inputs must be nearly equal to assure good common-mode rejection. A 5Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 80dB. If the source has a known mismatch in source impedance, an additional resistor in series with one input can be used to preserve good common-mode rejection.

The output is referred to the output reference terminal (pin 1) which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 2. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins would not provide specified performance.

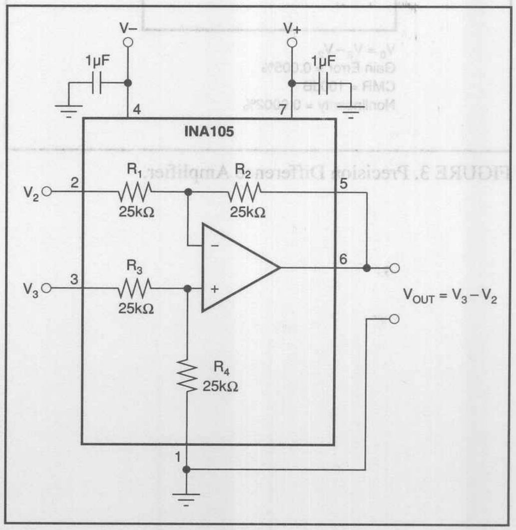


FIGURE 1. Basic Power Supply and Signal Connections.

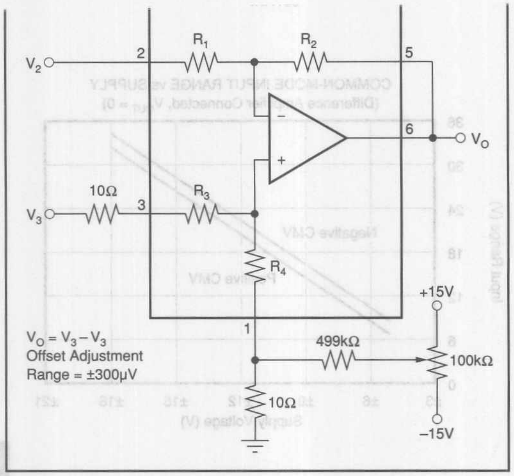


FIGURE 2. Offset Adjustment.

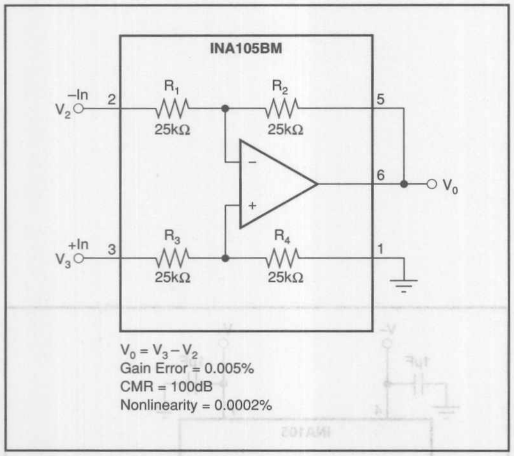
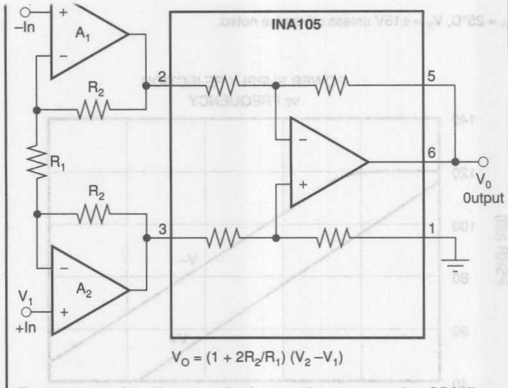


FIGURE 3. Precision Difference Amplifier.



For low source impedance applications, an input stage using OPA27 op amps will give the best low noise, offset, and temperature drift performance. At source impedances above about 10kΩ, the bias current noise of the OPA27 reacting with the input impedance begins to dominate the noise performance. For these applications, using the OPA111 or dual OPA2111 FET input op amp will provide lower noise performance. For lower cost use the OPA121 plastic. To construct an electrometer use the OPA128.

A_1, A_2	R_1 (Ω)	R_2 (Ω)	GAIN (V/V)	CMRR (dB)	MAX I_B	NOISE AT 1kHz (nV/√HZ)
OPA27A	50.5	2.5k	100	128	40nA	4
OPA111B	202	10k	100	110	1pA	10
OPA128LM	202	10k	100	118	75fA	38

FIGURE 4. Precision Instrumentation Amplifier.

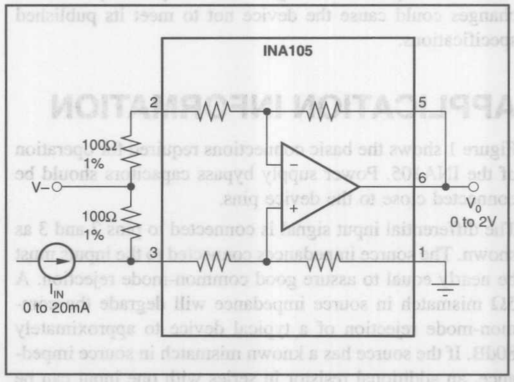


FIGURE 5. Current Receiver with Compliance to Rails.

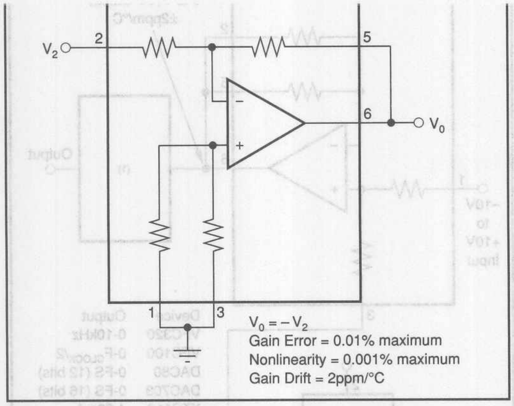


FIGURE 6. Precision Unity-Gain Inverting Amplifier.

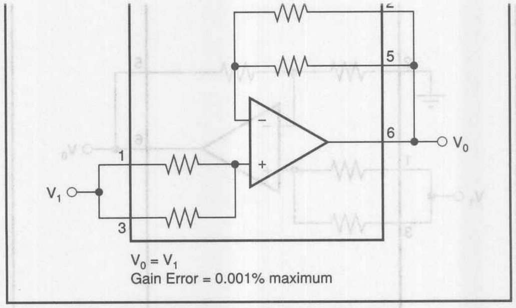


FIGURE 9. Precision Unity-Gain Buffer.

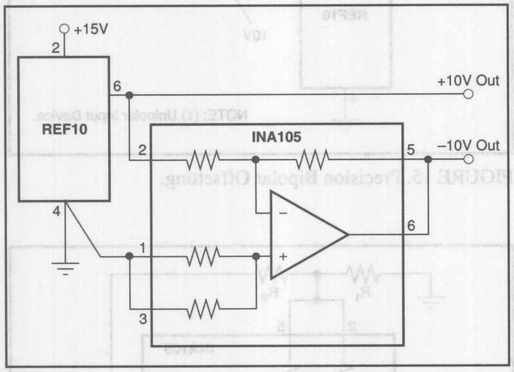


FIGURE 7. ±10V Precision Voltage Reference.

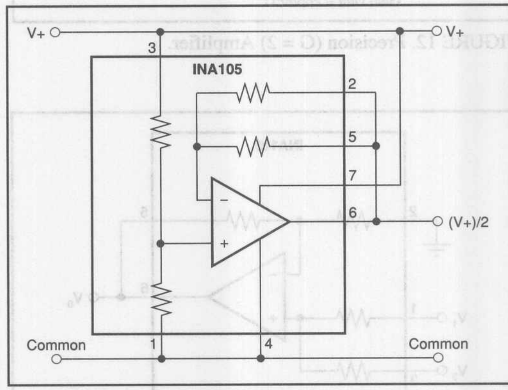


FIGURE 10. Pseudoground Generator.

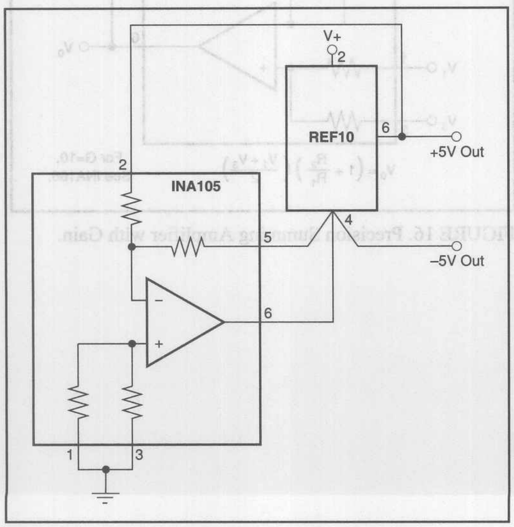


FIGURE 8. ±5V Precision Voltage Reference.

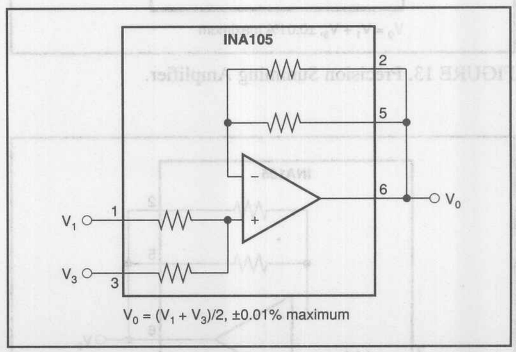


FIGURE 11. Precision Average Value Amplifier.

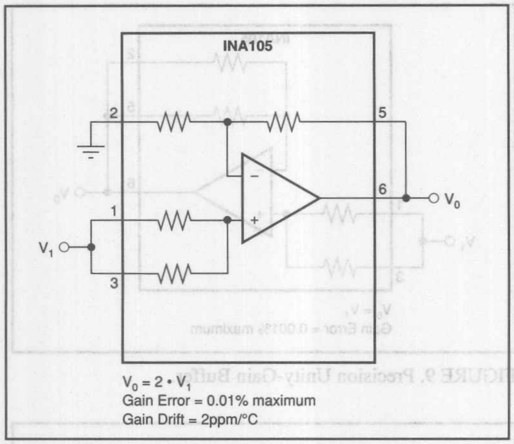


FIGURE 12. Precision (G = 2) Amplifier.

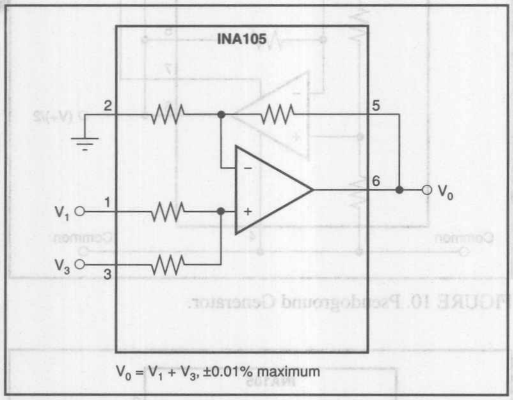


FIGURE 13. Precision Summing Amplifier.

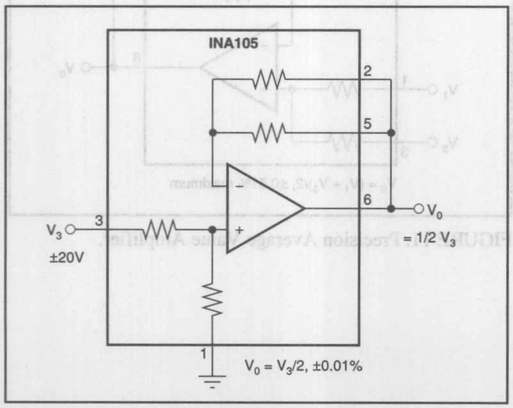


FIGURE 14. Precision Gain = 1/2 Amplifier.

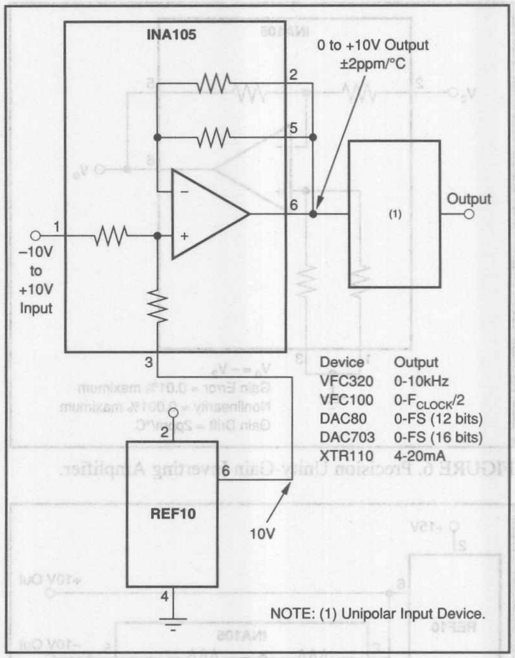


FIGURE 15. Precision Bipolar Offsetting.

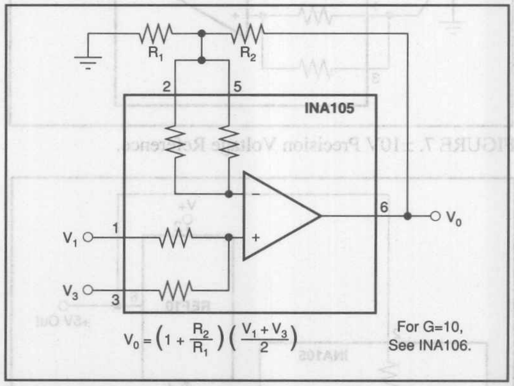


FIGURE 16. Precision Summing Amplifier with Gain.

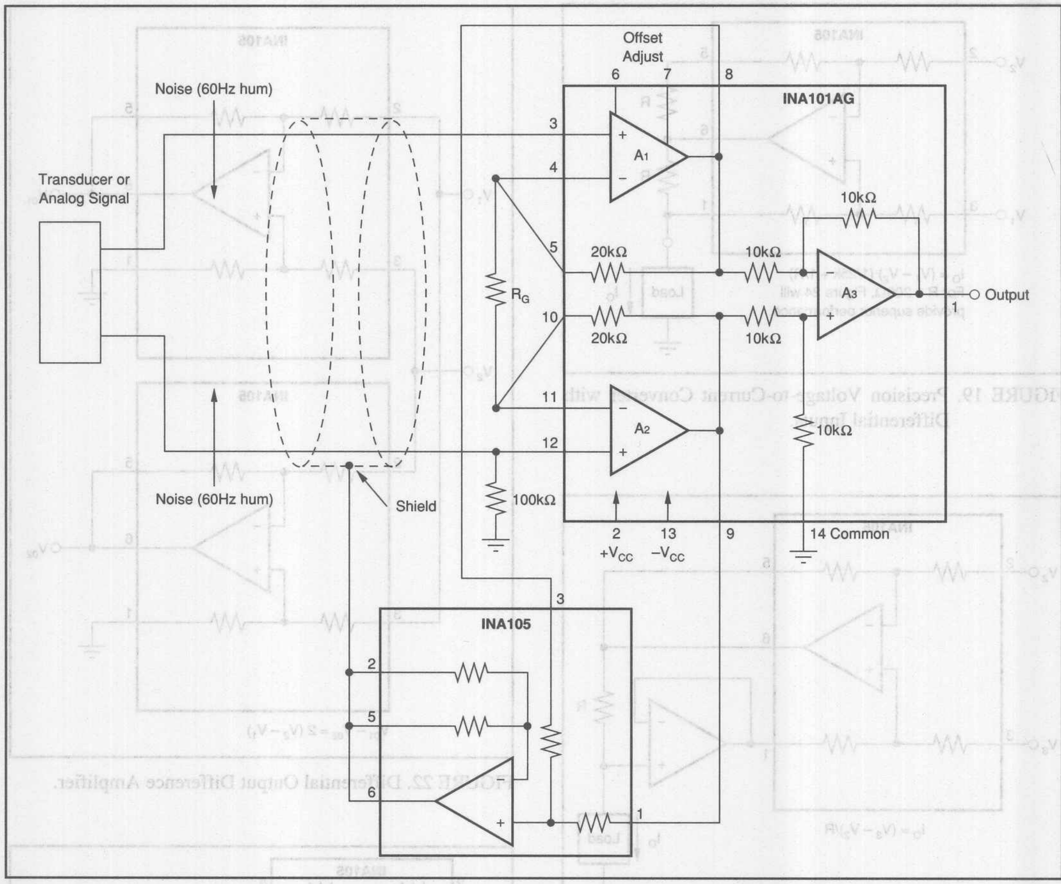


FIGURE 17. Instrumentation Amplifier Guard Drive Generator.

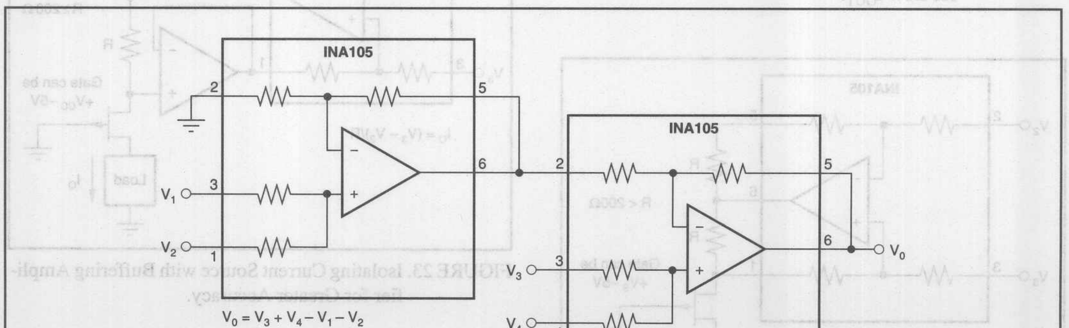


FIGURE 18. Precision Summing Instrumentation Amplifier.

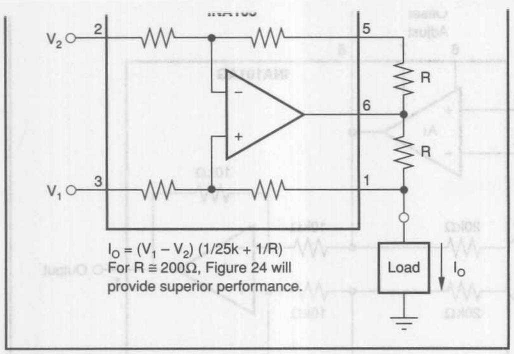


FIGURE 19. Precision Voltage-to-Current Converter with Differential Inputs.

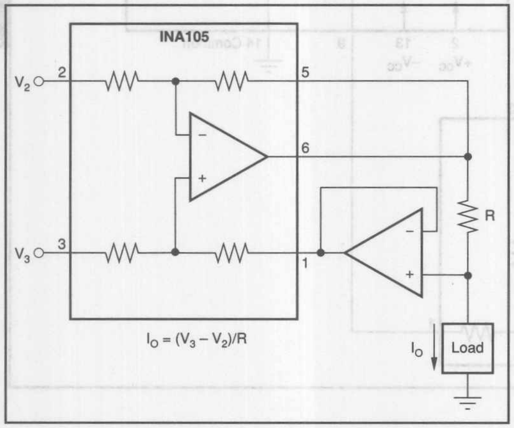


FIGURE 20. Differential Input Voltage-to-Current Converter for Low I_{OUT}.

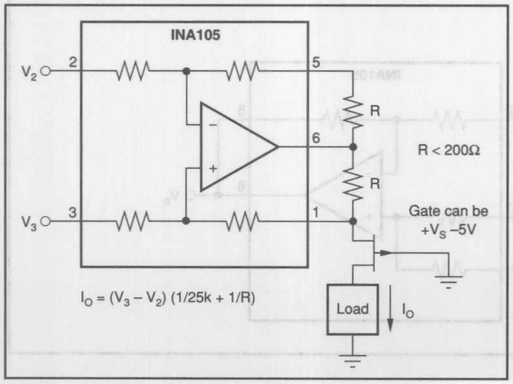


FIGURE 21. Isolating Current Source.

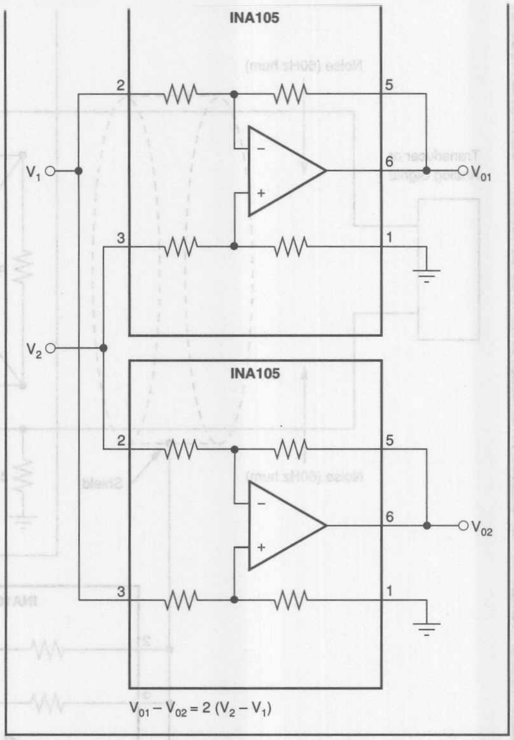


FIGURE 22. Differential Output Difference Amplifier.

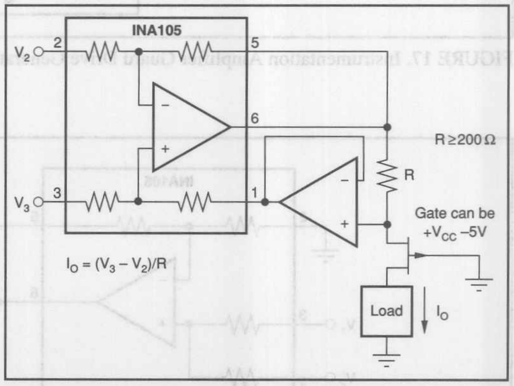


FIGURE 23. Isolating Current Source with Buffering Amplifier for Greater Accuracy.

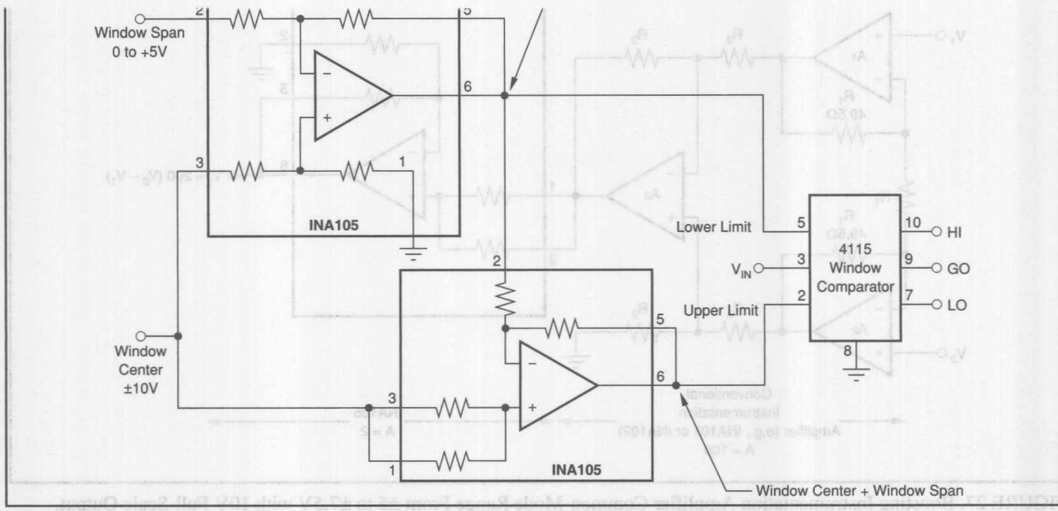


FIGURE 24. Window Comparator with Window Span and Window Center Inputs.

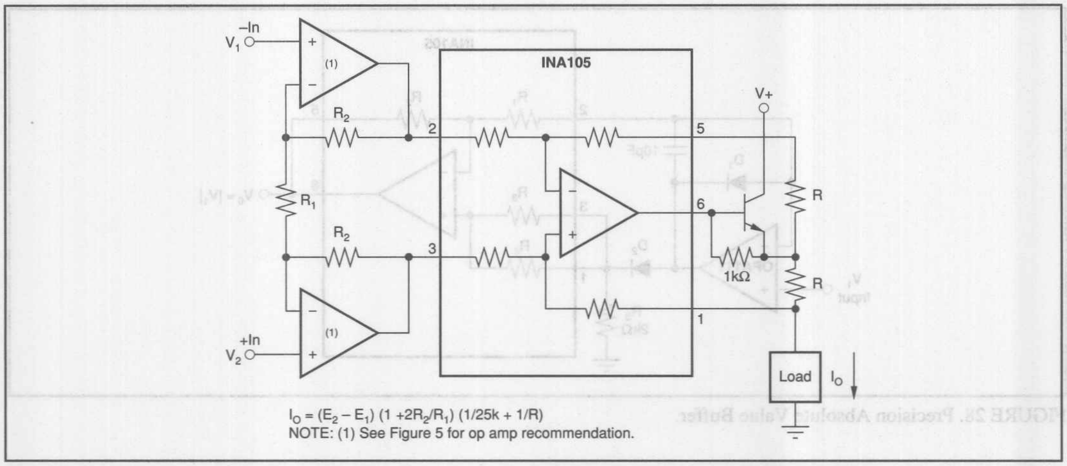
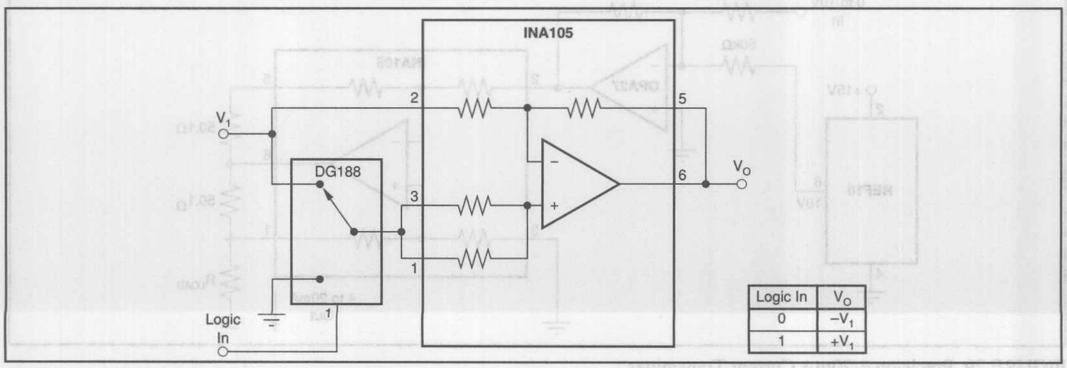


FIGURE 25. Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain.



Logic In	V_O
0	$-V_1$
1	$+V_1$

FIGURE 26. Digitally Controlled Gain of ±1 Amplifier.

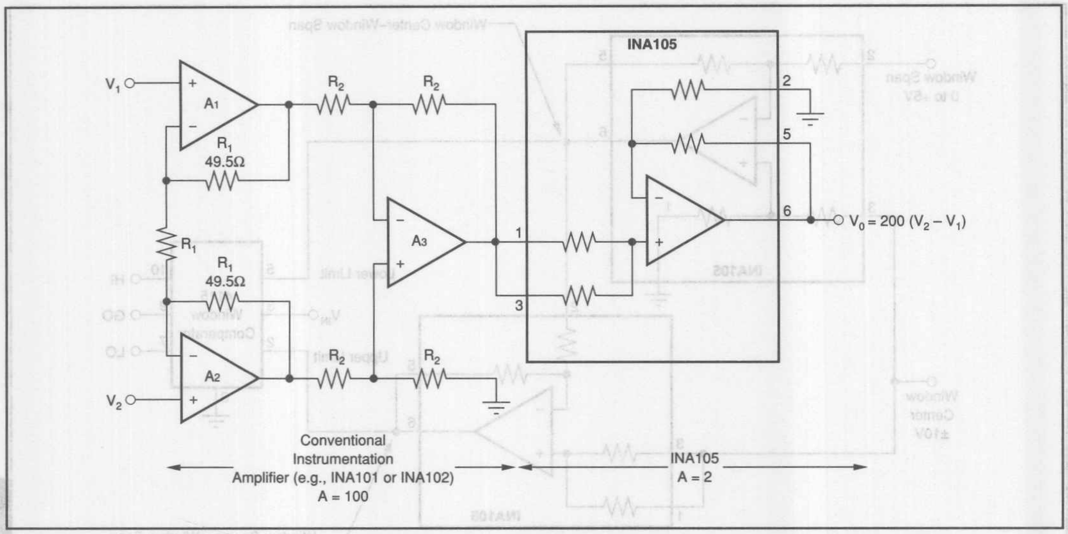


FIGURE 27. Boosting Instrumentation Amplifier Common-Mode Range From ±5 to ±7.5V with 10V Full-Scale Output.

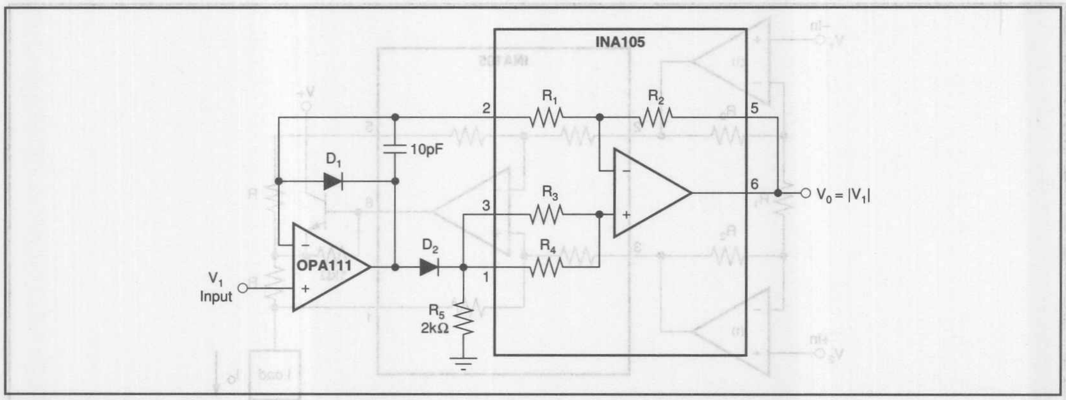


FIGURE 28. Precision Absolute Value Buffer.

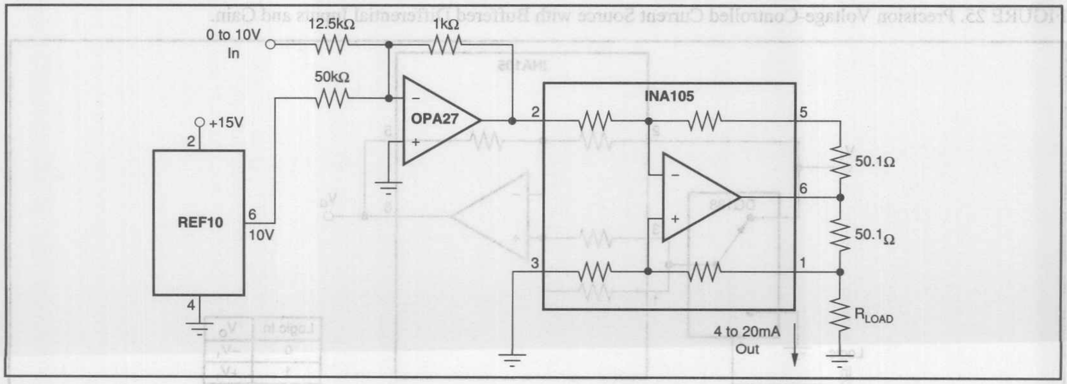
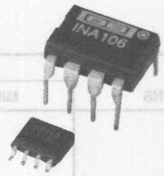


FIGURE 29. Precision 4-20mA Current Transmitter.

BURR - BROWN®



INA106

Precision Gain = 10 DIFFERENTIAL AMPLIFIER

FEATURES

- ACCURATE GAIN: ±0.025% max
- HIGH COMMON-MODE REJECTION: 86dB min
- NONLINEARITY: 0.001% max
- EASY TO USE
- PLASTIC 8-PIN DIP, SO-8 SOIC PACKAGES

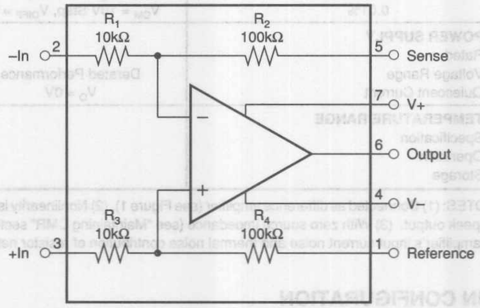
APPLICATIONS

- G = 10 DIFFERENTIAL AMPLIFIER
- G = +10 AMPLIFIER
- G = –10 AMPLIFIER
- G = +11 AMPLIFIER
- INSTRUMENTATION AMPLIFIER

DESCRIPTION

The INA106 is a monolithic Gain = 10 differential amplifier consisting of a precision op amp and on-chip metal film resistors. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature.

The differential amplifier is the foundation of many commonly used circuits. The INA106 provides this precision circuit function without using an expensive resistor network. The INA106 is available in 8-pin plastic DIP and SO-8 surface-mount packages.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

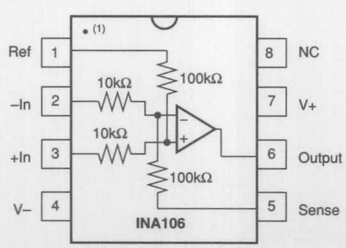
At +25°C, V_S = ±15V, unless otherwise specified.

PARAMETER	CONDITIONS	INA106KP, U			UNITS
		MIN	TYP	MAX	
GAIN					
Initial(1)			10		V/V
Error			0.01	0.025	%
vs Temperature			–4		ppm/°C
Nonlinearity(2)			0.0002	0.001	%
OUTPUT					
Related Voltage	I_O = +20mA, –5mA	10	12		V
Rated Current	V_O = 10V	+20, –5			mA
Impedance			0.01		Ω
Current Limit	To Common		+40/–10		mA
Capacitive Load	Stable Operation		1000		pF
INPUT					
Impedance	Differential		10		kΩ
	Common-Mode		110		kΩ
Voltage Range	Differential	±1			V
	Common-Mode	±11			V
Common-Mode Rejection(3)	T_A = T_{MIN} to T_{MAX}	86	100		dB
OFFSET VOLTAGE	RTI(4)				
Initial			50	200	µV
vs Temperature			0.2		µV/°C
vs Supply	±V_S = 6V to 18V		1	10	µV/V
vs Time			10		µV/mo
NOISE VOLTAGE	RTI(5)				
f_B = 0.01Hz to 10Hz			1		µVp-p
f_O = 10kHz			30		nV/√Hz
DYNAMIC RESPONSE					
Small Signal	–3dB		5		MHz
Full Power BW	V_O = 20Vp-p	30	50		kHz
Slew Rate		2	3		V/µs
Settling Time: 0.1%	V_O = 10V Step		5		µs
0.01%	V_O = 10V Step		10		µs
0.01%	V_{CM} = 10V Step, V_{DIFF} = 0V		5		µs
POWER SUPPLY					
Rated			5		V
Voltage Range	Derated Performance	±5		±18	V
Quiescent Current	V_O = 0V		±1.5	±2	mA
TEMPERATURE RANGE					
Specification		0		+70	°C
Operation		–40		+85	°C
Storage		–65		+150	°C

NOTES: (1) Connected as difference amplifier (see Figure 1). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see "Maintaining CMR" section). (4) Includes effects of amplifiers's input bias and offset currents. (5) Includes effect of amplifier's input current noise and thermal noise contribution of resistor network.

PIN CONFIGURATION

Top View | DIP/SOIC



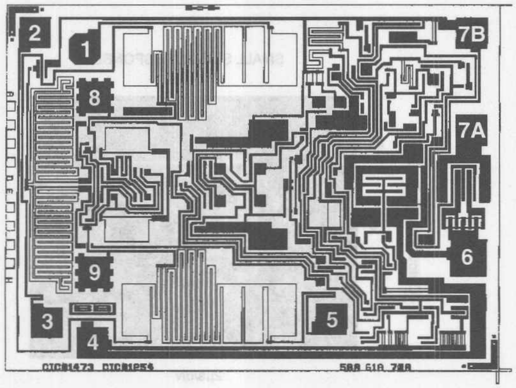
NOTE: (1) Pin 1 indentifier for SO-8 package. Model number identification may be abbreviated on SO-8 package due to limited available space.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

DICE INFORMATION



INA106 DIE TOPOGRAPHY

PAD	FUNCTION
1	Reference
2	–In
3	+In
4	V–
5	Sense
6	Output
7A, 7B	V+ (Connect Both)
8	(Op Amp +In)
9	(Op Amp –In)

Substrate Bias: Electrically connected to V– supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	83 x 63 ±5	2.11 x 1.60 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing:		Gold

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage Range	$\pm V_S$
Operating Temperature Range: P, U	–40°C to +85°C
Storage Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s): P	+300°C
Wave Soldering (3s, max) U	+260°C
Output Short Circuit to Common	Continuous

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA106KP	8-Pin Plastic DIP	0°C to +70°C
INA106U	SO-8 Surface Mount	0°C to +70°C

PACKAGING INFORMATION

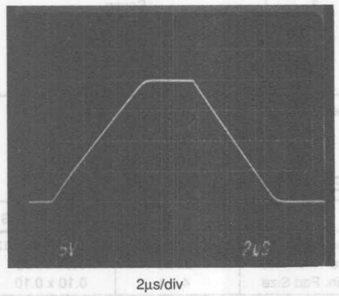
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA106KP	8-Pin Plastic DIP	006
INA106U	SO-8 Surface Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

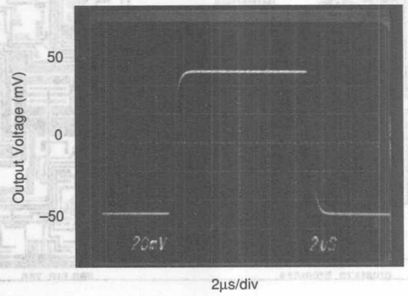
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.

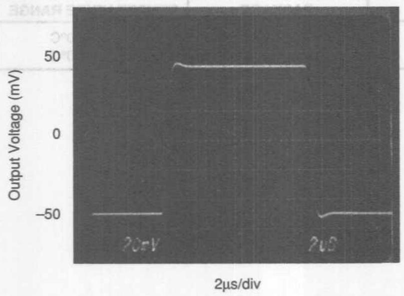
STEP RESPONSE



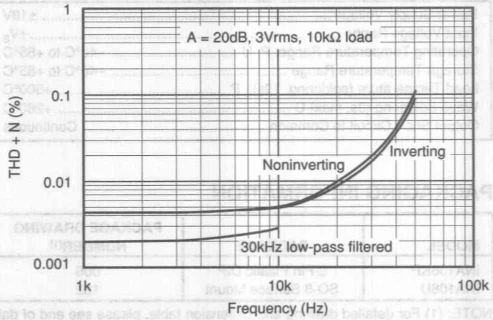
SMALL SIGNAL RESPONSE
(No Load)



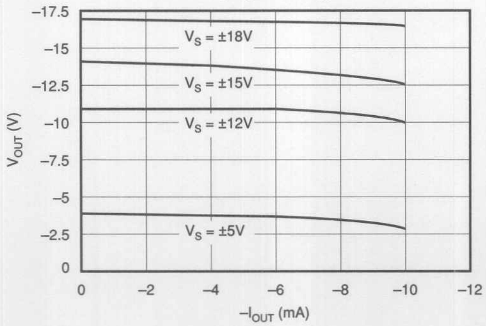
SMALL SIGNAL RESPONSE
($R_{LOAD} = \infty$, C_{LOAD} = 100pF)



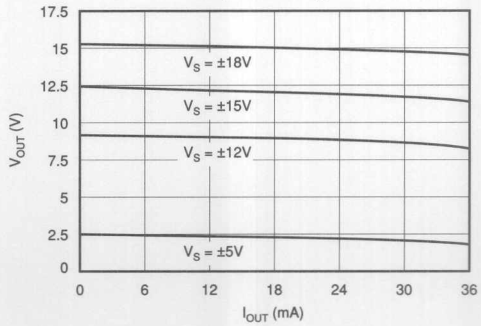
TOTAL HARMONIC DISTORTION AND NOISE
vs FREQUENCY



MAXIMUM V_{OUT} vs I_{OUT}
(Negative Swing)

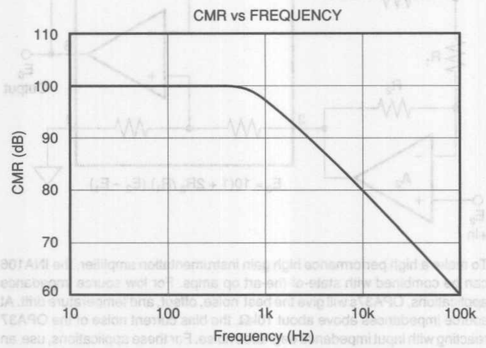


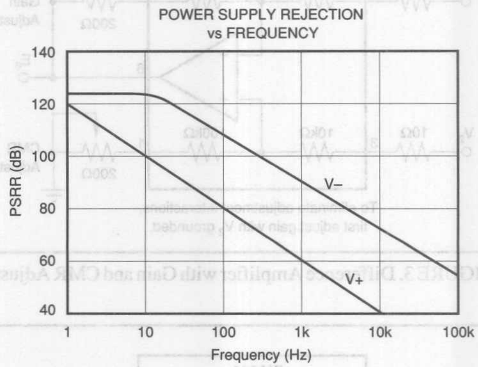
MAXIMUM V_{OUT} vs I_{OUT}
(Positive Swing)



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.





APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA106. Power supply bypass capacitors should be connected close to the device pins as shown.

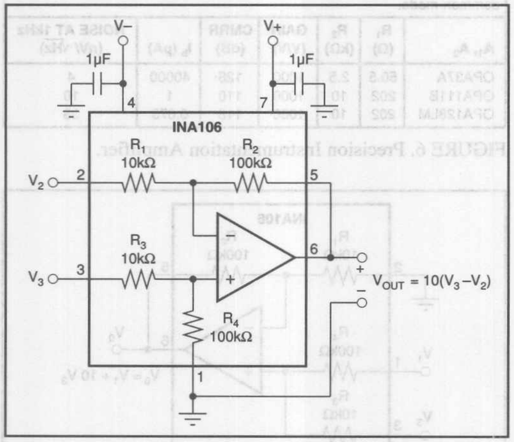


FIGURE 1. Basic Power Supply and Signal Connections.

The differential input signal is connected to pins 2 and 3 as shown. The source impedance connected to the inputs must be equal to assure good common-mode rejection. A 5Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 86dB. If the source has a known source impedance mismatch, an additional resistor in series with one input can be used to preserve good common-mode rejection.

The output is referred to the output reference terminal (pin 1) which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

Figure 2 shows a voltage applied to pin 1 to trim the offset voltage of the INA106. The known 100Ω source impedance of the trim circuit is compensated by the 10Ω resistor in series with pin 3 to maintain good CMR.

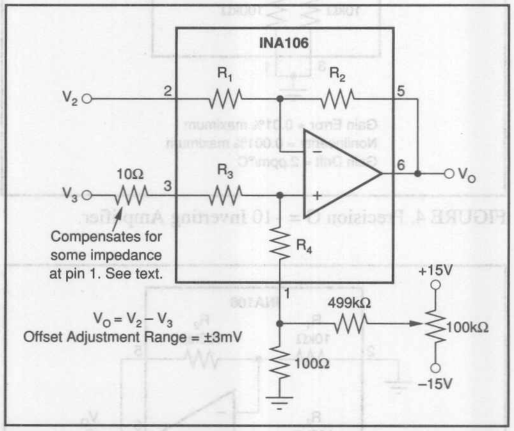


FIGURE 2. Offset Adjustment.

Referring to Figure 1, the CMR depends upon the match of the internal R_4/R_3 ratio to the R_1/R_2 ratio. A CMR of 106dB requires resistor matching of 0.005%. To maintain high CMR over temperature, the resistor TCR tracking must be better than 2ppm/°C. These accuracies are difficult and expensive to reliably achieve with discrete components.

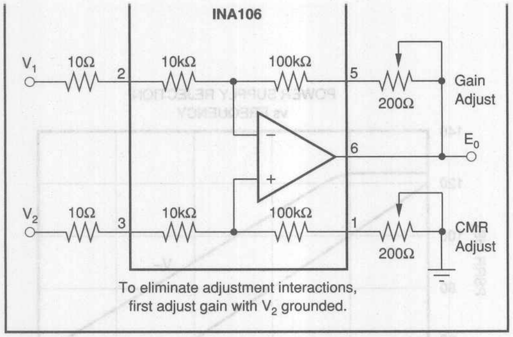


FIGURE 3. Difference Amplifier with Gain and CMR Adjust.

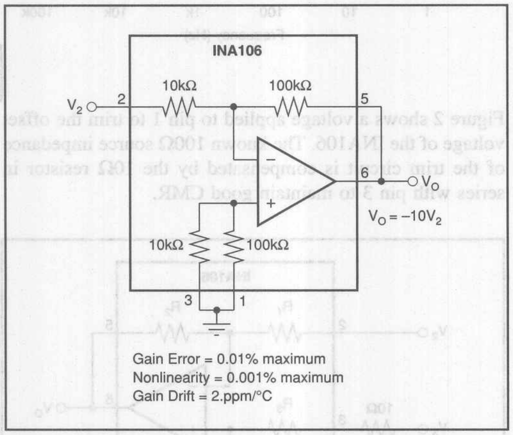


FIGURE 4. Precision G = –10 Inverting Amplifier.

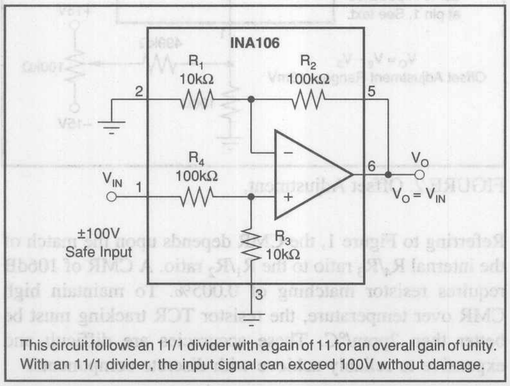
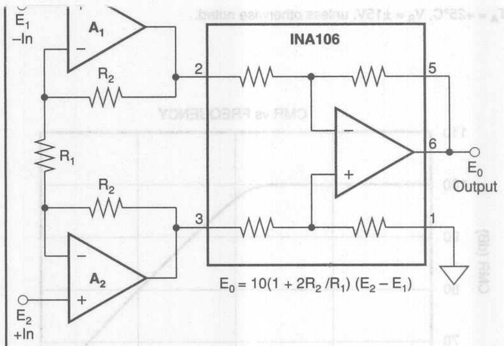


FIGURE 5. Voltage Follower with Input Protection.



To make a high performance high gain instrumentation amplifier, the INA106 can be combined with state-of-the-art op amps. For low source impedance applications, OPA37s will give the best noise, offset, and temperature drift. At source impedances above about 10kΩ, the bias current noise of the OPA37 reacting with input impedance degrades noise. For these applications, use an OPA111 or a dual OPA2111 FET input op amp for lower noise. For an electrometer grade IA, use the OPA128—see table below.

Using the INA106 for the difference amplifier also extends the input common-mode range of the instrumentation amplifier to ±10V. A conventional IA with a unity-gain difference amplifier has an input common-mode range limited to ±5V for an output swing of ±10V. This is because a unity-gain difference amp needs ±5V at the input for 10V at the output, allowing only 5V additional for common-mode.

A_1, A_2	R_1 (Ω)	R_2 (kΩ)	GAIN (V/V)	CMRR (dB)	I_b (pA)	NOISE AT 1kHz (nV/$\sqrt{Hz}$)
OPA37A	50.5	2.5	1000	128	40000	4
OPA111B	202	10	1000	110	1	10
OPA128LM	202	10	1000	118	0.075	38

FIGURE 6. Precision Instrumentation Amplifier.

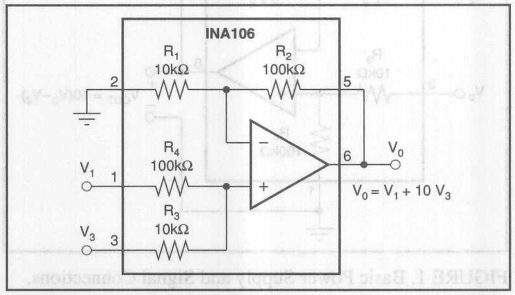


FIGURE 7. Precision Summing Amplifier.

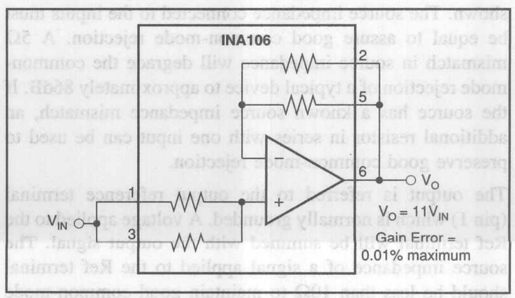
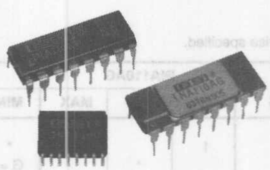


FIGURE 8. Precision G = 11 Buffer.

BURR - BROWN®



INA110

Fast-Settling FET-Input INSTRUMENTATION AMPLIFIER

FEATURES

- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 4μs to 0.01%
- HIGH CMR: 106dB min; 90dB at 10kHz
- INTERNAL GAINS: 1, 10, 100, 200, 500
- VERY LOW GAIN DRIFT: 10 to 50ppm/°C
- LOW OFFSET DRIFT: 2μV/°C
- LOW COST
- PINOUT SIMILAR TO AD524 AND AD624

APPLICATIONS

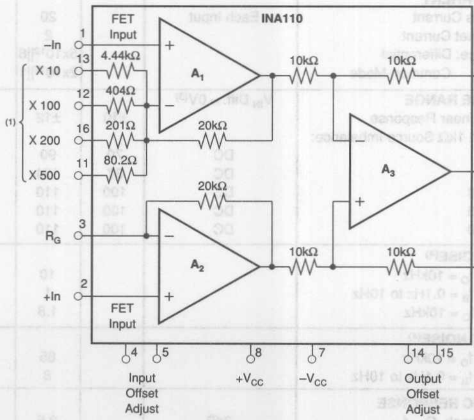
- MULTIPLEXED INPUT DATA ACQUISITION SYSTEM
- FAST DIFFERENTIAL PULSE AMPLIFIER
- HIGH SPEED GAIN BLOCK
- AMPLIFICATION OF HIGH IMPEDANCE SOURCES

DESCRIPTION

The INA110 is a versatile monolithic FET-input instrumentation amplifier. Its current-feedback circuit topology and laser trimmed input stage provide excellent dynamic performance and accuracy. The INA110 settles in 4μs to 0.01%, making it ideal for high speed or multiplexed-input data acquisition systems.

Internal gain-set resistors are provided for gains of 1, 10, 100, 200, and 500V/V. Inputs are protected for differential and common-mode voltages up to $\pm V_{CC}$. Its very high input impedance and low input bias current make the INA110 ideal for applications requiring input filters or input protection circuitry.

The INA110 is available in 16-pin plastic and ceramic DIPs, and in the SOL-16 surface-mount package. Military, industrial and commercial temperature range grades are available.



NOTE: (1) Connect to R_G for desired gain.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC, and R_L = 2kΩ, unless otherwise specified.

PARAMETER	CONDITIONS	INA110AG MIN	INA110AG TYP	INA110AG MAX	INA110BG, SG MIN	INA110BG, SG TYP	INA110BG, SG MAX	INA110KP, KU MIN	INA110KP, KU TYP	INA110KP, KU MAX	UNITS
GAIN											
Range of Gain		1		800	*		*	*		*	V/V
Gain Equation(1)			*		G = 1 + [40k/(R_G + 50Ω)]				*		V/V
Gain Error, DC: G = 1			0.002	0.04		*	0.02		*	*	%
G = 10			0.01	0.1		0.005	0.05		*	*	%
G = 100			0.02	0.2		0.01	0.1		*	*	%
G = 200			0.04	0.4		0.02	0.2		*	*	%
G = 500			0.1	1		0.05	0.5		*	*	%
Gain Temp. Coefficient: G = 1			±3	±20		*	±10		*		ppm/°C
G = 10			±4	±20		±2	±10		*		ppm/°C
G = 100			±6	±40		±3	±20		*		ppm/°C
G = 200			±10	±60		±5	±30		*		ppm/°C
G = 500			±25	±100		±10	±50		*		ppm/°C
Nonlinearity, DC: G = 1			±0.001	±0.01		±0.0005	±0.005		*	*	% of FS
G = 10			±0.002	±0.01		±0.001	±0.005		*	*	% of FS
G = 100			±0.004	±0.02		±0.002	±0.01		*	*	% of FS
G = 200			±0.006	±0.02		±0.003	±0.01		*	*	% of FS
G = 500			±0.01	±0.04		±0.005	±0.02		*	*	% of FS
OUTPUT											
Voltage, R_L = 2kΩ	Over Temperature	±10	±12.7		*	*		*	*		V
Current	Over Temperature	±5	±25		*	*		*	*		mA
Short-Circuit Current			±25			*			*		mA
Capacitive Load	Stability		5000			*			*		pF
INPUT OFFSET VOLTAGE(2)											
Initial Offset: G, P			±(100 + 1000/G)	±(500 + 5000/G)		±(50 + 600/G)	±(250 + 3000/G)		*	*	μV
U									±(200 + 2000/G)	±(1000 + 5000/G)	μV
vs Temperature			±(2 + 20/G)	±(5 + 100/G)		±(1 + 10/G)	±(2 + 50/G)		*		μV/°C
vs Supply	V_{CC} = ±6V to ±18V		±(4 + 60/G)	±(30 + 300/G)		±(2 + 30/G)	±(10 + 180/G)		*	*	μV/V
BIAS CURRENT											
Initial Bias Current	Each Input		20	100		10	50		*	*	pA
Initial Offset Current			2	50		1	25		*	*	pA
Impedance: Differential			$5 \times 10^{12} \| 6$			*			*		Ω || pF
Common-Mode			$2 \times 10^{12} \| 1$			*			*		Ω || pF
VOLTAGE RANGE	V_{IN} Diff. = 0V(3)										
Range, Linear Response		±10	±12					*	*		V
CMR with 1kΩ Source Imbalance:											
G = 1	DC	70	90		80	100		*	*		dB
G = 10	DC	87	104		96	112		*	*		dB
G = 100	DC	100	110		106	116		*	*		dB
G = 200	DC	100	110		106	116		*	*		dB
G = 500	DC	100	110		106	116		*	*		dB
INPUT NOISE(4)											
Voltage, f_O = 10kHz			10			*			*		nV/√Hz
f_B = 0.1Hz to 10Hz			1			*			*		μVp-p
Current, f_O = 10kHz			1.8			*			*		fA/√Hz
OUTPUT NOISE(4)											
Voltage, f_O = 10kHz			65			*			*		nV/√Hz
f_B = 0.1Hz to 10Hz			8			*			*		μVp-p
DYNAMIC RESPONSE											
Small Signal: G = 1	–3dB		2.5			*			*		MHz
G = 10			2.5			*			*		MHz
G = 100			470			*			*		kHz
G = 200			240			*			*		kHz
G = 500			100			*			*		kHz
Full Power	V_{OUT} = ±10V, G = 2 to 100	190	270		*	*			*	*	kHz
Slew Rate	G = 2 to 100	12	17		*	*			*	*	V/μs
Settling Time:											
0.1%, G = 1	V_O = 20V Step		4			*			*		μs
G = 10			2			*			*		μs
G = 100			3			*			*		μs
G = 200			5			*			*		μs
G = 500			11			*			*		μs

SPECIFICATIONS (CONT)

ELECTRICAL

At +25°C, $\pm V_{CC}$ 15VDC, and $R_L = 2K\Omega$, unless otherwise specified.

PARAMETER	CONDITIONS	INA110AG			INA110BG, SG			INA110KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE (CONT)											
Settling Time:											
0.01%,G = 1	V_O = 20V Step		5	12.5		*	*		*		µs
G = 10			3	7.5		*	*		*		µs
G = 100			4	7.5		*	*		*		µs
G = 200			7	12.5		*	*		*		µs
G = 500			16	25		*	*		*		µs
Recovery(5)	50% Overdrive		1			*			*		µs
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±6		±18	*		*	*		*	V
Quiescent Current	V_O = 0V		±3	±4.5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: A, B, K		–25		+85	*		*	0		+70	°C
S					–55		+125				°C
Operation		–55		+125	*		*	–25		+85	°C
Storage		–65		+150	*		*	–40		+85	°C
θ_{JA}			100			*			*		°C/W

* Same as INA110AG.

NOTES: (1) Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 11, 12 and 16. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. (2) Adjustable to zero. (3) For differential input voltage other than zero, see Typical Performance Curves. (4) $V_{NOISE\ RTI} = \sqrt{V_{N\ INPUT}^2 + (V_{N\ OUTPUT}/Gain)^2}$. (5) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

PIN CONFIGURATION

Top View — DIP/SOIC

Function	Pin	Pin	Function
–In	1	16	x200
+In	2	15	Output Offset Adj.
R_G	3	14	Output Offset Adj.
Input Offset Adj.	4	13	x10
Input Offset Adj.	5	12	x100
Reference	6	11	x500
$-V_{CC}$	7	10	Output Sense
$+V_{CC}$	8	9	Output

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±18V
Input Voltage Range .... $\pm V_{CC}$
Operating Temperature Range: G .... –55°C to +125°C
P, U .... –25°C to +85°C
Storage Temperature Range: G .... –65°C to +150°C
P, U .... –40°C to +85°C
Lead Temperature (soldering, 10s): G, P .... +300°C
(soldering, 3s): U .... +260°C
Output Short Circuit Duration .... Continuous to Common

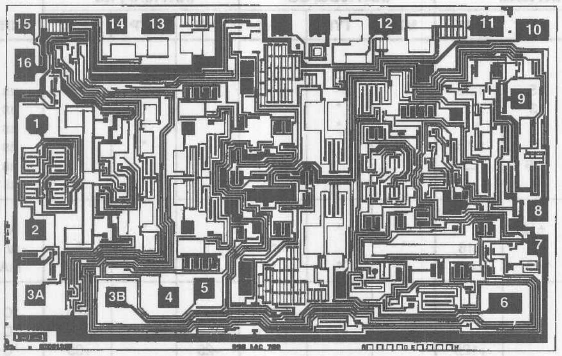
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA110AG	16-Pin Ceramic DIP	109
INA110BG	16-Pin Ceramic DIP	109
INA110SG	16-Pin Ceramic DIP	109
INA110KP	16-Pin Plastic DIP	180
INA110KU	SOL-16 SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA110AG	16-Pin Ceramic DIP	–25°C to +85°C
INA110BG	16-Pin Ceramic DIP	–25°C to +85°C
INA110SG	16-Pin Ceramic DIP	–55°C to +125°C
INA110KP	16-Pin Plastic DIP	0°C to +70°C
INA110KU	SOL-16 SOIC	0°C to +70°C



INA110 DIE TOPOGRAPHY

PAD	FUNCTION
1	–In
2	+In
3A,3B	R_G (connect both)
4	Input Offset Adjust
5	Input Offset Adjust
6	Reference
7	$-V_{CC}$
8	$+V_{CC}$
9	Output
10	Output Sense
11	x500
12	x100
13	x10
14	Output Offset Adjust
15	Output Offset Adjust
16	x200

Pads 3A and 3B must be connected.

Substrate Bias: Internally connected to $-V_{CC}$ power supply.

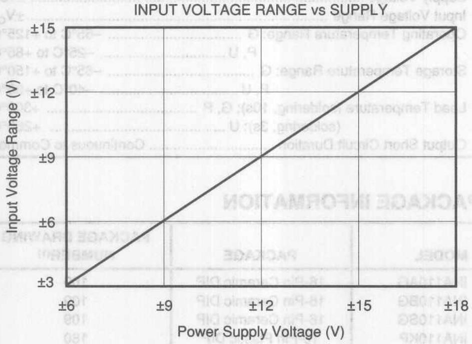
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	139 x 89 ±5	3.53 x 2.26 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

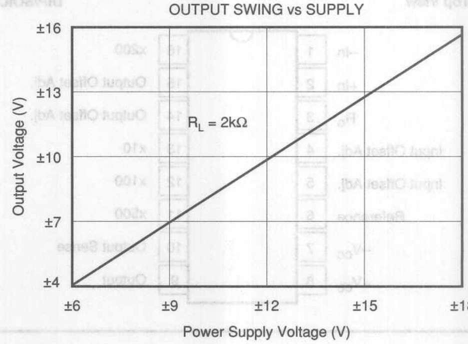
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, and $\pm V_{CC}$ = 15VDC, unless otherwise noted.

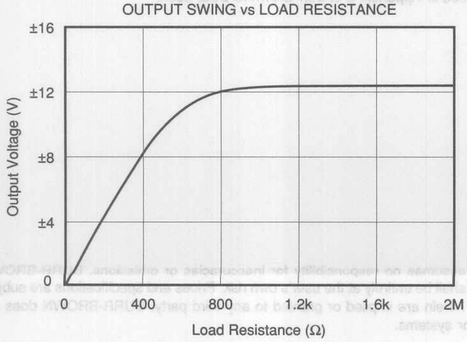
INPUT VOLTAGE RANGE vs SUPPLY



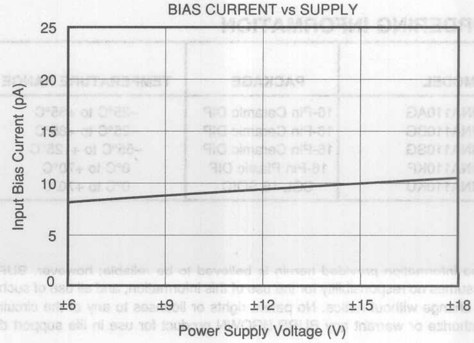
OUTPUT SWING vs SUPPLY



OUTPUT SWING vs LOAD RESISTANCE



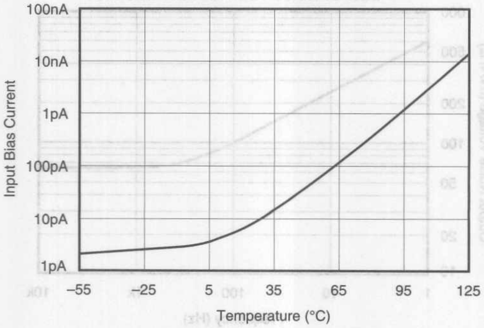
BIAS CURRENT vs SUPPLY



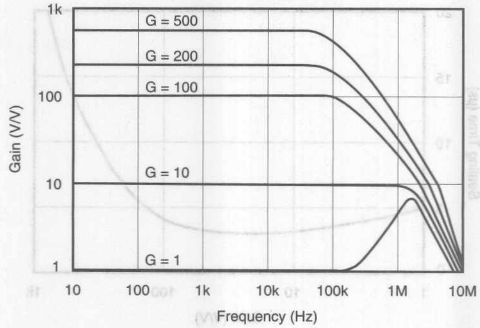
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $\pm V_{CC}$ = 15VDC, unless otherwise noted.

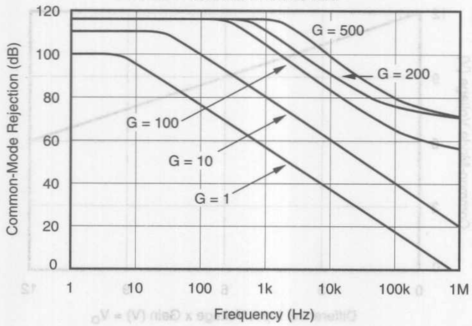
BIAS CURRENT vs TEMPERATURE



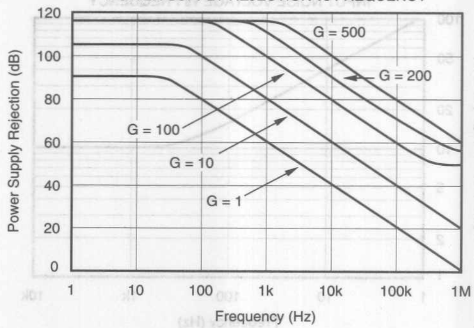
GAIN vs FREQUENCY



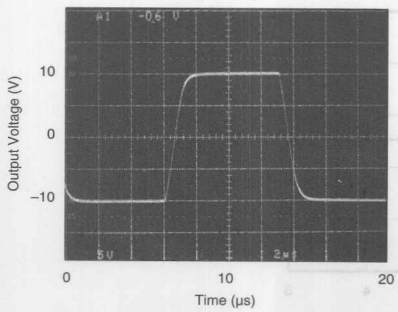
CMR vs FREQUENCY



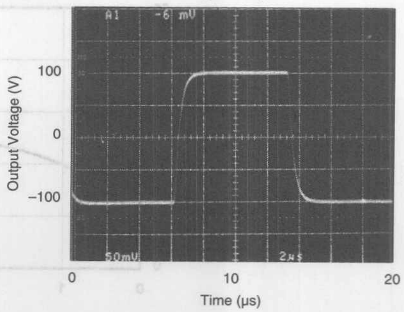
POWER SUPPLY REJECTION vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE
(G = 100)

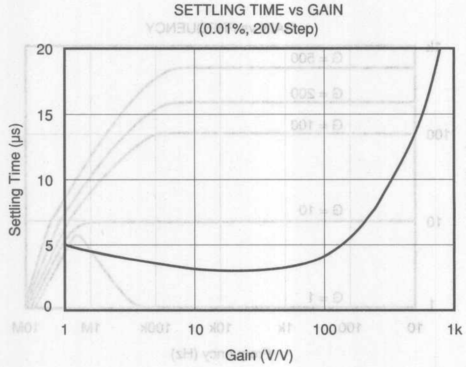


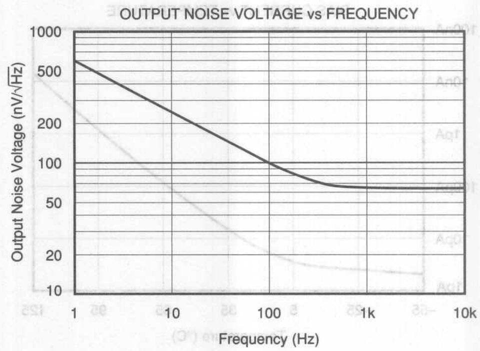
SMALL SIGNAL TRANSIENT RESPONSE
(G = 100)

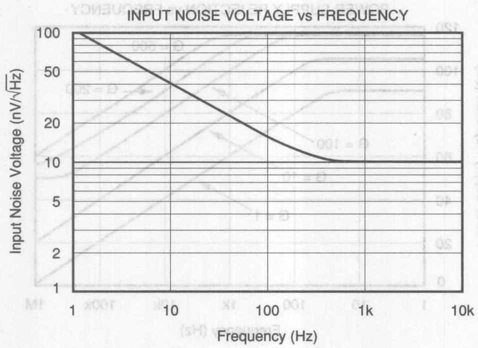


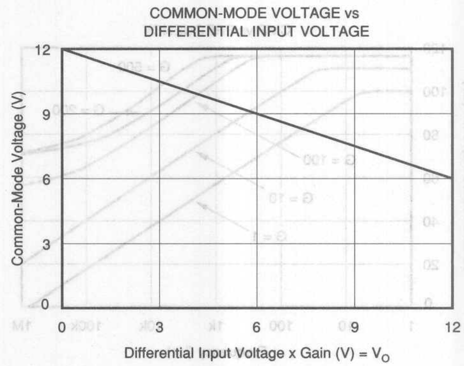
TYPICAL PERFORMANCE CURVES (CONT)

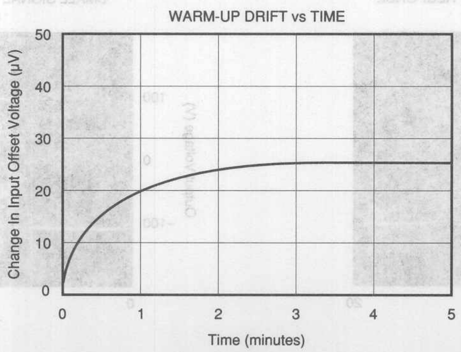
T_A = +25°C, $\pm V_{CC}$ = 15VDC, unless otherwise noted.











DISCUSSION OF PERFORMANCE

A simplified diagram of the INA110 is shown on the first page. The design consists of the classical three operational amplifier configuration using current-feedback type op amps with precision FET buffers on the input. The result is an instrumentation amplifier with premium performance not normally found in integrated circuits.

The input section (A_1 and A_2) incorporates high performance, low bias current, and low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide high input impedance ($10^{12}\Omega$). Laser-trimming is used to achieve low offset voltage. Input cascoding assures low bias current and high CMR. Thin-film resistors on the integrated circuit provide excellent gain accuracy and temperature stability.

The output section (A_3) is connected in a unity-gain difference amplifier configuration. Precision matching of the four $10k\Omega$ resistors, especially over temperature and time, assures high common-mode rejection.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1µF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Resistance in series with the reference (pin 6) will degrade CMR. To maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins.

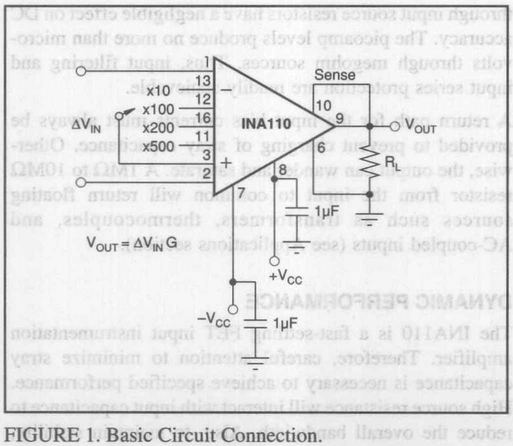


FIGURE 1. Basic Circuit Connection.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuit for the INA110. Both the offset of the input stage and output stage can be adjusted separately. Notice that the offset referred to the INA110's input (RTI) is the offset of the input stage plus the offset of the output stage divided by the gain of the input stage. This allows specification of offset independent of gain.

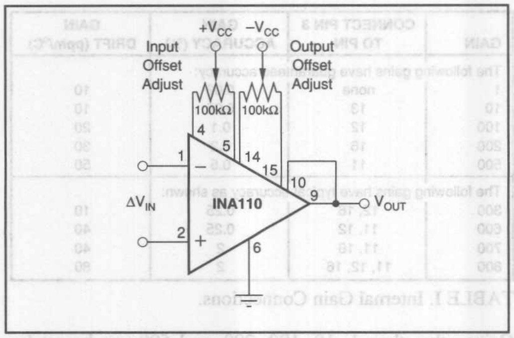


FIGURE 2. Offset Adjustment Circuit.

For systems using computer autozeroing techniques, neither offset nor offset drift are of concern. In many other applications, the factory-trimmed offset gives excellent results. When greater accuracy is desired, one adjustment is usually sufficient. In high gains (>100) adjust only the input offset, and in low gains the output offset. For higher precision in all gains, both can be adjusted by first selecting high gain and adjusting input offset and then low gain and adjusting output offset. The offset adjustment will, however, add to the drift by approximately 0.33µV/°C per 100µV of input offset voltage that is adjusted. Therefore, care should be taken when considering use of adjustment.

Output offsetting can be accomplished as shown in Figure 3 by applying a voltage to the reference (pin 6) through a buffer. This limits the resistance in series with pin 6 to minimize CMR error. Be certain to keep this resistance low. Note that the offset error can be adjusted at this reference point with no appreciable degradation in offset drift.

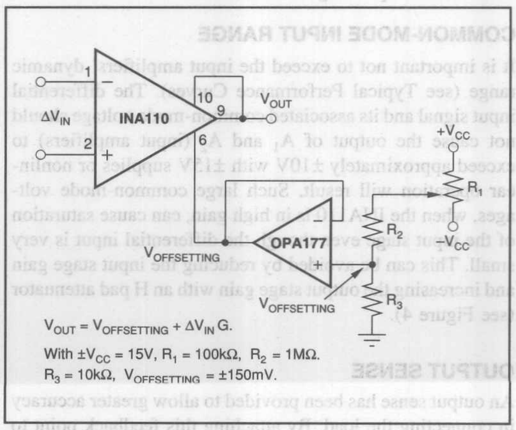


FIGURE 3. Output Offsetting.

INA110

4

INSTRUMENTATION AMPLIFIERS

Gain selection is accomplished by connecting the appropriate pins together on the INA110. Table I shows possible gains from the internal resistors. Keep the connections as short as possible to maintain accuracy.

GAIN	CONNECT PIN 3 TO PIN	GAIN ACCURACY (%)	GAIN DRIFT (ppm/°C)
The following gains have guaranteed accuracy:			
1	none	0.02	10
10	13	0.05	10
100	12	0.1	20
200	16	0.2	30
500	11	0.5	50
The following gains have typical accuracy as shown:			
300	12, 16	0.25	10
600	11, 12	0.25	40
700	11, 16	2	40
800	11, 12, 16	2	80

TABLE I. Internal Gain Connections.

Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 12, 16, and 11. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. The equation for choosing R_G is shown below.

$$R_G = \frac{40k}{G-1} - 50\Omega$$

Gain can also be changed in the output stage by adding resistance to the feedback loop shown in Figure 4. This is useful for increasing the total gain or reducing the input stage gain to prevent saturation of input amplifiers.

The output gain can be changed as shown in Table II. Matching of R_1 and R_3 is required to maintain high CMR. R_2 sets the gain with no effect on CMR.

OUTPUT STAGE GAIN	R_1 AND R_3	R_2
2	1.2kΩ	2.74kΩ
5	1kΩ	511Ω
10	1.5kΩ	340Ω

TABLE II. Output Stage Gain Control.

COMMON-MODE INPUT RANGE

It is important not to exceed the input amplifiers' dynamic range (see Typical Performance Curves). The differential input signal and its associated common-mode voltage should not cause the output of A_1 and A_2 (input amplifiers) to exceed approximately ±10V with ±15V supplies or nonlinear operation will result. Such large common-mode voltages, when the INA110 is in high gain, can cause saturation of the input stage even though the differential input is very small. This can be avoided by reducing the input stage gain and increasing the output stage gain with an H pad attenuator (see Figure 4).

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to load currents that Proper connection is shown in Figure 1. When more current is to be supplied, a power booster can be placed within the feedback loop as shown in Figure 5. Buffer errors are minimized by the loop gain of the output amplifier.

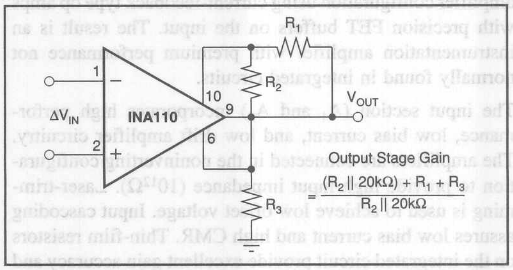


FIGURE 4. Gain Adjustment of Output Stage Using H Pad Attenuator.

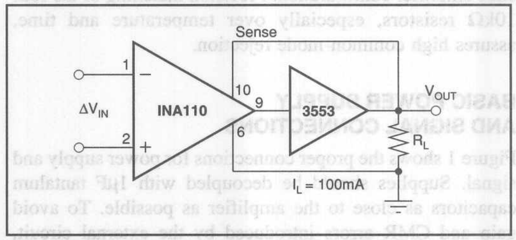


FIGURE 5. Current Boosting the Output.

LOW BIAS CURRENT OF FET INPUT ELIMINATES DC ERRORS

Because the INA110 has FET inputs, bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp levels produce no more than microvolts through megohm sources. Thus, input filtering and input series protection are readily achievable.

A return path for the input bias currents must always be provided to prevent charging of stray capacitance. Otherwise, the output can wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as transformers, thermocouples, and AC-coupled inputs (see Applications section).

DYNAMIC PERFORMANCE

The INA110 is a fast-settling FET input instrumentation amplifier. Therefore, careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with input capacitance to reduce the overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins.

Applications with balanced-source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the

negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the circuit stability. If the impedance in the positive input is greater, the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback depends upon source impedance imbalance, operating gain, and board layout. The addition of a small bypass capacitor of 5pF to 50pF directly between the inputs of the IA will generally eliminate any positive feedback. CMR errors due to the input impedance mismatch will also be reduced by the capacitor.

The INA110 is designed for fast settling with easy gain selection. It has especially excellent settling in high gain. It can also be used in fast-settling unity-gain applications. As with all such amplifiers, the INA110 does exhibit significant gain peaking when set to a gain of 1. It is, however, unconditionally stable. The gain peaking can be cancelled by band-limiting the negative input to 400kHz with a simple external RC circuit for applications requiring flat response. CMR is not affected by the addition of the 400kHz RC in a gain of 1.

Another distinct advantage of the INA110 is the high frequency CMR response. High frequency noise and sharp common-mode transients will be rejected. To preserve AC CMR, be sure to minimize stray capacitance on the input lines. Matching the RCs in the two inputs will help to maintain high AC CMR.

APPLICATIONS

In addition to general purpose uses, the INA110 is designed to accurately handle two important and demanding applications: (1) inputs with high source impedances such as capacitance/crystal/photodetector sensors and low-pass filters and series-input protection devices, and (2) rapid-scanning data acquisition systems requiring fast settling time. Because the user has access to the output sense, current sources can also be constructed using a minimum of external components. Figures 6 through 19 show application circuits.

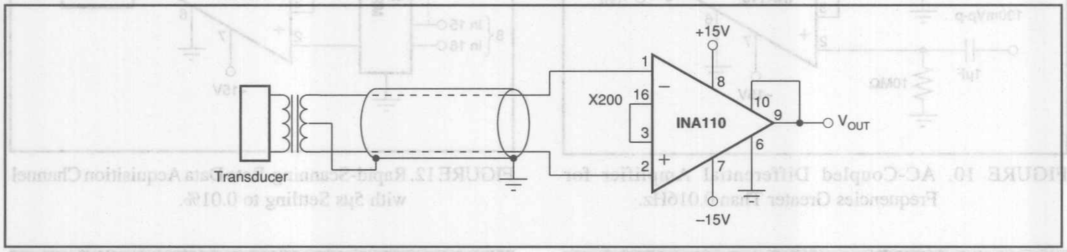


FIGURE 6. Transformer-Coupled Amplifier.

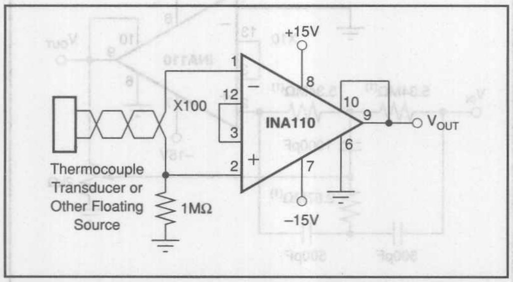


FIGURE 7. Floating Source Instrumentation Amplifier.

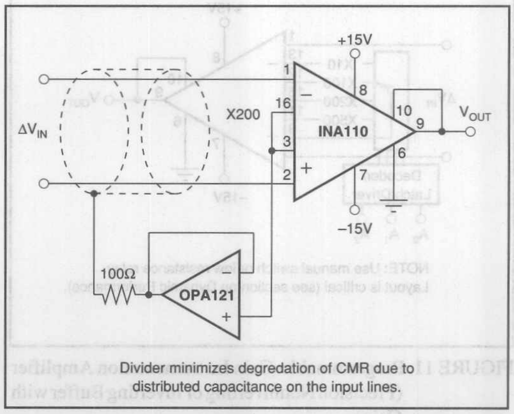
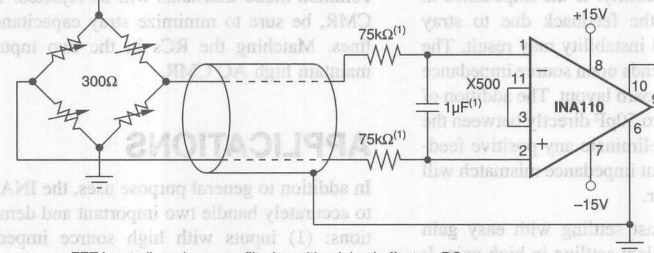


FIGURE 8. Instrumentation Amplifier with Shield Driver.



FET input allows low-pass filtering with minimal effect on DC accuracy.

NOTE: (1) Larger resistors and a smaller capacitor can be used.

FIGURE 9. Bridge Amplifier with 1Hz Low-Pass Input Filter.

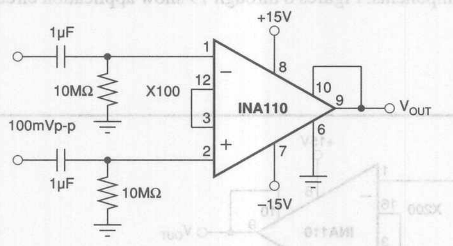


FIGURE 10. AC-Coupled Differential Amplifier for Frequencies Greater Than 0.016Hz.

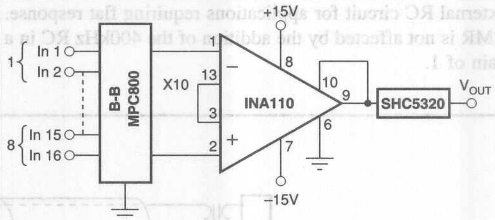
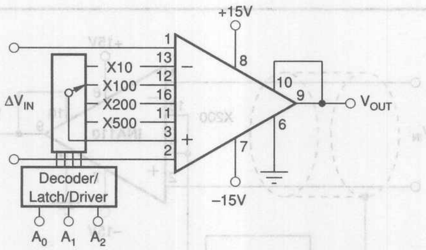
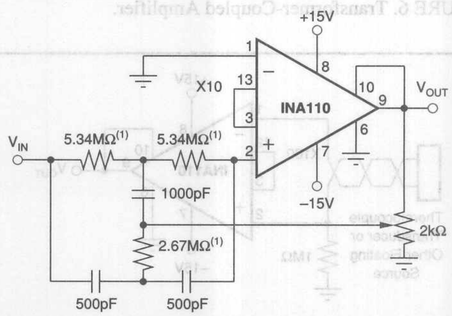


FIGURE 12. Rapid-Scanning-Rate Data Acquisition Channel with 5μs Settling to 0.01%.



NOTE: Use manual switch or low resistance relay.
Layout is critical (see section on Dynamic Performance).

FIGURE 11. Programmable-Gain Instrumentation Amplifier (Precision Noninverting or Inverting Buffer with Gain).



NOTE: (1) For 50Hz use 3.16MΩ and 6.37MΩ.
2kΩ potentiometer sets Q.

FIGURE 13. 60Hz Input Notch Filter.

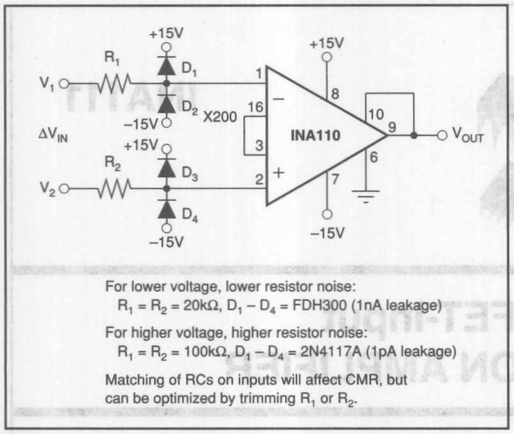


FIGURE 14. Input-Protected Instrumentation Amplifier.

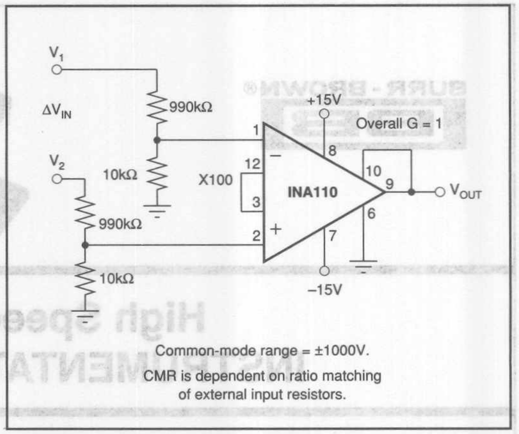
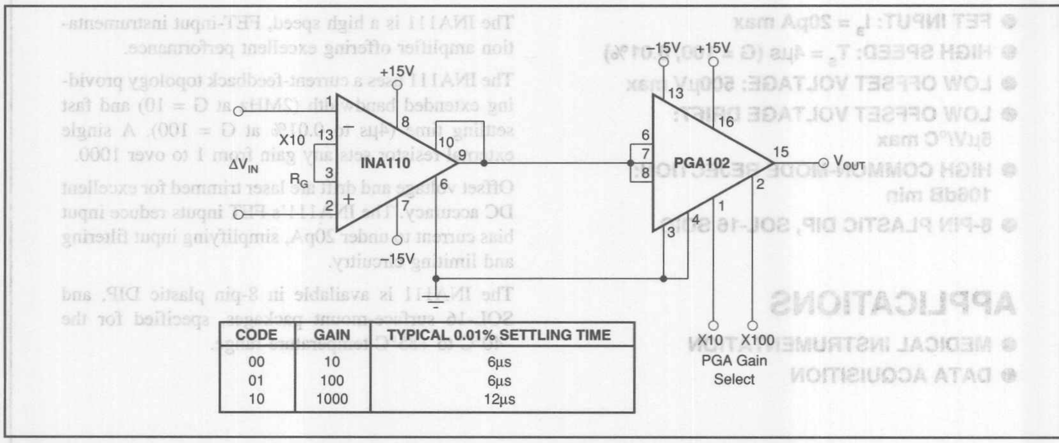


FIGURE 15. High Common-Mode Voltage Differential Amplifier.



CODE	GAIN	TYPICAL 0.01% SETTLING TIME
00	10	6μs
01	100	6μs
10	1000	12μs

FIGURE 16. Digitally-Controlled Fast-Settling Programmable Gain Instrumentation Amplifier.

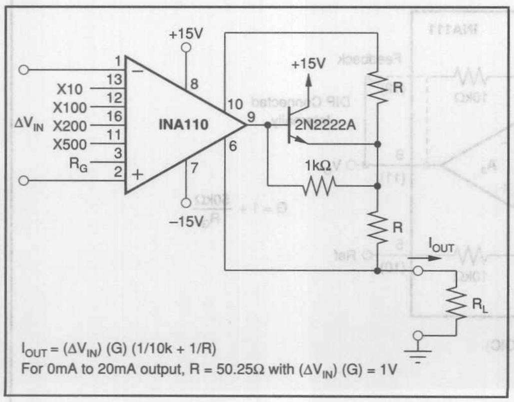


FIGURE 17. Differential Input FET Buffered Current Source.

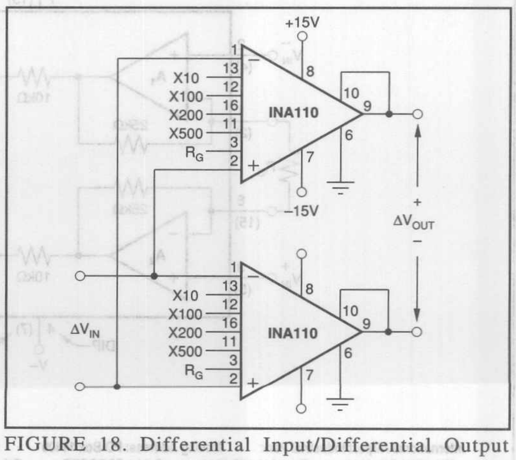
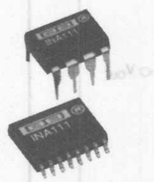


FIGURE 18. Differential Input/Differential Output Amplifier.

BURR - BROWN®



INA111

High Speed FET-Input INSTRUMENTATION AMPLIFIER

FEATURES

- FET INPUT: I_B = 20pA max
- HIGH SPEED: T_S = 4μs (G = 100, 0.01%)
- LOW OFFSET VOLTAGE: 500μV max
- LOW OFFSET VOLTAGE DRIFT: 5μV/°C max
- HIGH COMMON-MODE REJECTION: 106dB min
- 8-PIN PLASTIC DIP, SOL-16 SOIC

APPLICATIONS

- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

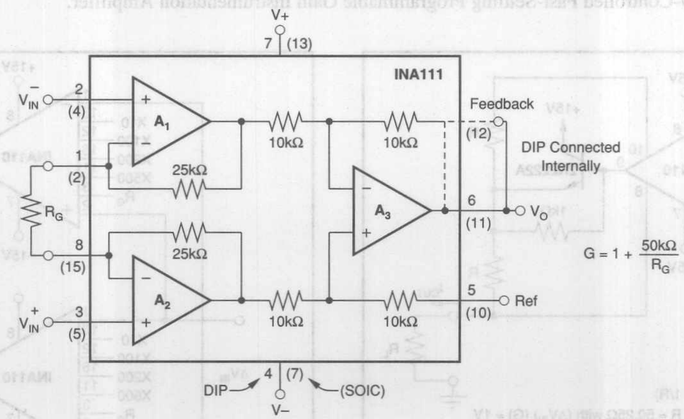
DESCRIPTION

The INA111 is a high speed, FET-input instrumentation amplifier offering excellent performance.

The INA111 uses a current-feedback topology providing extended bandwidth (2MHz at G = 10) and fast settling time (4μs to 0.01% at G = 100). A single external resistor sets any gain from 1 to over 1000.

Offset voltage and drift are laser trimmed for excellent DC accuracy. The INA111's FET inputs reduce input bias current to under 20pA, simplifying input filtering and limiting circuitry.

The INA111 is available in 8-pin plastic DIP, and SOL-16 surface-mount packages, specified for the −40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1143D

SPECIFICATIONS

ELECTRICAL

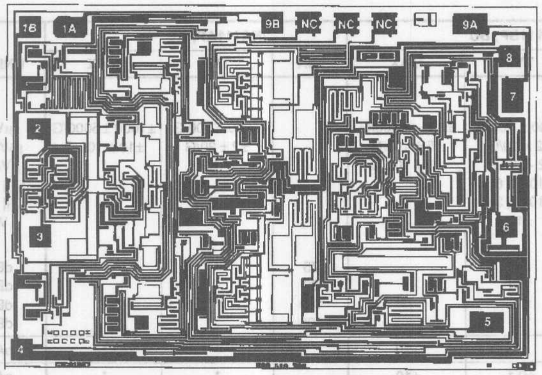
$T_A = +25°C$, $V_S = ±15V$, $R_L = 2kΩ$, unless otherwise noted.

		INA111BP, BU			INA111AP, AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
Offset Voltage, RTI								
Initial	$T_A = +25°C$		±100 ± 500/G	±500 ±2000/G		±200 ± 500/G	±1000 ±5000/G	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		±2 ± 10/G	±5 ± 100/G		±2 ± 20/G	±10 ± 100/G	µV/°C
vs Power Supply	$V_S = ±6V$ to ±18V		2 +10/G	30 + 100/G		*	*	µV/V
Impedance, Differential			10^{12} || 6			*		Ω || pF
Common-Mode			10^{12} || 3			*		Ω || pF
Input Common-Mode Range	$V_{DIFF} = 0V$	±10	±12		*	*		V
Common-Mode Rejection	$V_{CM} = ±10V$, $ΔR_S = 1kΩ$							
	G = 1	80	90		75	*		dB
	G = 10	96	110		90	*		dB
	G = 100	106	115		100	*		dB
	G = 1000	106	115		100	*		dB
BIAS CURRENT			±2	±20		*	*	pA
OFFSET CURRENT			±0.1	±10		*	*	pA
NOISE VOLTAGE, RTI	G = 1000, $R_S = 0Ω$							
f = 100Hz			13			*		nV/√Hz
f = 1kHz			10			*		nV/√Hz
f = 10kHz			10			*		nV/√Hz
$f_B = 0.1Hz$ to 10Hz			1			*		µVp-p
Noise Current								
f = 10kHz			0.8			*		fA/√Hz
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G = 1, $R_L = 10kΩ$		±0.01	±0.02		*	0.05	%
	G = 10, $R_L = 10kΩ$		±0.1	±0.5		*	*	%
	G = 100, $R_L = 10kΩ$		±0.15	±0.5		*	±0.7	%
	G = 1000, $R_L = 10kΩ$		±0.25	±1		*	±2	%
Gain vs Temperature	G = 1		±1	±10		*	*	ppm/°C
50kΩ Resistance(1)			±25	±100		*	*	ppm/°C
Nonlinearity	G = 1		±0.0005	±0.005		*	*	% of FSR
	G = 10		±0.001	±0.005		*	±0.01	% of FSR
	G = 100		±0.001	±0.005		*	±0.01	% of FSR
	G = 1000		±0.005	±0.02		*	±0.04	% of FSR
OUTPUT								
Voltage	$I_O = 5mA$, T_{MIN} to T_{MAX}	±11	±12.7		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+30/–25			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		2			*		MHz
	G = 10		2			*		MHz
	G = 100		450			*		kHz
	G = 1000		50			*		kHz
Slew Rate	$V_O = ±10V$, G = 2 to 100		17			*		V/µs
Settling Time, 0.01%	G = 1		2			*		µs
	G = 10		2			*		µs
	G = 100		4			*		µs
	G = 1000		30			*		µs
Overload Recovery	50% Overdrive		1			*		µs
POWER SUPPLY								
Voltage Range		±6	±15	±18	*	*	*	V
Current	$V_{IN} = 0V$		±3.3	±4.5		*		mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating	Plastic P, U	–40		125	*		*	°C
$θ_{JA}$	Plastic P, U		100			*		°C/W

* Specification same as INA111BP.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.

DICE INFORMATION



INA111 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B	R_G	6	V_O
2	V^-_{IN}	7	Feedback
3	V^+_{IN}	8	V+
4	V–	9A, 9B	R_G
5	Ref		

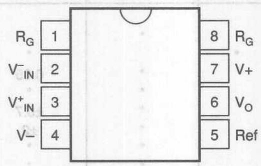
Pads 1A and 1B must be connected. Pads 9A and 9B must be connected.
NC = No Connection.
Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

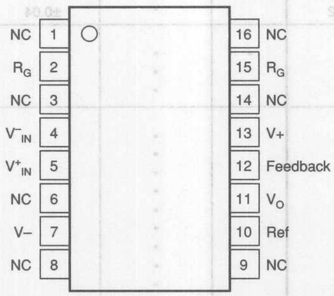
	MILS (0.001")	MILLIMETERS
Die Size	129 x 90 ±5	3.28 x 2.29 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

PIN CONFIGURATIONS

Top View | DIP



Top View | SOL-16 Surface Mount



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	(V–) –0.7V to (V+) +15V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA111AP	8-Pin Plastic DIP	–40°C to +85°C
INA111BP	8-Pin Plastic DIP	–40°C to +85°C
INA111AU	SOL-16 Surface-Mount	–40°C to +85°C
INA111BU	SOL-16 Surface-Mount	–40°C to +85°C

PACKAGE INFORMATION

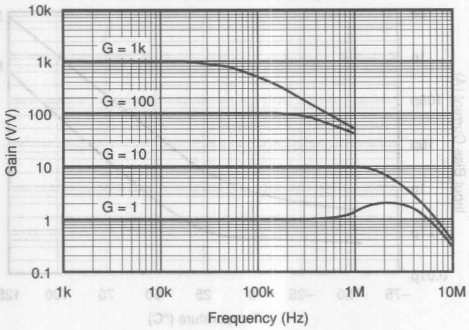
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA111AP	8-Pin Plastic DIP	006
INA111BP	8-Pin Plastic DIP	006
INA111AU	16-Pin Surface Mount	211
INA111BU	16-Pin Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

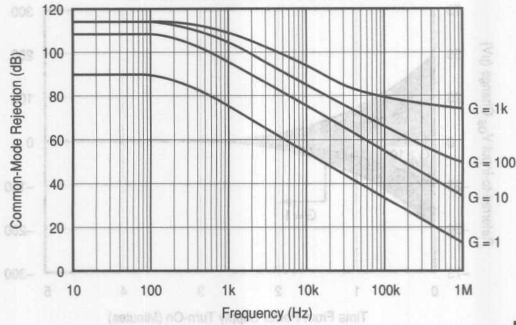
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

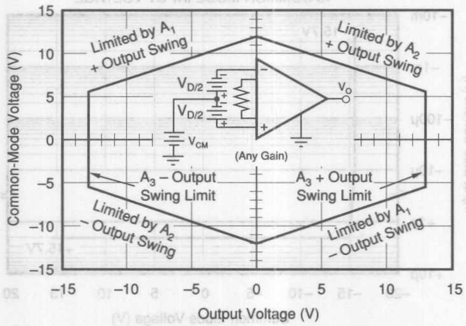
GAIN vs FREQUENCY



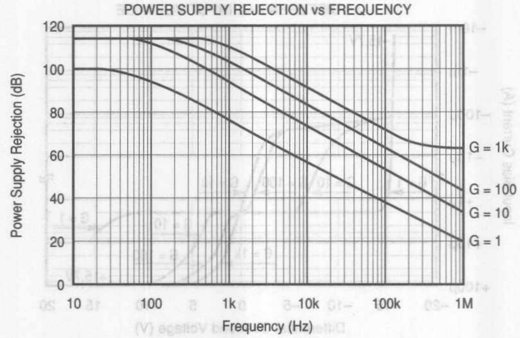
COMMON-MODE REJECTION vs FREQUENCY



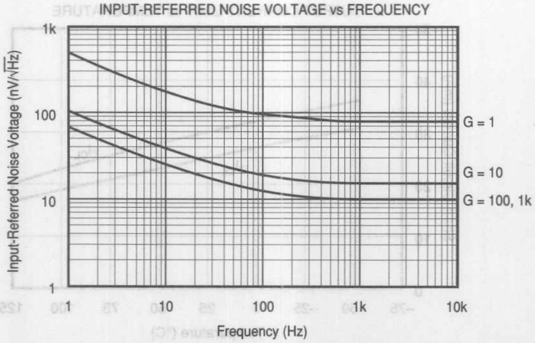
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



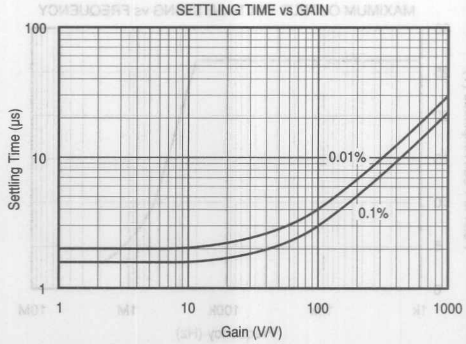
POWER SUPPLY REJECTION vs FREQUENCY



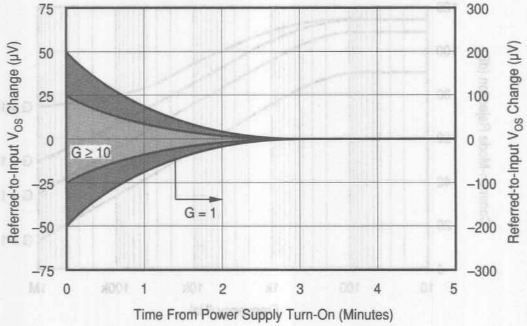
INPUT-REFERRED NOISE VOLTAGE vs FREQUENCY



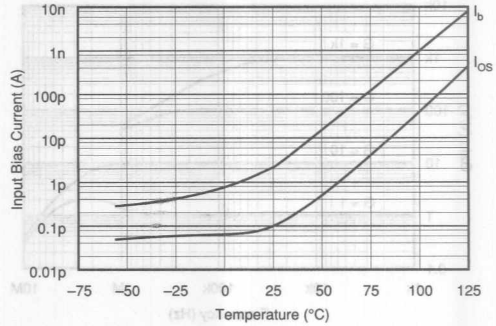
SETTLING TIME vs GAIN



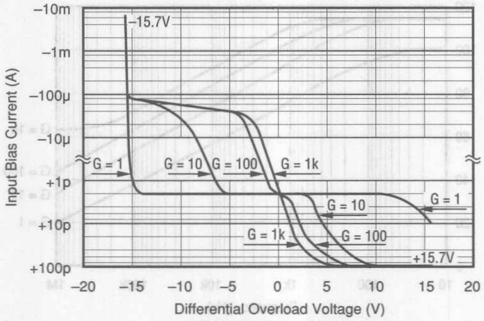
OFFSET VOLTAGE WARM-UP vs TIME



INPUT BIAS CURRENT vs TEMPERATURE

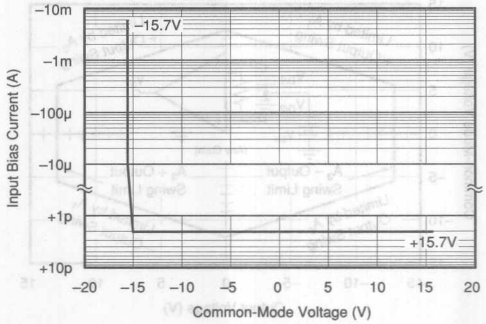


INPUT BIAS CURRENT
vs DIFFERENTIAL INPUT VOLTAGE

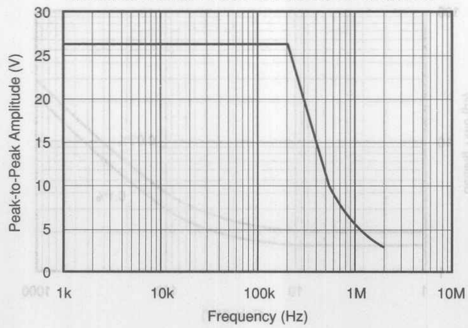


NOTE: One input grounded.

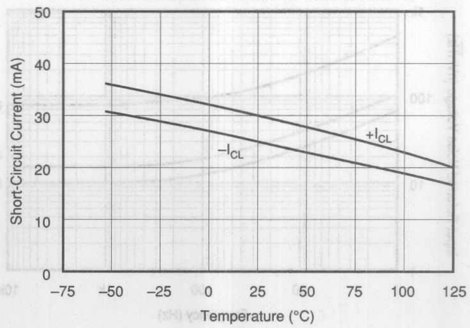
INPUT BIAS CURRENT
vs COMMON-MODE INPUT VOLTAGE



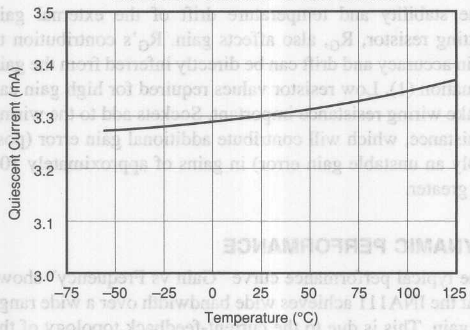
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



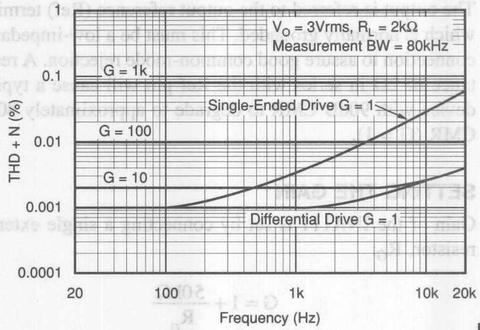
OUTPUT CURRENT LIMIT vs TEMPERATURE



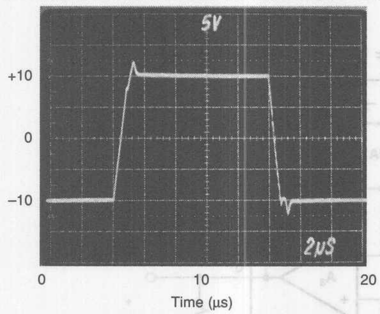
QUIESCENT CURRENT vs TEMPERATURE



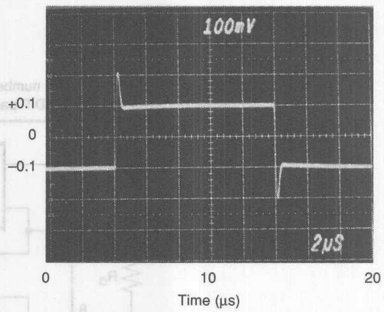
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



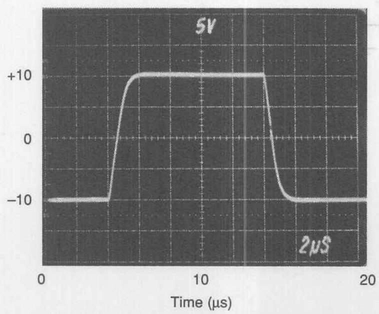
LARGE SIGNAL RESPONSE, G = 100



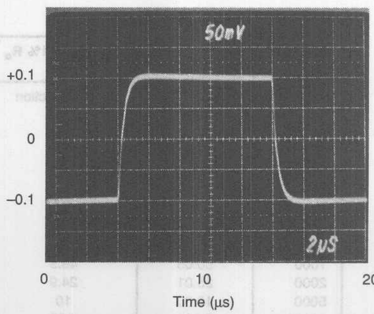
SMALL SIGNAL RESPONSE, G = 1



LARGE SIGNAL RESPONSE, G = 100



SMALL SIGNAL RESPONSE, G = 1



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA111. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 2Ω in series with the Ref pin will cause a typical device with 90dB CMR to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain of the INA111 is set by connecting a single external resistor, R_G:

$$G = 1 + \frac{50k\Omega}{R_G} \tag{1}$$

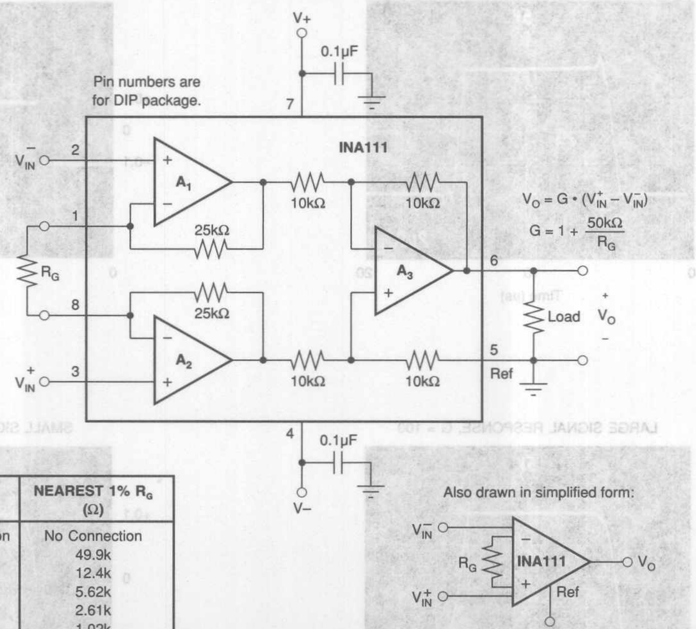
Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in equation 1 comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA111.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that the INA111 achieves wide bandwidth over a wide range of gain. This is due to the current-feedback topology of the INA111. Settling time also remains excellent over wide gains.



DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	No Connection	No Connection
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

FIGURE 1. Basic Connections

The INA111 exhibits approximately 6dB rise in gain at 2MHz in unity gain. This is a result of its current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable +6dB/octave due to a response zero. A simple pole at 700kHz or lower will produce a flat passband response (see Input Filtering).

The INA111 provides excellent rejection of high frequency common-mode signals. The typical performance curve, "Common-Mode Rejection vs Frequency" shows this behavior. If the inputs are not properly balanced, however, common-mode signals can be converted to differential signals. Run the V_{IN}^{+} and V_{IN}^{-} connections directly adjacent each other, from the source signal all the way to the input pins. If possible use a ground plane under both input traces. Avoid running other potentially noisy lines near the inputs.

NOISE AND ACCURACY PERFORMANCE

The INA111's FET input circuitry provides low input bias current and high speed. It achieves lower noise and higher accuracy with high impedance sources. With source impedances of 2kΩ to 50kΩ the INA114 may provide lower offset voltage and drift. For very low source impedance (≤1kΩ), the INA103 may provide improved accuracy and lower noise.

OFFSET TRIMMING

The INA111 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. The op amp shown maintains low output impedance at high frequency. Trim circuits with higher source impedance should be buffered with an op amp follower circuit to assure low impedance on the Ref pin.

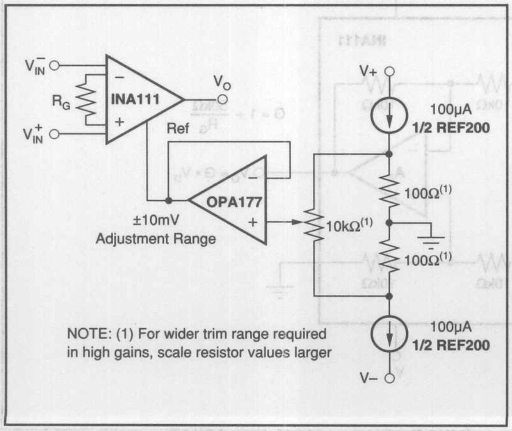


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA111 is extremely high—approximately $10^{12}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than 10pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA111 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA111 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

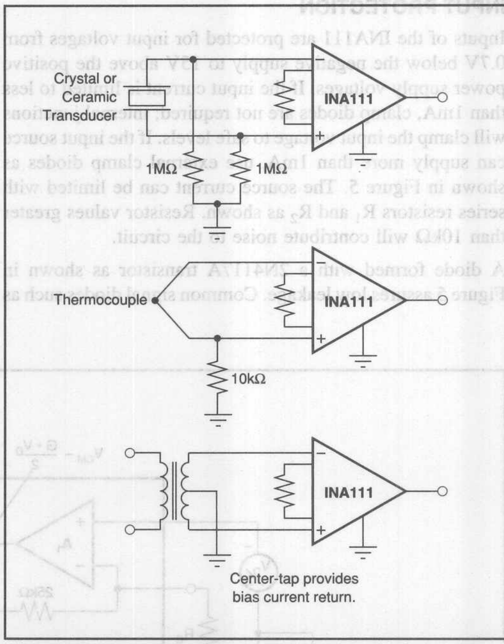


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA111 is approximately ±12V (or 3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2. The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage".

INA111

4

INSTRUMENTATION AMPLIFIERS

voltage can cause the output of A_1 or A_2 to saturate. Figure 4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA111 in a lower gain (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the INA111 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, consider an input voltage of +14V on one input and +15V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA111 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

Inputs of the INA111 are protected for input voltages from 0.7V below the negative supply to 15V above the positive power supply voltages. If the input current is limited to less than 1mA, clamp diodes are not required; internal junctions will clamp the input voltage to safe levels. If the input source can supply more than 1mA, use external clamp diodes as shown in Figure 5. The source current can be limited with series resistors R_1 and R_2 as shown. Resistor values greater than 10kΩ will contribute noise to the circuit.

A diode formed with a 2N4117A transistor as shown in Figure 5 assures low leakage. Common signal diodes such as input bias current of the INA111 and are usually sensitive to light.

INPUT FILTERING

The INA111's FET input allows use of an R/C input filter without creating large offsets due to input bias current. Figure 6 shows proper implementation of this input filter to preserve the INA111's excellent high frequency common-mode rejection. Mismatch of the common-mode input capacitance (C_1 and C_2), either from stray capacitance or

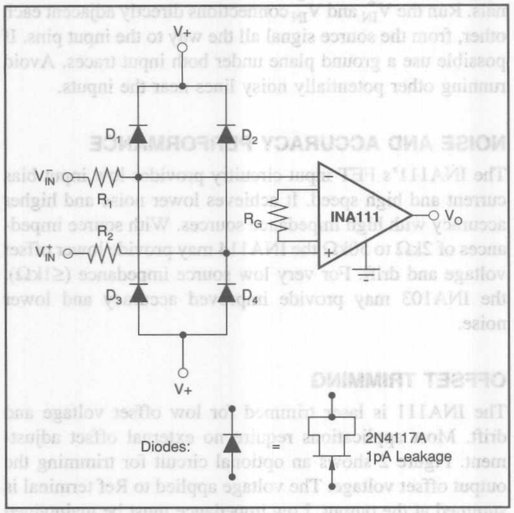


FIGURE 5. Input Protection Voltage Clamp.

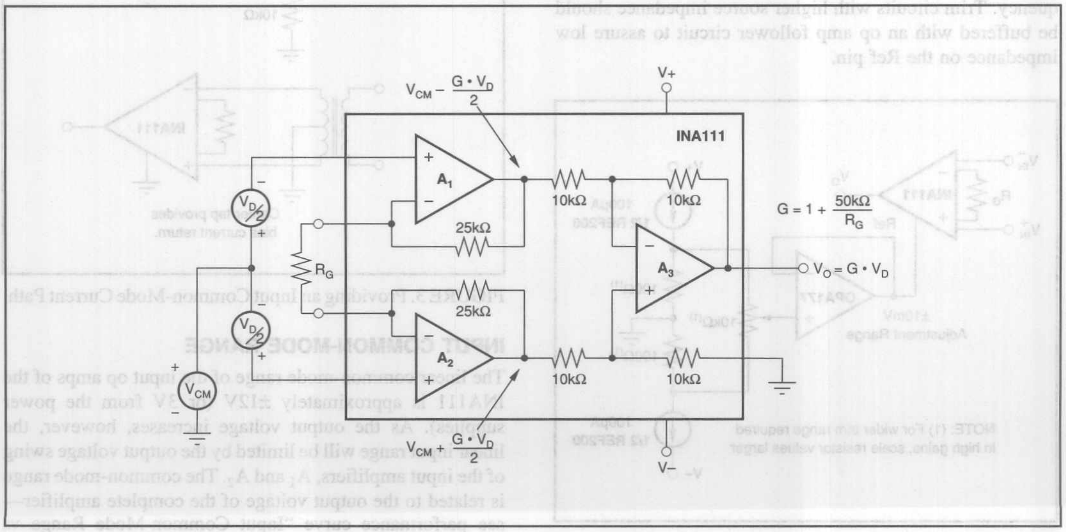


FIGURE 4. Voltage Swing of A_1 and A_2.

common-mode rejection. The differential input capacitor, C_3, reduces the bandwidth and mitigates the effects of mismatch in C_1 and C_2. Make C_3 much larger than C_1 and C_2. If properly matched, C_1 and C_2 also improve CMR.

OUTPUT VOLTAGE SENSE (SOL-16 Package Only)

The surface-mount version of the INA111 has a separate output sense feedback connection (pin 12). Pin 12 must be connected, usually to the output terminal, pin 11, for proper operation. (This connection is made internally on the DIP version of the INA111.)

The output feedback connection can be used to sense the output voltage directly at the load for best accuracy. Figure 8 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through C_1.

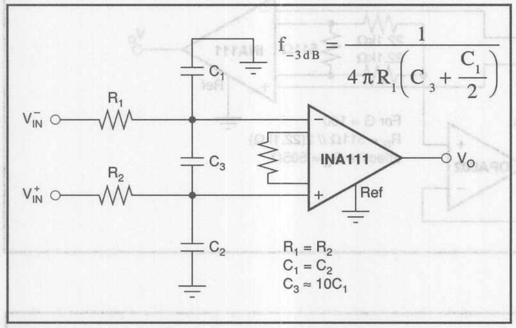


FIGURE 6. Input Low-Pass Filter.

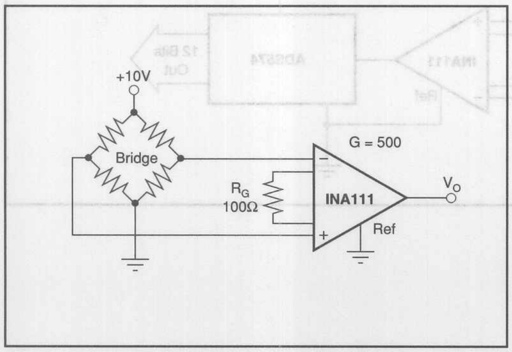


FIGURE 7. Bridge Transducer Amplifier.

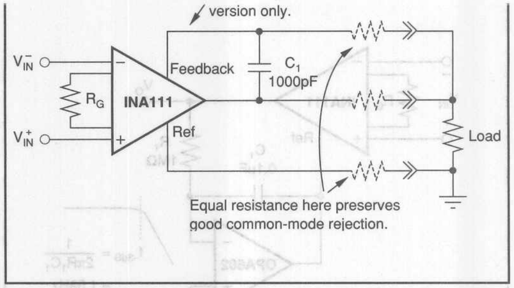


FIGURE 8. Remote Load and Ground Sensing.

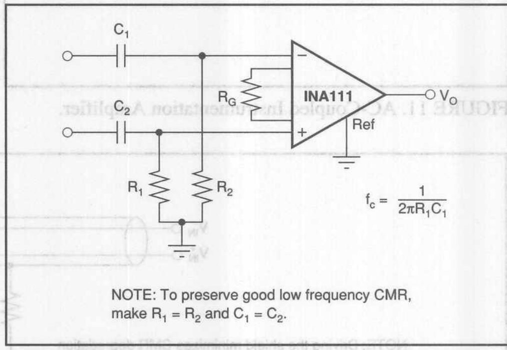


FIGURE 9. High-Pass Input Filter.

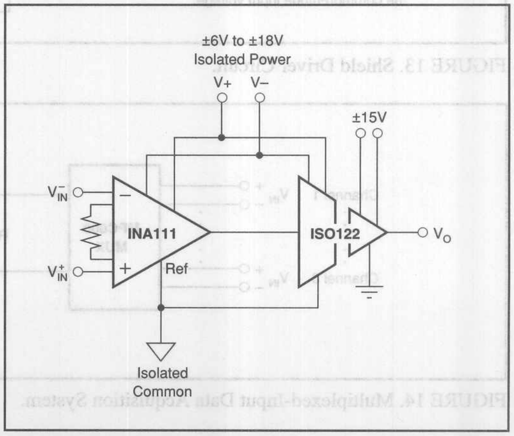


FIGURE 10. Galvanically Isolated Instrumentation Amplifier.

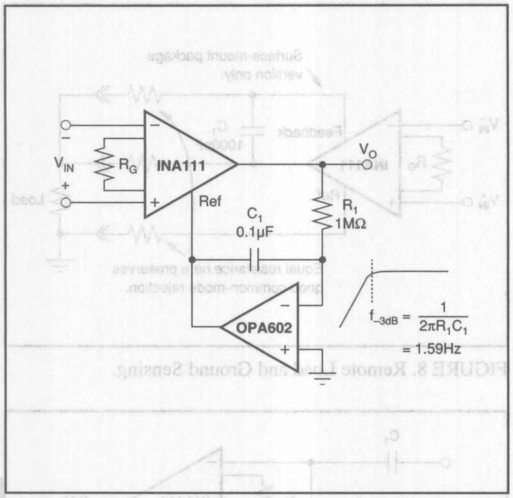


FIGURE 11. AC-Coupled Instrumentation Amplifier.

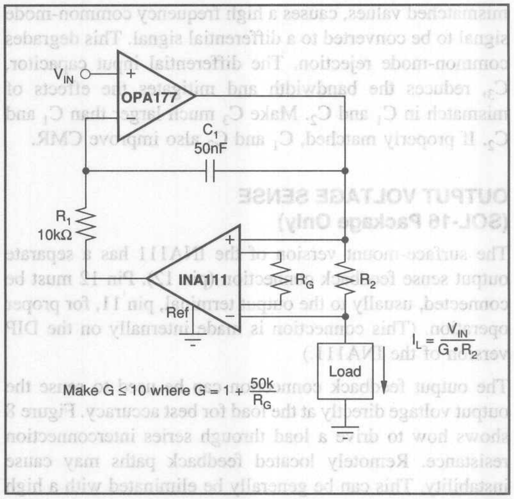


FIGURE 12. Voltage Controlled Current Source.

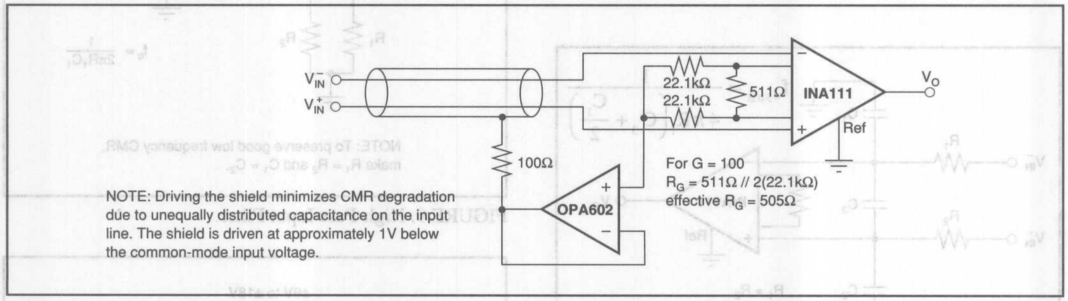


FIGURE 13. Shield Driver Circuit.

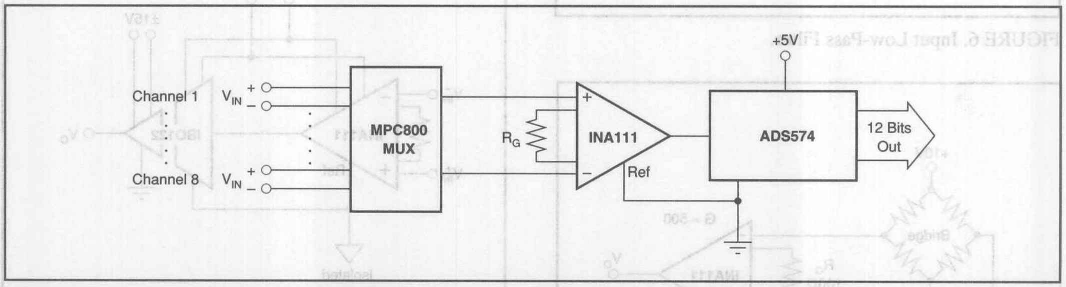
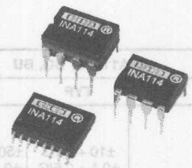


FIGURE 14. Multiplexed-Input Data Acquisition System.

BURR - BROWN®



INA114

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.25μV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 115dB min
- INPUT OVER-VOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 3mA max
- 8-PIN PLASTIC AND CERAMIC DIP, SOL-16

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

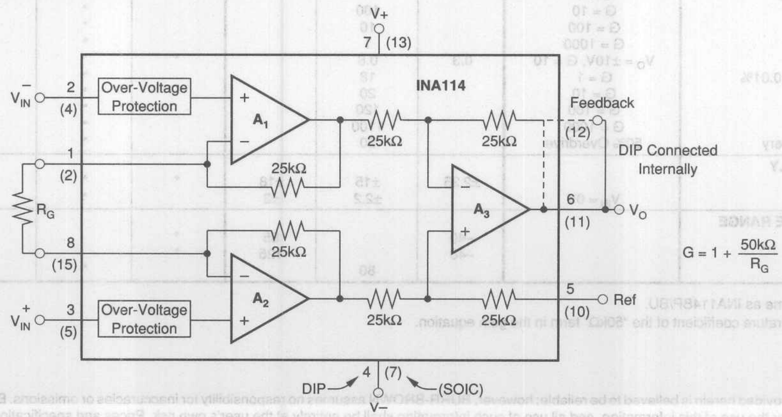
DESCRIPTION

The INA114 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA114 is laser trimmed for very low offset voltage (50μV), drift (0.25μV/°C) and high common-mode rejection (115dB at G = 1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA114 is available in 8-pin plastic and ceramic DIPs, and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

4 INSTRUMENTATION AMPLIFIERS INA114

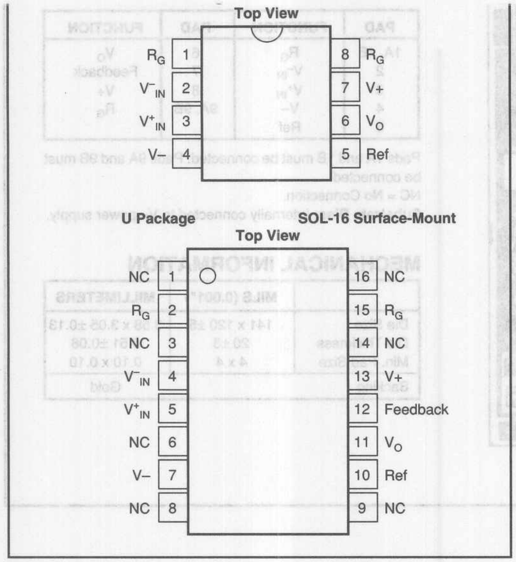
ELECTRICAL

At $T_A = +25°C$, $V_S = ±15V$, $R_L = 2kΩ$ unless otherwise noted.

PARAMETER	CONDITIONS	INA114BP, BG, BU MIN	INA114BP, BG, BU TYP	INA114BP, BG, BU MAX	INA114AP, AG, AU MIN	INA114AP, AG, AU TYP	INA114AP, AG, AU MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	$T_A = +25°C$		±10 + 20/G	±50 + 100/G		±25 + 30/G	±125 + 500/G	μV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		±0.1 + 0.5/G	±0.25 + 5/G		±0.25 + 5/G	±1 + 10/G	μV/°C
vs Power Supply	$V_S = ±2.25V$ to ±18V		0.5 + 2/G	3 + 10/G		*	*	μV/V
Long-Term Stability			±0.2 + 0.5/G			*		μV/mo
Impedance, Differential			10^{10} || 6			*		Ω || pF
Common-Mode			10^{10} || 6			*		Ω || pF
Input Common-Mode Range		±11	±13.5		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	$V_{CM} = ±10V$, $ΔR_S = 1kΩ$							
	G = 1	80	96		75	90		dB
	G = 10	96	115		90	106		dB
	G = 100	110	120		106	110		dB
	G = 1000	115	120		106	110		dB
BIAS CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
OFFSET CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
NOISE VOLTAGE, RTI	G = 1000, $R_S = 0Ω$							
f = 10Hz			15			*		$nV/\sqrt{Hz}$
f = 100Hz			11			*		$nV/\sqrt{Hz}$
f = 1kHz			11			*		$nV/\sqrt{Hz}$
$f_B = 0.1Hz$ to 10Hz			0.4			*		μVp-p
Noise Current								
f=10Hz			0.4			*		$pA/\sqrt{Hz}$
f=1kHz			0.2			*		$pA/\sqrt{Hz}$
$f_B = 0.1Hz$ to 10Hz			18			*		pAp-p
GAIN								
Gain Equation			1+ $(50kΩ/R_G)$			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G = 1		±0.01	±0.05		*	*	%
	G = 10		±0.02	±0.4		*	±0.5	%
	G = 100		±0.05	±0.5		*	±0.7	%
	G = 1000		±0.5	±1		*	±2	%
Gain vs Temperature	G = 1		±2	±10		*	±10	ppm/°C
50kΩ Resistance(1)			±25	±100		*	*	ppm/°C
Nonlinearity	G = 1		±0.0001	±0.001		*	±0.002	% of FSR
	G = 10		±0.0005	±0.002		*	±0.004	% of FSR
	G = 100		±0.0005	±0.002		*	±0.004	% of FSR
	G = 1000		±0.002	±0.01		*	±0.02	% of FSR
OUTPUT								
Voltage	$I_O = 5mA$, T_{MIN} to T_{MAX}	±13.5	±13.7		*	*		V
	$V_S = ±11.4V$, $R_L = 2kΩ$	±10	±10.5		*	*		V
	$V_S = ±2.25V$, $R_L = 2kΩ$	±1	±1.5		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+20/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		1			*		MHz
	G = 10		100			*		kHz
	G = 100		10			*		kHz
	G = 1000		1			*		kHz
Slew Rate	$V_O = ±10V$, G = 10	0.3	0.6		*	*		V/μs
Settling Time, 0.01%	G = 1		18			*		μs
	G = 10		20			*		μs
	G = 100		120			*		μs
	G = 1000		1100			*		μs
Overload Recovery	50% Overdrive		20			*		μs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current	$V_{IN} = 0V$		±2.2	±3		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as INA114BP/BU.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.



This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

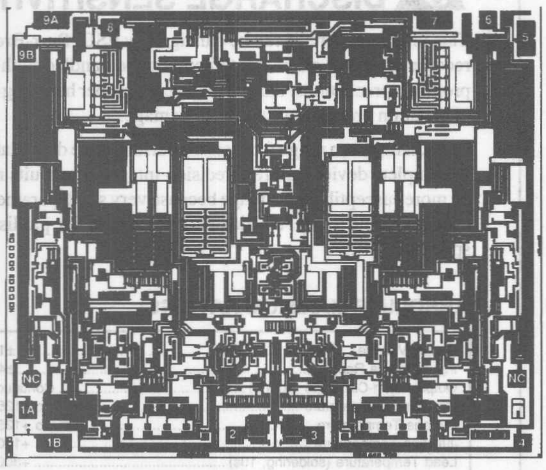
MODEL	PACKAGE	TEMPERATURE RANGE
INA114AP	Plastic DIP	–40°C to +85°C
INA114BP	Plastic DIP	–40°C to +85°C
INA114AG	Ceramic DIP	–40°C to +85°C
INA114BG	Ceramic DIP	–40°C to +85°C
INA114AU	Surface-Mount	–40°C to +85°C
INA114BU	Surface-Mount	–40°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA114AP	8-Pin Plastic DIP	006
INA114BP	8-Pin Plastic DIP	006
INA114AG	8-Pin Ceramic DIP	254
INA114BG	8-Pin Ceramic DIP	254
INA114AU	SOL-16 Surface-Mount	211
INA114BU	SOL-16 Surface-Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

DICE INFORMATION



INA114 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B	R_G	6	V_O
2	V^-_{IN}	7	Feedback
3	V^+_{IN}	8	V+
4	V–	9A, 9B	R_G
5	Ref		

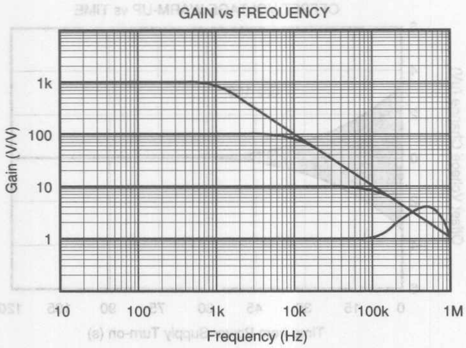
Pads 1A and 1B must be connected. Pads 9A and 9B must be connected.
NC = No Connection.
Substrate Bias: Internally connected to V– power supply.

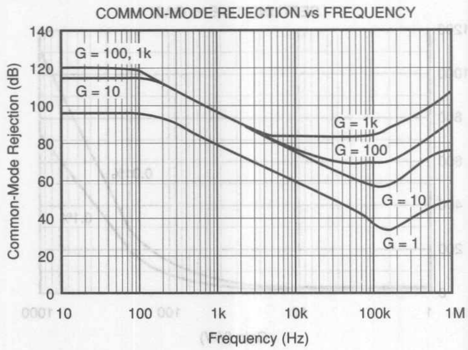
MECHANICAL INFORMATION

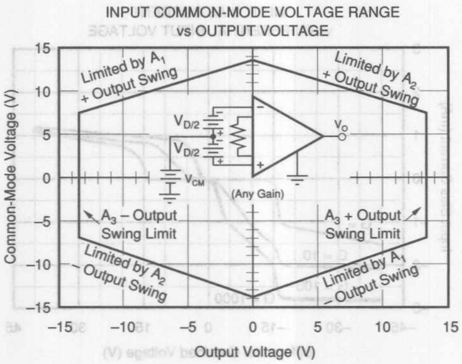
	MILS (0.001")	MILLIMETERS
Die Size	141 x 120 ±5	3.58 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

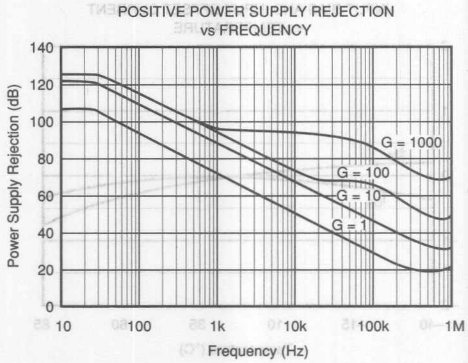
TYPICAL PERFORMANCE CURVES

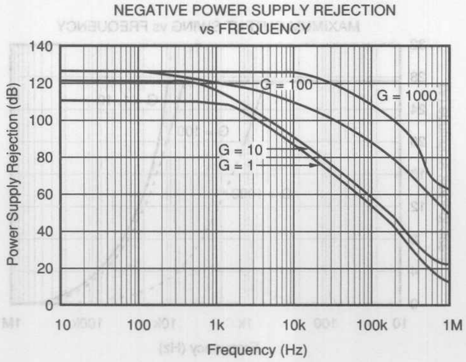
At T_A = +25°C, V_S = ±15V, unless otherwise noted.

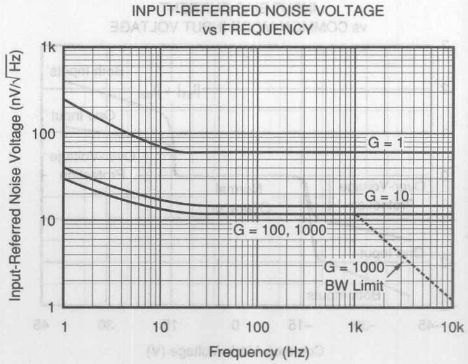












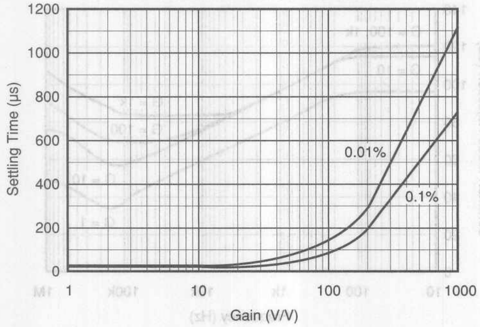
INA114

4

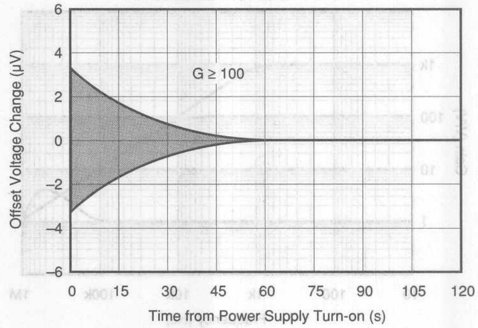
INSTRUMENTATION AMPLIFIERS

At $T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.

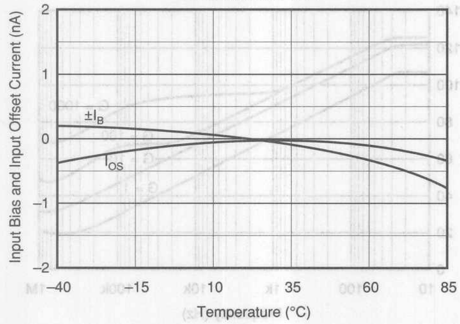
SETTLING TIME vs GAIN



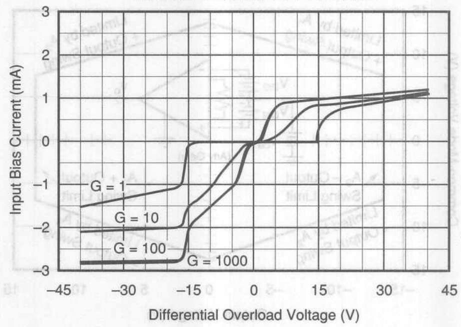
OFFSET VOLTAGE WARM-UP vs TIME



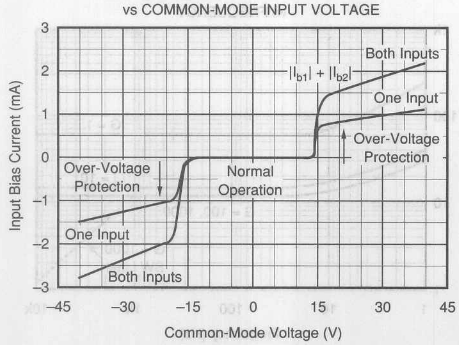
INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE



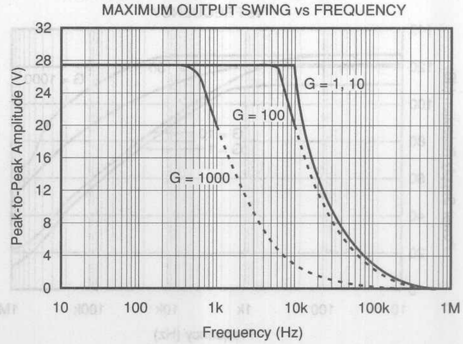
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



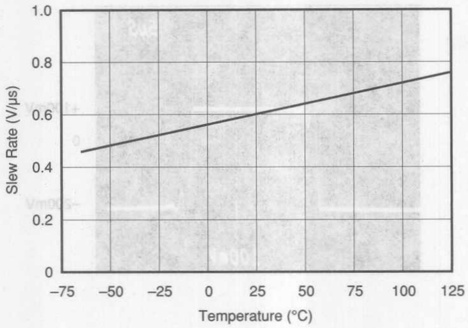
INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE



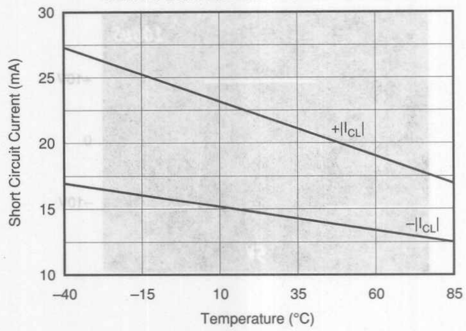
MAXIMUM OUTPUT SWING vs FREQUENCY



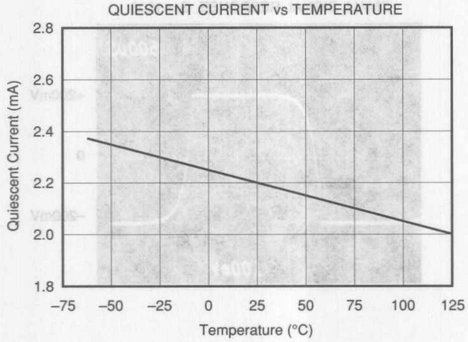
SLEW RATE vs TEMPERATURE



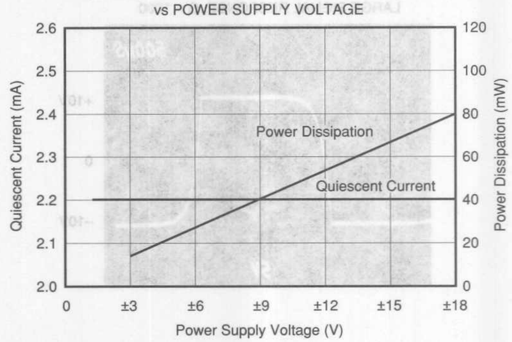
OUTPUT CURRENT LIMIT vs TEMPERATURE



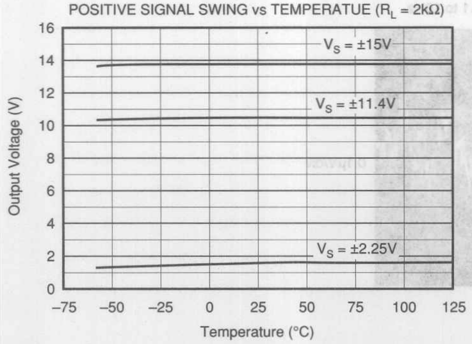
QUIESCENT CURRENT vs TEMPERATURE



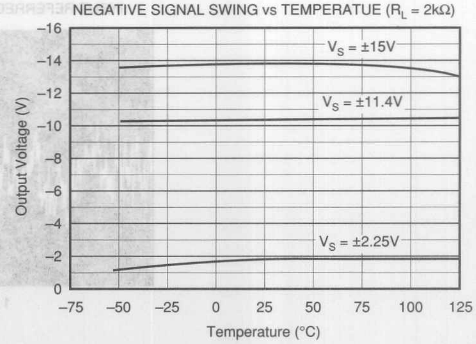
QUIESCENT CURRENT AND POWER DISSIPATION vs POWER SUPPLY VOLTAGE



POSITIVE SIGNAL SWING vs TEMPERATUE (R_L = 2kΩ)



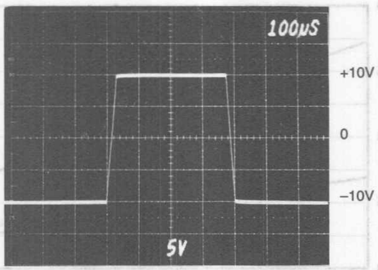
NEGATIVE SIGNAL SWING vs TEMPERATUE (R_L = 2kΩ)



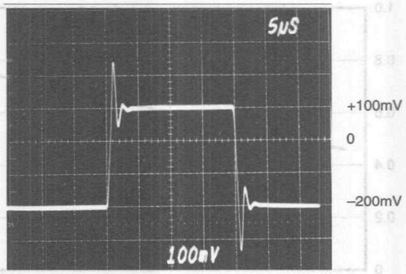
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = ±15V$, unless otherwise noted.

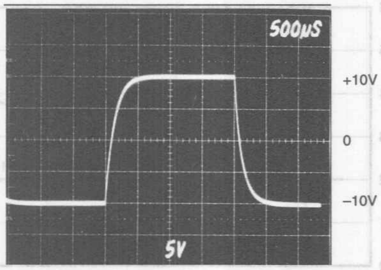
LARGE SIGNAL RESPONSE, G = 1



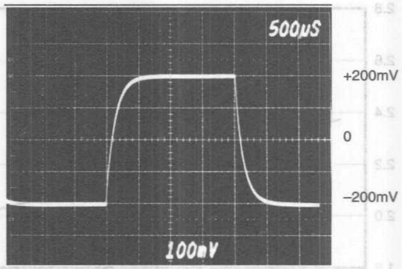
SMALL SIGNAL RESPONSE, G = 1



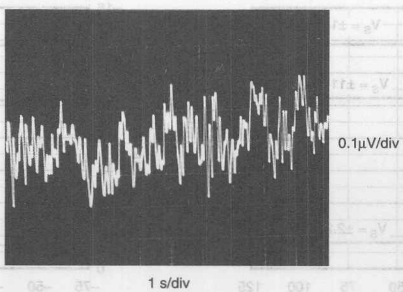
LARGE SIGNAL RESPONSE, G = 1000



SMALL SIGNAL RESPONSE, G = 1000



INPUT-REFERRED NOISE, 0.1 to 10Hz



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA114. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain of the INA114 is set by connecting a single external resistor, R_G:

$$G = 1 + \frac{50\ k\Omega}{R_G} \qquad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

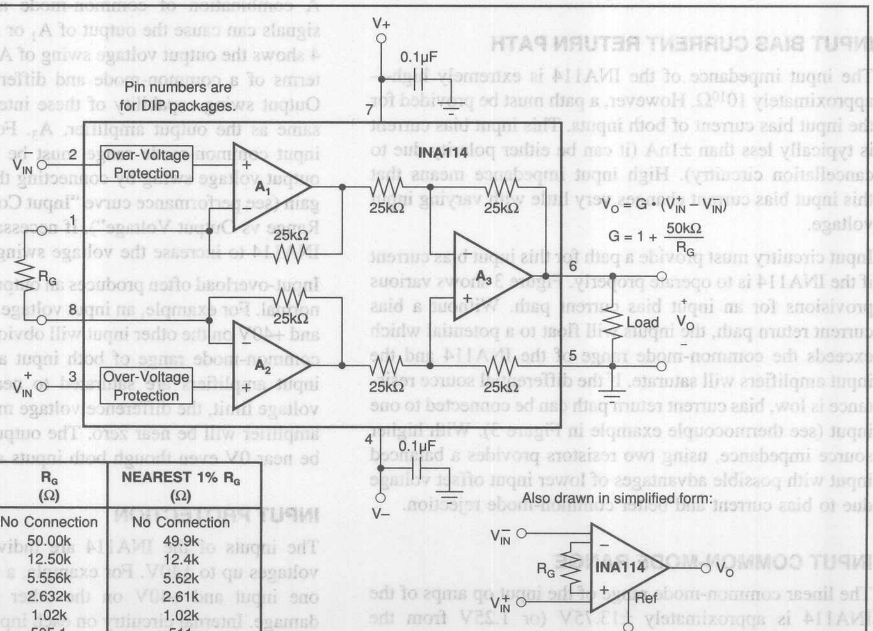
The 50kΩ term in equation (1) comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA114.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

NOISE PERFORMANCE

The INA114 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-input instrumentation amplifier may provide lower noise.

Low frequency noise of the INA114 is approximately 0.4μVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of "low noise" chopper-stabilized amplifiers.



DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	No Connection	No Connection
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA114 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering trim voltage with an op amp as shown.

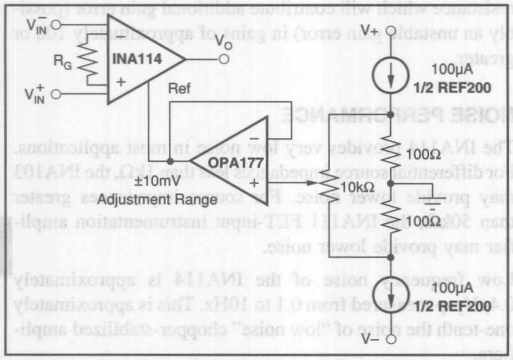


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA114 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA114 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA114 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA114 is approximately ±13.75V (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2. The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage."

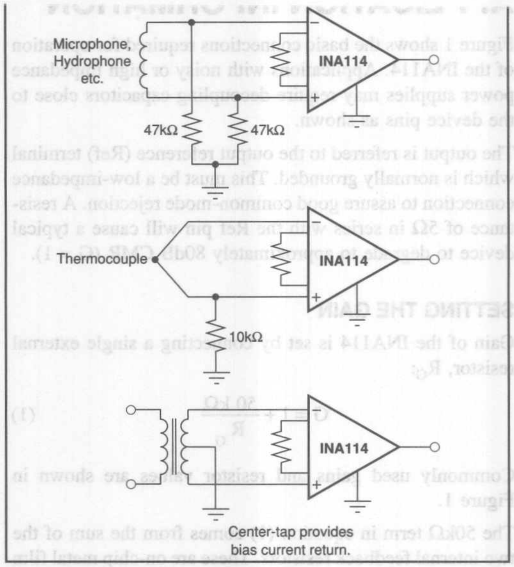


FIGURE 3. Providing an Input Common-Mode Current Path.

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. Figure 4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA114 in a lower gain (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the INA114 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA114 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA114 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input

power supply voltage is present.

OUTPUT VOLTAGE SENSE (SOL-16 package only)

The surface-mount version of the INA114 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA114.)

voltage directly at the load for best accuracy. Figure 5 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through C_1. Heavy loads or long lines can be driven by connecting a buffer inside the feedback path (Figure 6).

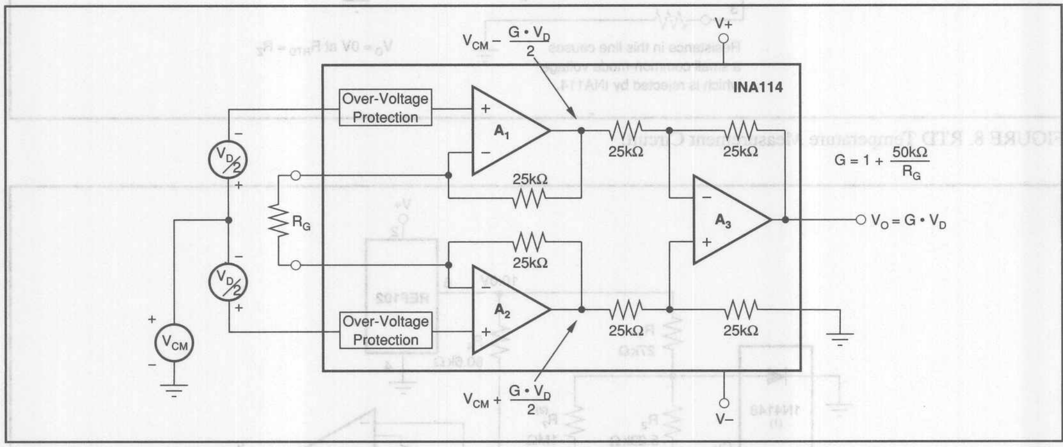


FIGURE 4. Voltage Swing of A_1 and A_2.

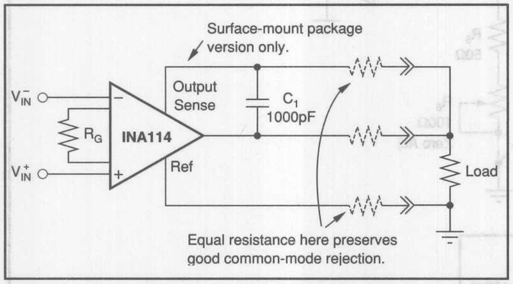


FIGURE 5. Remote Load and Ground Sensing.

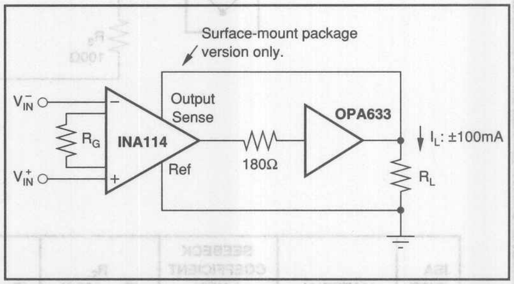


FIGURE 6. Buffered Output for Heavy Loads.

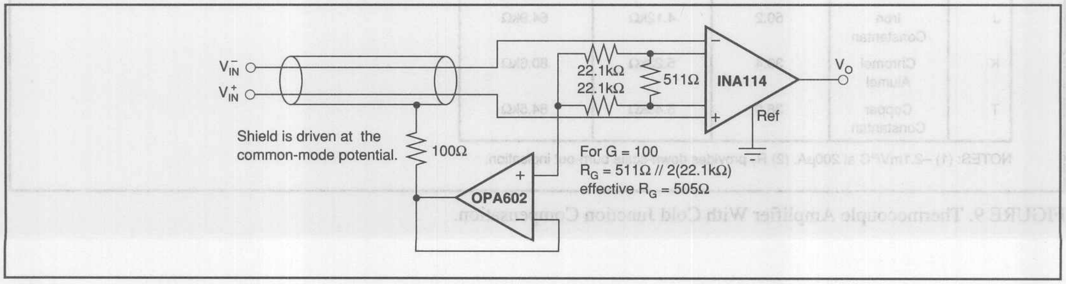


FIGURE 7. Shield Driver Circuit.

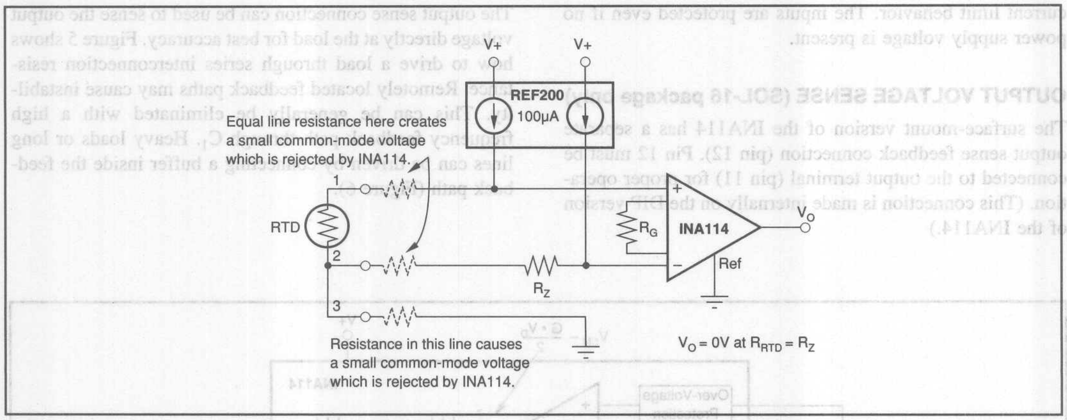
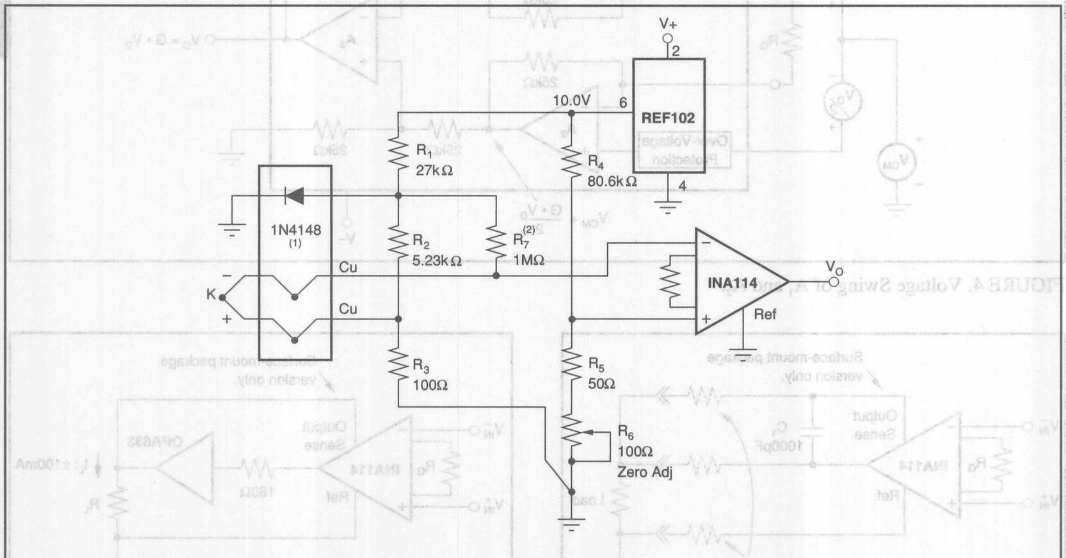


FIGURE 8. RTD Temperature Measurement Circuit.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

NOTES: (1) –2.1mV/°C at 200µA. (2) R_7 provides down-scale burn-out indication.

FIGURE 9. Thermocouple Amplifier With Cold Junction Compensation.

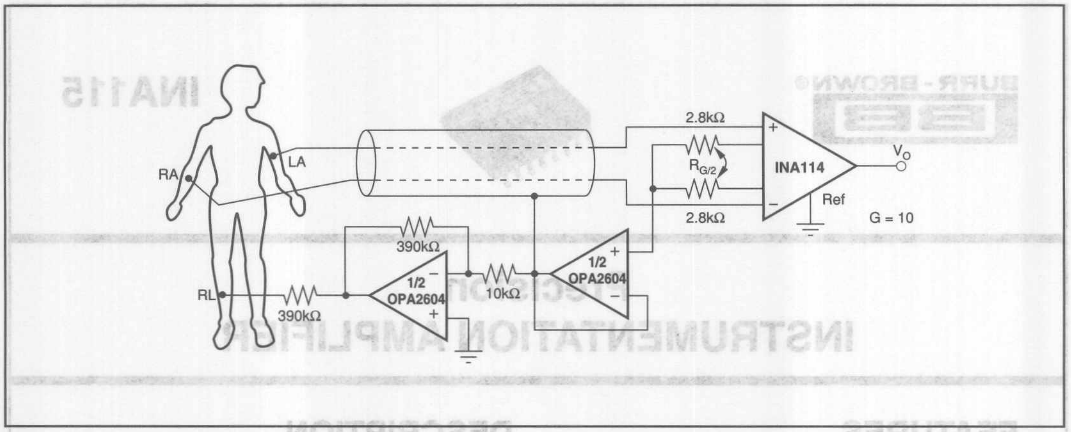


FIGURE 10. ECG Amplifier With Right-Leg Drive.

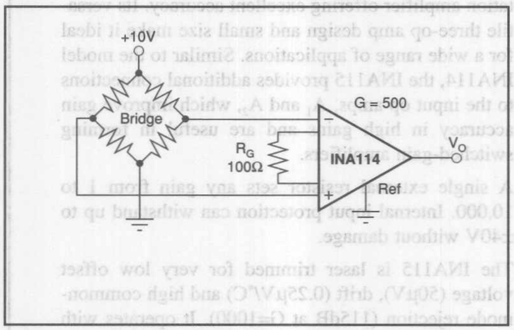


FIGURE 11. Bridge Transducer Amplifier.

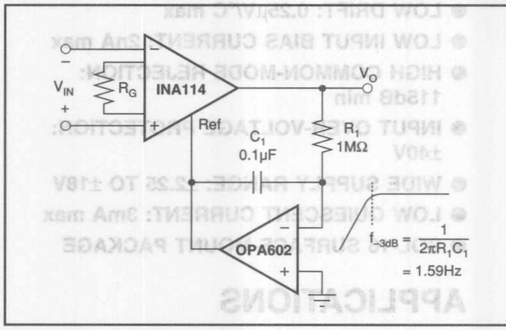
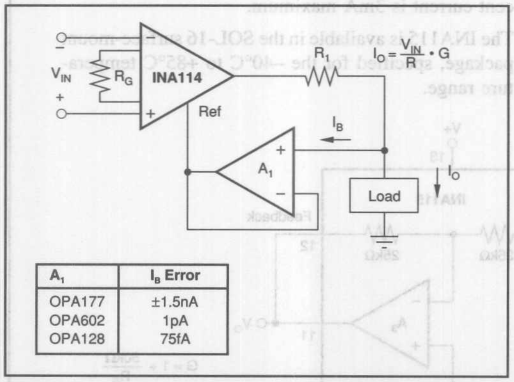


FIGURE 12. AC-Coupled Instrumentation Amplifier.

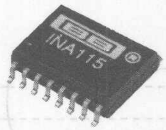


A_1	I_B Error
OPA177	±1.5nA
OPA602	1pA
OPA128	75fA

FIGURE 13. Differential Voltage-to-Current Converter.

BURR - BROWN®

INA115



Precision INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW DRIFT: 0.25µV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 115dB min
- INPUT OVER-VOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 TO ±18V
- LOW QUIESCENT CURRENT: 3mA max
- SOL-16 SURFACE-MOUNT PACKAGE

APPLICATIONS

- SWITCHED-GAIN AMPLIFIER
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

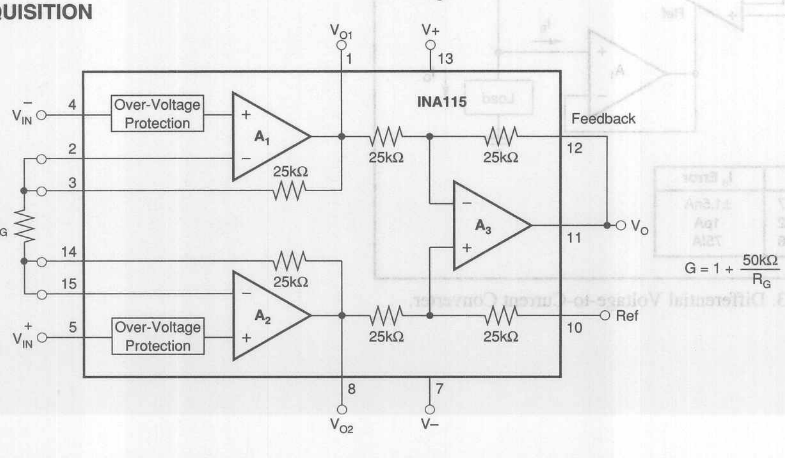
DESCRIPTION

The INA115 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile three-op amp design and small size make it ideal for a wide range of applications. Similar to the model INA114, the INA115 provides additional connections to the input op amps, A_1 and A_2, which improve gain accuracy in high gains and are useful in forming switched-gain amplifiers.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA115 is laser trimmed for very low offset voltage (50µV), drift (0.25µV/°C) and high common-mode rejection (115dB at G=1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA115 is available in the SOL-16 surface-mount package, specified for the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

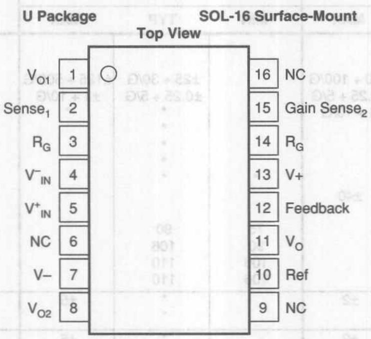
At $T_A = +25°C$, $V_S = ±15V$, $R_L = 2kΩ$ unless otherwise noted.

		INA115BU			INA115AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
Offset Voltage, RTI								
Initial	$T_A = +25°C$		±10 + 20/G	±50 + 100/G		±25 + 30/G	±125 + 500/G	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		±0.1 + 0.5/G	±0.25 + 5/G		±0.25 + 5/G	±1 + 10/G	µV/°C
vs Power Supply	$V_S = ±2.25V$ to ±18V		0.5 + 2/G	3 + 10/G		*	*	µV/V
Long-Term Stability			±0.2 + 0.5/G			*		µV/mo
Impedance, Differential			10^{10} || 6			*		Ω || pF
Common-Mode			10^{10} || 6			*		Ω || pF
Input Common-Mode Range		±11	±13.5		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	$V_{CM} = ±10V$, $ΔR_S = 1kΩ$							
	G = 1	80	96		75	90		dB
	G = 10	96	115		90	106		dB
	G = 100	110	120		106	110		dB
	G = 1000	115	120		106	110		dB
BIAS CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
OFFSET CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
NOISE VOLTAGE, RTI	G = 1000, $R_S = 0Ω$							
f = 10Hz			15			*		nV/√Hz
f = 100Hz			11			*		nV/√Hz
f = 1kHz			11			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.4			*		µVp-p
Noise Current								
f=10Hz			0.4			*		pA/√Hz
f=1kHz			0.2			*		pA/√Hz
f_B = 0.1Hz to 10Hz			18			*		pAp-p
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G = 1		±0.01	±0.05		*	*	%
	G = 10		±0.02	±0.4		*	±0.5	%
	G = 100		±0.05	±0.5		*	±0.7	%
	G = 1000		±0.5	±1		*	±2	%
Gain vs Temperature	G = 1		±2	±10		*	±10	ppm/°C
50kΩ Resistance(1)			±25	±100		*	*	ppm/°C
Nonlinearity	G = 1		±0.0001	±0.001		*	±0.002	% of FSR
	G = 10		±0.0005	±0.002		*	±0.004	% of FSR
	G = 100		±0.0005	±0.002		*	±0.004	% of FSR
	G = 1000		±0.002	±0.01		*	±0.02	% of FSR
OUTPUT(2)								
Voltage	$I_O = 5mA$, T_{MIN} to T_{MAX}	±13.5	±13.7		*	*		V
	$V_S = ±11.4V$, $R_L = 2kΩ$	±10	±10.5		*	*		V
	$V_S = ±2.25V$, $R_L = 2kΩ$	±1	±1.5		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+20/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		1			*		MHz
	G = 10		100			*		kHz
	G = 100		10			*		kHz
	G = 1000		1			*		kHz
Slew Rate	$V_O = ±10V$, G = 10	0.3	0.6		*	*		V/µs
Settling Time, 0.01%	G = 1		18			*		µs
	G = 10		20			*		µs
	G = 100		120			*		µs
	G = 1000		1100			*		µs
Overload Recovery	50% Overdrive		20			*		µs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current	$V_{IN} = 0V$		±2.2	±3		*	*	mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operating		–40		+125	*		*	°C
$θ_{JA}$			80			*		°C/W

* Specification same as INA115BU.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation. (2) Output specifications are for output amplifier, A_3. A_1 and A_2 provide the same output voltage swing but have less output current drive. A_1 and A_2 can drive external loads of 25kΩ || 200pF.

PIN CONFIGURATIONS

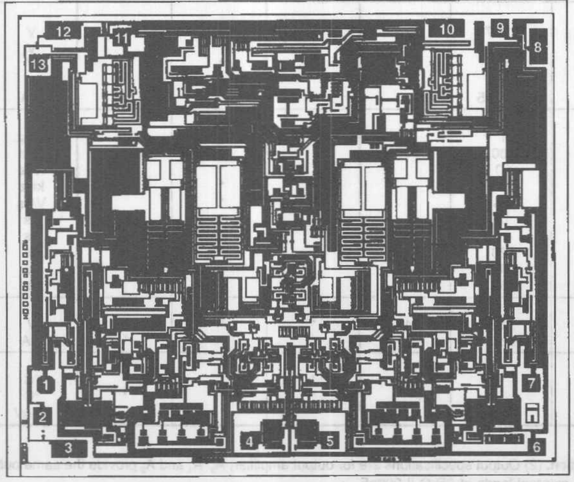


PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA115AU	SOL-16 Surface-Mount	211
INA115BU	SOL-16 Surface-Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

DICE INFORMATION



INA115 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	V_{O1}	8	Ref
2	Gain Sense$_1$	9	V_O
3	R_G	10	Feedback
4	V^-_{IN}	11	V+
5	V^+_{IN}	12	R_G
6	V–	13	Gain Sense$_2$
7	V_{O2}		

Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	141 x 120 ±5	3.58 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

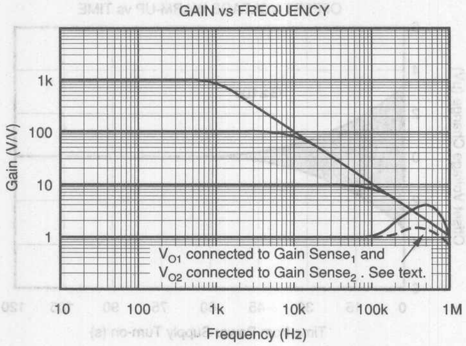
Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

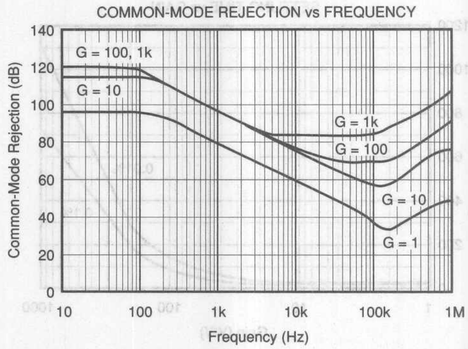
ORDERING INFORMATION

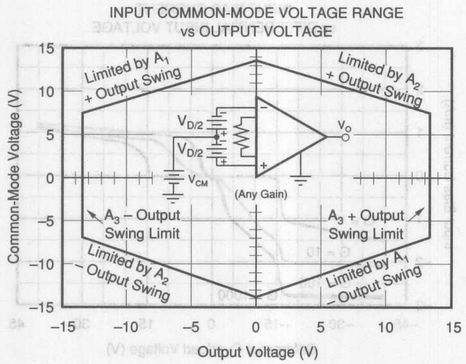
MODEL	PACKAGE	TEMPERATURE RANGE
INA115AU	SOL-16 Surface-Mount	–40°C to +85°C
INA115BU	SOL-16 Surface-Mount	–40°C to +85°C

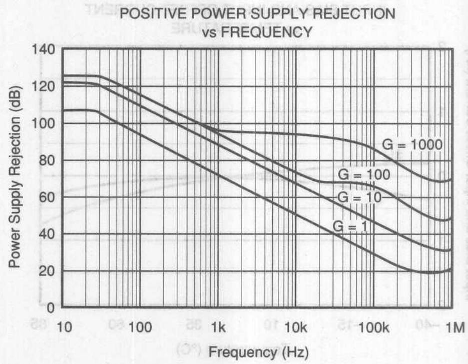
TYPICAL PERFORMANCE CURVES

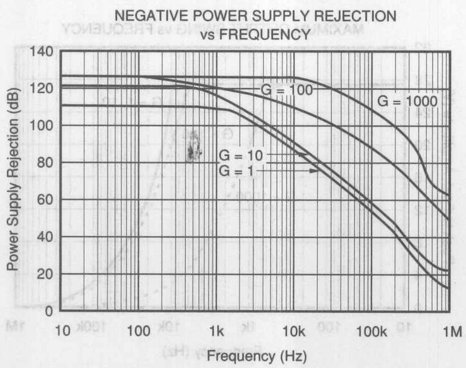
At $T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.

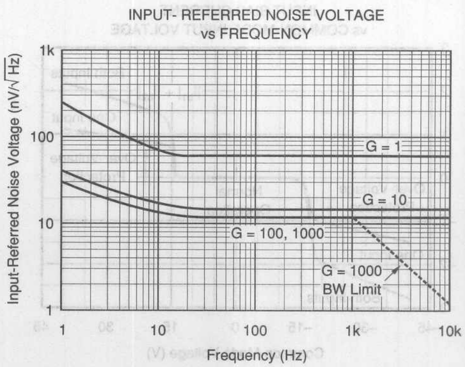


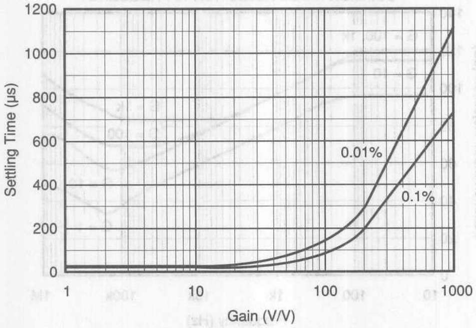




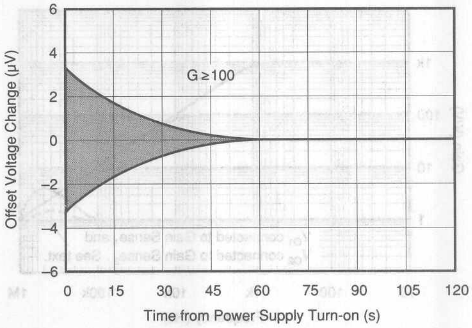




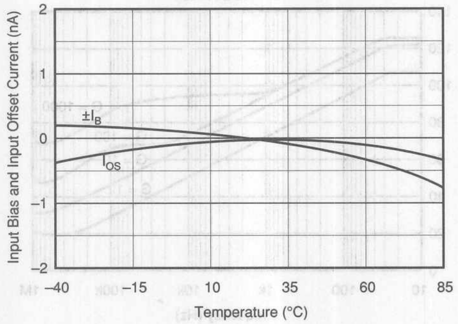




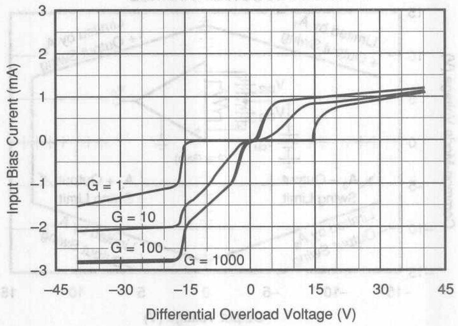
SETTLING TIME vs GAIN



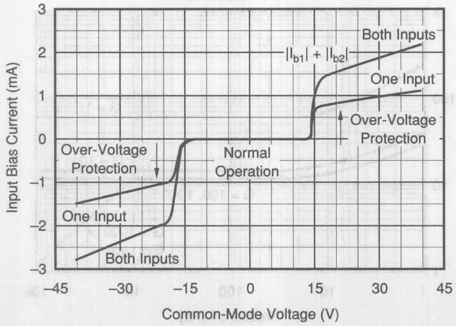
OFFSET VOLTAGE WARM-UP vs TIME



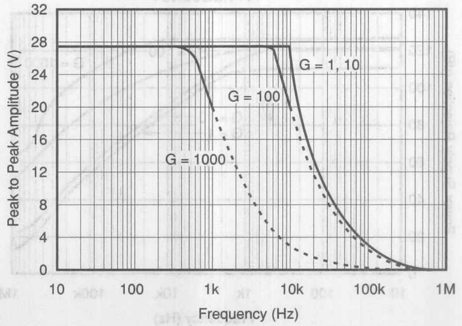
INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

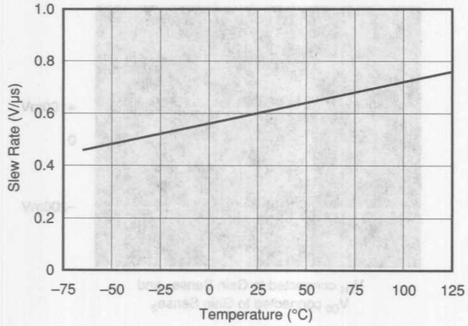


INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

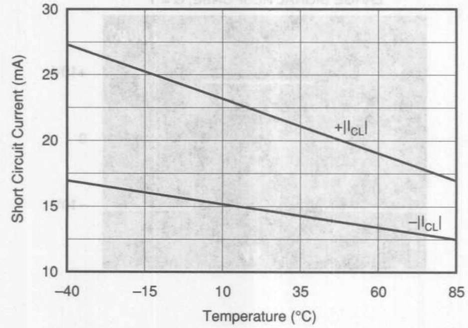


MAXIMUM OUTPUT SWING vs FREQUENCY

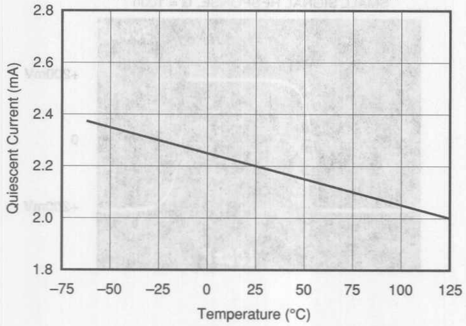
SLEW RATE vs TEMPERATURE



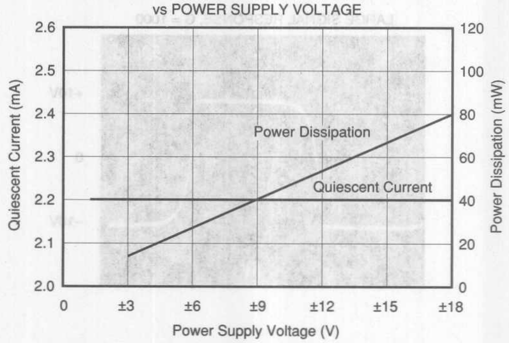
OUTPUT CURRENT LIMIT vs TEMPERATURE



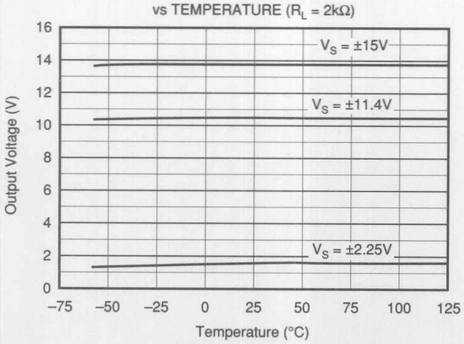
QUIESCENT CURRENT vs TEMPERATURE



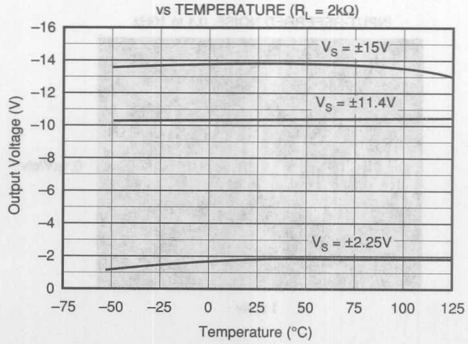
QUIESCENT CURRENT AND POWER DISSIPATION vs POWER SUPPLY VOLTAGE



POSITIVE SIGNAL SWING vs TEMPERATURE ($R_L = 2kΩ$)



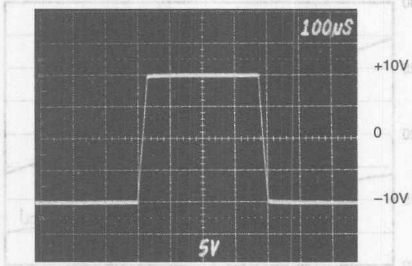
NEGATIVE SIGNAL SWING vs TEMPERATURE ($R_L = 2kΩ$)



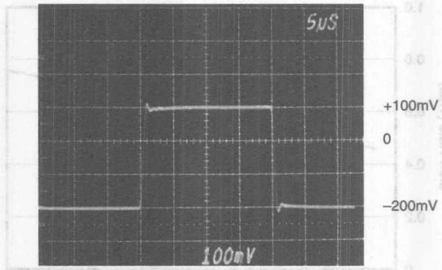
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.

LARGE SIGNAL RESPONSE, G = 1

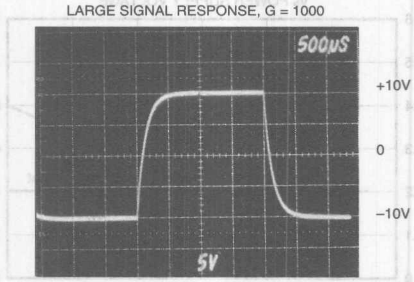


SMALL SIGNAL RESPONSE, G = 1

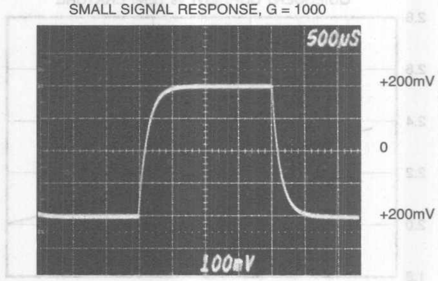


V_{O1} connected to Gain $Sense_1$ and V_{O2} connected to Gain $Sense_2$

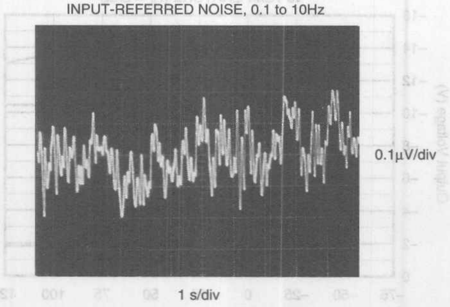
LARGE SIGNAL RESPONSE, G = 1000



SMALL SIGNAL RESPONSE, G = 1000



INPUT-REFERRED NOISE, 0.1 to 10Hz



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA115. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G=1).

The INA115 has a separate output sense feedback connection (pin 12). Pin 12 must be connected (normally to the output terminal, pin 11) for proper operation. The output sense connection can be used to sense the output voltage directly at the load for best accuracy.

SETTING THE GAIN

Gain of the INA115 is set by connecting a single external resistor, R_G:

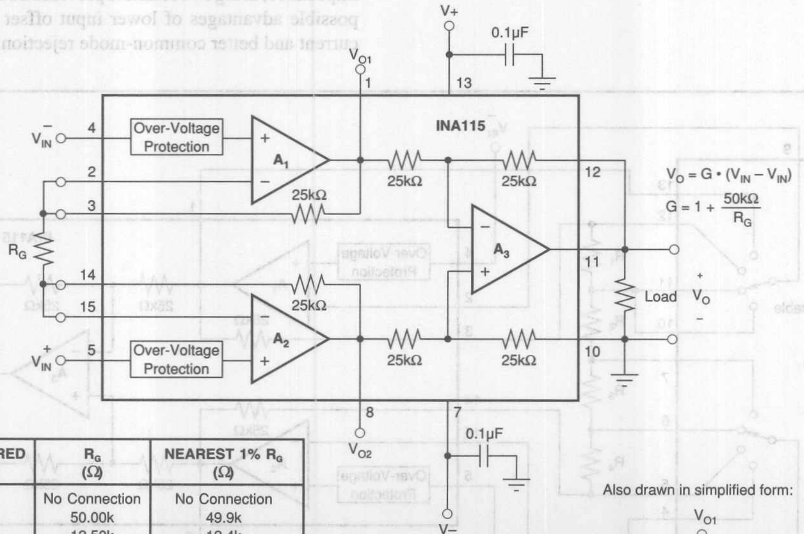
$$G = 1 + \frac{50\ \text{k}\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

For G=1, no resistor is required, but connect pins 2-3 and connect pins 14-15. Gain peaking in G=1 can be reduced by shorting the internal 25kΩ feedback resistors (see typical performance curve Gain vs Frequency). To do this, connect pins 1-2-3 and connect pins 8-14-15.

The 50kΩ term in equation 1 comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA115.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain error and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. The "force and sense" type connections illustrated in Figure 1 help reduce the effect of interconnection resistance.



DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	No Connection	No Connection
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

Also drawn in simplified form:

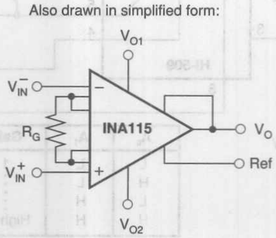


FIGURE 1. Basic Connections.

Multiplexer "on" resistance does not significantly affect gain. The resistor values required for some commonly used gain steps are shown. This circuit uses the internal 25kΩ feedback resistors, so the resistor values shown cannot be scaled to a different impedance level.

Figure 3 shows an alternative switchable gain configuration. This circuit does not use the internal 25kΩ feedback resistors, so the nominal values shown can be scaled to other impedance levels. This circuit is ideal for use with a precision resistor network to achieve excellent gain accuracy and lowest gain drift.

NOISE PERFORMANCE

The INA115 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

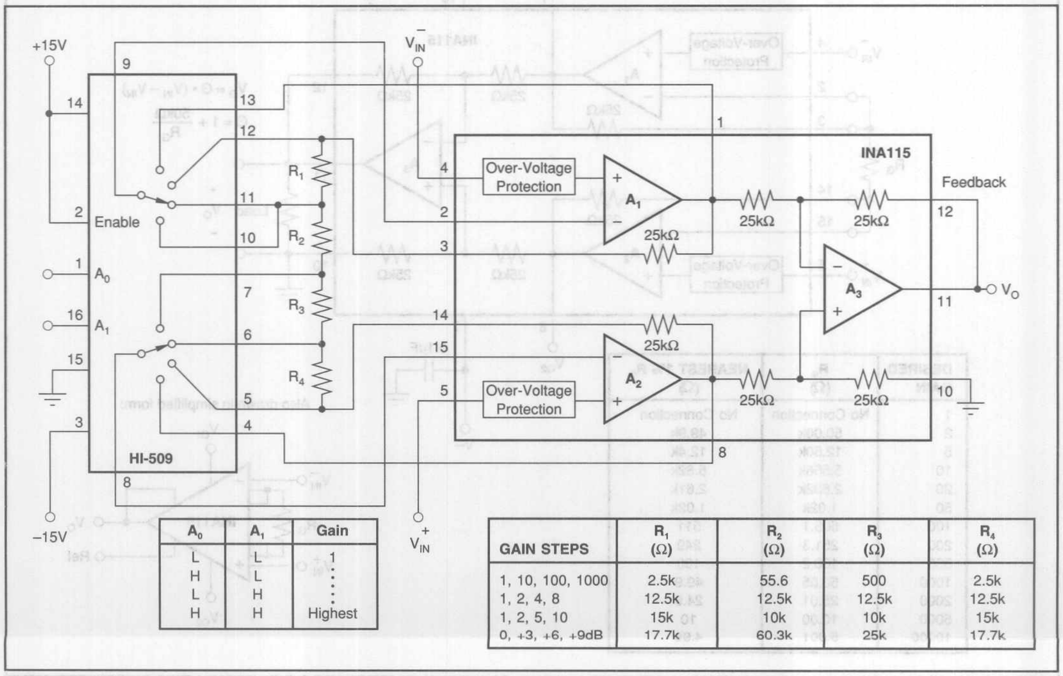
Low frequency noise of the INA115 is approximately 0.4μVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of "low noise" chopper-stabilized amplifiers.

drift. Most applications require no external offset adjustment. Figure 4 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering the trim voltage with an op amp as shown.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA115 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

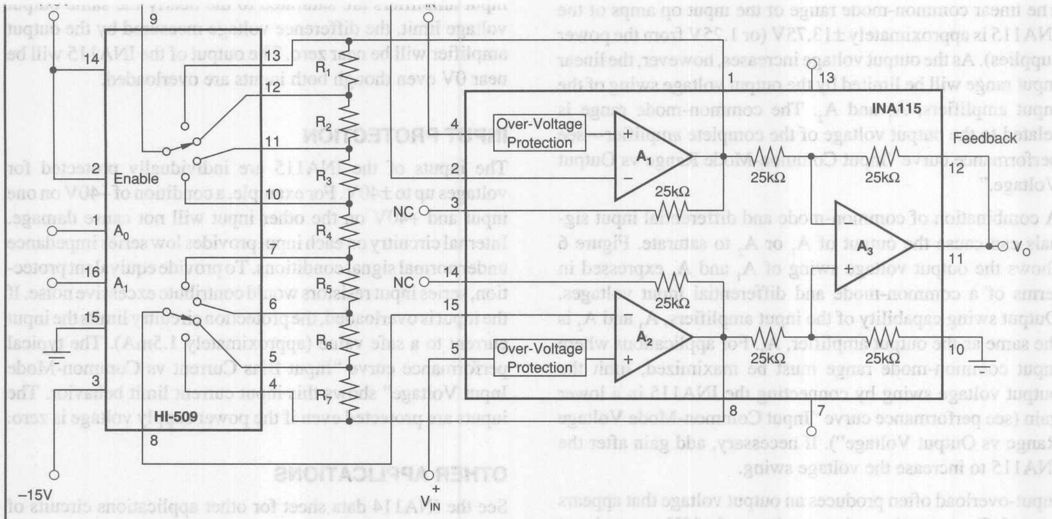
Input circuitry must provide a path for this input bias current if the INA115 is to operate properly. Figure 5 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA115 and the input amplifiers will saturate. If the differential source resistance is low, a bias current return path can be connected to one input (see thermocouple example in Figure 5). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due bias current and better common-mode rejection.



A_0	A_1	Gain
L	L	1
H	L	:
L	H	:
H	H	Highest

GAIN STEPS	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)
1, 10, 100, 1000	2.5k	55.6	500	2.5k
1, 2, 4, 8	12.5k	12.5k	12.5k	12.5k
1, 2, 5, 10	15k	10k	10k	15k
0, +3, +6, +9dB	17.7k	60.3k	25k	17.7k

FIGURE 2. Switched-Gain Instrumentation Amplifier (minimum components).



A_0	A_1	Gain
L	L	1
H	L	⋮
L	H	⋮
H	H	Highest

GAIN STEPS	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	R_5 (Ω)	R_6 (Ω)	R_7 (Ω)
1, 10, 100, 1000V/V	18k	1.8k	180	40	180	1.8k	18k
1, 2, 4, 8V/V	18k	9k	4.5k	9k	4.5k	9k	18k
1, 2, 5, 10V/V	18k	10.8k	3.6k	7.2k	3.6k	10.8k	18k
0, +3, +6, +9dB	18k	12.74k	9.02k	43.7k	9.02k	12.74k	18k

FIGURE 3. Switched-Gain Instrumentation Amplifier (improved gain drift).

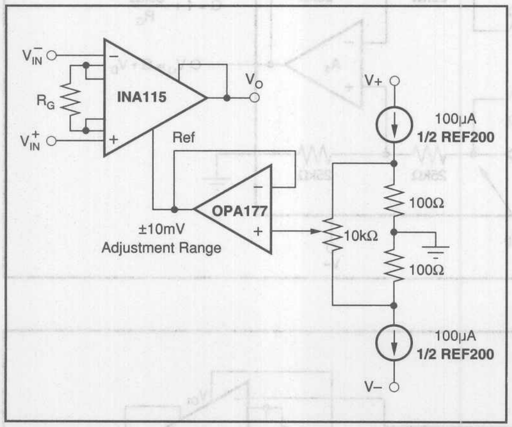


FIGURE 4. Optional Trimming of Output Offset Voltage.

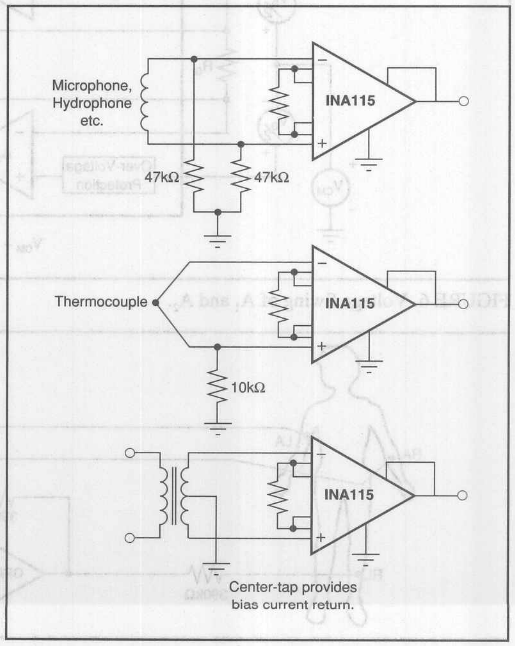


FIGURE 5. Providing an Input Common-Mode Current Path.

INSTRUMENTATION AMPLIFIERS

4

INA115

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA115 is approximately ±13.75V (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2. The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage."

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. Figure 6 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of the input amplifiers, A_1 and A_2 is the same as the output amplifier, A_3. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA115 in a lower gain (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the INA115 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA115 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA115 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if the power supply voltage is zero.

OTHER APPLICATIONS

See the INA114 data sheet for other applications circuits of general interest.

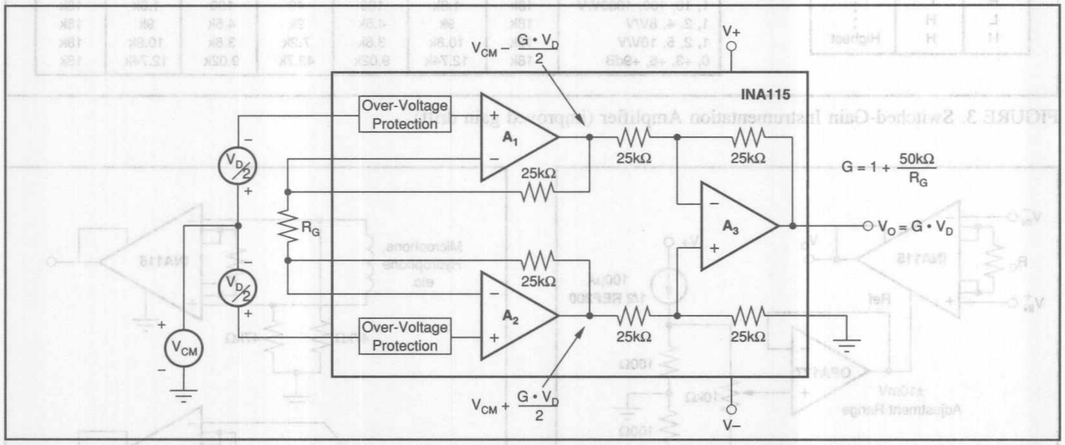


FIGURE 6. Voltage Swing of A_1 and A_2.

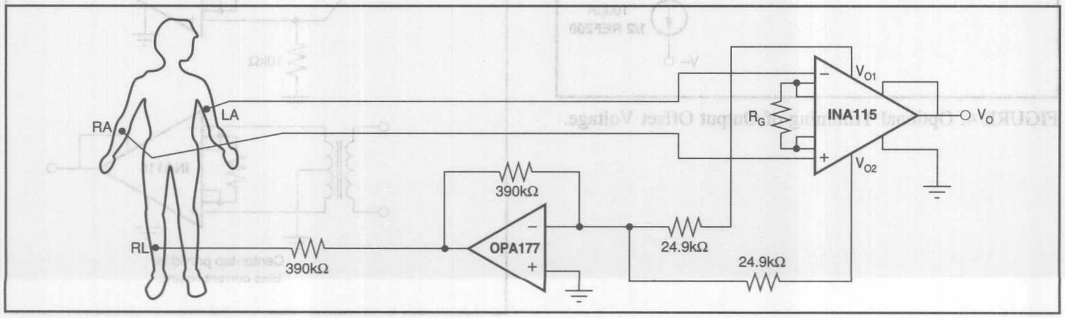
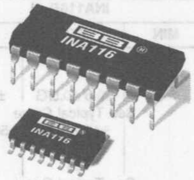


FIGURE 7. ECG Amplifier with Right Leg Drive.

BURR - BROWN®

INA116



Ultra Low Input Bias Current INSTRUMENTATION AMPLIFIER

FEATURES

- LOW INPUT BIAS CURRENT: 3fA typ
- BUFFERED GUARD DRIVE PINS
- LOW OFFSET VOLTAGE: 2mV max
- HIGH COMMON-MODE REJECTION: 84dB (G = 10)
- LOW QUIESCENT CURRENT: 1mA
- INPUT OVER-VOLTAGE PROTECTION: ±40V

APPLICATIONS

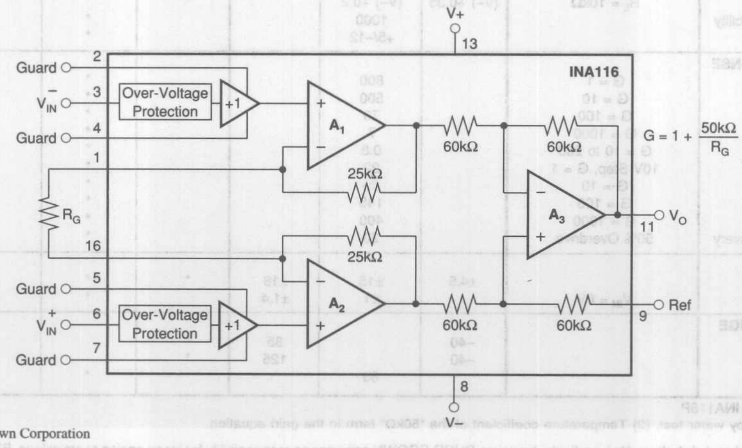
- LABORATORY INSTRUMENTATION
- pH MEASUREMENT
- ION–SPECIFIC PROBES
- LEAKAGE CURRENT MEASUREMENT

DESCRIPTION

The INA116 is a complete monolithic FET-input instrumentation amplifier with extremely low input bias current. ***Difet***® inputs and special guarding techniques yield input bias currents of 3fA at 25°C, and only 25fA at 85°C. Its 3-op amp topology allows gains to be set from 1 to 1000 by connecting a single external resistor.

Guard pins adjacent to both input connections can be used to drive circuit board and input cable guards to maintain extremely low input bias current.

The INA116 is available in 16-pin plastic DIP and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.



Difet®; Burr-Brown Corporation

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

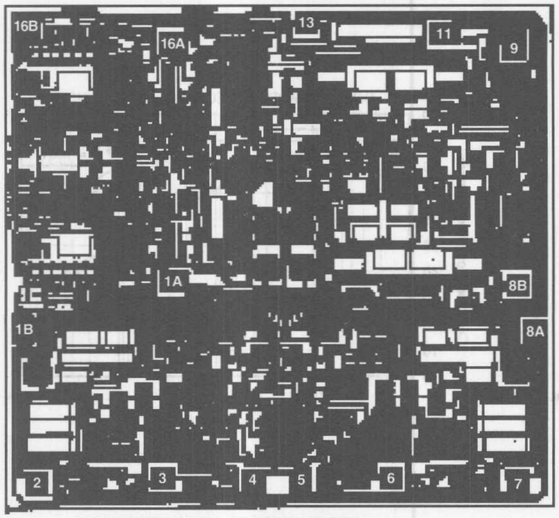
$T_A = +25°C$, $V_S = ±15V$, $R_L = 10kΩ$ unless otherwise noted.

PARAMETER	CONDITIONS	INA116P, U MIN	INA116P, U TYP	INA116P, U MAX	INA116PA, UA MIN	INA116PA, UA TYP	INA116PA, UA MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	$T_A = +25°C$		±0.5 ±0.5/G	±2 ±2/G		*	±5 ±5/G	mV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		See Typical Curve			*		
vs Power Supply	$V_S = ±4.5V$ to ±18V		±10 ±15/G	±50 ±100/G		*	±100 ±200/G	µV/V
Long-Term Stability			±1 ±5/G			*		µV/mo
Bias Current			±3	±25		*	±100	fA
vs Temperature			See Typical Curve			*		
Offset Current			±1	±25		*	±100	fA
vs Temperature			See Typical Curve			*		
Impedance, Differential			$>10^{15}/0.2$			*		Ω/pF
Common-Mode			$>10^{15}/7$			*		Ω/pF
Common-Mode Voltage Range		(V+)–4	(V+)–2		*	*		V
		(V–)+4	(V–)+2.4		*	*		V
Safe Input Voltage		±40			*			V
Common-Mode Rejection	$V_{CM} = ±11V$, $ΔR_S = 1kΩ$							
	G = 1	80	89		73	*		dB
	G = 10	84	92		78	*		dB
	G = 100	86	94		80	*		dB
	$V_{CM} = ±5V$, G = 1000	86	94		80	*		dB
NOISE								
Voltage Noise, RTI	G = 1000, $R_S = 0Ω$							
f = 1kHz			28			*		nV/√Hz
$f_B = 0.1Hz$ to 10Hz			2			*		µVp-p
Current Noise								
f = 1kHz			0.1			*		fA/√Hz
GAIN								
Gain Equation			$1+(50kΩ/R_G)$			*		V/V
Range of Gain		1		1000	*		*	V/V
Gain Error	G = 1		±0.01	±0.05		*	0.1	%
	G = 10		±0.25	±0.4		*	±0.5	%
	G = 100		±0.35	±0.5		*	±0.7	%
	G = 1000		±1.25			*		%
Gain vs Temperature(1)	G = 1		±5	±10		*	±20	ppm/°C
50kΩ Resistance(1)(2)			±25	±100		*	±100	ppm/°C
Nonlinearity	G = 1		±0.0005	±0.005		*	±0.01	% of FSR
	G = 10		±0.001	±0.005		*	±0.01	% of FSR
	G = 100		±0.001	±0.005		*	±0.01	% of FSR
	G = 1000		±0.005			*		% of FSR
GUARD OUTPUTS								
Offset Voltage			±15	±50		*	*	mV
Output Impedance			650			*		Ω
Current Drive			+2/–0.05			*		mA
OUTPUT								
Voltage Positive	$R_L = 10kΩ$	(V+) –1	(V+) –0.7		*	*		V
Negative	$R_L = 10kΩ$	(V–) +0.35	(V–) +0.2		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+5/–12			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		800			*		kHz
	G = 10		500			*		kHz
	G = 100		70			*		kHz
	G = 1000		7			*		kHz
Slew Rate	G = 10 to 200		0.8			*		V/µs
Settling Time, 0.01%	10V Step, G = 1		22			*		µs
	G = 10		25			*		µs
	G = 100		145			*		µs
	G = 1000		400			*		µs
Output Overload Recovery	50% Overdrive		20			*		µs
POWER SUPPLY								
Voltage Range		±4.5	±15	±18	*	*	*	V
Current	$V_{IN} = 0V$		±1	±1.4		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85		*	*	°C
Operating		–40		125	*		*	°C
$θ_{JA}$			80			*		°C/W

* Specification same as INA116P

NOTE: *(1) Guaranteed by wafer test. (2) Temperature coefficient of the "50kΩ" term in the gain equation.*

DICE INFORMATION



INA116 DIE TOPOGRAPHY

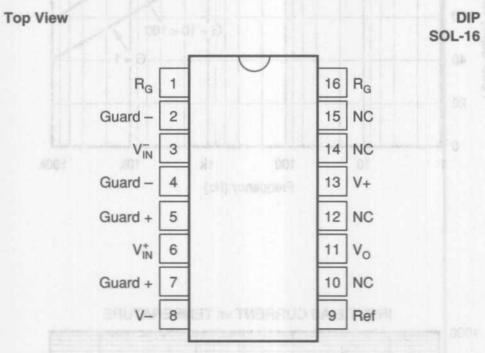
PAD	FUNCTION	PAD	FUNCTION
1A, 1B	R_G	9	Ref
2	Guard –	10	—
3	V_{IN}^-	11	V_O
4	Guard –	12	—
5	Guard +	13	V+
6	V_{IN}^+	14	—
7	Guard +	15	—
8A, 8B	V–	16A, 16B	R_G

Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	112 x 121 ±5	2.84 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATION



NC: No Internal Connection.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION

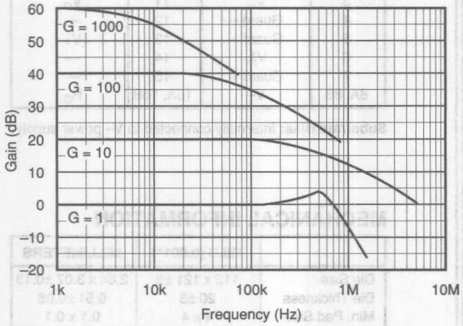
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
INA116PA	16-Pin Plastic DIP	180
INA116P	16-Pin Plastic DIP	180
INA116UA	SOL-16 Surface-Mount	211
INA116U	SOL-16 Surface-Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

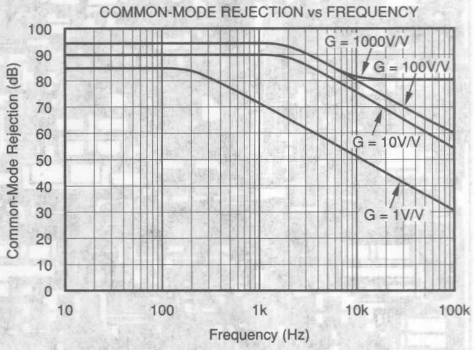
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = ±15V$, $R_L = 10kΩ$ unless otherwise noted.

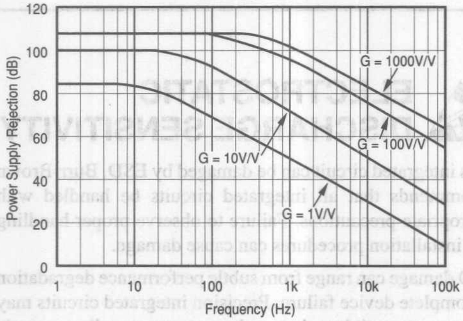
GAIN vs FREQUENCY



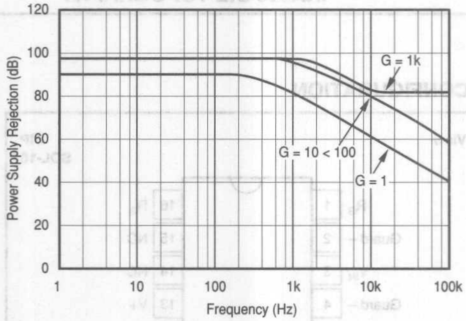
COMMON-MODE REJECTION vs FREQUENCY



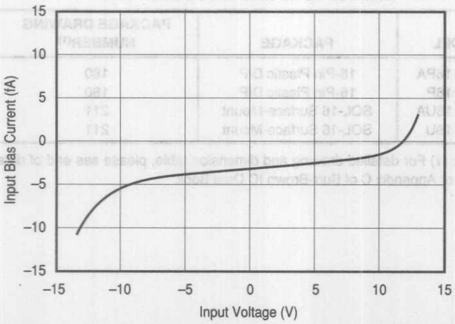
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



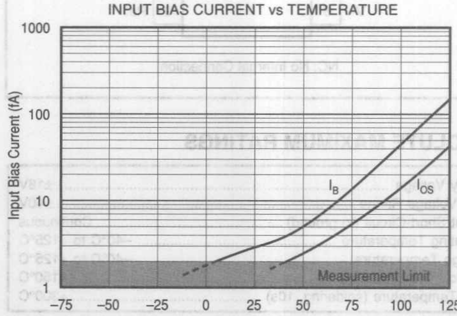
NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



INPUT BIAS CURRENT vs INPUT VOLTAGE

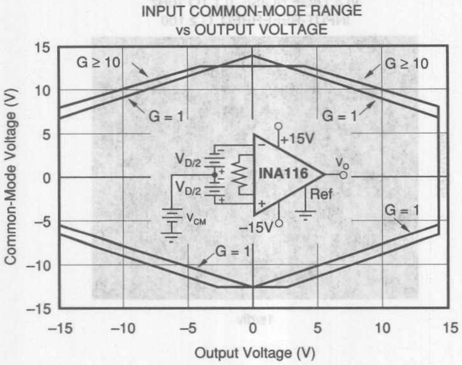


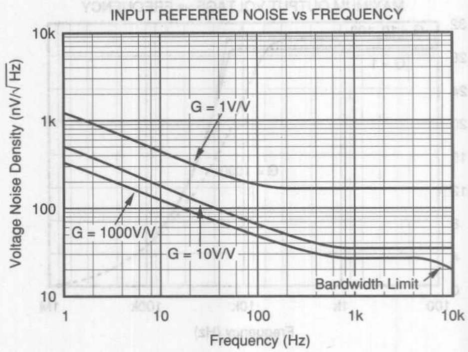
INPUT BIAS CURRENT vs TEMPERATURE

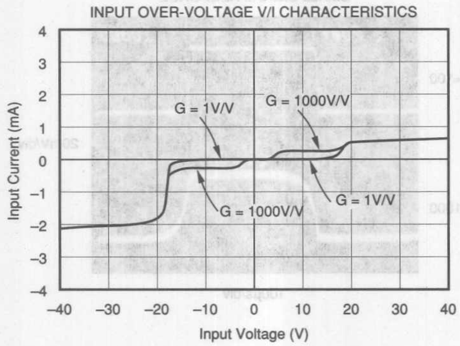


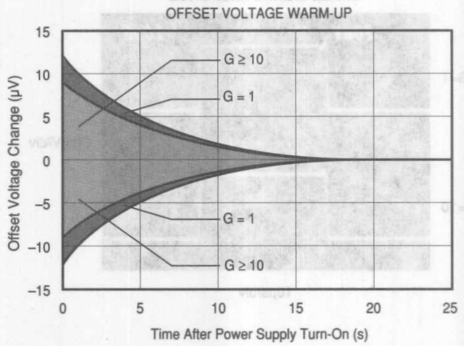
TYPICAL PERFORMANCE CURVES (CONT)

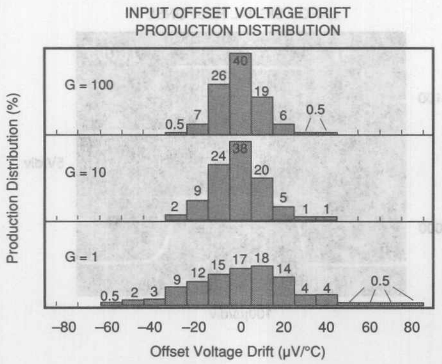
$T_A = +25°C$, $V_S = \pm15V$, $R_L = 10k\Omega$ unless otherwise noted.

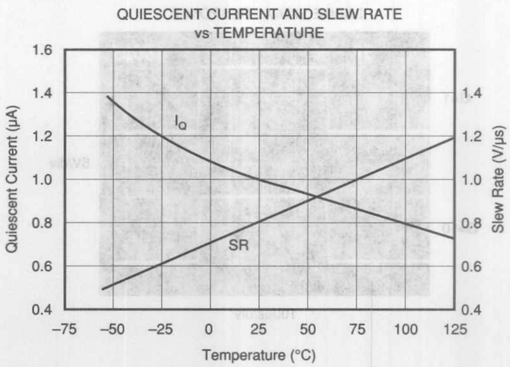






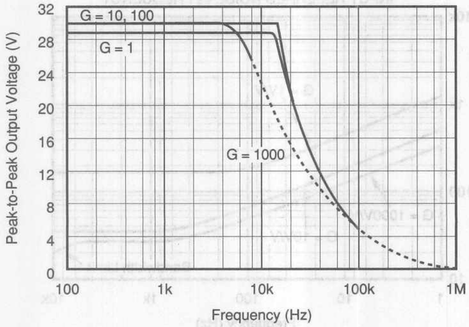




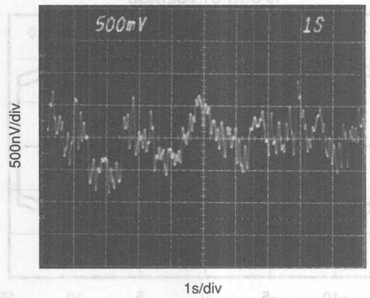


$T_A = +25°C$, $V_S = \pm15V$, $R_L = 10k\Omega$ unless otherwise noted.

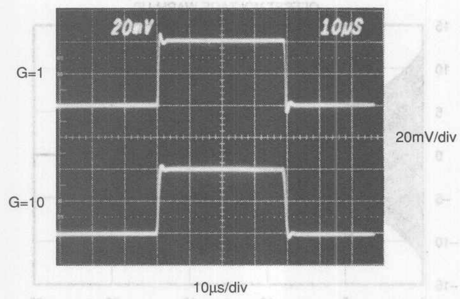
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



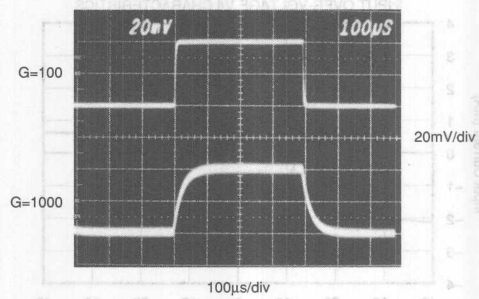
VOLTAGE NOISE, 0.1 TO 10Hz
INPUT-REFERRED, G ≥ 100



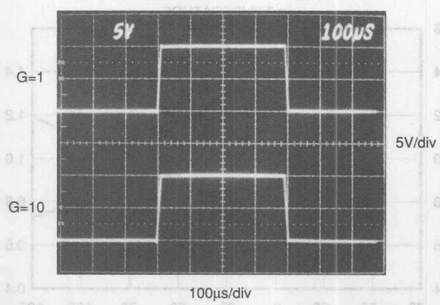
SMALL SIGNAL RESPONSE



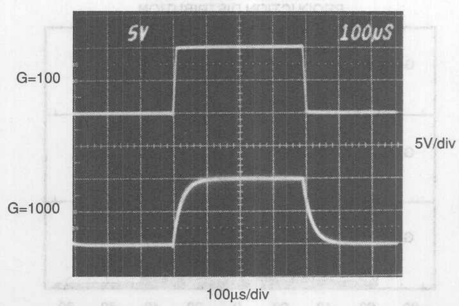
SMALL SIGNAL RESPONSE



LARGE SIGNAL RESPONSE



LARGE SIGNAL RESPONSE



APPLICATIONS INFORMATION

Figure 1 shows the connections required for basic operation of the INA116. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the supply pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low impedance connection to assure good common-mode rejection. A resistance of 30Ω in series with this connection will cause a typical device to degrade to approximately 72dB CMR at G = 1.

SETTING THE GAIN

Gain of the INA116 is set by connecting a single external resistor, R_G, as shown. The gain is—

$$G = 1 + \frac{50k\Omega}{R_G} \qquad (1)$$

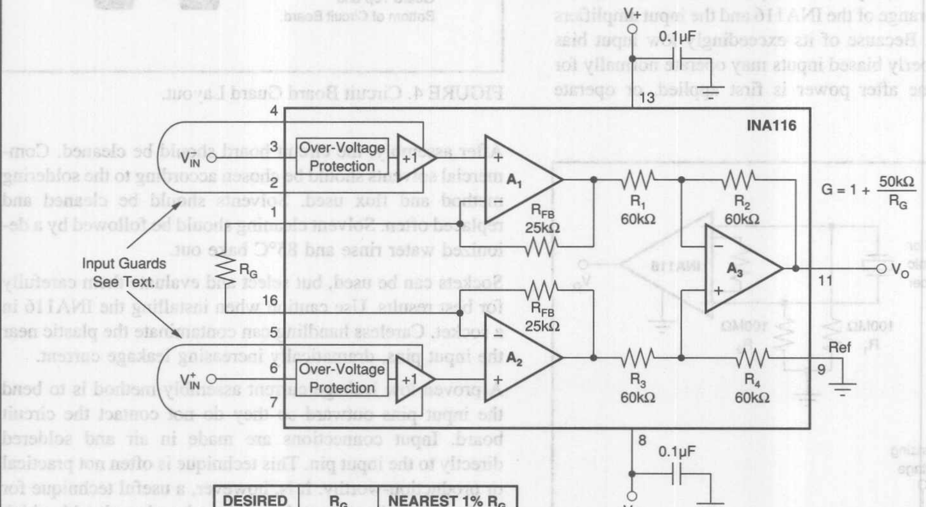
Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in equation 1 is the sum of the two feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA116.

The stability and temperature drift of R_G also affect gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain make wiring resistance important. Sockets add to the wiring resistance that will contribute additional gain error in gains of approximately 100 or greater.

OFFSET TRIMMING

The INA116 is laser trimmed for low offset voltage and offset voltage drift; most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. A voltage applied to the Ref terminal is summed at the output. Op amp A_1 provides a low source impedance for the Ref terminal, assuring good common-mode rejection.



DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.

Also drawn in simplified form:

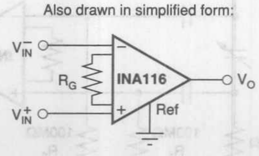


FIGURE 1. Basic Connections.

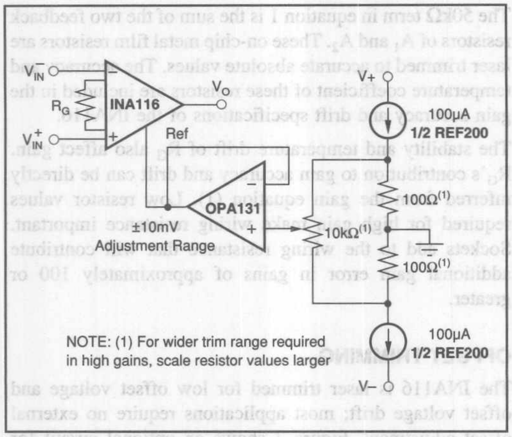


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

Input circuitry must provide an input bias current path for proper operation. Figure 3 shows resistors R_1 and R_2 to provide an input current path. Without these resistors, the inputs would eventually float to a potential that exceeds the common-mode range of the INA116 and the input amplifiers would saturate. Because of its exceedingly low input bias current, improperly biased inputs may operate normally for a period of time after power is first applied, or operate intermittently.

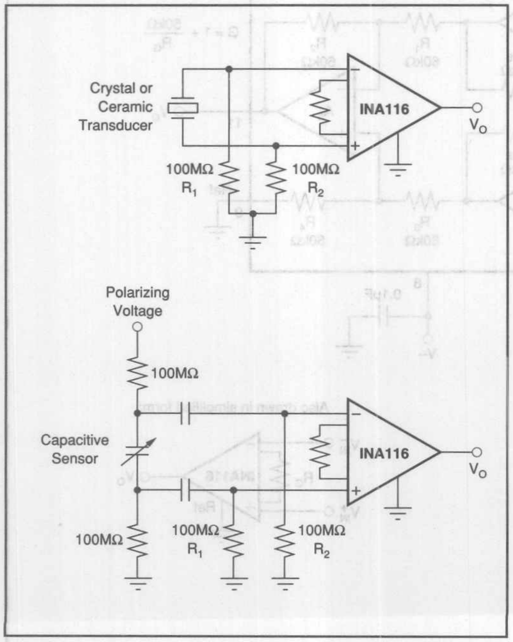


FIGURE 3. Providing An Input Bias Current Path.

CIRCUIT BOARD LAYOUT AND ASSEMBLY

Careful circuit board layout and assembly techniques are required to achieve the exceptionally low input bias current performance of the INA116. Guard terminals adjacent to both inputs make it easy to properly guard the critical input terminal layout. Since traces are not required to run between device pins, this layout is easily accomplished, even with the surface mount package. The guards should completely encircle their respective input connections—see Figure 4. Both sides of the circuit board should be guarded, even if only one side has an input terminal conductor. Route any time-varying signals away from the input terminals. Solder mask should not cover the input and guard traces since this can increase leakage.

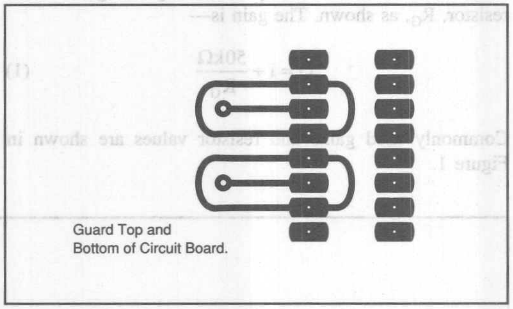


FIGURE 4. Circuit Board Guard Layout.

After assembly, the circuit board should be cleaned. Commercial solvents should be chosen according to the soldering method and flux used. Solvents should be cleaned and replaced often. Solvent cleaning should be followed by a de-ionized water rinse and 85°C bake out.

Sockets can be used, but select and evaluate them carefully for best results. Use caution when installing the INA116 in a socket. Careless handling can contaminate the plastic near the input pins, dramatically increasing leakage current.

A proven low leakage current assembly method is to bend the input pins outward so they do not contact the circuit board. Input connections are made in air and soldered directly to the input pin. This technique is often not practical or production-worthy. It is, however, a useful technique for evaluation and testing and provides a benchmark with which to compare other wiring techniques. The circuit board guarding techniques discussed normally reduce leakage to acceptable levels.

A solid mechanical assembly is required for good results. Nearby plastic parts can be especially troublesome since a static charge can develop and the slightest motion or vibration will couple charge to the inputs. Place a Faraday shield around the whole amplifier and input connection assembly to eliminate stray fields.

INPUT CONNECTIONS

Some applications must make high impedance input connections to external sensors or input connectors. To assure low leakage, the input should be guarded all the way to the signal source—see Figure 5. Coaxial cable can be used with the shield driven by the guard. A separate connection is required to provide a ground reference at the signal source. Triaxial cable may reduce noise pickup and provides the ground reference at the source. Drive the inner shield at guard potential and ground the outer shield. Two separate guarded lines are required if both the inverting and non-inverting inputs are brought to the source.

The guard drive output current is limited to approximately +2mA/–50µA. For slow input signals the internal guard output can directly drive a cable shield. With fast input signals, however, the guard may not provide sufficient output current to rapidly charge the cable capacitance. An op amp buffer may be required as shown in Figure 6.

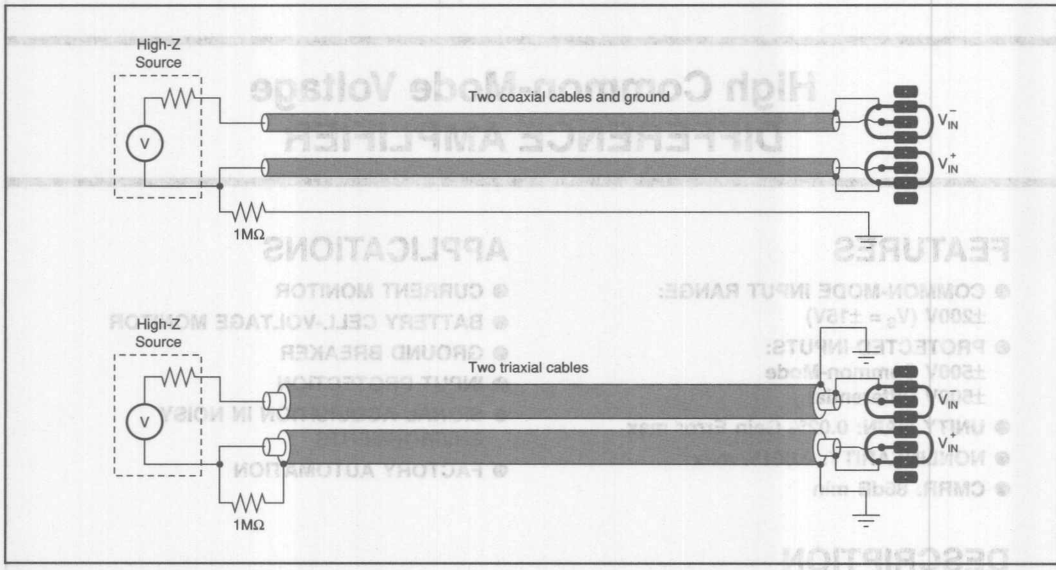


FIGURE 5. Input Cable Guarding Circuits.

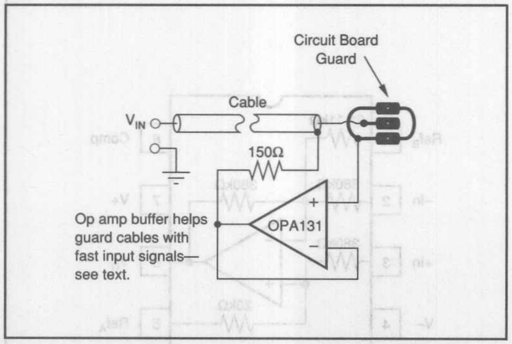


FIGURE 6. Buffered Guard Drive.

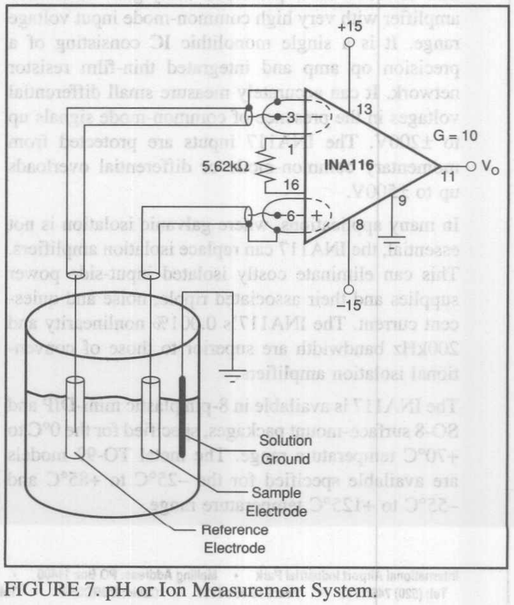


FIGURE 7. pH or Ion Measurement System.

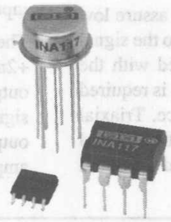
INA116

4

INSTRUMENTATION AMPLIFIERS

BURR - BROWN®

INA117



High Common-Mode Voltage DIFFERENCE AMPLIFIER

FEATURES

- **COMMON-MODE INPUT RANGE: ±200V (V_S = ±15V)**
- **PROTECTED INPUTS: ±500V Common-Mode ±500V Differential**
- **UNITY GAIN: 0.02% Gain Error max**
- **NONLINEARITY: 0.001% max**
- **CMRR: 86dB min**

APPLICATIONS

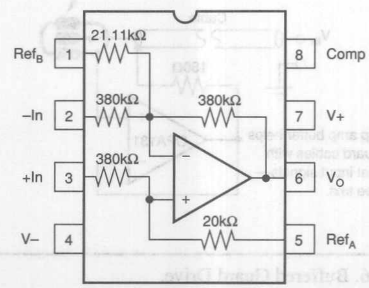
- **CURRENT MONITOR**
- **BATTERY CELL-VOLTAGE MONITOR**
- **GROUND BREAKER**
- **INPUT PROTECTION**
- **SIGNAL ACQUISITION IN NOISY ENVIRONMENTS**
- **FACTORY AUTOMATION**

DESCRIPTION

The INA117 is a precision unity-gain difference amplifier with very high common-mode input voltage range. It is a single monolithic IC consisting of a precision op amp and integrated thin-film resistor network. It can accurately measure small differential voltages in the presence of common-mode signals up to ±200V. The INA117 inputs are protected from momentary common-mode or differential overloads up to ±500V.

In many applications, where galvanic isolation is not essential, the INA117 can replace isolation amplifiers. This can eliminate costly isolated input-side power supplies and their associated ripple, noise and quiescent current. The INA117's 0.001% nonlinearity and 200kHz bandwidth are superior to those of conventional isolation amplifiers.

The INA117 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the 0°C to +70°C temperature range. The metal TO-99 models are available specified for the –25°C to +85°C and –55°C to +125°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

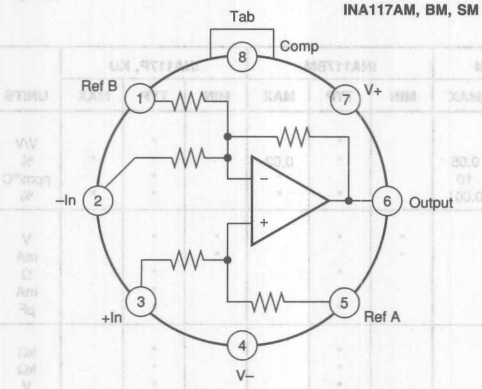
At T_A = +25°C, V_S = ±15V unless otherwise noted.

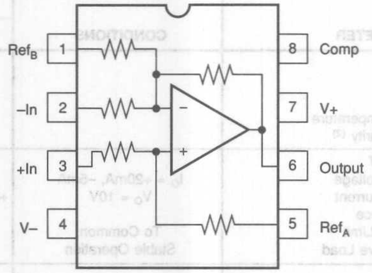
PARAMETER	CONDITIONS	INA117AM, SM			INA117BM			INA117P, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Initial (1)			1			*			*		V/V
Error			0.01	0.05		*	0.02		*	*	%
vs Temperature			2	10			*		*		ppm/°C
Nonlinearity (2)			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, –5mA	10	12		*	*		*	*		V
Rated Current	V_O = 10V	+20, –5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To Common		+49, –13			*			*		mA
Capacitive Load	Stable Operation		1000			*			*		pF
INPUT											
Impedance	Differential		800			*			*		kΩ
	Common-Mode		400			*			*		kΩ
Voltage Range	Differential	±10				*			*		V
	Common-Mode, Continuous	±200			*			*			V
Common-Mode Rejection (3)											
DC		70	80		86	94		*	*		dB
AC, 60Hz	V_{CM} = 400Vp-p	66	80		66	94		*	*		dB
vs Temperature, DC	$T_A = T_{MIN}$ to T_{MAX}										
AM, BM, P, KU		66	75		80	90			*		dB
SM		60	75								dB
OFFSET VOLTAGE	RTO (4)										
Initial			120	1000		*	1000		*	*	µV
KU Grade (SO-8 Package)									600	2000	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		8.5	40		*	20		*		µV/°C
vs Supply	V_S = ±5V to ±18V	74	90		80	*		*	*		dB
vs Time			200			*			*		µV/mo
OUTPUT NOISE VOLTAGE	RTO (5)										
f_B = 0.01Hz to 10Hz			25			*			*		µVp-p
f_B = 10kHz			550			*			*		$nV/\sqrt{Hz}$
DYNAMIC RESPONSE											
Gain Bandwidth, –3dB			200			*			*		kHz
Full Power Bandwidth	V_O = 20Vp-p	30			*			*			kHz
Slew Rate		2	2.6		*	*		*	*		V/µs
Settling Time: 0.1%	V_O = 10V Step		6.5			*			*		µs
0.01%	V_O = 10V Step		10			*			*		µs
0.01%	V_{CM} = 10V Step, V_{DIFF} = 0V		4.5			*			*		µs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated Performance	±5		±18	*		*	*		*	V
Quiescent Current	V_O = 0V		1.5	2		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: AM, BM, P, KU		–25		+85	*		*	0		+70	°C
SM		–55		+125							°C
Operation		–55		+125	*		*	–25		+85	°C
Storage		–65		+150	*		*	–40		+85	°C

*Specification same as for INA117AM.

NOTES: (1) Connected as difference amplifier (see Figure 1). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see discussion of common-mode rejection in Application Information section). (4) Includes effects of amplifier's input bias and offset currents. (5) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Input Voltage Range, Continuous	±200V
Common-Mode and Differential, 10s	±500V
Operating Temperature	
M Metal TO-99	–55 to +125°C
P Plastic DIP and U SO-8	–40 to +85°C
Storage Temperature	
M Package	–65 to +150°C
P Plastic DIP and U SO-8	–40 to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common	Continuous

PACKAGE INFORMATION

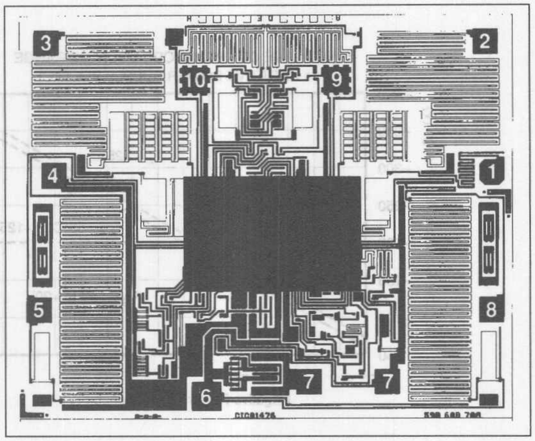
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA117P	8-Pin Plastic DIP	006
INA117KU	SO-8 Surface Mount	182
INA117AM	TO-99 Metal	001
INA117BM	TO-99 Metal	001
INA117SM	TO-99 Metal	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA117P	8-Pin Plastic DIP	0°C to +70°C
INA117KU	SO-8 Surface-Mount	0°C to +70°C
INA117AM	TO-99 Metal	–25°C to +85°C
INA117BM	TO-99 Metal	–25°C to +85°C
INA117SM	TO-99 Metal	–55°C to +125°C

DICE INFORMATION



INA117 DIE TOPOGRAPHY

PAD	FUNCTION
1	Ref B
2	−In
3	+In
4	V−
5	Ref A
6	Output
7	V+ (connect both pads)
8	Comp
9	(Op Amp −In)
10	(Op Amp +In)

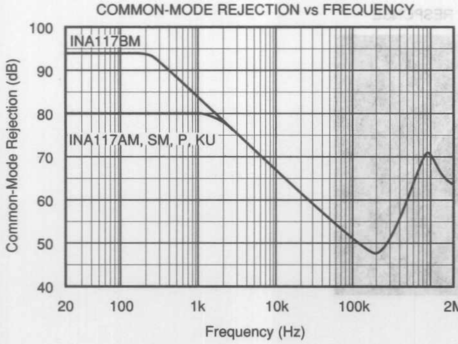
Substrate Bias: Electrically connected to −V supply.

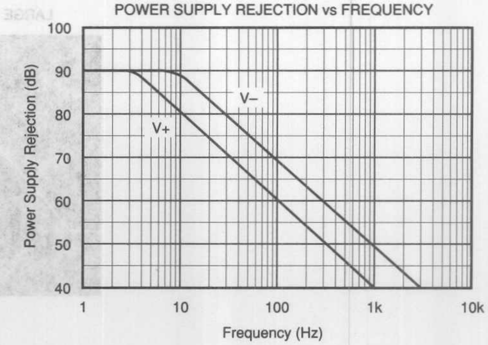
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	85 x 103 ±5	2.16 x 2.62 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.01 x 0.01
Backing		Gold

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V, unless otherwise noted.





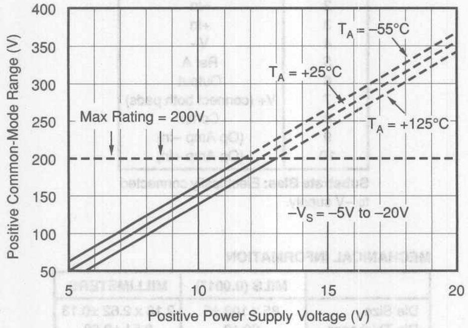
INA117

4

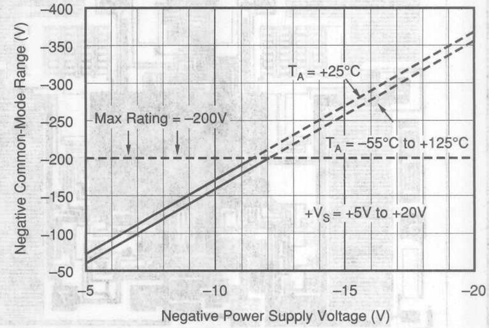
INSTRUMENTATION AMPLIFIERS

T_A = +25°C, V_S = ±15V unless otherwise noted.

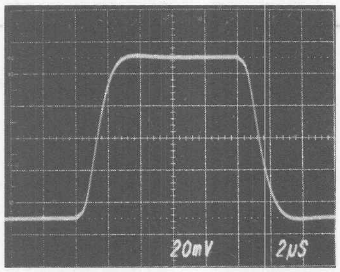
POSITIVE COMMON-MODE VOLTAGE RANGE vs POSITIVE POWER SUPPLY VOLTAGE



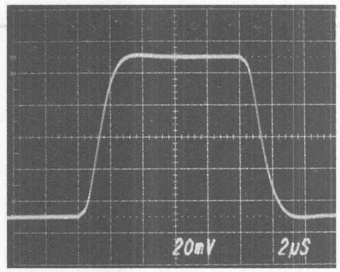
NEGATIVE COMMON-MODE VOLTAGE RANGE vs NEGATIVE POWER SUPPLY VOLTAGE



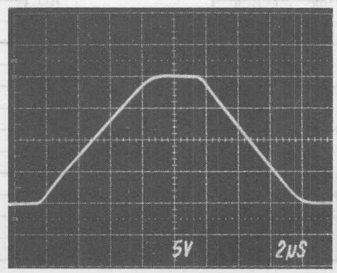
SMALL SIGNAL STEP RESPONSE $C_L = 0$



SMALL SIGNAL STEP RESPONSE C_L = 1000pF



LARGE SIGNAL STEP RESPONSE



Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins.

The output voltage is equal to the differential input voltage between pins 2 and 3. The common mode input voltage is rejected.

Internal circuitry connected to the compensation pin 8 cancels the parasitic distributed capacitance between the feedback resistor, R_2, and the IC substrate. For specified dynamic performance, pin 8 should be grounded or connected through a 0.1µF capacitor to an AC ground such as V+.

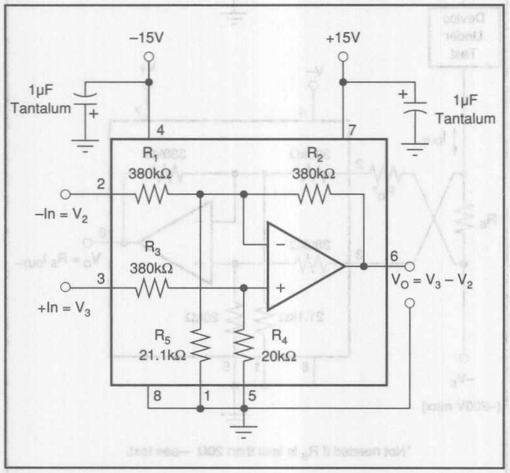


FIGURE 1. Basic Power and Signal Connections.

COMMON-MODE REJECTION

Common-mode rejection (CMR) of the INA117 is dependent on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, it is important to have low source impedances driving the two inputs. A 75Ω resistance in series with pin 2 or 3 will decrease CMR from 86dB to 72dB.

Resistance in series with the reference pins will also degrade CMR. A 4Ω resistance in series with pin 1 or 5 will decrease CMRR from 86dB to 72dB.

Most applications do not require trimming. Figures 2 and 3 show optional circuits that may be used for trimming offset voltage and common-mode rejection.

TRANSFER FUNCTION

Most applications use the INA117 as a simple unity-gain difference amplifier. The transfer function is:

$$V_O = V_3 - V_2$$

V_3 and V_2 are the voltages at pins 3 and 2.

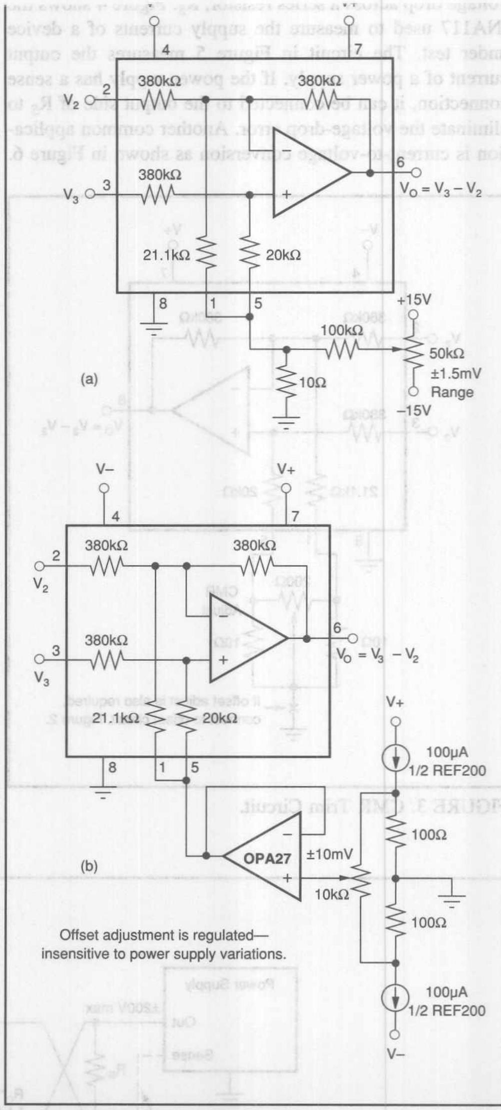


FIGURE 2. Offset Voltage Trim Circuits.

Some applications, however, apply voltages to the reference terminals (pins 1 and 5). A more complete transfer function is:

$$V_O = V_3 - V_2 + 19 \cdot V_5 - 18 \cdot V_1$$

V_5 and V_1 are the voltages at pins 5 and 1.

MEASURING CURRENT

The INA117 can be used to measure a current by sensing the voltage drop across a series resistor, R_S. Figure 4 shows the INA117 used to measure the supply currents of a device under test. The circuit in Figure 5 measures the output current of a power supply. If the power supply has a sense connection, it can be connected to the output side of R_S to eliminate the voltage-drop error. Another common application is current-to-voltage conversion as shown in Figure 6.

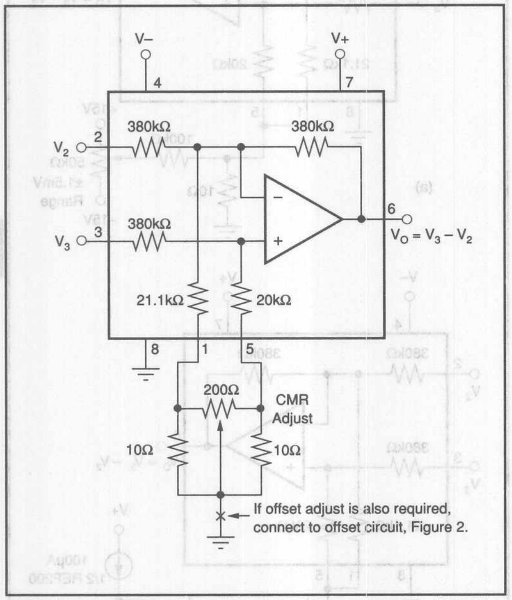


FIGURE 3. CMR Trim Circuit.

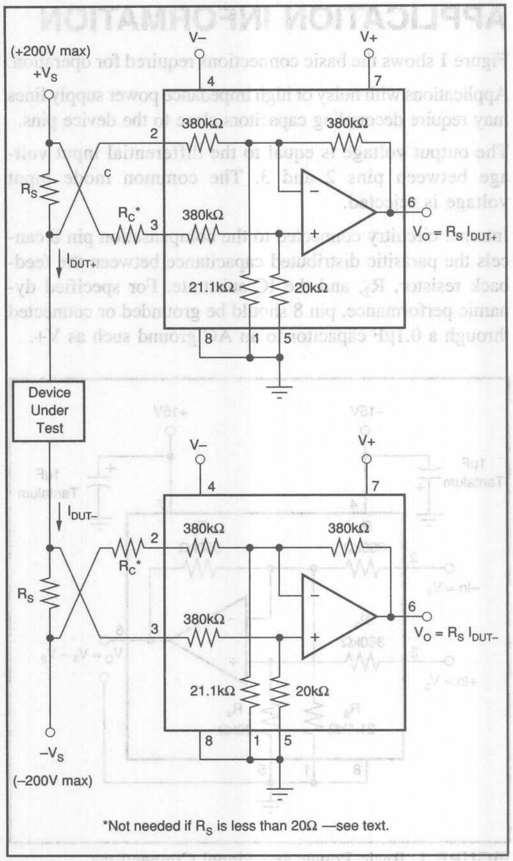


FIGURE 4. Measuring Supply Currents of Device Under Test.

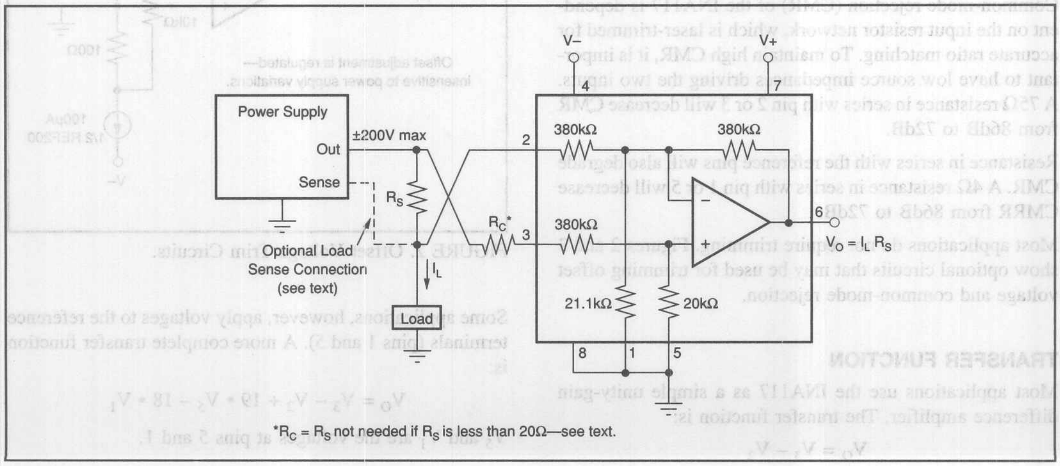


FIGURE 5. Measuring Power Supply Output Current.

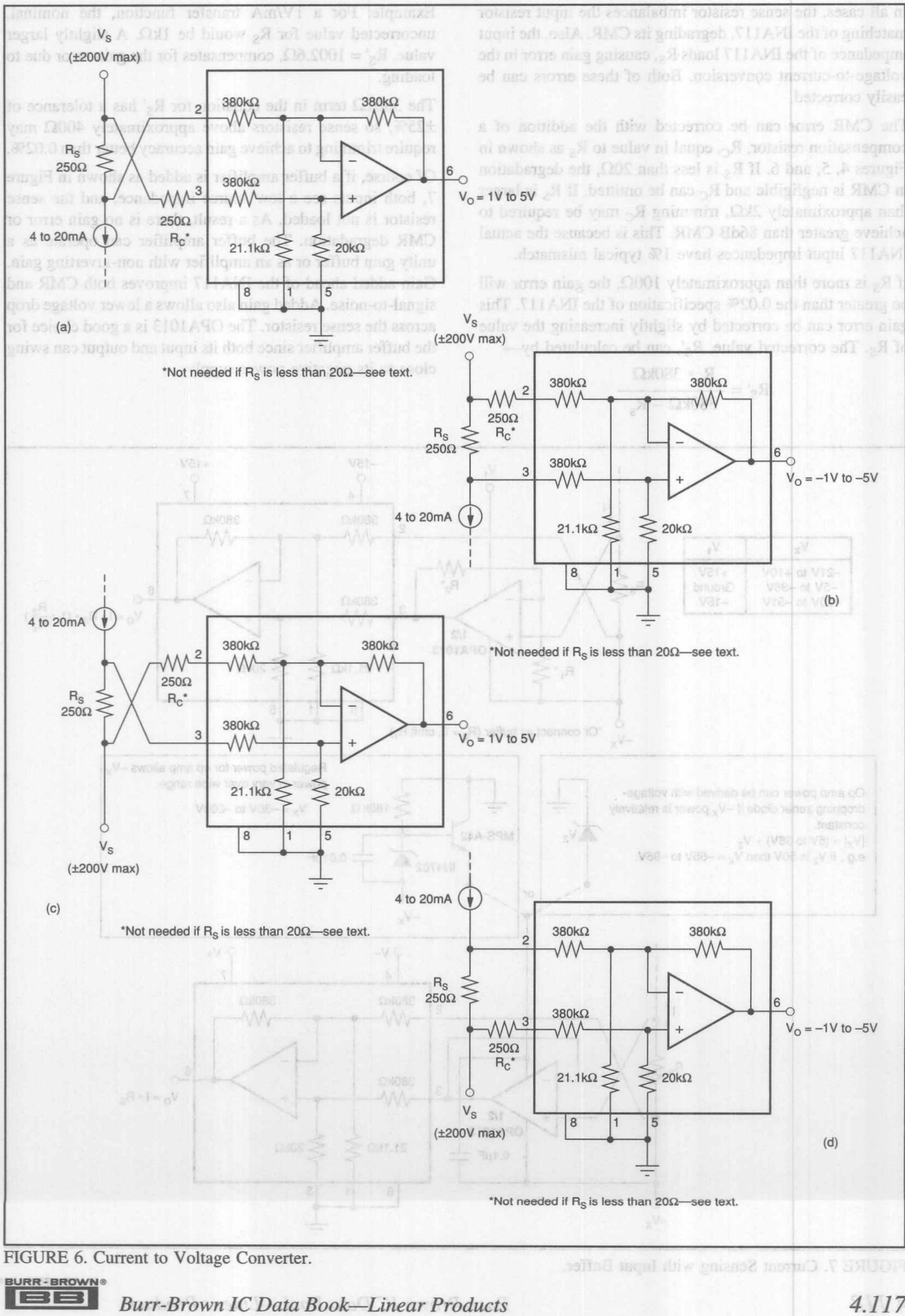


FIGURE 6. Current to Voltage Converter.

In all cases, the sense resistor imbalances the input resistor matching of the INA117, degrading its CMR. Also, the input impedance of the INA117 loads R_S, causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor, R_C, equal in value to R_S as shown in Figures 4, 5, and 6. If R_S is less than 20Ω, the degradation in CMR is negligible and R_C can be omitted. If R_S is larger than approximately 2kΩ, trimming R_C may be required to achieve greater than 86dB CMR. This is because the actual INA117 input impedances have 1% typical mismatch.

If R_S is more than approximately 100Ω, the gain error will be greater than the 0.02% specification of the INA117. This gain error can be corrected by slightly increasing the value of R_S. The corrected value, R_S', can be calculated by—

$$R_S' = \frac{R_S \cdot 380k\Omega}{380k\Omega - R_S}$$

Example: For a 1V/mA transfer function, the nominal, uncorrected value for R_S would be 1kΩ. A slightly larger value, R_S' = 1002.6Ω, compensates for the gain error due to loading.

The 380kΩ term in the equation for R_S' has a tolerance of ±25%, so sense resistors above approximately 400Ω may require trimming to achieve gain accuracy better than 0.02%.

Of course, if a buffer amplifier is added as shown in Figure 7, both inputs see a low source impedance, and the sense resistor is not loaded. As a result, there is no gain error or CMR degradation. The buffer amplifier can operate as a unity gain buffer or as an amplifier with non-inverting gain. Gain added ahead of the INA117 improves both CMR and signal-to-noise. Added gain also allows a lower voltage drop across the sense resistor. The OPA1013 is a good choice for the buffer amplifier since both its input and output can swing close to its negative power supply.

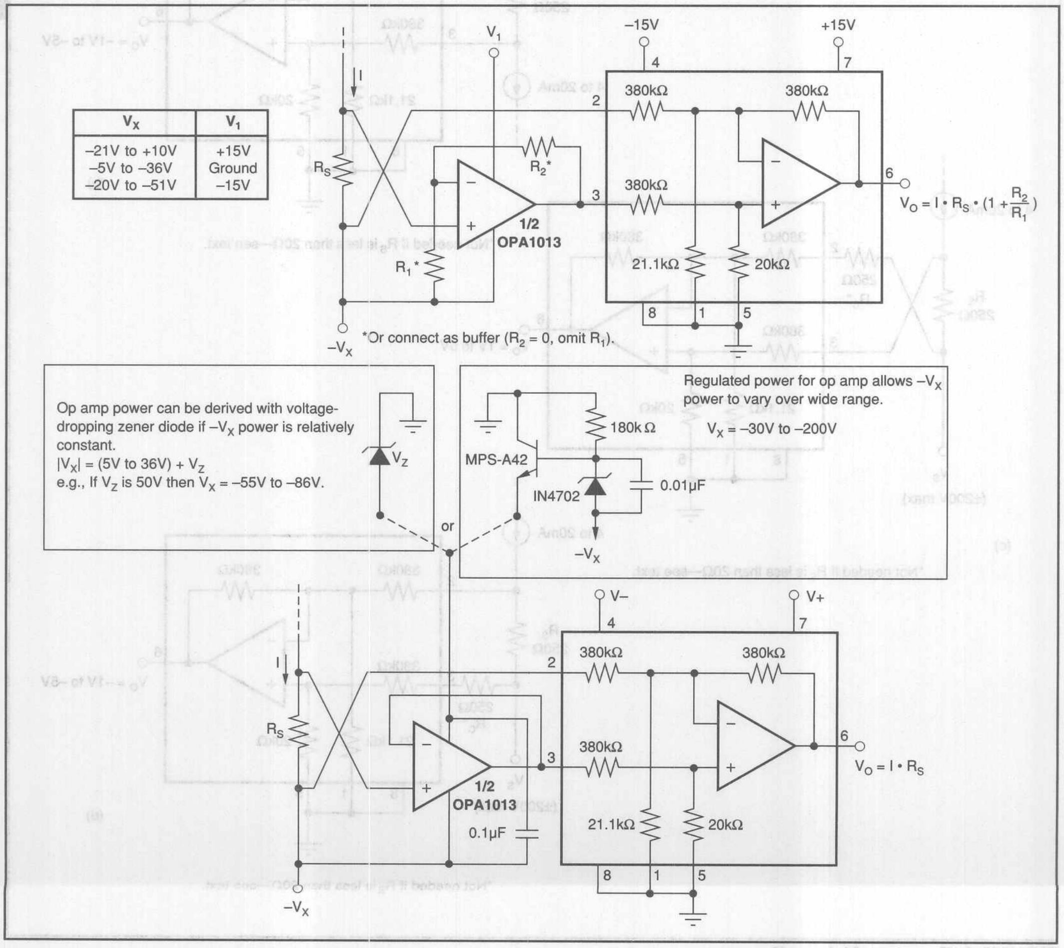


FIGURE 7. Current Sensing with Input Buffer.

an isolated power supply allows full ±200V common-mode input range.

NOISE PERFORMANCE

The noise performance of the INA117 is dominated by the internal resistor network. The thermal or Johnson noise of

Many applications may be satisfied with less than the full 200kHz bandwidth of the INA117. In these cases, the noise can be reduced with a low-pass filter on the output. The two-pole filter shown in Figure 9 limits bandwidth to 1kHz and reduces noise by more than 15:1. Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, a cutoff frequency below 100Hz will not further reduce noise.

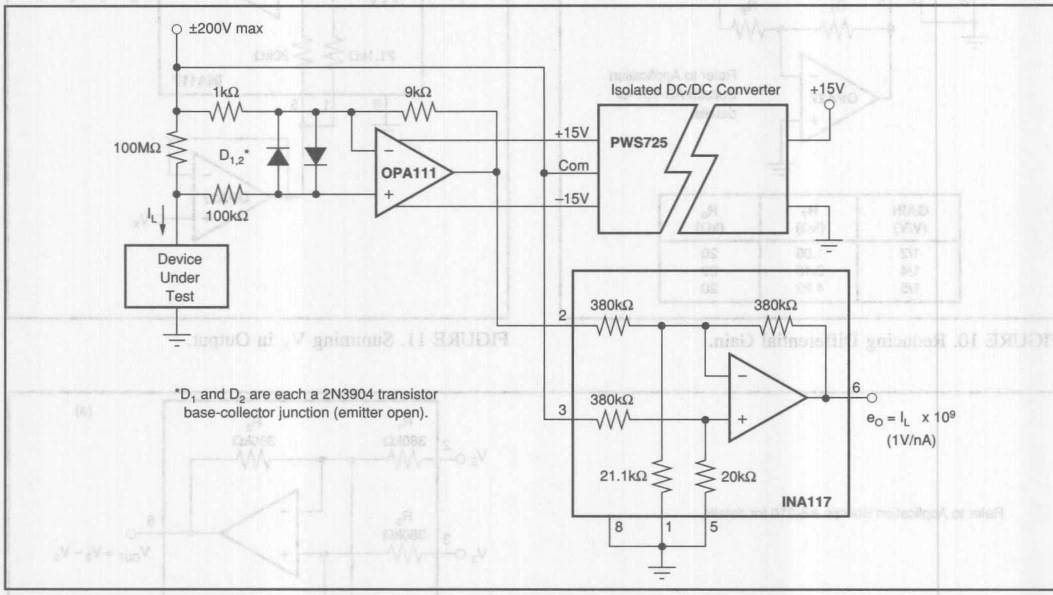
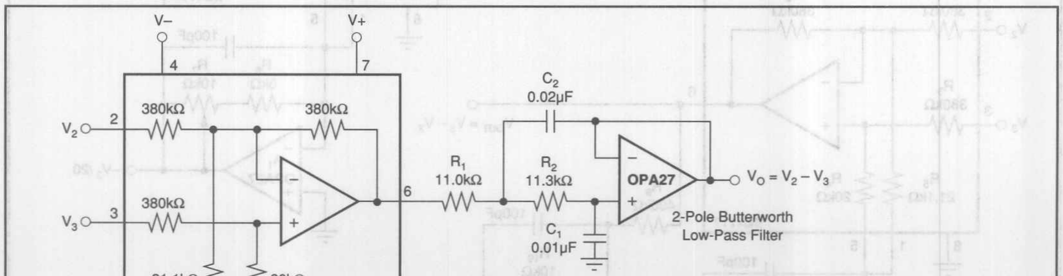


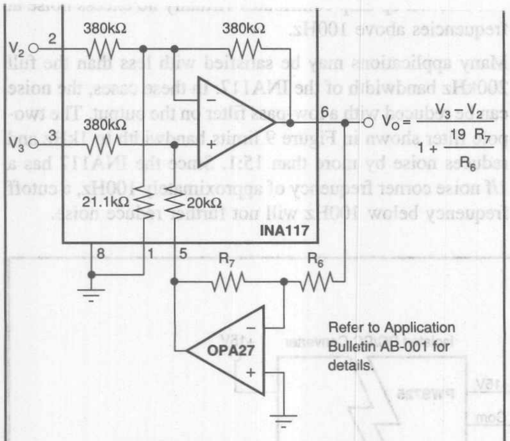
FIGURE 8. Leakage Current Measurement Circuit.



BUTTERWORTH LOW-PASS f_{-3dB}	OUTPUT NOISE (mVp-p)	R_1	R_2	C_1	C_2
200kHz	1.8	No Filter			
100kHz	1.1	11kΩ	11.3kΩ	100pF	200pF
10kHz	0.35	11kΩ	11.3kΩ	1nF	2nF
1kHz	0.11	11kΩ	11.3kΩ	10nF	20nF
≤100Hz(1)	0.05	11kΩ	11.3kΩ	0.1µF	0.2µF

NOTE: (1) Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, bandwidth reduction below this frequency will not significantly reduce noise.

FIGURE 9. Output Filter for Noise Reduction.



GAIN (V/V)	R_7 (kΩ)	R_6 (kΩ)
1/2	1.05	20
1/4	3.16	20
1/5	4.22	20

FIGURE 10. Reducing Differential Gain.

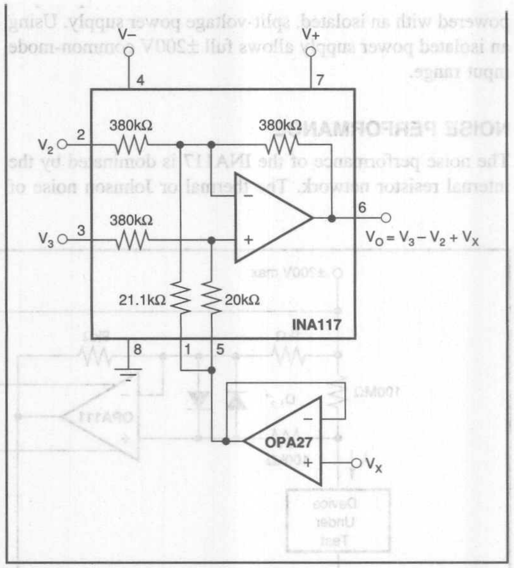


FIGURE 11. Summing V_X in Output.

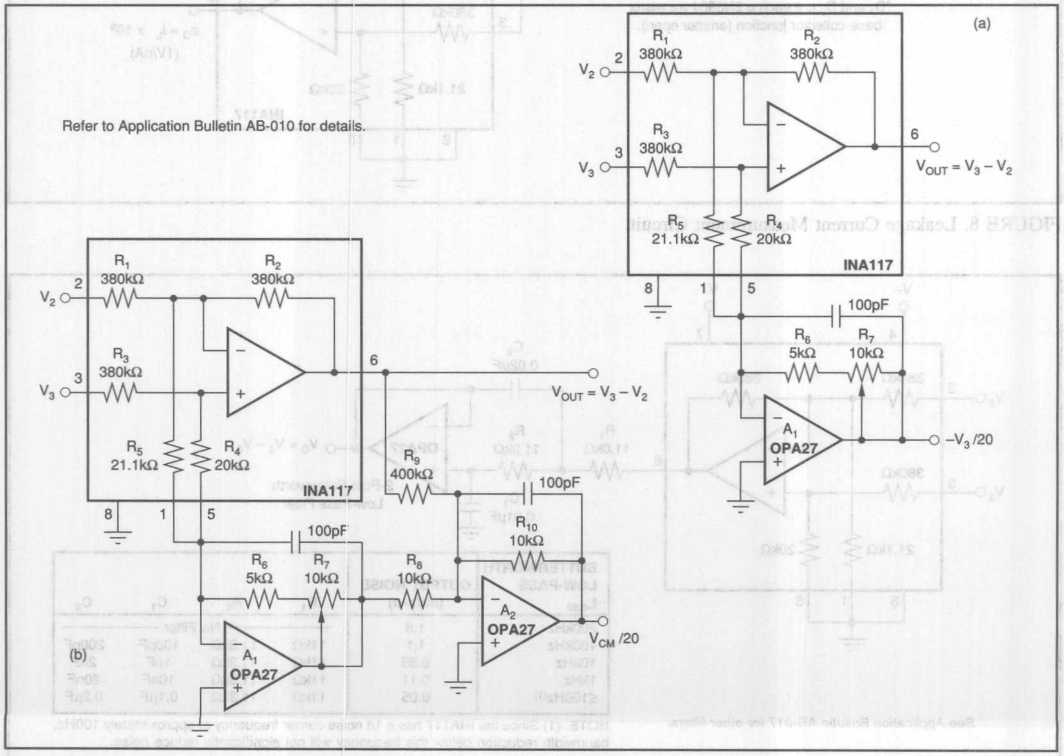


FIGURE 12. Common-Mode Voltage Monitoring.

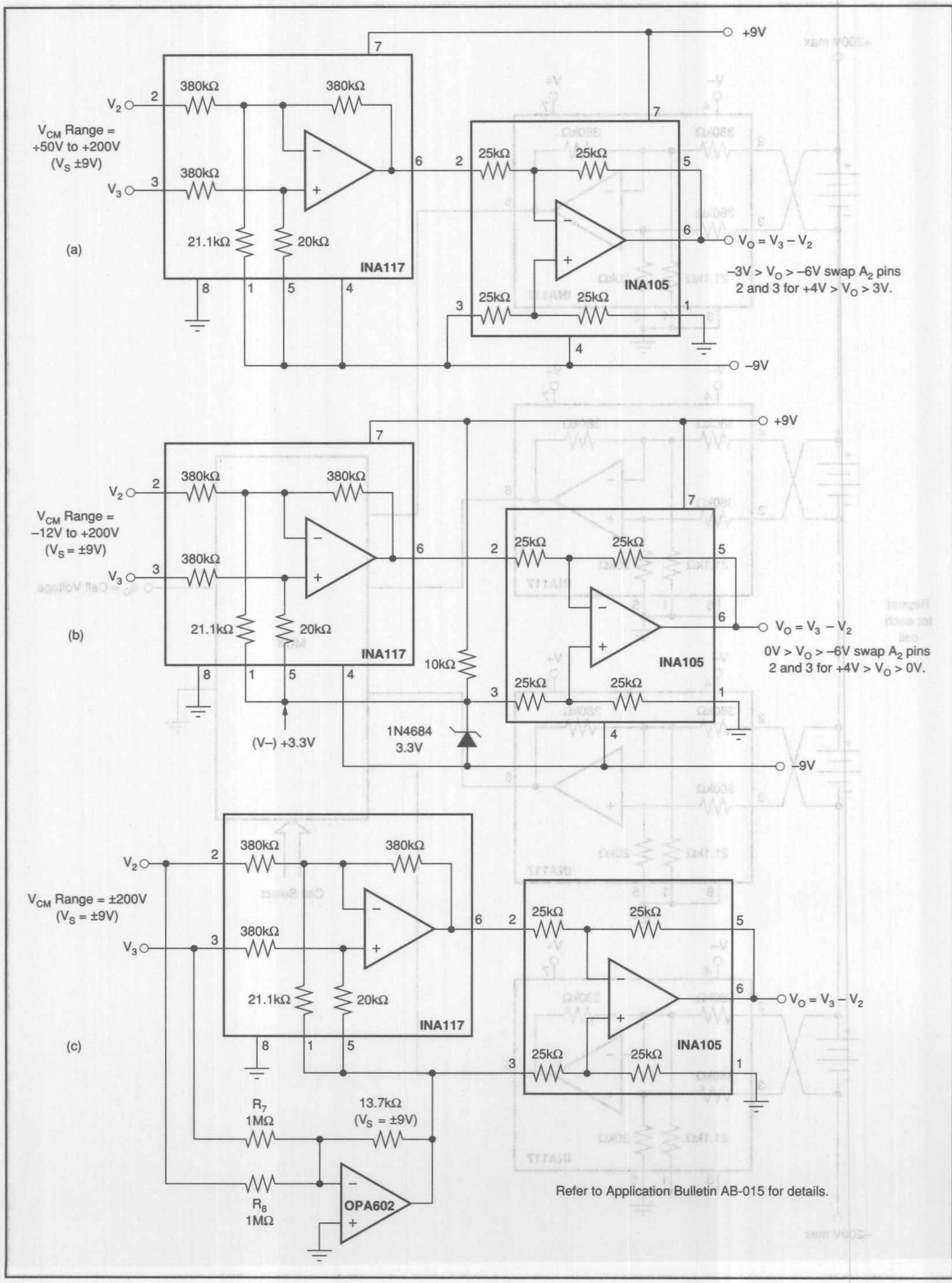


FIGURE 13. Offsetting or Boosting Common-Mode Voltage Range for Reduced Power Supply Voltage Operation.

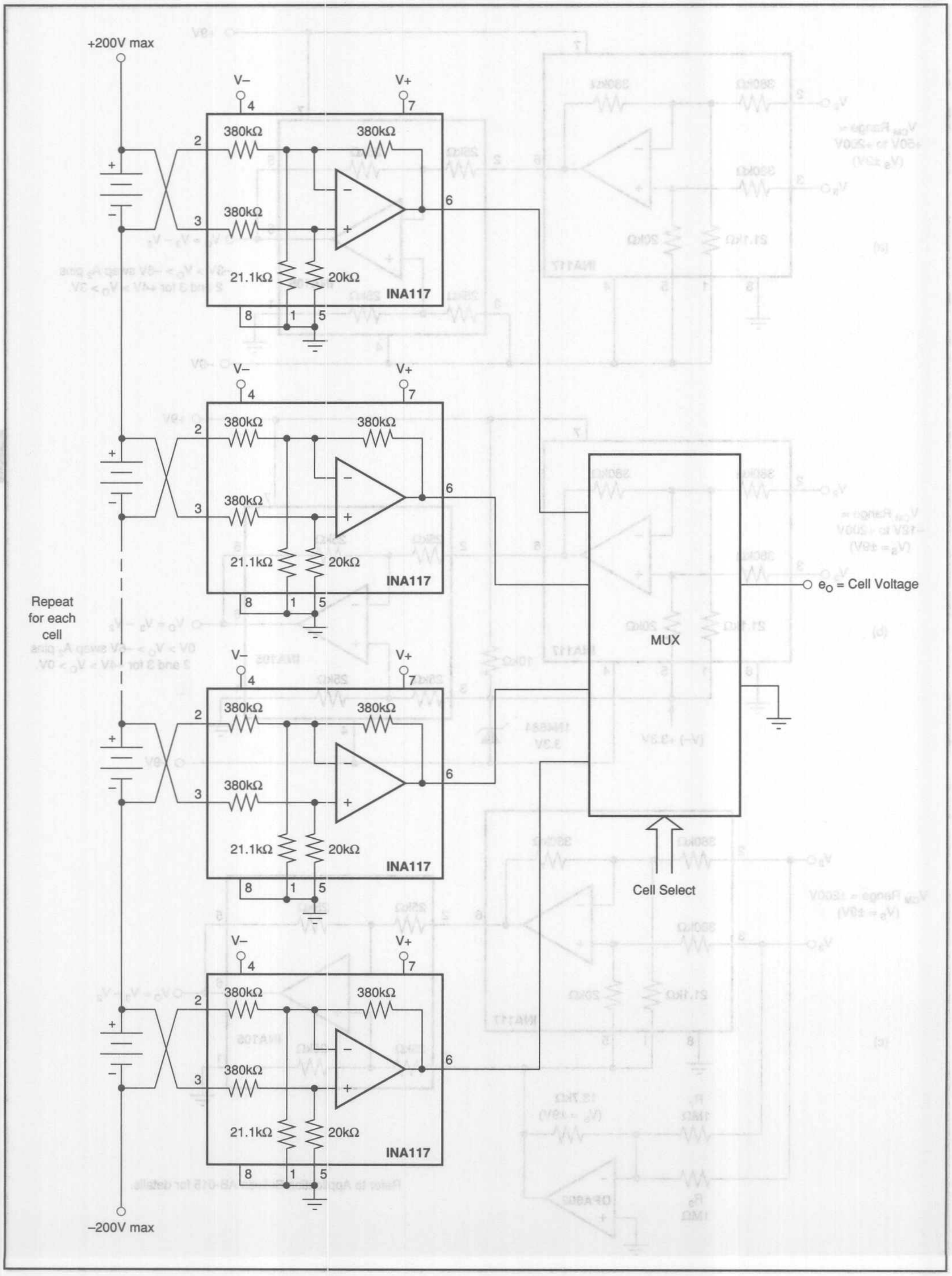


FIGURE 14. Battery Cell Voltage Monitor.

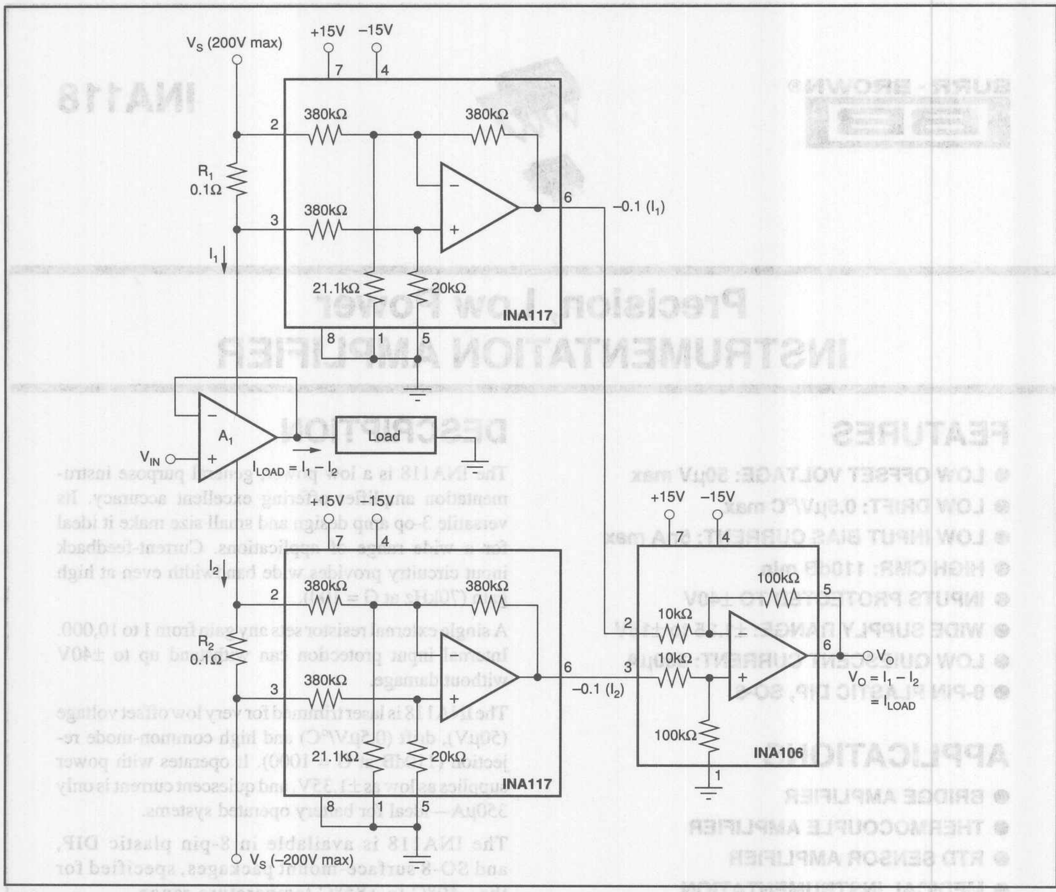


FIGURE 15. Measuring Amplifier Load Current.

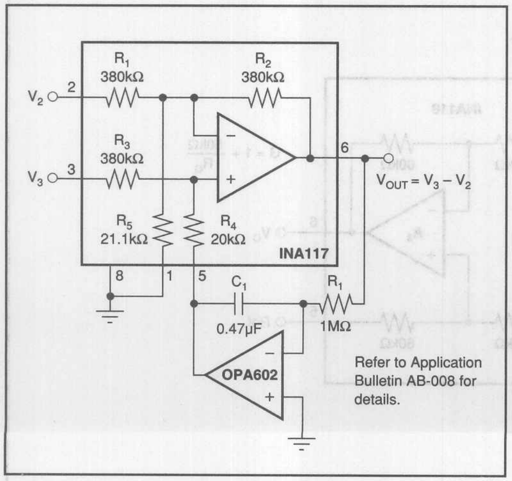
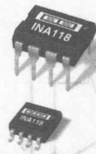


FIGURE 16. AC-Coupled INA117.

BURR - BROWN®



INA118

Precision, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW DRIFT: 0.5µV/°C max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 110dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±1.35 to ±18V
- LOW QUIESCENT CURRENT: 350µA
- 8-PIN PLASTIC DIP, SO-8

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

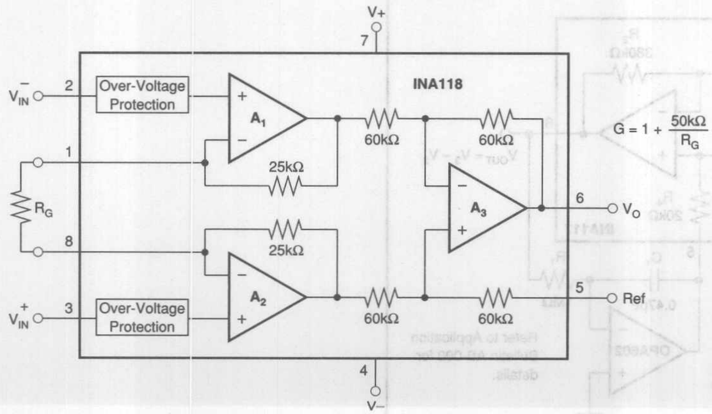
DESCRIPTION

The INA118 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (70kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA118 is laser trimmed for very low offset voltage (50µV), drift (0.5µV/°C) and high common-mode rejection (110dB at G = 1000). It operates with power supplies as low as ±1.35V, and quiescent current is only 350µA—ideal for battery operated systems.

The INA118 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

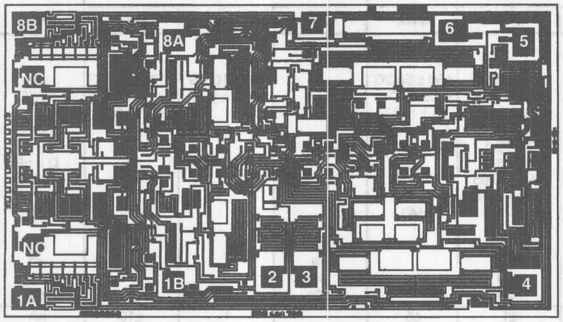
ELECTRICAL

At $T_A = +25°C$, $V_S = ±15V$, $R_L = 10kΩ$ unless otherwise noted.

PARAMETER	CONDITIONS	INA118PB, UB MIN	INA118PB, UB TYP	INA118PB, UB MAX	INA118P, U MIN	INA118P, U TYP	INA118P, U MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	$T_A = +25°C$		±10 ± 50/G	±50 ± 500/G		±25±100/G	±125±1000/G	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		±0.2 ± 2/G	±0.5 ± 20/G		±0.2 ± 5/G	±1 ± 20/G	µV/°C
vs Power Supply	$V_S = ±1.35V$ to ±18V		±1 ±10/G	±5 ± 100/G		*	±10 ±100/G	µV/V
Long-Term Stability			±0.4 ±5/G			*		µV/mo
Impedance, Differential			10^{10} || 1			*		Ω || pF
Common-Mode			10^{10} || 4			*		Ω || pF
Linear Input Voltage Range		(V+) – 1	(V+) – 0.65		*	*		V
		(V–) + 1.1	(V–) + 0.95		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	$V_{CM} = ±10V$, $ΔR_S = 1kΩ$							
	G = 1	80	90		73	*		dB
	G = 10	97	110		89	*		dB
	G = 100	107	120		98	*		dB
	G = 1000	110	125		100	*		dB
BIAS CURRENT			±1	±5		*	±10	nA
vs Temperature			±40			*		pA/°C
OFFSET CURRENT			±1	±5		*	±10	nA
vs Temperature			±40			*		pA/°C
NOISE VOLTAGE, RTI	G = 1000, $R_S = 0Ω$							
f = 10Hz			11			*		nV/√Hz
f = 100Hz			10			*		nV/√Hz
f = 1kHz			10			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.28			*		µVp-p
Noise Current								
f=10Hz			2.0			*		pA/√Hz
f=1kHz			0.3			*		pA/√Hz
f_B = 0.1Hz to 10Hz			80			*		pAp-p
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G = 1		±0.01	±0.024		*	±0.1	%
	G = 10		±0.02	±0.4		*	±0.5	%
	G = 100		±0.05	±0.5		*	±0.7	%
	G = 1000		±0.5	±1		*	±2	%
Gain vs Temperature	G = 1		±1	±10		*	±10	ppm/°C
50kΩ Resistance(1)			±25	±100		*	*	ppm/°C
Nonlinearity	G = 1		±0.0003	±0.001		*	±0.002	% of FSR
	G = 10		±0.0005	±0.002		*	±0.004	% of FSR
	G = 100		±0.0005	±0.002		*	±0.004	% of FSR
	G = 1000		±0.002	±0.01		*	±0.02	% of FSR
OUTPUT								
Voltage: Positive	$R_L = 10kΩ$	(V+) – 1	(V+) – 0.8		*	*		V
Negative	$R_L = 10kΩ$	(V–) + 0.35	(V–) + 0.2		*	*		V
Single Supply High	V_S = +2.7V/0V(2), $R_L = 10kΩ$	1.8	2.0		*	*		V
Single Supply Low	V_S = +2.7V/0V(2), $R_L = 10kΩ$	60	35		*	*		mV
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+5/–12			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		800			*		kHz
	G = 10		500			*		kHz
	G = 100		70			*		kHz
	G = 1000		7			*		kHz
Slew Rate	$V_O = ±10V$, G = 10		0.9			*		V/µs
Settling Time, 0.01%	G = 1		15			*		µs
	G = 10		15			*		µs
	G = 100		21			*		µs
	G = 1000		210			*		µs
Overload Recovery	50% Overdrive		20			*		µs
POWER SUPPLY								
Voltage Range		±1.35	±15	±18	*	*	*	V
Current	$V_{IN} = 0V$		±350	±385		*	*	µA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
$θ_{JA}$			80			*		°C/W

* Specification same as INA118PB, UB.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation. (2) V_{CM} = 2V. Common-mode input voltage range is limited. See text for discussion of low power supply and single power supply operation.



INA118 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B(1)	R_G	6	V_O
2	$V-_{IN}$	7	V+
3	$V+_{IN}$	8A, 8B(1)	R_G
4	V–		
5	Ref		

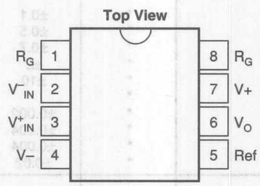
NC = No Connection.
NOTES: (1) Connect both indicated pads.
Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	120 x 70 ±5	3.05 x 1.78 ±0.13
Die Thickness	14 ±3	0.36 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATION

8-Pin DIP and SO-8



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

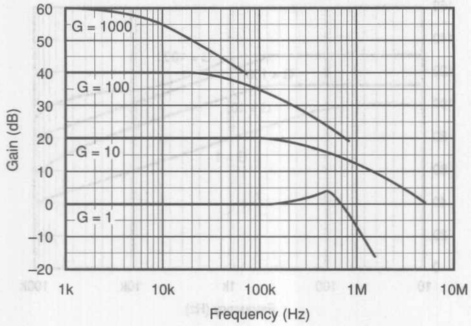
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
INA118P	8-Pin Plastic DIP	006	–40°C to +85°C
INA118PB	8-Pin Plastic DIP	006	–40°C to +85°C
INA118U	SO-8 Surface-Mount	182	–40°C to +85°C
INA118UB	SO-8 Surface-Mount	182	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

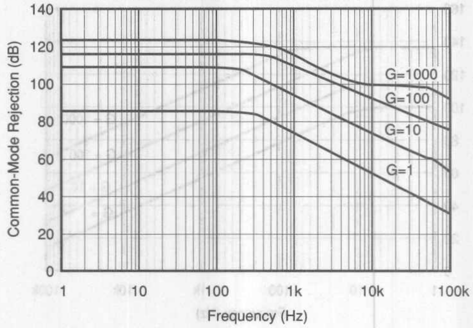
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

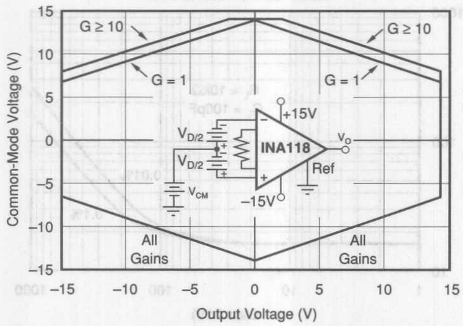
GAIN vs FREQUENCY



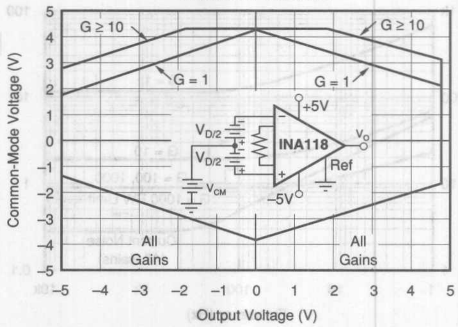
COMMON-MODE REJECTION vs FREQUENCY



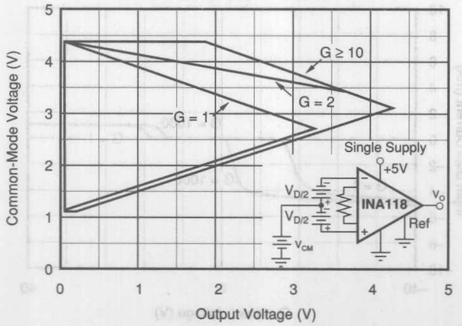
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE



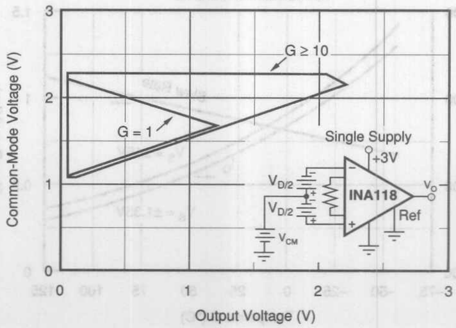
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE



INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE



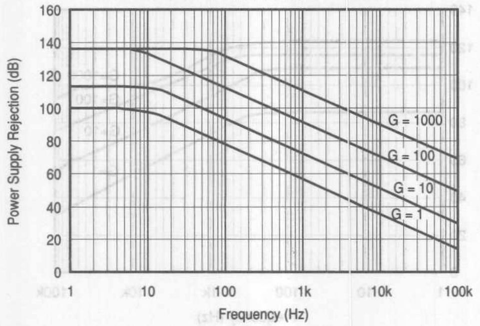
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE



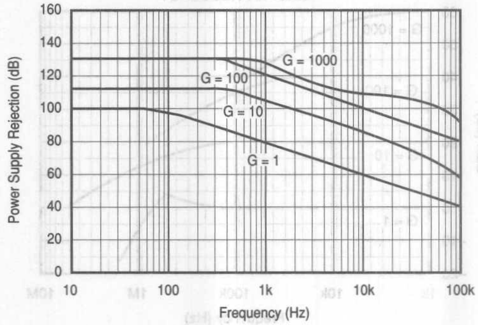
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

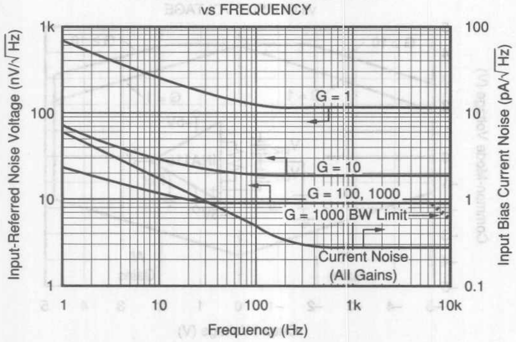
POSITIVE POWER SUPPLY REJECTION
vs FREQUENCY



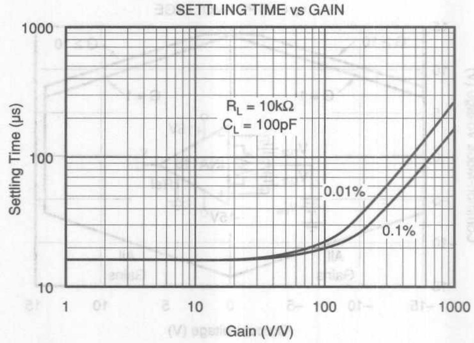
NEGATIVE POWER SUPPLY REJECTION
vs FREQUENCY



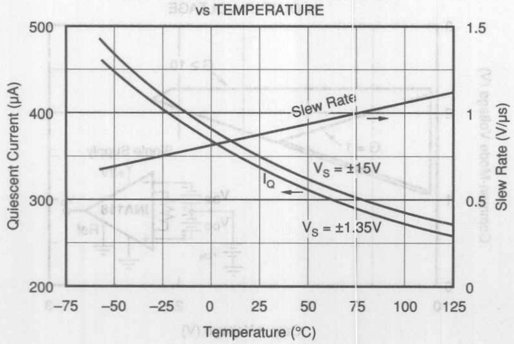
INPUT- REFERRED NOISE VOLTAGE
vs FREQUENCY



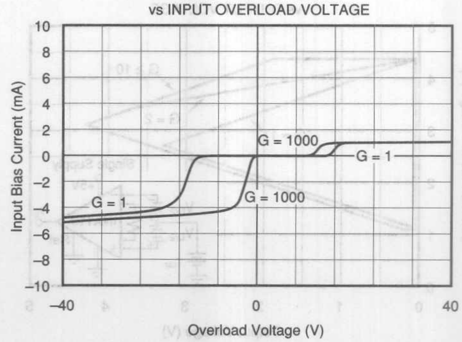
SETTLING TIME vs GAIN



QUIESCENT CURRENT and SLEW RATE
vs TEMPERATURE

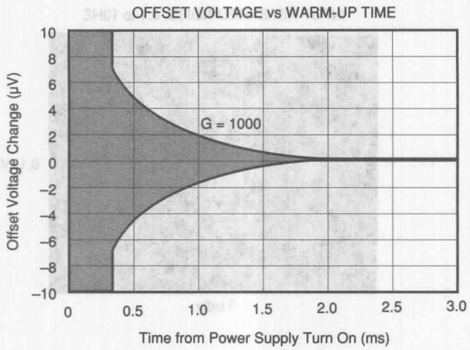


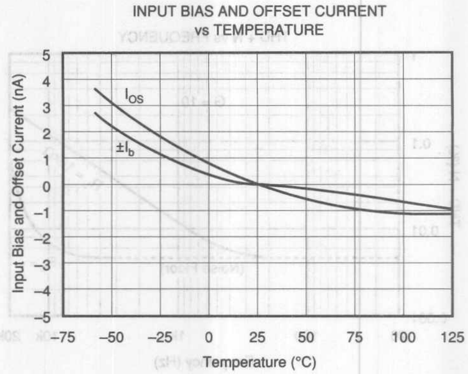
INPUT BIAS CURRENT
vs INPUT OVERLOAD VOLTAGE

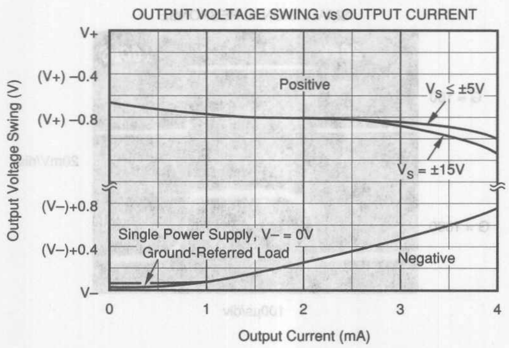


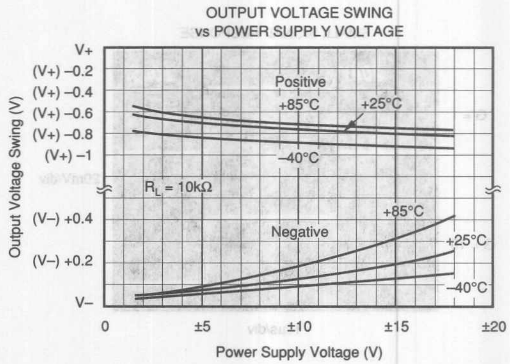
TYPICAL PERFORMANCE CURVES (CONT)

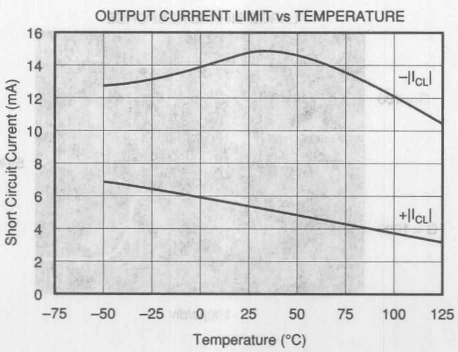
At $T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.

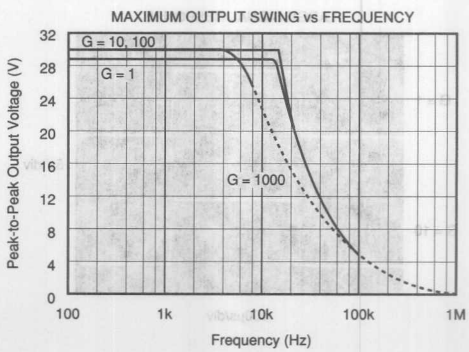




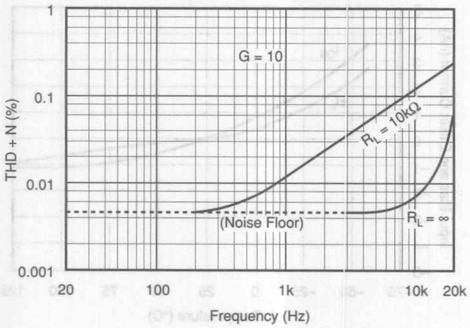




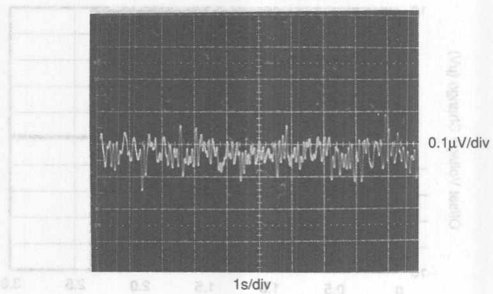




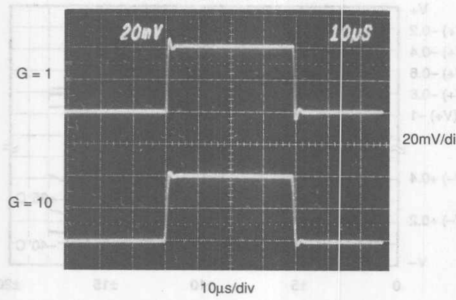
THD + N vs FREQUENCY



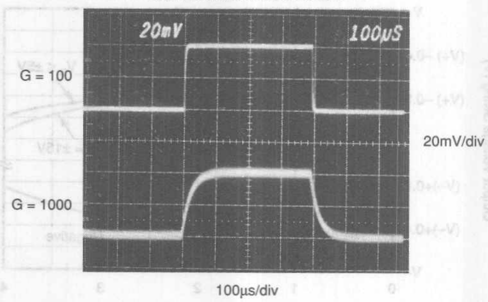
INPUT REFERRED NOISE, 0.1 to 10HZ



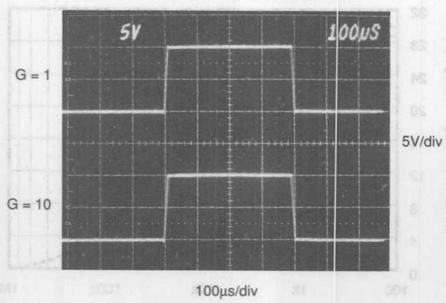
SMALL SIGNAL RESPONSE



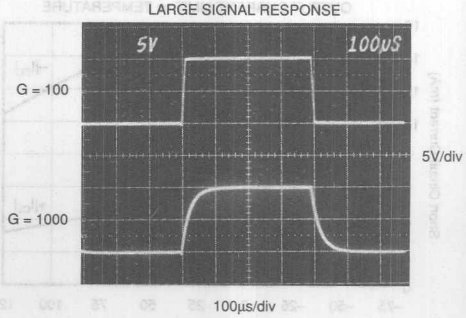
SMALL SIGNAL RESPONSE



LARGE SIGNAL RESPONSE



LARGE SIGNAL RESPONSE



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA118. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 12Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain of the INA118 is set by connecting a single external resistor, R_G, connected between pins 1 and 8:

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA118.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA118 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA118. Settling time also remains excellent at high gain.

The INA118 exhibits approximately 3dB peaking at 500kHz in unity gain. This is a result of its current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable +6dB/octave due to a response zero. A simple pole at 300kHz or lower will produce a flat passband unity gain response.

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.

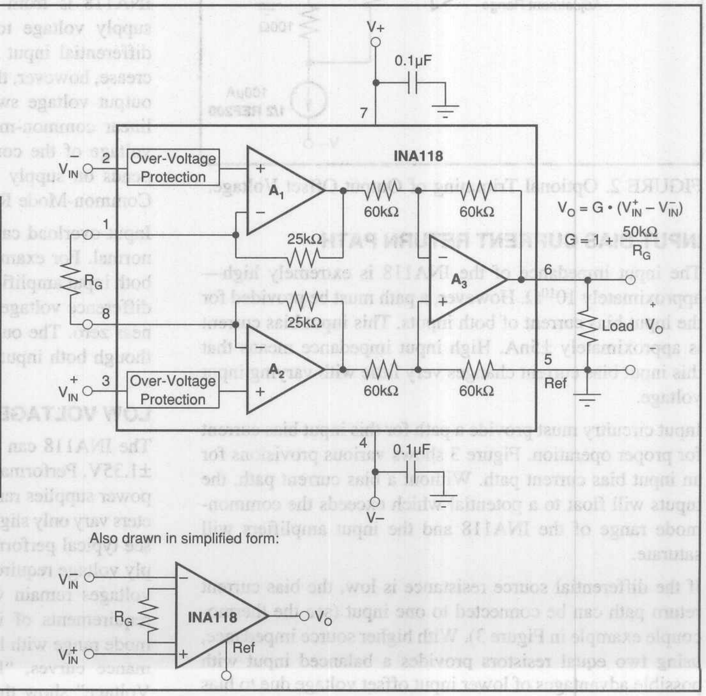


FIGURE 1. Basic Connections.

NOISE PERFORMANCE

The INA118 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low frequency noise of the INA118 is approximately 0.28µVp-p measured from 0.1 to 10Hz (G≥100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

OFFSET TRIMMING

The INA118 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

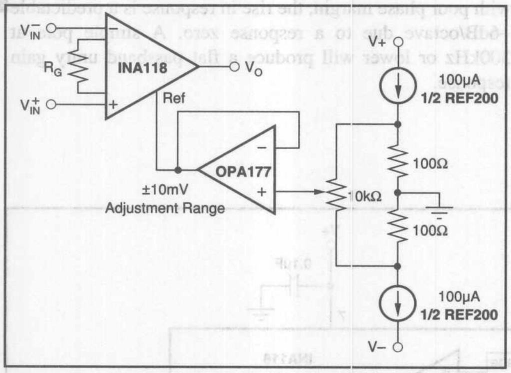


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA118 is extremely high—approximately 10^{10}Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±5nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA118 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

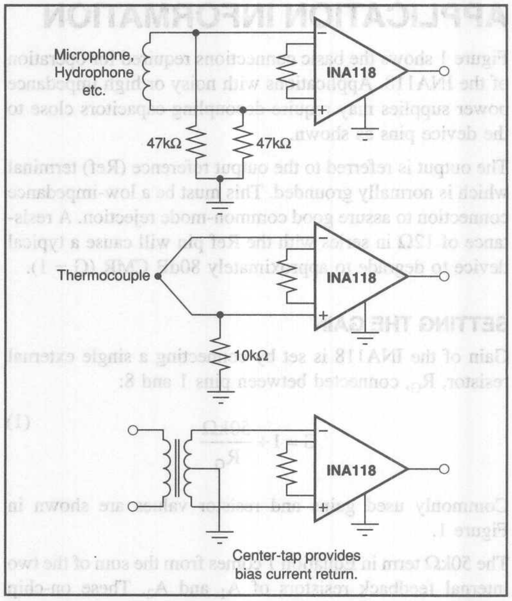


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA118 is from approximately 0.6V below the positive supply voltage to 1V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range will be limited by the output voltage swing of amplifiers A_1 and A_2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage".

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA118 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA118 can be operated on power supplies as low as ±1.35V. Performance of the INA118 remains excellent with power supplies ranging from ±1.35V to ±18V. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for a various supply voltages and gains.

SINGLE SUPPLY OPERATION

The INA118 can be used on single power supplies of +2.7V to +36V. Figure 5 shows a basic single supply circuit. The output Ref terminal is connected to ground. Zero differential input voltage will demand an output voltage of 0V (ground). Actual output voltage swing is limited to approximately 35mV above ground, when the load is referred to ground as shown. The typical performance curve "Output Voltage vs Output Current" shows how the output voltage swing varies with output current.

With single supply operation, V_{IN}^{+} and V_{IN}^{-} must both be 1.1V above ground for linear operation. You cannot, for instance, connect the inverting input to ground and measure a voltage connected to the non-inverting input.

To illustrate the issues affecting low voltage operation, consider the circuit in Figure 5. It shows the INA118, operating from a single 3V supply. A resistor in series with the low side of the bridge assures that the bridge output voltage is within the common-mode range of the amplifier's inputs. Refer to the typical performance curve "Input Common-Mode Range vs Output Voltage" for 3V single supply operation.

INPUT PROTECTION

The inputs of the INA118 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5mA. The typical performance curve "Input Bias Current vs Input Overload Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

INSIDE THE INA118

Figure 1 shows a simplified representation of the INA118. The more detailed diagram shown here provides additional insight into its operation.

Each input is protected by two FET transistors that provide a low series resistance under normal signal conditions, preserving excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 1.5 to 5mA.

The differential input voltage is buffered by Q_1 and Q_2 and impressed across R_G, causing a signal current to flow through R_G, R_1 and R_2. The output difference amp, A_3, removes the common-mode component of the input signal and refers the output signal to the Ref terminal.

Equations in the figure describe the output voltages of A_1 and A_2. The V_{BE} and IR drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 1V lower than the input voltages.

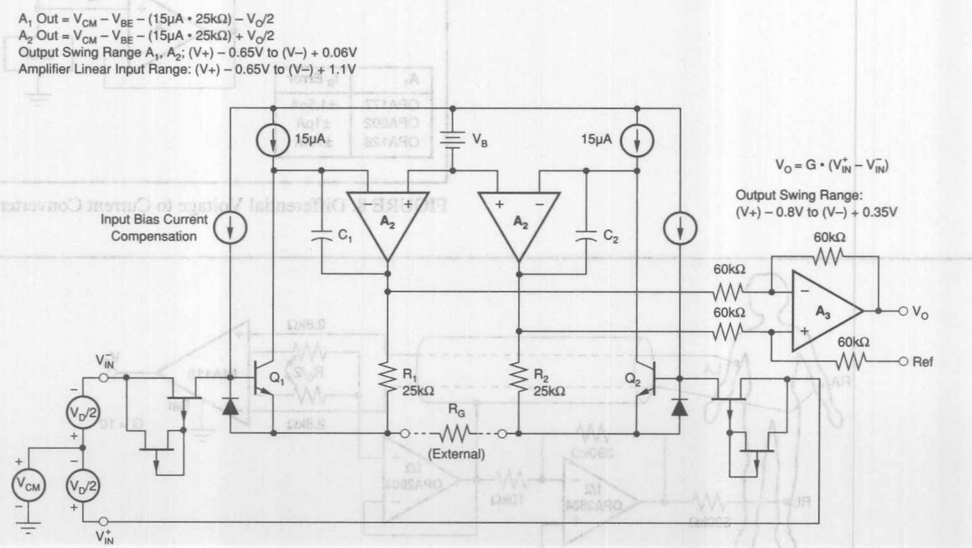


FIGURE 4. INA118 Simplified Circuit Diagram.

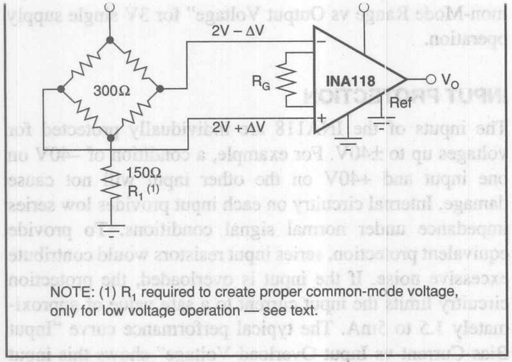


FIGURE 5. Single-Supply Bridge Amplifier.

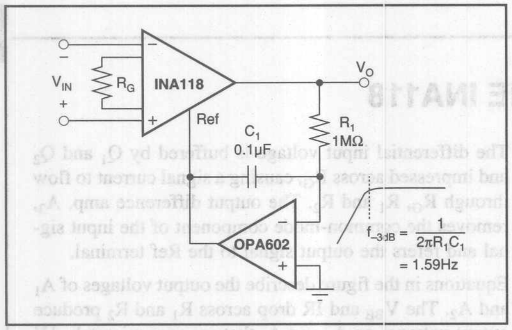
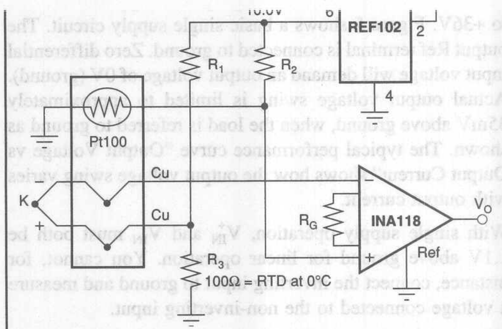
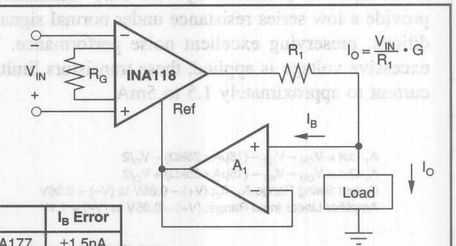


FIGURE 6. AC-Coupled Instrumentation Amplifier.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

FIGURE 7. Thermocouple Amplifier With Cold Junction Compensation.



A_1	I_B Error
OPA177	±1.5nA
OPA602	±1pA
OPA128	±75fA

FIGURE 8. Differential Voltage to Current Converter.

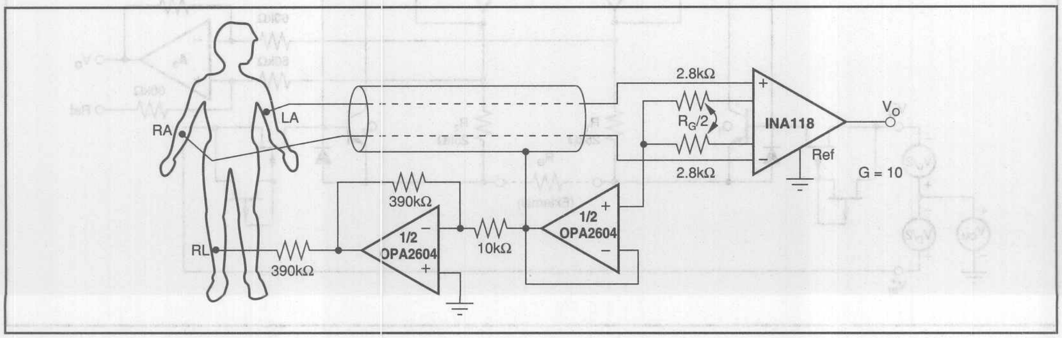
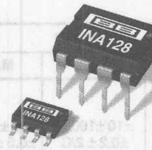


FIGURE 9. ECG Amplifier With Right-Leg Drive.



INA128

Precision, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW DRIFT: 0.5µV/°C max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 120dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 700µA
- 8-PIN PLASTIC DIP, SO-8

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

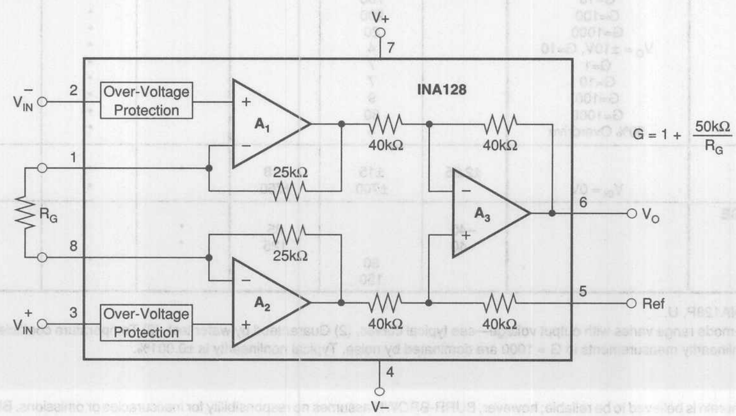
DESCRIPTION

The INA128 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA128 is laser trimmed for very low offset voltage (50µV), drift (0.5µV/°C) and high common-mode rejection (120dB at G ≥ 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 700µA—ideal for battery operated systems.

The INA128 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

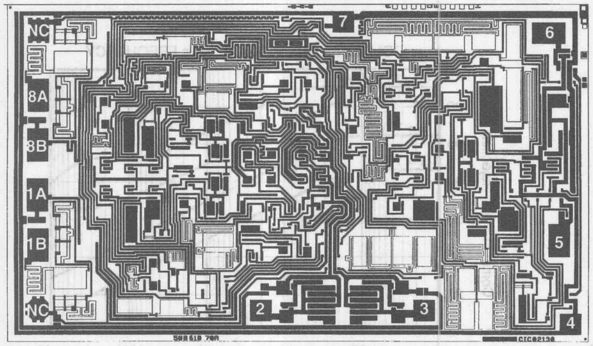
At T_A = +25°C, V_S = ±15V, R_L = 10kΩ unless otherwise noted.

PARAMETER	CONDITIONS	INA128P, U MIN	INA128P, U TYP	INA128P, U MAX	INA128PA, UA MIN	INA128PA, UA TYP	INA128PA, UA MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±10 ±100/G	±50 ±500/G		±25 ±100/G	±125 ±1000/G	μV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		±0.2 ± 2/G	±0.5 ± 20/G		±0.2 ± 5/G	±1 ± 20/G	μV/°C
vs Power Supply	V_S = ±2.25V to ±18V		±0.2 ±20/G	±1 ±100/G		*	±2 ±200/G	μV/V
Long-Term Stability			±0.1 ±3/G			*		μV/mo
Impedance, Differential			10^{10} ‖ 2			*		Ω ‖ pF
Common-Mode			10^{11} ‖ 9			*		Ω ‖ pF
Common-Mode Voltage Range(1)	V_O = 0V	(V+) – 2	(V+) – 1.4		*			V
		(V–) + 2	(V–) + 1.7		*			V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = ±13V, ΔR_S = 1kΩ							
	G=1	80	86		73	*		dB
	G=10	100	106		93	*		dB
	G=100	120	125		110	*		dB
	G=1000	120	130		110	*		dB
BIAS CURRENT			±2	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
Offset Current			±1	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
NOISE VOLTAGE, RTI	G = 1000, R_S = 0Ω							
f = 10Hz			10			*		nV/√Hz
f = 100Hz			8			*		nV/√Hz
f = 1kHz			8			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.2			*		μVp-p
Noise Current								
f=10Hz			0.9			*		pA/√Hz
f=1kHz			0.3			*		pA/√Hz
f_B = 0.1Hz to 10Hz			30					pAp-p
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G=1		±0.01	±0.024			±0.1	%
	G=10		±0.02	±0.4		*	±0.5	%
	G=100		±0.05	±0.5		*	±0.7	%
	G=1000		±0.5	±1		*	±2	%
Gain vs Temperature(2)	G=1		±1	±10		*	*	ppm/°C
50kΩ Resistance(2, 3)			±25	±100		*	*	ppm/°C
Nonlinearity	V_O = ±13.6V, G=1		±0.0001	±0.001		*	±0.002	% of FSR
	G=10		±0.0003	±0.002		*	±0.004	% of FSR
	G=100		±0.0005	±0.002		*	±0.004	% of FSR
	G=1000		±0.001	(Note 4)		*	*	% of FSR
OUTPUT								
Voltage: Positive	R_L = 10kΩ	(V+) – 1.4	(V+) – 0.9		*	*		V
Negative	R_L = 10kΩ	(V–) + 1.4	(V–) + 0.8		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+6/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G=1		1.3			*		MHz
	G=10		700			*		kHz
	G=100		200			*		kHz
	G=1000		20			*		kHz
Slew Rate	V_O = ±10V, G=10		4			*		V/μs
Settling Time, 0.01%	G=1		7			*		μs
	G=10		7			*		μs
	G=100		9			*		μs
	G=1000		80			*		μs
Overload Recovery	50% Overdrive		4			*		μs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current, Total	V_{IN} = 0V		±700	±750		*	*	μA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA} 8-Pin Dip			80			*		°C/W
SO-8 SOIC			150					°C/W

* Specification same as INA128P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test. (3) Temperature coefficient of the "50kΩ" term in the gain equation. (4) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.

DICE INFORMATION



INA128 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B(1)	R_G	5	Ref
2	V^-_{IN}	6	V_O
3	V^+_{IN}	7	V+
4	V–	8A, 8B(1)	R_G

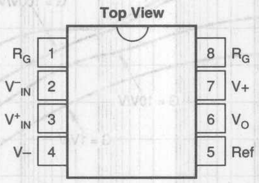
NC = No Connection.
NOTES: (1) Connect both indicated pads.
Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	128 x 76 ±5	3.05 x 1.78 ±0.13
Die Thickness	14 ±3	0.35 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

PIN CONFIGURATION

8-Pin DIP and SO-8



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

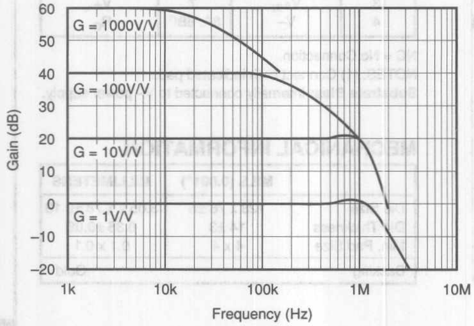
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

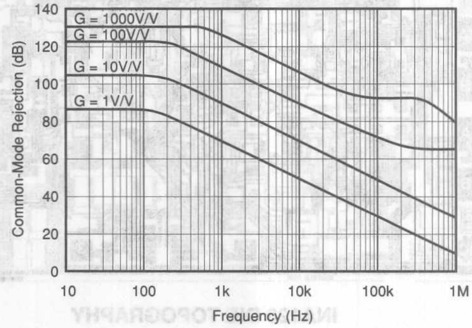
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
INA128PA	8-Pin Plastic DIP	006	–40°C to +85°C
INA128P	8-Pin Plastic DIP	006	–40°C to +85°C
INA128UA	SO-8 Surface-Mount	182	–40°C to +85°C
INA128U	SO-8 Surface-Mount	182	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

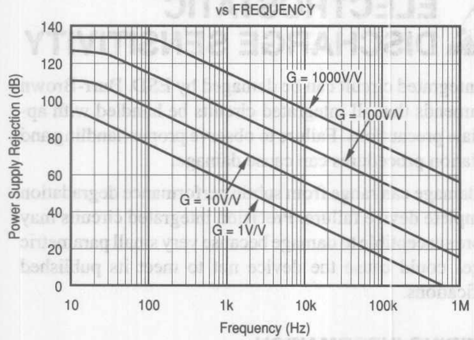
GAIN vs FREQUENCY



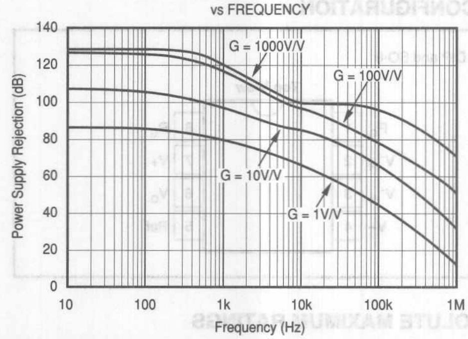
COMMON-MODE REJECTION vs FREQUENCY



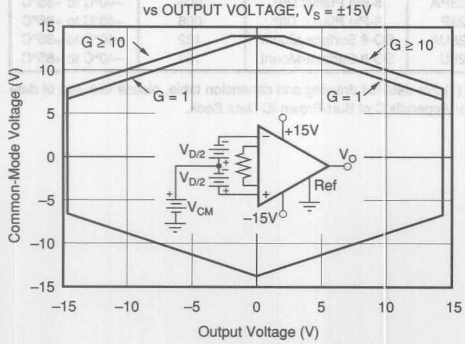
POSITIVE POWER SUPPLY REJECTION
vs FREQUENCY



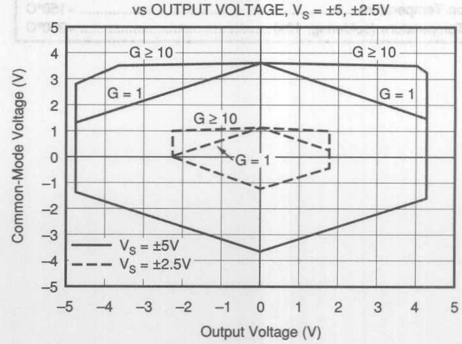
NEGATIVE POWER SUPPLY REJECTION
vs FREQUENCY



INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE, $V_S = \pm15V$



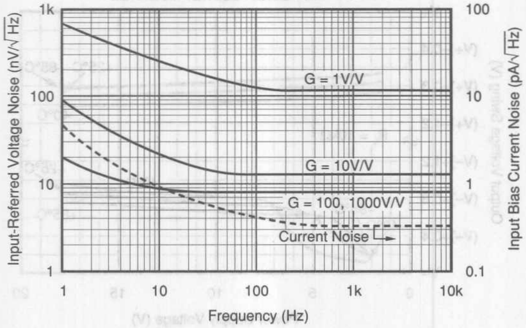
INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE, $V_S = \pm5, \pm2.5V$



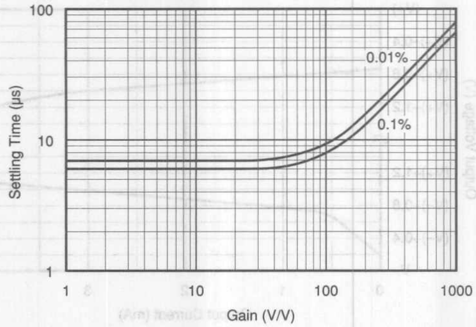
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

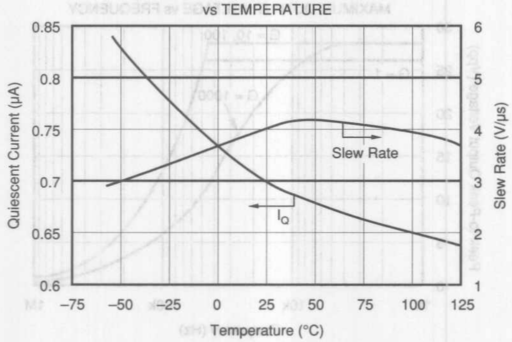
INPUT- REFERRED NOISE vs FREQUENCY



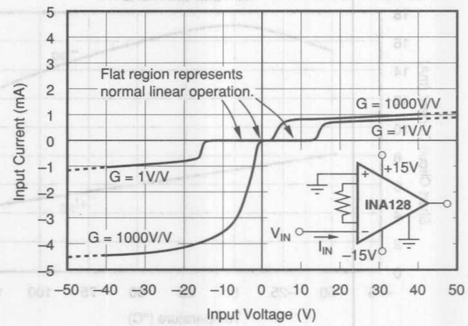
SETTLING TIME vs GAIN



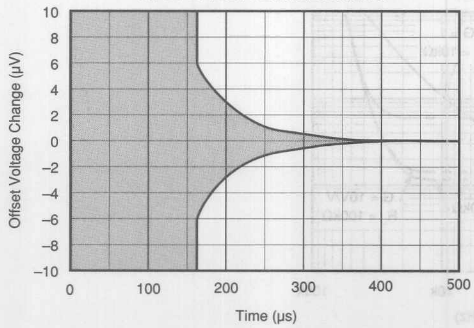
QUIESCENT CURRENT and SLEW RATE vs TEMPERATURE



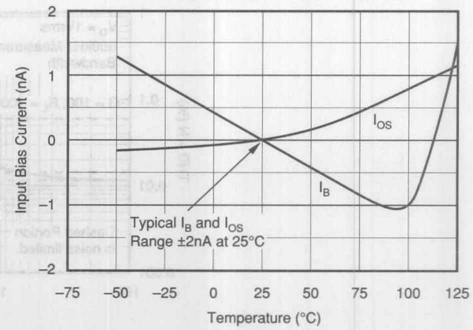
INPUT OVER-VOLTAGE V/I CHARACTERISTICS



INPUT OFFSET VOLTAGE WARM-UP

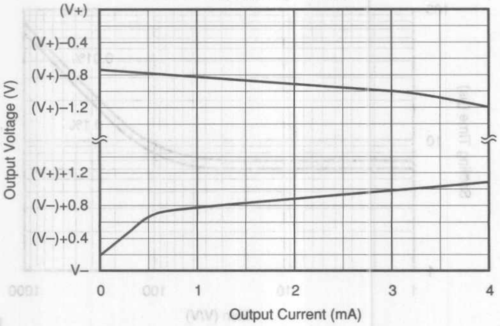


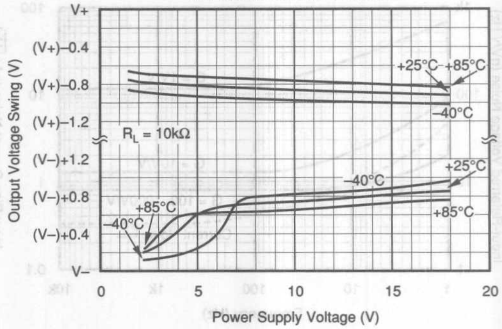
INPUT BIAS CURRENT vs TEMPERATURE

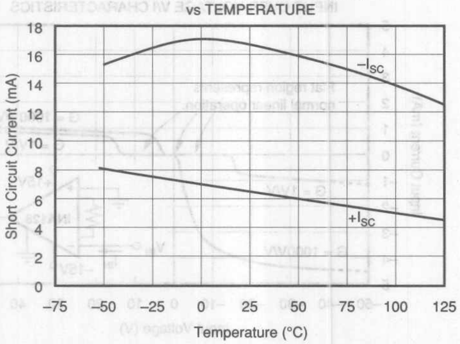


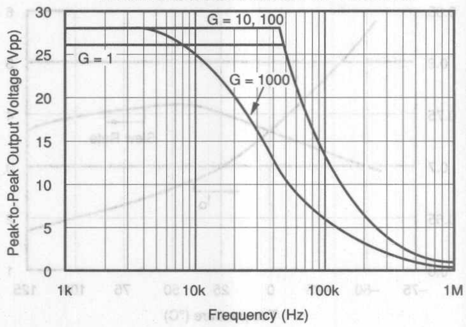
TYPICAL PERFORMANCE CURVES (CONT)

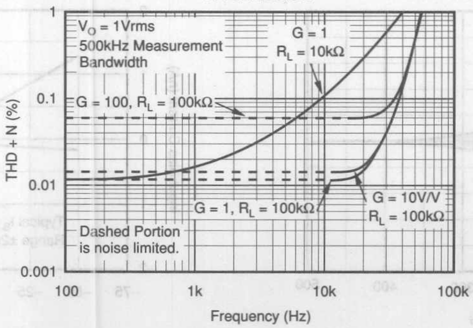
At $T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.











TYPICAL PERFORMANCE CURVES (CONT)

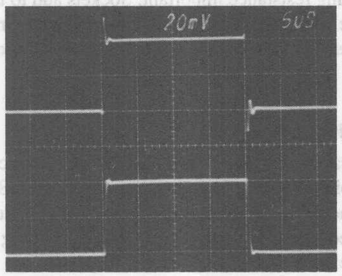
At $T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.

SMALL-SIGNAL
(G = 1, 10)

G = 1

20mV/div

G = 10



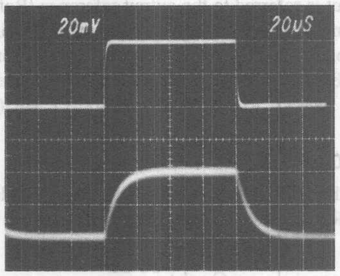
5µs/div

SMALL-SIGNAL
(G = 100, 1000)

G = 100

20mV/div

G = 1000



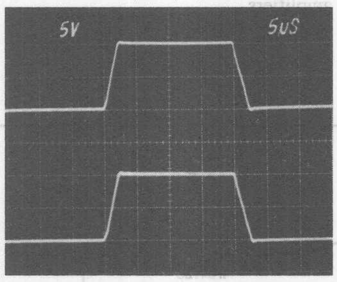
20µs/div

LARGE-SIGNAL
(G = 1, 10)

G = 1

5V/div

G = 10



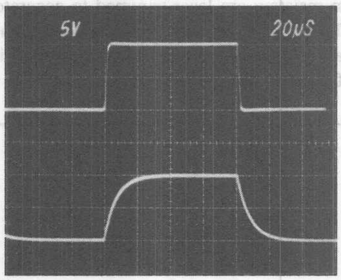
5µs/div

LARGE-SIGNAL
(G = 100, 1000)

G = 100

5V/div

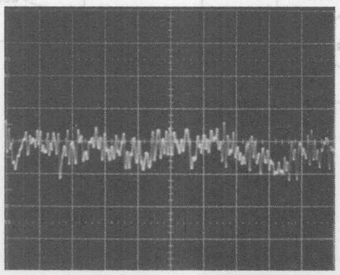
G = 1000



20µs/div

VOLTAGE NOISE 0.1 to 10Hz
INPUT-REFERRED, G ≥ 100

0.1µV/div



1s/div

Figure 1 shows the basic connections required for operation of the INA128. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain of the INA128 is set by connecting a single external resistor, R_G, connected between pins 1 and 8:

$$G = 1 + \frac{50k\Omega}{R_G} \tag{1}$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA128.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA128 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA128. Settling time also remains excellent at high gain.

NOISE PERFORMANCE

The INA128 provides very low noise in most applications. Low frequency noise is approximately 0.2µVp-p measured from 0.1 to 10Hz (G ≥ 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.

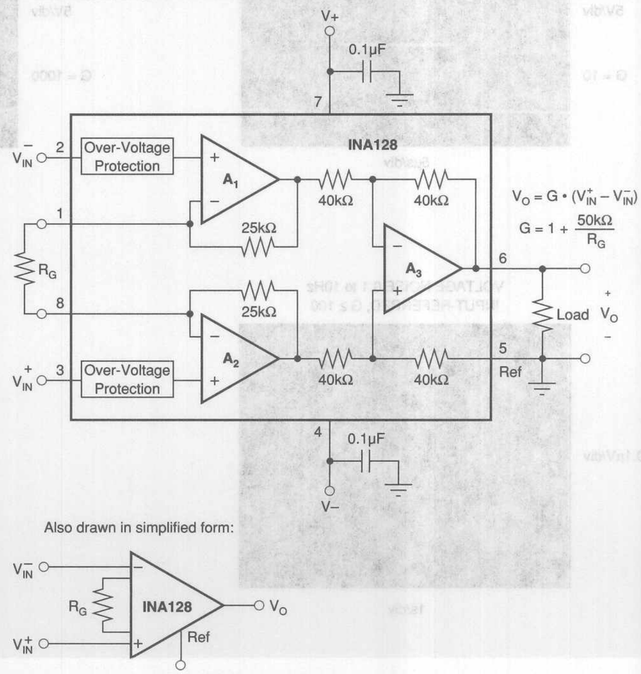


FIGURE 1. Basic Connections.

The INA128 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

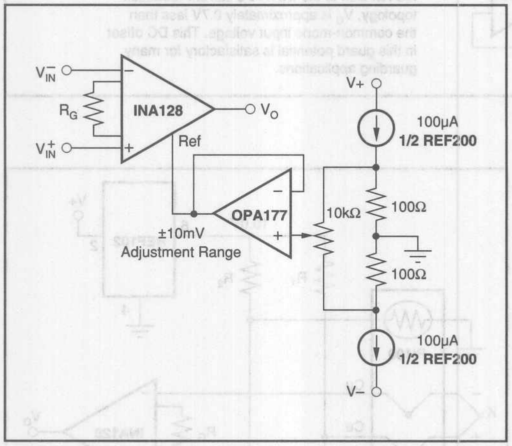


FIGURE 2. Optional Trimming of Output Offset Voltage.

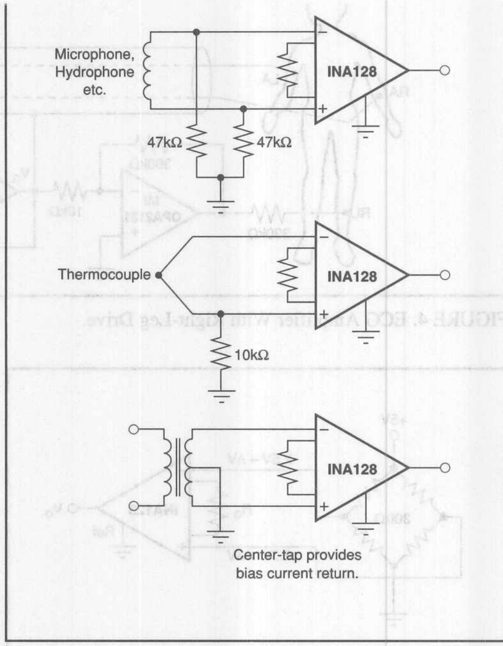


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA128 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA128 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA128 is from approximately 1.4V below the positive supply voltage to 1.7V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output voltage swing of amplifiers A_1 and A_2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage".

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA128 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA128 can be operated on power supplies as low as ±2.25V. Performance remains excellent with power supplies ranging from ±2.25V to ±18V. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for ±15V, ±5V, and ±2.5V supplies.

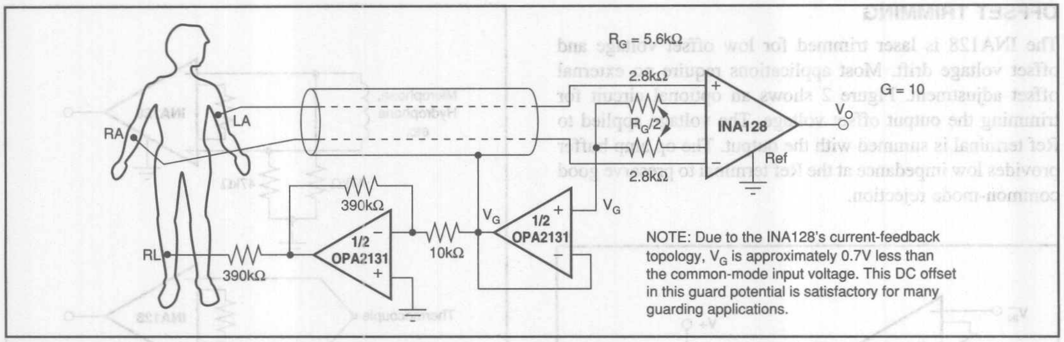


FIGURE 4. ECG Amplifier With Right-Leg Drive.

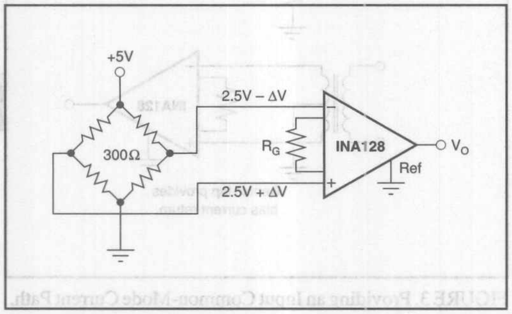


FIGURE 5. Bridge Amplifier.

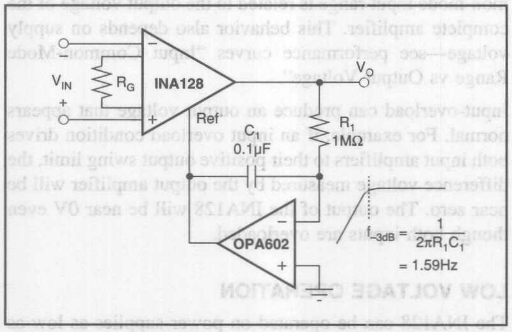
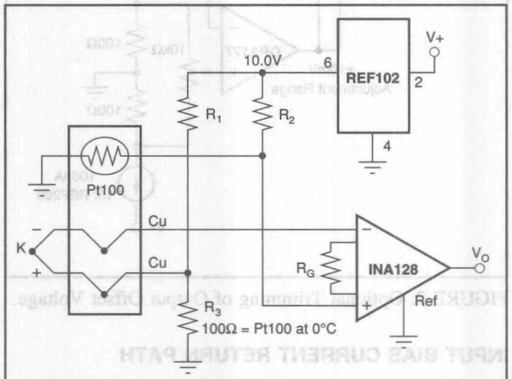
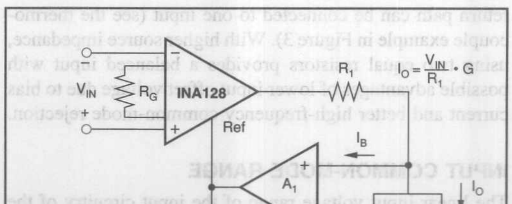


FIGURE 6. AC-Coupled Instrumentation Amplifier.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

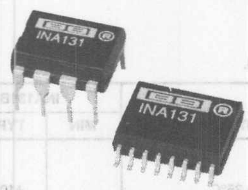
FIGURE 7. Thermocouple Amplifier With RTD Cold-Junction Compensation.



A_1	I_B Error
OPA177	±1.5nA
OPA131	50pA
OPA602	±1pA
OPA128	±75fA

FIGURE 8. Differential Voltage to Current Converter.

BURR - BROWN®



INA131

Precision G = 100 INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW DRIFT: 0.25µV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 110dB min
- INPUT OVERVOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 3mA
- 8-PIN PLASTIC DIP, SOL-16 SOIC

APPLICATIONS

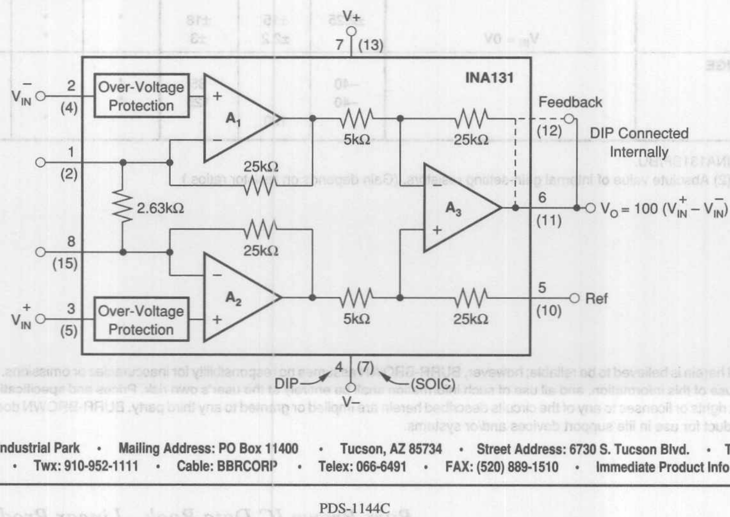
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

DESCRIPTION

The INA131 is a low cost, general purpose G = 100 instrumentation amplifier offering excellent accuracy. Its 3-op amp design and small size make it ideal for a wide range of applications.

On-chip laser trimmed resistors accurately set a fixed gain of 100. The INA131 is laser trimmed to achieve very low offset voltage (50µV), drift (0.25µV/°C), and high CMR (110dB). Internal input protection can withstand up to ±40V inputs without damage.

The INA131 is available in 8-pin plastic DIP and SOL-16 surface-mount packages. They are specified over the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

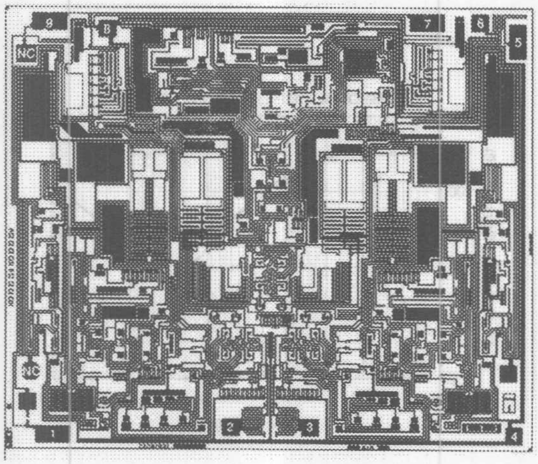
ELECTRICAL

$T_A = +25°C$, $V_S = ±15V$, $R_L = 2kΩ$, unless otherwise noted.

PARAMETER	CONDITIONS	INA131BP, BU			INA131AP, AU			
		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	$T_A = +25°C$		±10	±50		±25	±125	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		±0.1	±0.25		±0.25	±1	µV/°C
vs Power Supply	$V_S = ±2.25V$ to $±18V$		0.5	3		*	*	µV/V
Long-Term Stability			0.2			*		µV/mo
Impedance, Differential			10^{10} || 6			*		Ω || pF
Common-Mode			10^{10} || 6			*		Ω || pF
Input Common-Mode Range		±11	±13.5		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	$V_{CM} = ±10V$, $ΔR_S = 1kΩ$	110	120		106	110		dB
BIAS CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
OFFSET CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
NOISE VOLTAGE, RTI	$R_S = 0Ω$							
f = 10Hz			16			*		nV/√Hz
f = 100Hz			12			*		nV/√Hz
f = 1kHz			12			*		nV/√Hz
f = 10kHz			12			*		nV/√Hz
$f_B = 0.1Hz$ to $10Hz$			0.4			*		µVp-p
Noise Current								
f = 10Hz			0.4			*		pA/√Hz
f= 1kHz			0.2			*		pA/√Hz
$f_B = 0.1Hz$ to $100Hz$			18			*		pAp-p
GAIN								
Gain Error(1)			±0.01	±0.024		*	±0.1	%
Resistor Value(2)			±10	±40		*	*	%
Gain vs Temperature			±5	±10		*	±20	ppm/°C
Nonlinearity			±0.0003	±0.002		*	±0.004	% of FSR
OUTPUT								
Voltage	$I_O = 5mA$, T_{MIN} to T_{MAX}	±13.5	±13.7		*	*		V
	$V_S = ±11.4V$, $R_L = 2kΩ$	±10	10.5		*	*		V
	$V_S = ±2.25V$, $R_L = 2kΩ$	±1	1.5		*	*		V
Load Capacitance, max	Stable Operation		1000			*		pF
Short Circuit Current			+20/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB			70			*		kHz
Slew Rate	$V_O = ±10V$	0.3	0.7		*	*		V/µs
Settling Time, 0.01%			100			*		µs
Overload Recovery	50% Overdrive		20			*		µs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current	$V_{IN} = 0V$		±2.2	±3		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA}			100			*		°C/W

* Specification same as INA131BP/BU.

NOTES: (1) $R_L = 10kΩ$. (2) Absolute value of internal gain-setting resistors. (Gain depends on resistor ratios.)



INA131 DIE TOPOGRAPHY

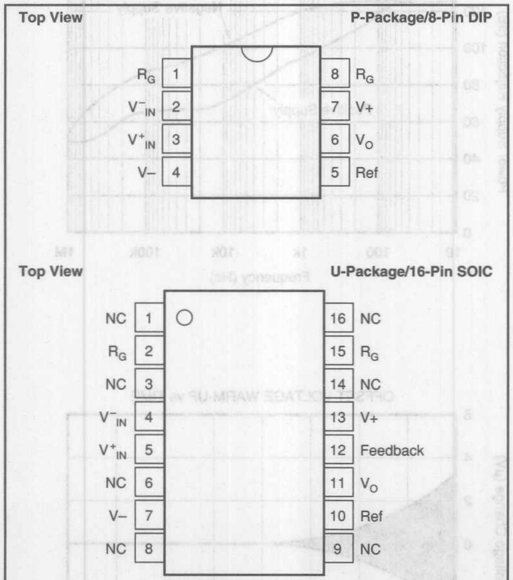
PAD	FUNCTION	PAD	FUNCTION
1	R_G	6	V_O
2	V^-_{IN}	7	Feedback
3	V^+_{IN}	8	V+
4	V–	9	R_G
5	Ref		

NC = No Connection.
Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	141 x 120 ±5	3.58 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering –10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA131AP	8-Pin Plastic DIP	–40°C to +85°C
INA131BP	8-Pin Plastic DIP	–40°C to +85°C
INA131AU	SOL-16 Surface-Mount	–40°C to +85°C
INA131BU	SOL-16 Surface-Mount	–40°C to +85°C

PACKAGE INFORMATION

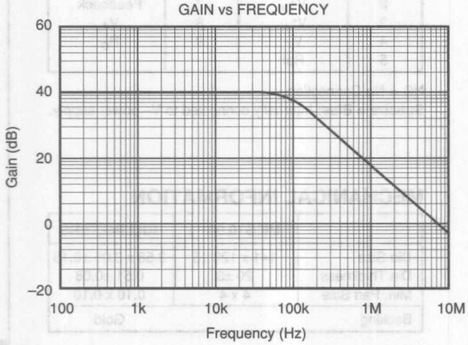
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
INA131AP	8-Pin Plastic DIP	006
INA131BP	8-Pin Plastic DIP	006
INA131AU	SOL-16 Surface-Mount	211
INA131BU	SOL-16 Surface-Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

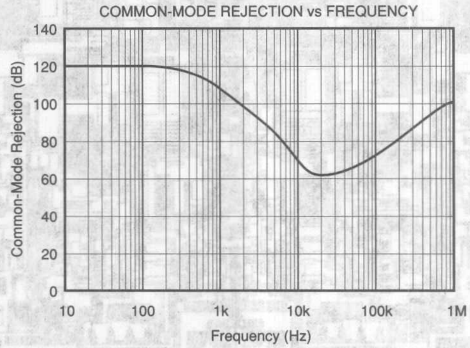
TYPICAL PERFORMANCE CURVES

At 25°C, V_S = ±15V, unless otherwise noted.

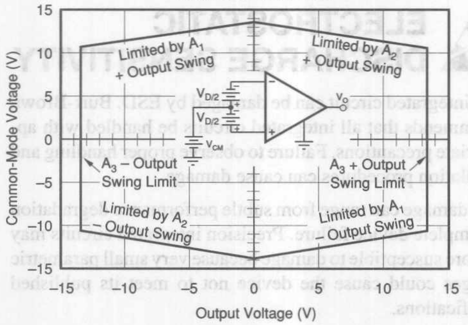
GAIN vs FREQUENCY



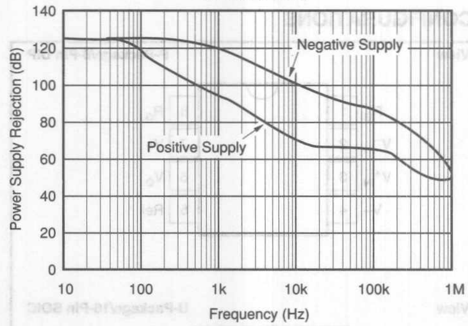
COMMON-MODE REJECTION vs FREQUENCY



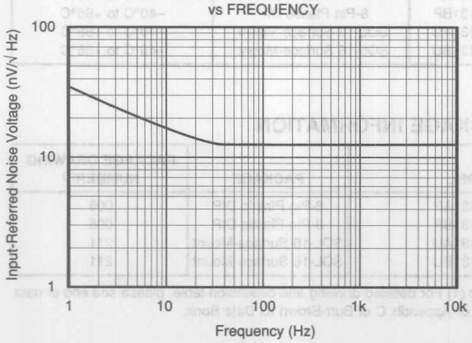
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



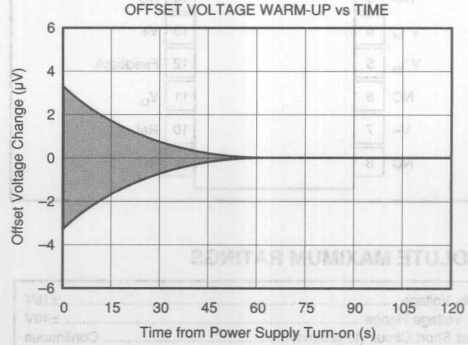
POWER SUPPLY REJECTION vs FREQUENCY



INPUT- REFERRED NOISE VOLTAGE vs FREQUENCY

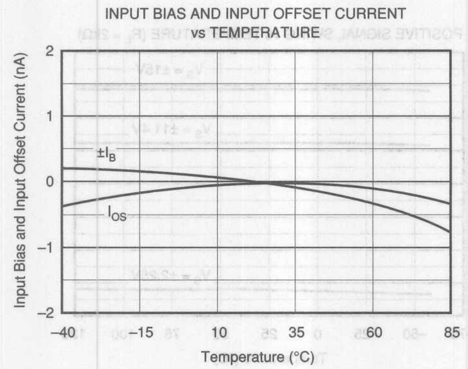


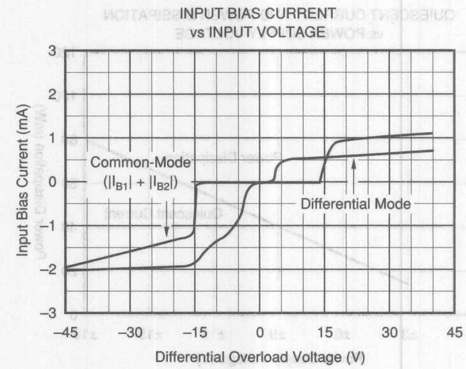
OFFSET VOLTAGE WARM-UP vs TIME

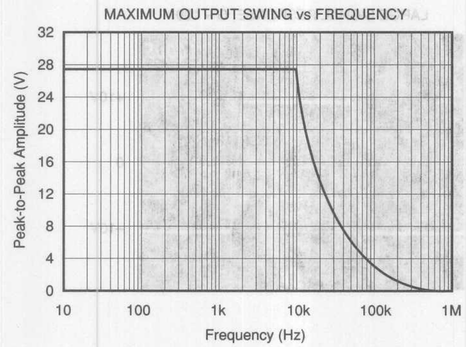


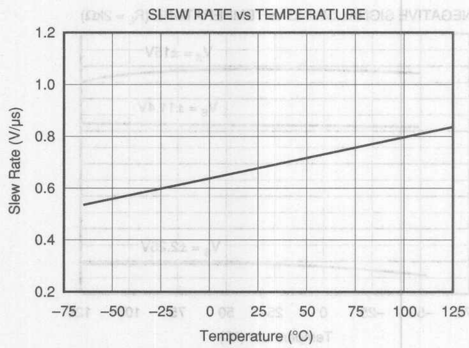
TYPICAL PERFORMANCE CURVES (CONT)

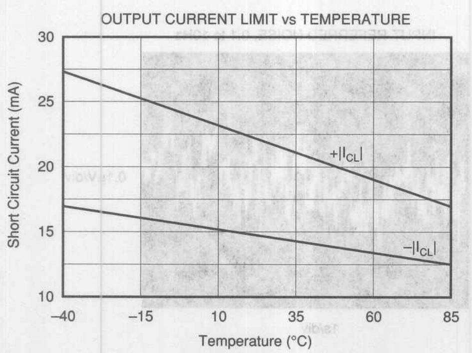
At 25°C, V_S = ±15V, unless otherwise noted.

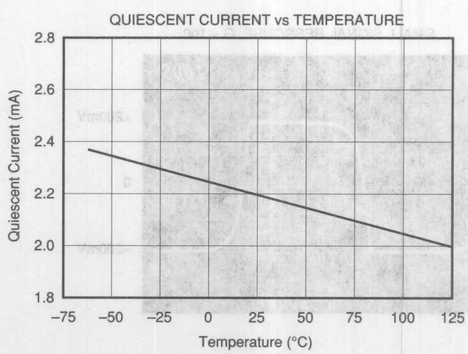








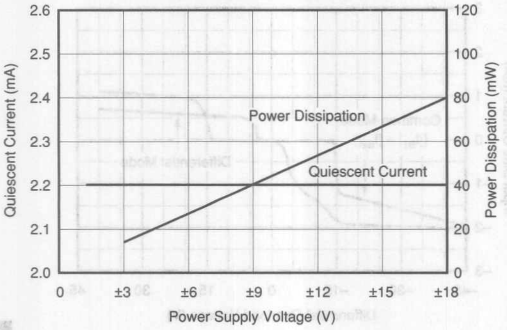




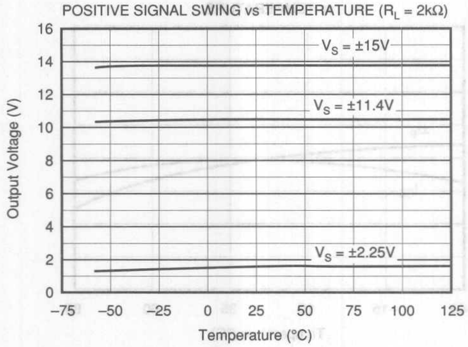
TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, $V_S = \pm15V$, unless otherwise noted.

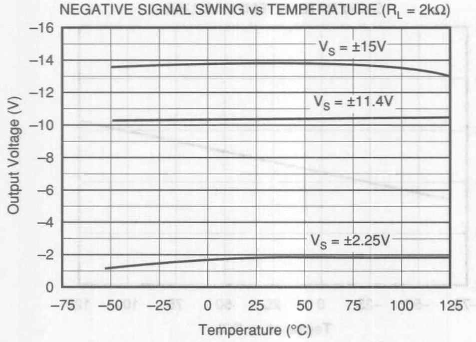
QUIESCENT CURRENT AND POWER DISSIPATION vs POWER SUPPLY VOLTAGE



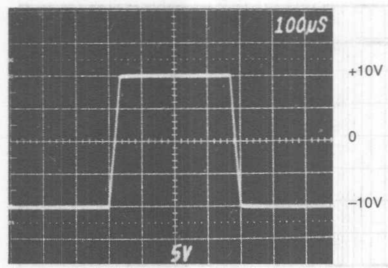
POSITIVE SIGNAL SWING vs TEMPERATURE ($R_L = 2k\Omega$)



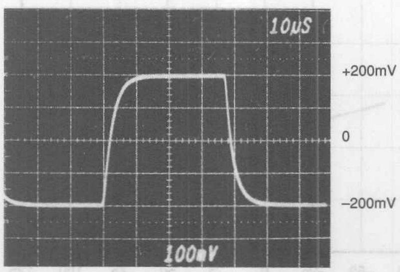
NEGATIVE SIGNAL SWING vs TEMPERATURE ($R_L = 2k\Omega$)



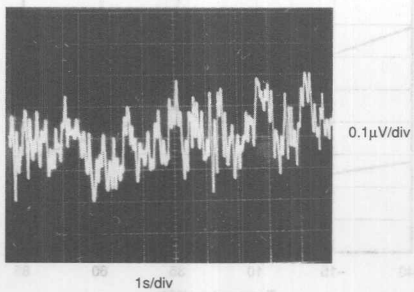
LARGE SIGNAL RESPONSE, G = 100



SMALL SIGNAL RESPONSE, G = 100



INPUT-REFERRED NOISE, 0.1 to 10Hz



BURR-BROWN®

Figure 1 shows the basic connections required for operation of the INA131. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a device with 110dB CMR to degrade to approximately 106dB CMR.

SETTING THE GAIN

No external resistors are required for G = 100. On-chip laser-trimmed resistors set the gain, providing excellent gain accuracy and temperature stability. Gain is distributed between the input and output stages of the INA131. Bandwidth is increased by approximately five times (compared to the INA114 in G = 100). Input common-mode range is also improved (see "Input Common-Mode Range").

Although the INA131 is primarily intended for fixed G = 100 applications, the gain can be increased by connecting an external resistor to the R_G pins. The internal resistors are trimmed for precise ratios, not to absolute values, so the influence of an external resistor will vary from device to

calculated by:

$$G = 100 + \frac{250\ \text{k}\Omega}{R_G} \quad (1)$$

Where: R_G is the external gain resistor.

Accuracy of the 250kΩ term is ±40%.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1).

NOISE PERFORMANCE

The INA131 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low frequency noise of the INA131 is approximately 0.4µVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of state-of-the-art chopper-stabilized amplifiers.

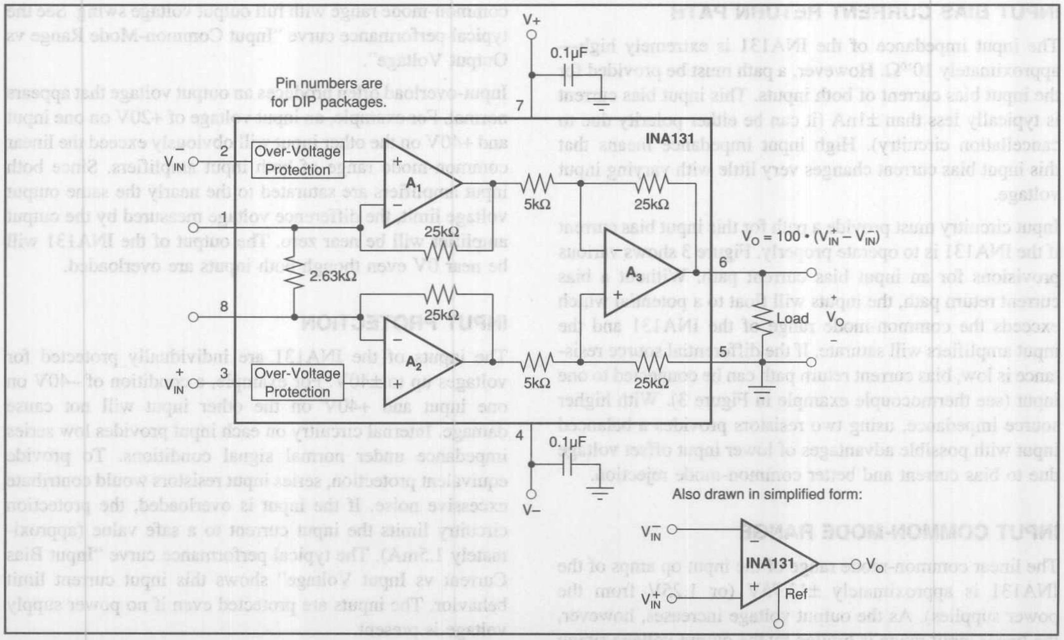


FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA131 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering trim voltage with an op amp as shown.

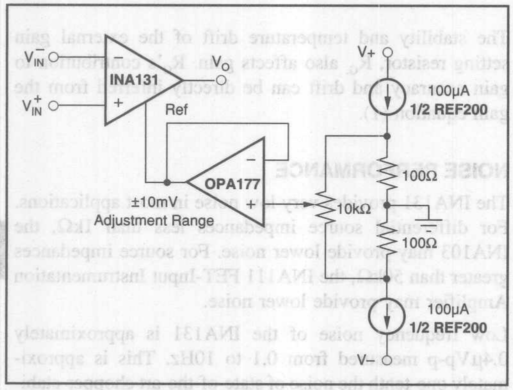


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA131 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA131 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA131 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA131 is approximately ±13.75V (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range is limited by the output voltage swing of the input amplifiers, A_1 and A_2. The 5V/V output stage gain of the INA131 reduces this effect. Compared to the INA114 and other unity output gain instrumentation amplifiers, the INA131 provides several additional volts of input common-mode range with full output voltage swing. See the typical performance curve "Input Common-Mode Range vs Output Voltage".

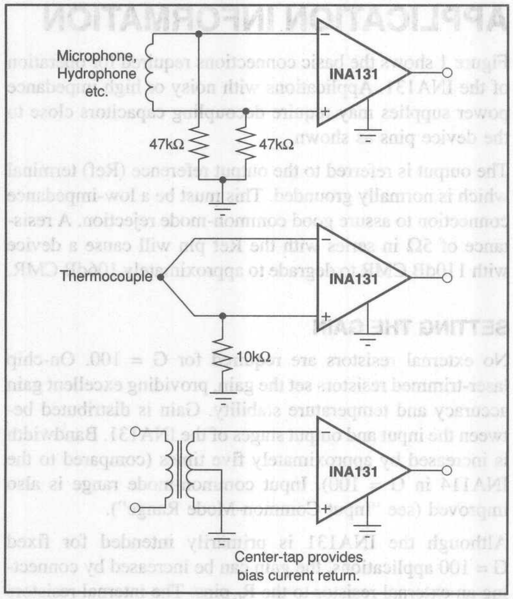


FIGURE 3. Providing an Input Common-Mode Current Path.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA131 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA131 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

OUTPUT VOLTAGE SENSE (SOL-16 package only)

The surface-mount version of the INA131 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA131.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. Figure 4 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through C_1. Heavy loads or long lines can be driven by connecting a buffer inside the feedback path (Figure 5).

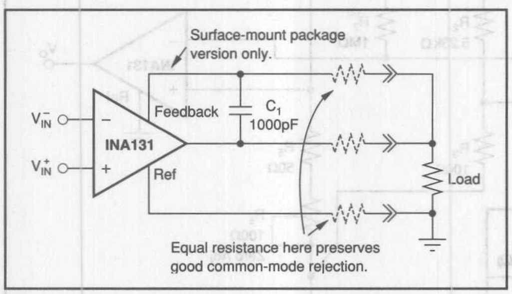


FIGURE 4. Remote Load and Ground Sensing.

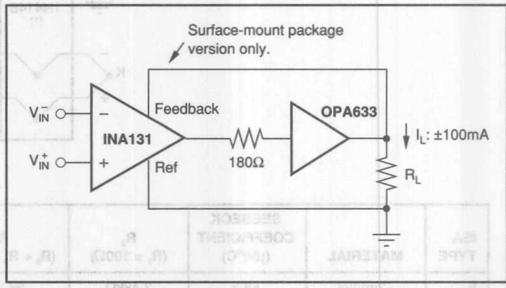


FIGURE 5. Buffered Output for Heavy Loads.

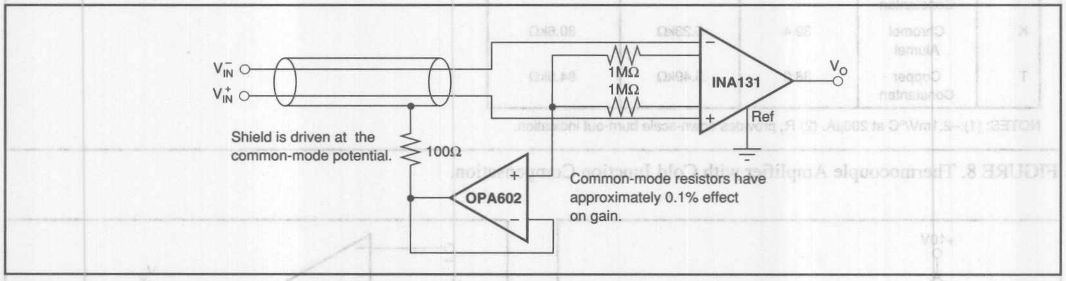


FIGURE 6. Shield Driver Circuit.

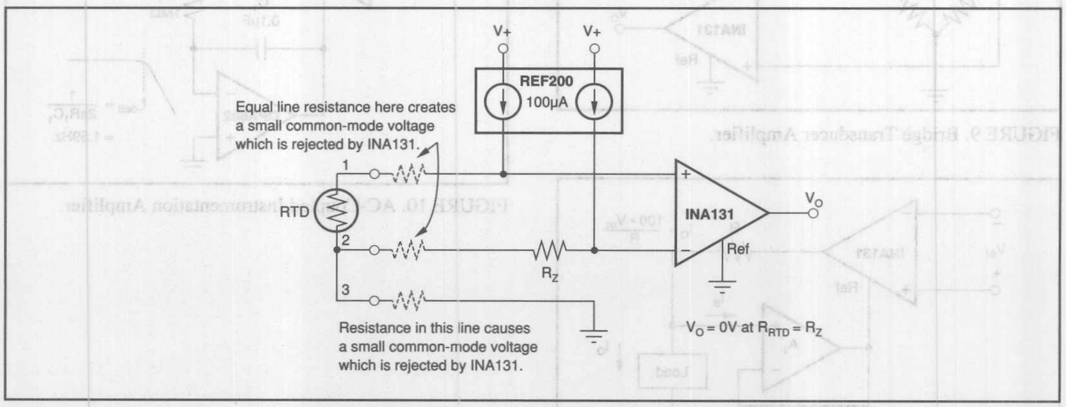
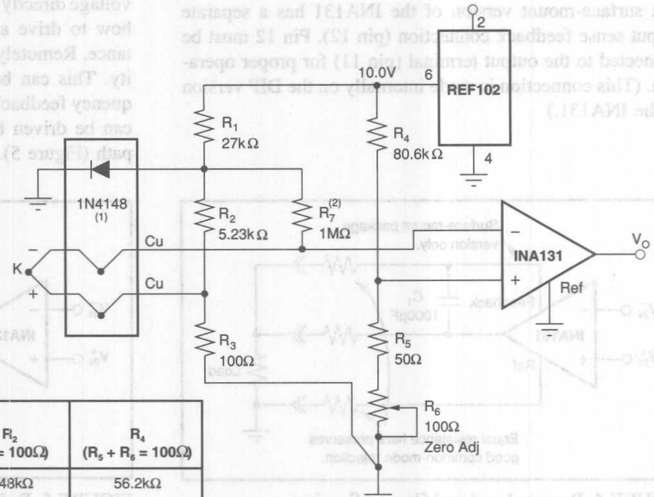


FIGURE 7. RTD Temperature Measurement Circuit.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

NOTES: (1) –2.1mV/°C at 200μA. (2) R_7 provides down-scale burn-out indication.

FIGURE 8. Thermocouple Amplifier with Cold Junction Compensation.

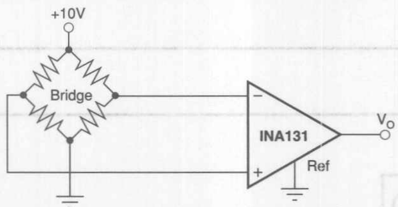


FIGURE 9. Bridge Transducer Amplifier.

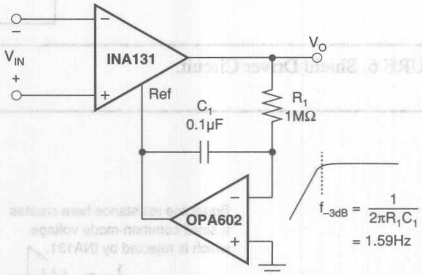
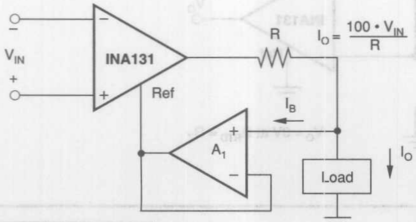


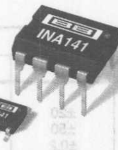
FIGURE 10. AC-Coupled Instrumentation Amplifier.



A_1	I_B Error
OPA177	±1.5nA
OPA602	1pA
OPA128	75fA

FIGURE 11. Differential Voltage to Current Converter.

BURR - BROWN®



INA141

Precision, Low Power, G = 10, 100 INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.5μV/°C max
- ACCURATE GAIN: ±0.05% at G = 10
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 117dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 750μA
- 8-PIN PLASTIC DIP, SO-8

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

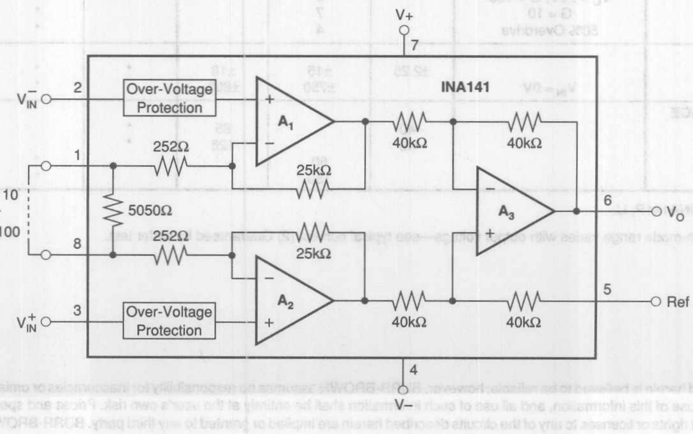
DESCRIPTION

The INA141 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

Simple pin connections set an accurate gain of 10 or 100V/V without external resistors. Internal input protection can withstand up to ±40V without damage.

The INA141 is laser trimmed for very low offset voltage (50μV), drift (0.5μV/°C) and high common-mode rejection (117dB at G = 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 750μA—ideal for battery operated systems.

The INA141 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

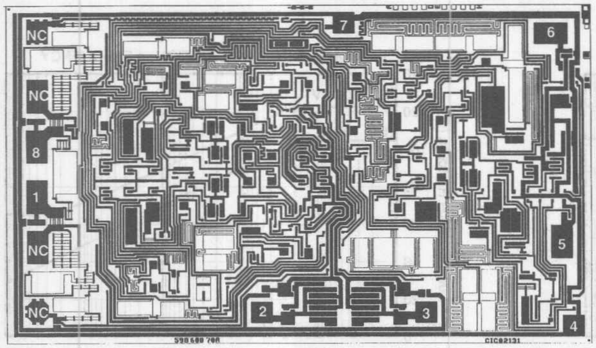
At $T_A = +25°C$, $V_S = ±15V$, and $R_L = 10kΩ$, unless otherwise noted.

		INA141P, U			INA141PA, UA			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
Offset Voltage, RTI	G = 100		±20	±50		*	±125	μV
	G = 10		±50	±100		*	±250	μV
vs Temperature	G = 100		±0.2	±0.5		*	±1.5	μV/°C
	G = 10(2)		±0.5	±2		*	±2.5	μV/°C
vs Power Supply	V_S = ±2.25 to ±18V, G = 100		±0.4	±1		*	±3	μV/V
	G = 10		±2	±10		*	±20	μV/V
Long-Term Stability	G = 100		0.2			*		μV/mo
	G = 10		0.5			*		μV/mo
Impedance, Differential			10^{10} ∥ 2			*		Ω ∥ pF
Common-Mode			10^{10} ∥ 9			*		Ω ∥ pF
Common-Mode Voltage Range(1)	V_O = 0V	(V+) – 2	(V+) – 1.4		*	*		V
		(V–) + 2	(V–) + 1.7		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = ±13V, $ΔR_S$ = 1kΩ							
	G = 100	117	125		110	120		dB
	G = 10	100	106		93	100		dB
BIAS CURRENT			±2	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
Offset Current			±1	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
NOISE VOLTAGE, RTI								
f = 10Hz	G = 100, R_S = 0Ω		10			*		nV/√Hz
f = 100Hz			8			*		nV/√Hz
f = 1kHz			8			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.2			*		μVp-p
f = 10Hz	G = 10, R_S = 0Ω		22			*		nV/√Hz
f = 100Hz			13			*		nV/√Hz
f = 1kHz			12			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.6			*		μVp-p
Noise Current								
f = 10Hz			0.9			*		pA/√Hz
f = 1kHz			0.3			*		pA/√Hz
f_B = 0.1Hz to 10Hz			30			*		pAp-p
GAIN								
Gain Error	V_O = ±13.6V, G = 100		±0.03	±0.075		*	±0.15	%
	G = 10		±0.01	±0.05		*	±0.15	%
Gain vs Temperature(2)	G = 10, 100		±2	±10		*	*	ppm/°C
Nonlinearity	G = 100		±0.0005	±0.002		*	±0.004	% of FSR
	G = 10		±0.0003	±0.001		*	±0.002	% of FSR
OUTPUT								
Voltage: Positive	R_L = 10kΩ	(V+) – 1.4	(V+) – 0.9		*	*		V
Negative	R_L = 10kΩ	(V–) + 1.4	(V–) + 0.9		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+6/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 100		200			*		kHz
	G = 10		1			*		MHz
Slew Rate	V_O = ±10V, G = 10		4			*		V/μs
Settling Time, 0.01%	V_O = ±5V, G = 100		9			*		μs
	G = 10		7			*		μs
Overload Recovery	50% Overdrive		4			*		μs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current, Total	V_{IN} = 0V		±750	±800		*	*	μA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
$θ_{JA}$ 8-Pin DIP			80			*		°C/W
SO-8 SOIC			150			*		°C/W

* Specification same as INA141P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.

DICE INFORMATION



INA141 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	J	5	Ref
2	V^-_{IN}	6	V_O
3	V^+_{IN}	7	V+
4	V–	8	J

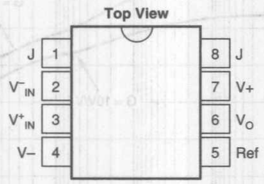
NC = No Connection.
Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	128 x 76 ±5	3.05 x 1.78 ±0.13
Die Thickness	14 ±3	0.36 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

PIN CONFIGURATION

8-Pin DIP and SO-8



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

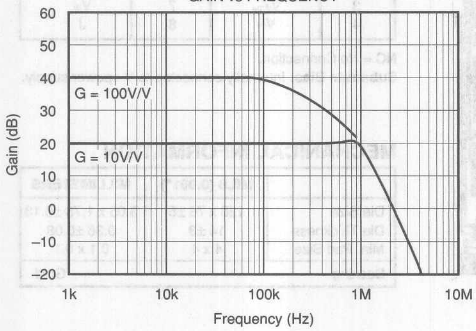
ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
INA141PA	8-Pin Plastic DIP	006	–40°C to +85°C
INA141P	8-Pin Plastic DIP	006	–40°C to +85°C
INA141UA	SO-8 Surface-Mount	182	–40°C to +85°C
INA141U	SO-8 Surface-Mount	182	–40°C to +85°C

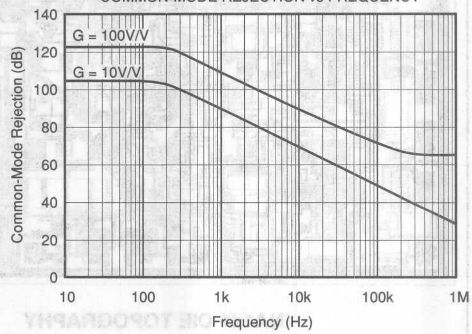
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

At $T_A = +25°C$ and $V_S = \pm15V$, unless otherwise noted.

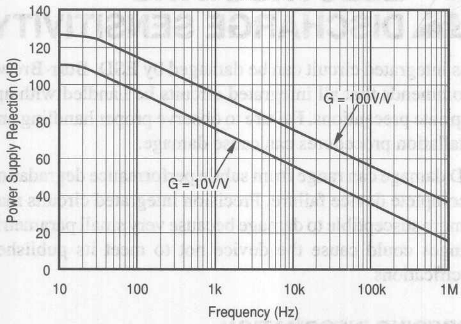
GAIN vs FREQUENCY



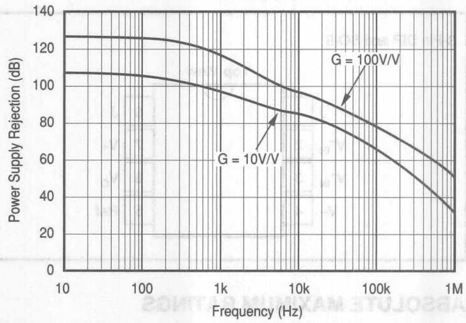
COMMON-MODE REJECTION vs FREQUENCY



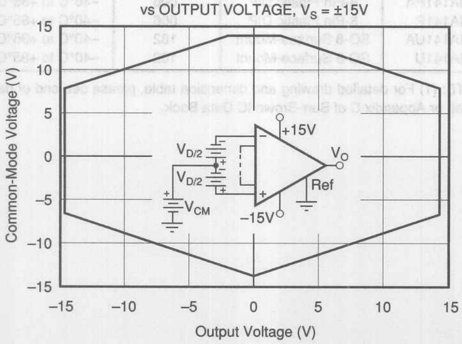
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



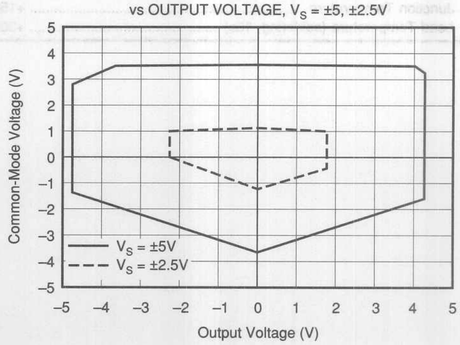
NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



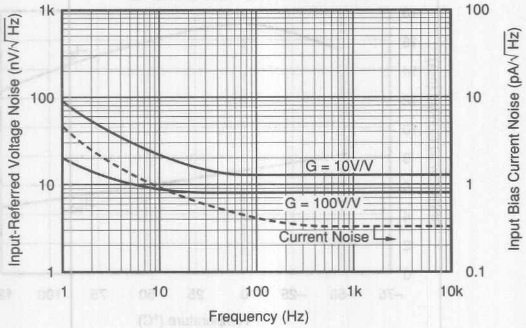
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, $V_S = \pm15V$



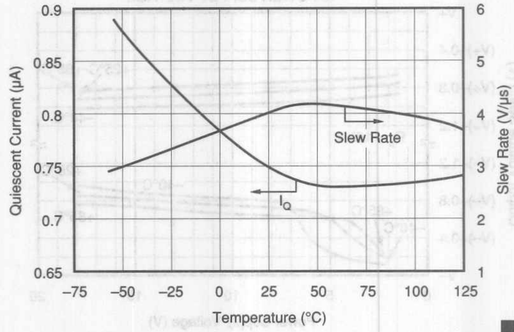
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, $V_S = \pm5, \pm2.5V$



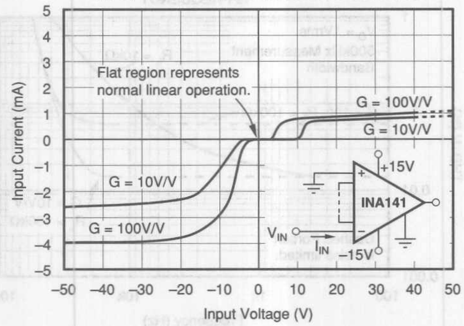
INPUT- REFERRED NOISE vs FREQUENCY



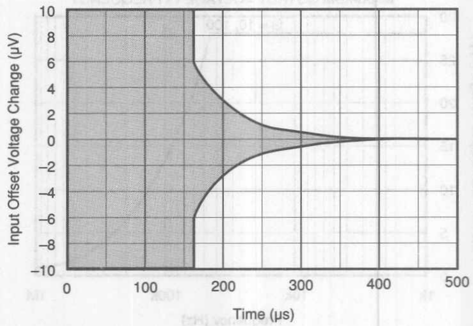
QUIESCENT CURRENT and SLEW RATE vs TEMPERATURE



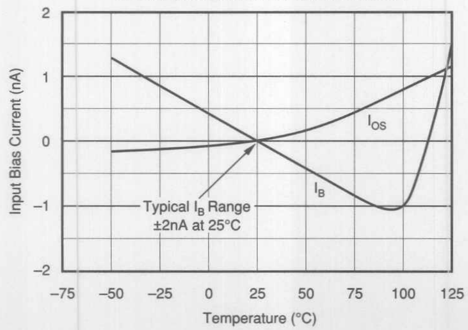
INPUT OVER-VOLTAGE V/I CHARACTERISTICS



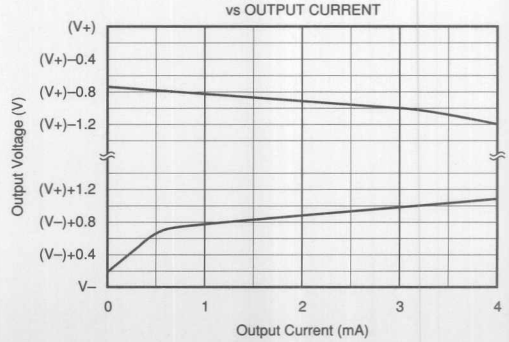
INPUT OFFSET VOLTAGE WARM-UP



INPUT BIAS CURRENT vs TEMPERATURE

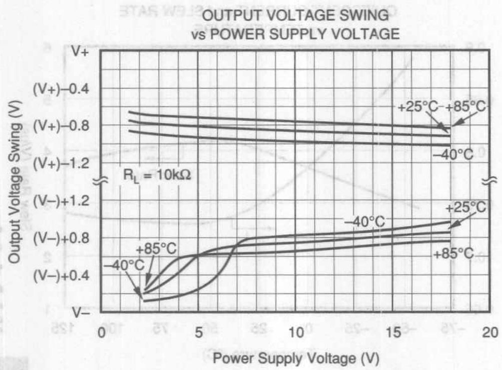


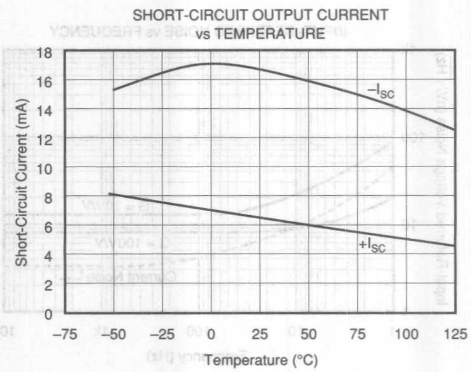
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

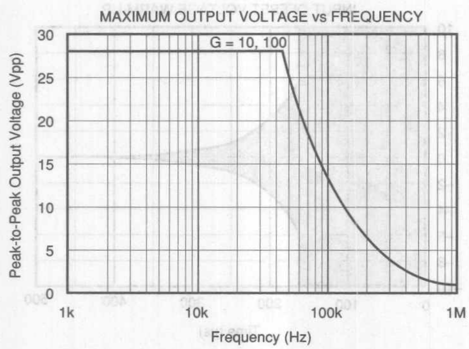


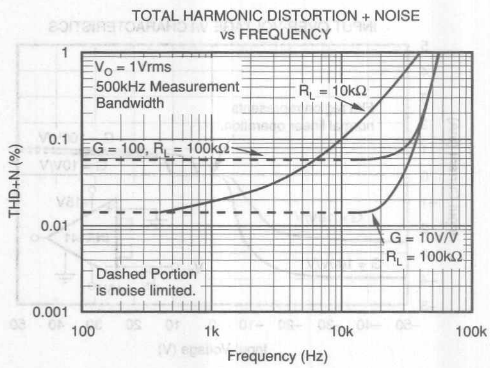
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$ and $V_S = \pm15V$, unless otherwise noted.









TYPICAL PERFORMANCE CURVES (CONT)

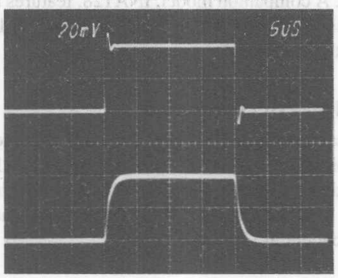
At $T_A = +25°C$ and $V_S = \pm15V$, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE

G = 10

20mV/div

G = 100



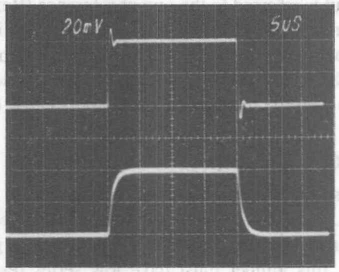
5µs/div

LARGE-SIGNAL STEP RESPONSE

G = 10

5V/div

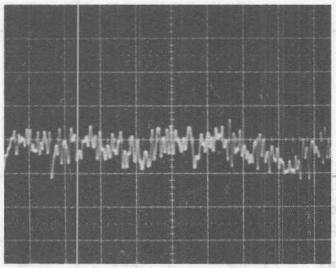
G = 100



5µs/div

VOLTAGE NOISE 0.1 to 10Hz
INPUT-REFERRED, G = 100

0.1µV/div



1s/div

Figure 1 shows the basic connections required for operation of the INA141. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain is selected with a jumper connection as shown in Figure 1. G = 10V/V with no jumper installed. With a jumper installed, G = 100V/V. To preserve good gain accuracy, this jumper must have low series resistance. A resistance of 0.5Ω in series with the jumper will decrease the gain by 0.1%.

Internal resistor ratios are laser trimmed to assure excellent gain accuracy. Actual resistor values can vary by approximately ±25% from the nominal values shown.

Gains between 10 and 100 can be achieved by connecting an external resistor to the jumper pins. This is not recommended, however, because the ±25% variation of internal resistor values makes the required external resistor value uncertain. A companion model, INA128, features accurately trimmed internal resistors so that gains from 1 to 10,000 can be set with an external resistor.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA141 achieves wide bandwidth, even at G = 100. This is due to the current-feedback topology of the INA141. Settling time also remains excellent at G = 100.

NOISE PERFORMANCE

The INA141 provides very low noise in most applications. Low frequency noise is approximately 0.2µVp-p measured from 0.1 to 10Hz (G = 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

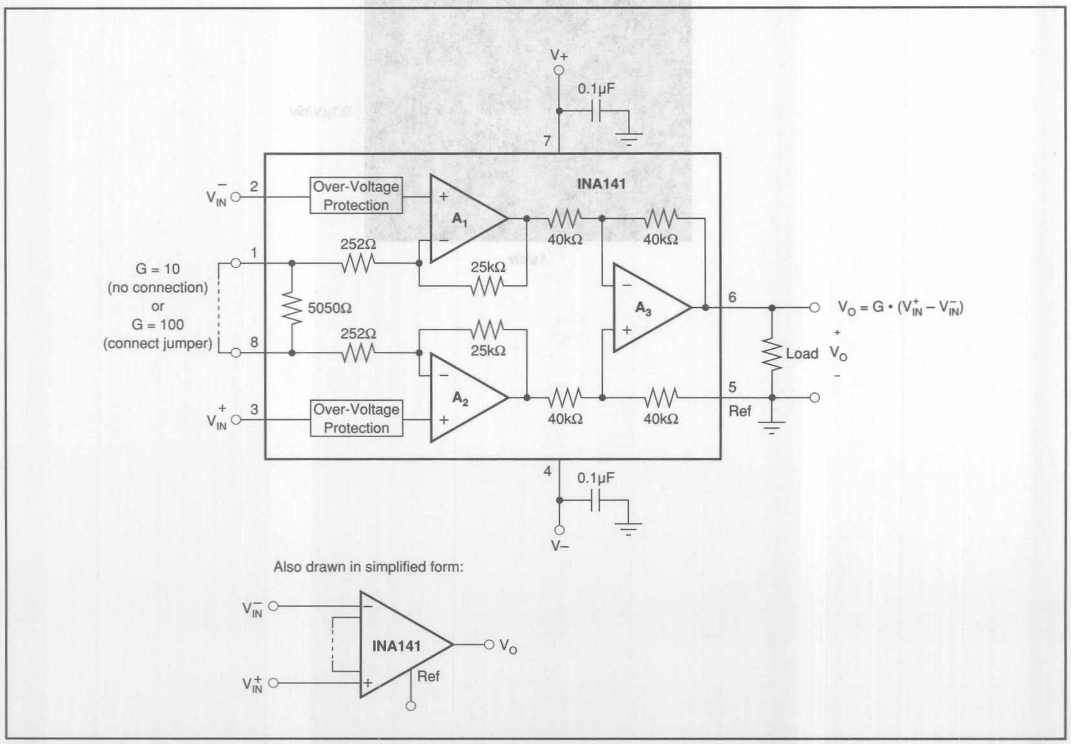


FIGURE 1. Basic Connections.

offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

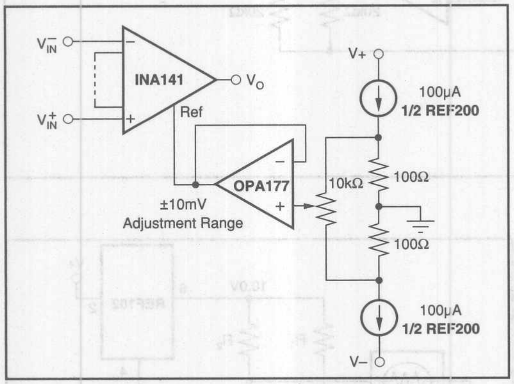


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA141 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA141 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA141 is from approximately 1.4V below the positive supply voltage to 1.7V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range will be limited by the output voltage swing of amplifiers A_1 and A_2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage".

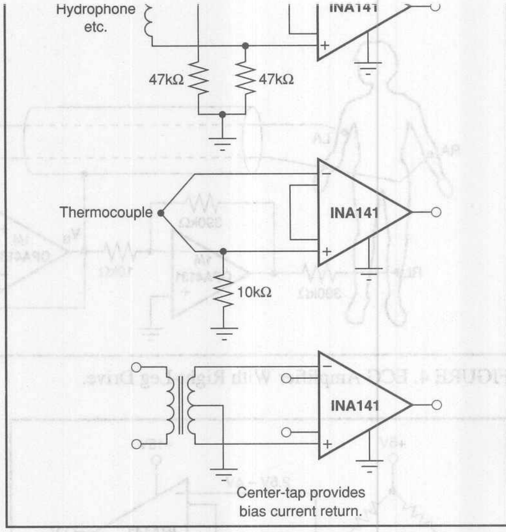


FIGURE 3. Providing an Input Common-Mode Current Path.

Input overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA141 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA141 can be operated on power supplies as low as ±2.25V. Performance remains excellent with power supplies ranging from ±2.25V to ±18V. Most parameters vary only slightly through this supply voltage range—see Typical Performance Curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for ±15V, ±5, and ±2.5V supplies.

INPUT PROTECTION

The inputs of the INA141 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5mA. The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

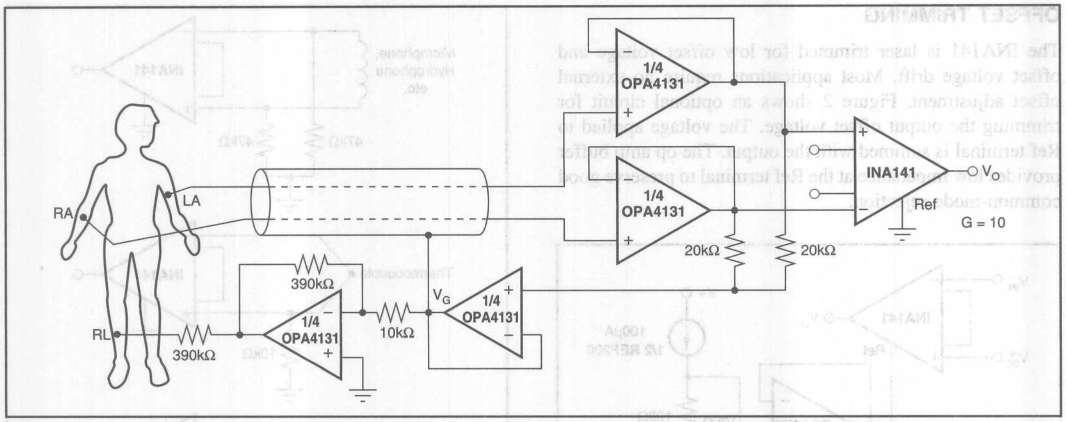


FIGURE 4. ECG Amplifier With Right-Leg Drive.

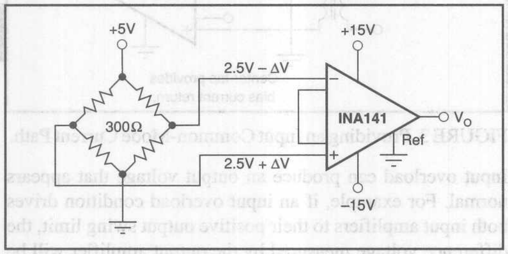


FIGURE 5. Bridge Amplifier.

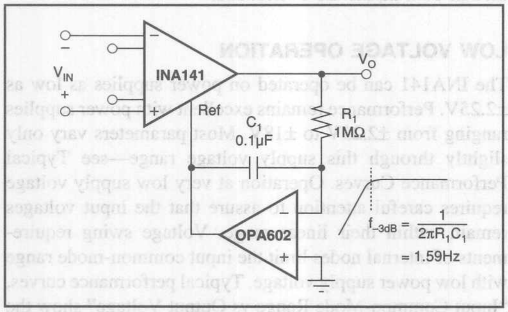
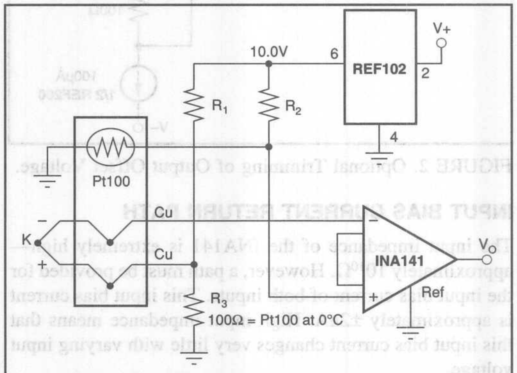
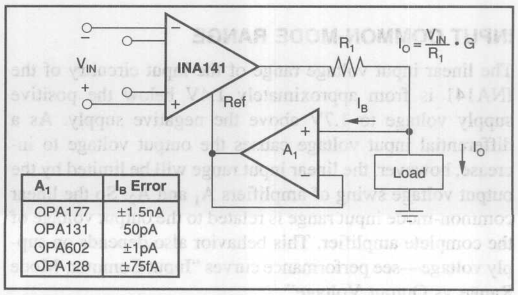


FIGURE 6. AC-Coupled Instrumentation Amplifier.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

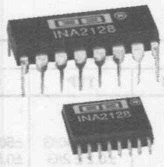
FIGURE 7. Thermocouple Amplifier With RTD Cold-Junction Compensation.



A_1	I_B Error
OPA177	±1.5nA
OPA131	50pA
OPA602	±1pA
OPA128	±75fA

FIGURE 8. Differential Voltage to Current Converter.

BURR - BROWN®



INA2128

Dual, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW DRIFT: 0.5µV/°C max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 120dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±2.25V to ±18V
- LOW QUIESCENT CURRENT: 700µA / IA
- 16-PIN PLASTIC DIP, SOL-16

APPLICATIONS

- SENSOR AMPLIFIER THERMOCOUPLE, RTD, BRIDGE
- MEDICAL INSTRUMENTATION
- MULTIPLE-CHANNEL SYSTEMS
- BATTERY OPERATED EQUIPMENT

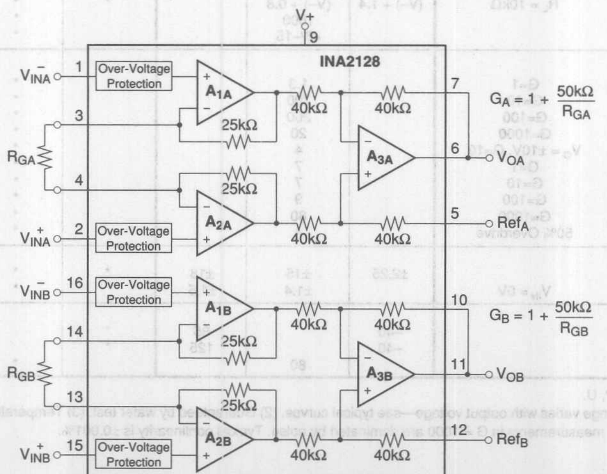
DESCRIPTION

The INA2128 is a dual, low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA2128 is laser trimmed for very low offset voltage (50µV), drift (0.5µV/°C) and high common-mode rejection (120dB at G ≥ 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 700µA per IA—ideal for battery operated and multiple-channel systems.

The INA2128 is available in 16-pin plastic DIP, and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.



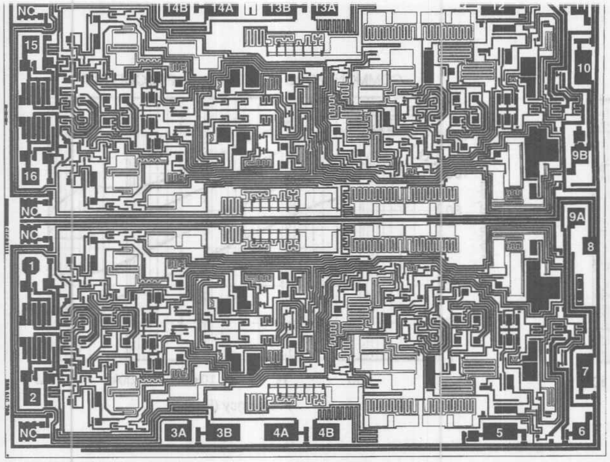
International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ unless otherwise noted.

PARAMETER	CONDITIONS	INA2128P, U MIN	INA2128P, U TYP	INA2128P, U MAX	INA2128PA, UA MIN	INA2128PA, UA TYP	INA2128PA, UA MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±10 ±100/G	±50 ±500/G		±25 ±100/G	±125 ±1000/G	µV
vs Temperature	T_A = T_{MIN} to T_{MAX}		±0.2 ± 2/G	±0.5 ± 20/G		±0.2 ± 5/G	±1 ± 20/G	µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		±0.2 ±20/G	±1 ±100/G		*	±2 ±200/G	µV/V
Long-Term Stability			±0.1 ±3/G			*		µV/mo
Impedance, Differential			10^{10} || 2			*		Ω || pF
Common-Mode			10^{11} || 9			*		Ω || pF
Common-Mode Voltage Range(1)	V_O = 0V	(V+) – 2	(V+) – 1.4		*	*		V
		(V–) + 2	(V–) + 1.7		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = ±13V, ΔR_S = 1kΩ							
	G=1	80	86		73	*		dB
	G=10	100	106		93	*		dB
	G=100	120	125		110	*		dB
	G=1000	120	130		110	*		dB
BIAS CURRENT			±2	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
Offset Current			±1	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
NOISE VOLTAGE, RTI	G = 1000, R_S = 0Ω							
f = 10Hz			10			*		nV/√Hz
f = 100Hz			8			*		nV/√Hz
f = 1kHz			8			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.2			*		µVp-p
Noise Current								
f=10Hz			0.9			*		pA/√Hz
f=1kHz			0.3			*		pA/√Hz
f_B = 0.1Hz to 10Hz			30			*		pAp-p
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G=1		±0.01	±0.024		*	±0.1	%
	G=10		±0.02	±0.4		*	±0.5	%
	G=100		±0.05	±0.5		*	±0.7	%
	G=1000		±0.5	±1		*	±2	%
Gain vs Temperature(2)	G=1		±1	±10		*	*	ppm/°C
50kΩ Resistance(2, 3)			±25	±100		*	*	ppm/°C
Nonlinearity	V_O = ±13.6V, G=1		±0.0001	±0.001		*	±0.002	% of FSR
	G=10		±0.0003	±0.002		*	±0.004	% of FSR
	G=100		±0.0005	±0.002		*	±0.004	% of FSR
	G=1000		±0.001	(Note 4)		*	*	% of FSR
OUTPUT								
Voltage: Positive	R_L = 10kΩ	(V+) – 1.4	(V+) – 0.9		*	*		V
Negative	R_L = 10kΩ	(V–) + 1.4	(V–) + 0.8		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+6/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G=1		1.3			*		MHz
	G=10		700			*		kHz
	G=100		200			*		kHz
	G=1000		20			*		kHz
Slew Rate	V_O = ±10V, G=10		4			*		V/µs
Settling Time, 0.01%	G=1		7			*		µs
	G=10		7			*		µs
	G=100		9			*		µs
	G=1000		80			*		µs
Overload Recovery	50% Overdrive		4			*		µs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current, Total	V_{IN} = 0V		±1.4	±1.5		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as INA2128P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test. (3) Temperature coefficient of the "50kΩ" term in the gain equation. (4) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.



INA2128 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	V_{INA}^-	9	V+
2	V_{INA}^+	10	$Sense_B$
3	R_{GA}	11	V_{OB}
4	R_{GA}	12	Ref_B
5	Ref_A	13	R_{GB}
6	V_{OA}	14	R_{GB}
7	$Sense_A$	15	V_{INB}^+
8	V–	16	V_{INB}^-

NC = No Connection.
NOTES: (1) Connect both indicated pads.
Substrate Bias: Internally connected to V– power supply.

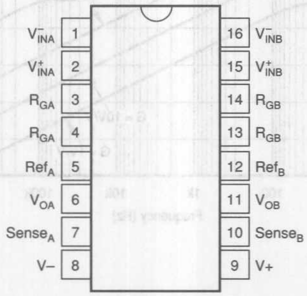
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	163 x 130 ±5	4.14 x 3.30 ±0.13
Die Thickness	18 ±3	0.45 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

PIN CONFIGURATION

Top View

DIP
SOL-16



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

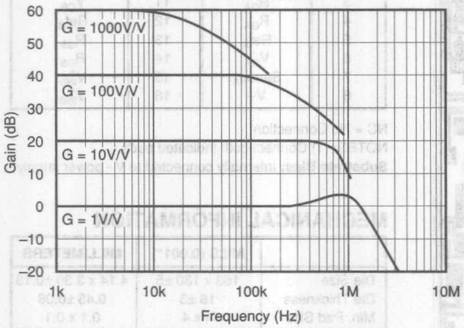
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]	TEMPERATURE RANGE
INA2128PA	16-Pin Plastic DIP	180	–40°C to +85°C
INA2128P	16-Pin Plastic DIP	180	–40°C to +85°C
INA2128UA	SOL-16 Surface-Mount	211	–40°C to +85°C
INA2128U	SOL-16 Surface-Mount	211	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

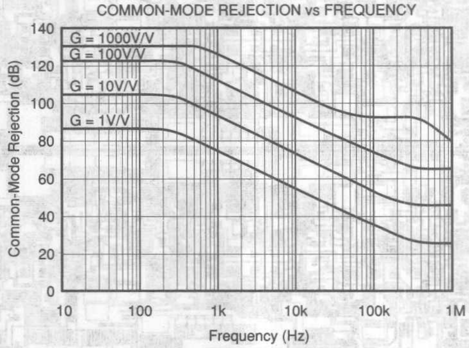
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, $V_S = \pm 15V$, unless otherwise noted.

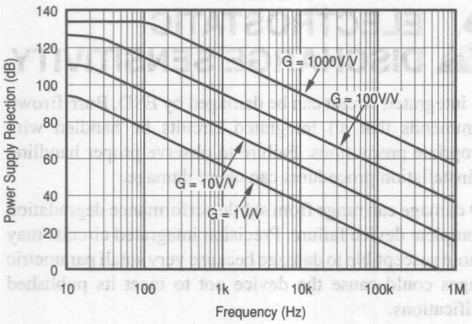
GAIN vs FREQUENCY



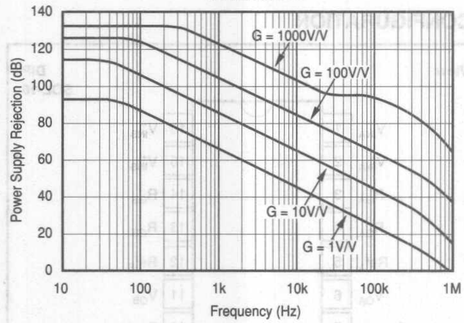
COMMON-MODE REJECTION vs FREQUENCY



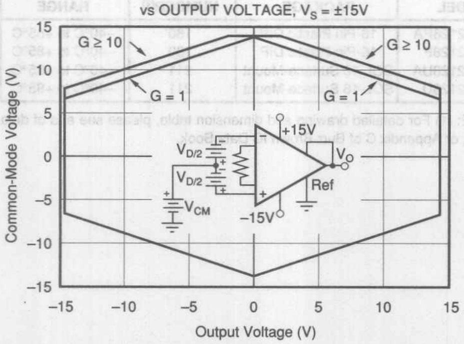
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



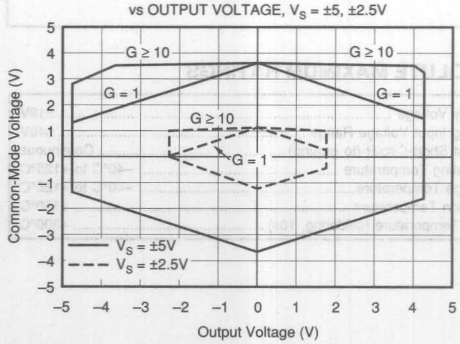
NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, $V_S = \pm 15V$



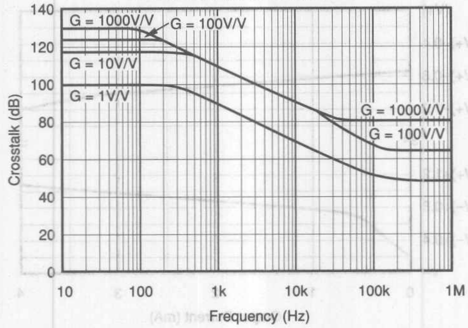
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, $V_S = \pm 5, \pm 2.5V$



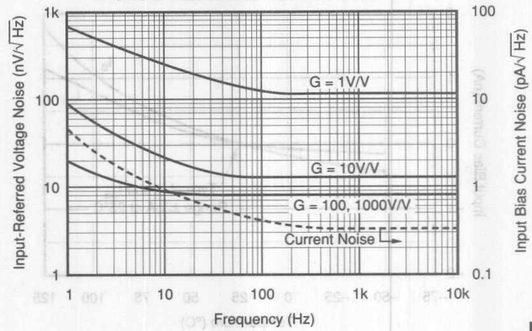
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = ±15V$, unless otherwise noted.

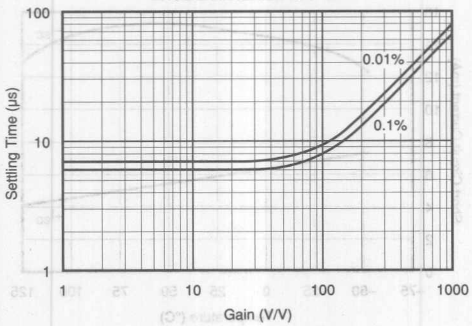
CROSSTALK vs FREQUENCY



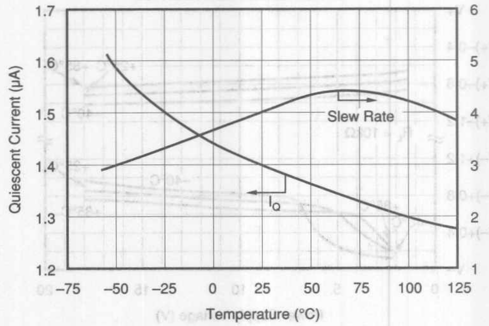
INPUT- REFERRED NOISE vs FREQUENCY



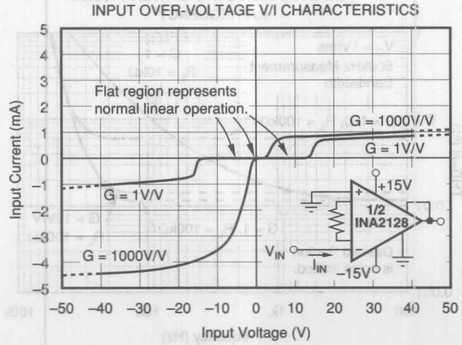
SETTLING TIME vs GAIN



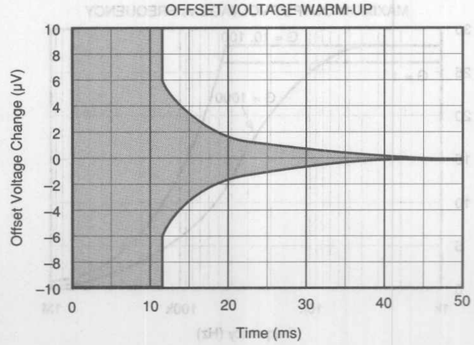
QUIESCENT CURRENT and SLEW RATE vs TEMPERATURE



INPUT OVER-VOLTAGE V/I CHARACTERISTICS



OFFSET VOLTAGE WARM-UP



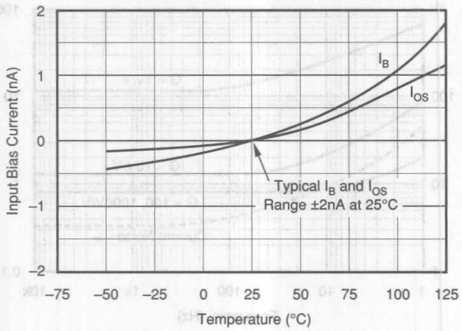
INA2128

4

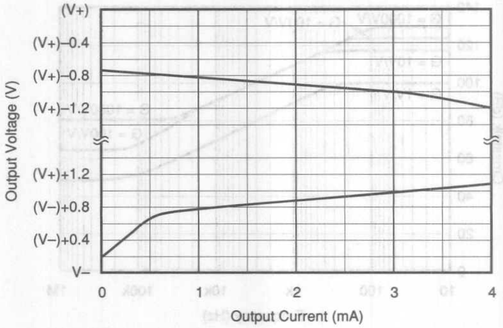
INSTRUMENTATION AMPLIFIERS

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

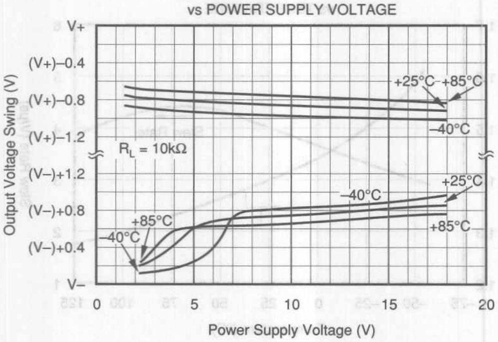
INPUT BIAS CURRENT vs TEMPERATURE



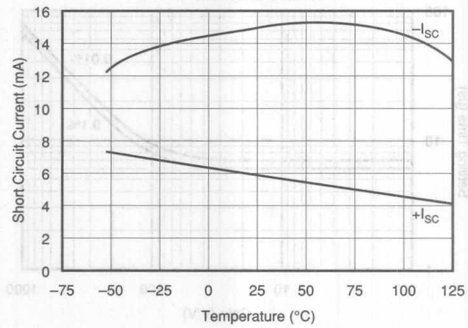
OUTPUT VOLTAGE SWING
vs OUTPUT CURRENT



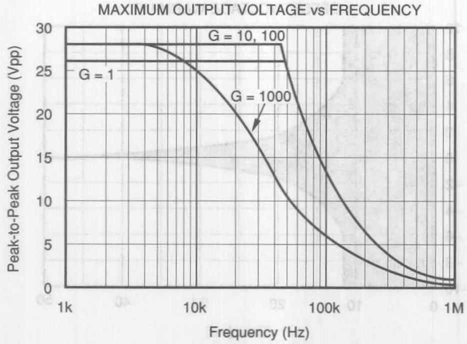
OUTPUT VOLTAGE SWING
vs POWER SUPPLY VOLTAGE



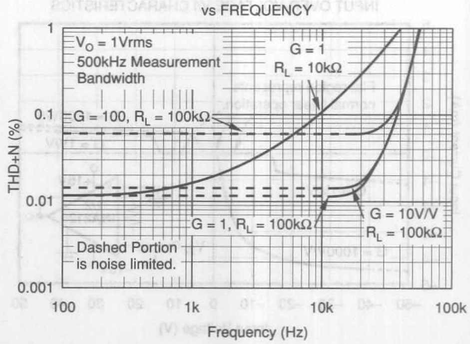
SHORT-CIRCUIT OUTPUT CURRENT
vs TEMPERATURE



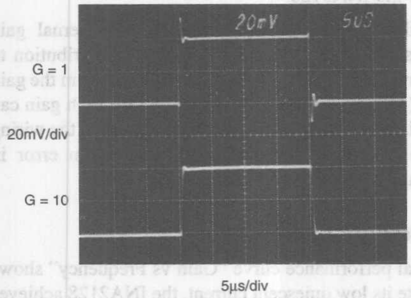
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



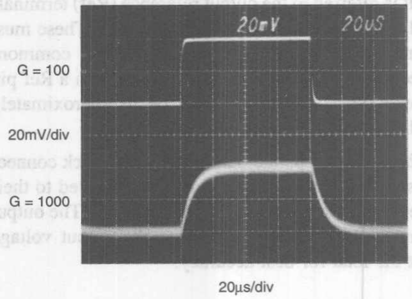
TOTAL HARMONIC DISTORTION + NOISE
vs FREQUENCY



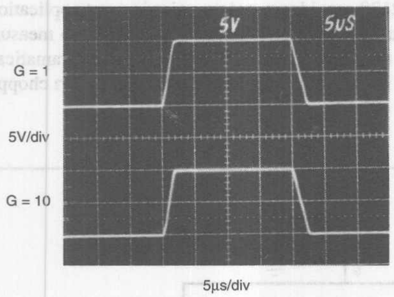
SMALL-SIGNAL STEP RESPONSE
(G = 1, 10)



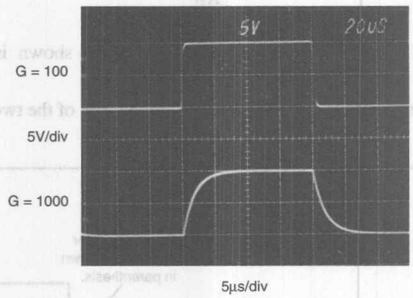
SMALL-SIGNAL STEP RESPONSE
(G = 100, 1000)



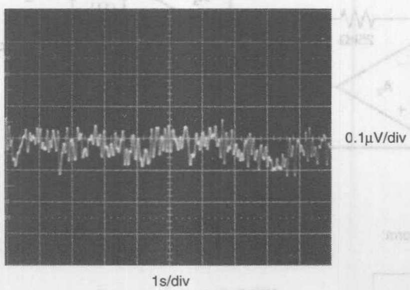
LARGE-SIGNAL STEP RESPONSE
(G = 1, 10)



LARGE-SIGNAL STEP RESPONSE
(G = 100, 1000)



VOLTAGE NOISE 0.1 to 10Hz
INPUT-REFERRED, G ≥ 100



INA2128

4

INSTRUMENTATION AMPLIFIERS

APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA2128. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminals (Ref_A and Ref_B) which are normally grounded. These must be low-impedance connections to assure good common-mode rejection. A resistance of 8Ω in series with a Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

The INA2128 has a separate output sense feedback connections $Sense_A$ and $Sense_B$. These must be connected to their respective output terminals for proper operation. The output sense connection can be used to sense the output voltage directly at the load for best accuracy.

SETTING THE GAIN

Gain of the INA2128 is set by connecting a single external resistor, R_G, connected as shown:

$$G = 1 + \frac{50k\Omega}{R_G} \qquad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA2128.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that despite its low quiescent current, the INA2128 achieves wide bandwidth, even at high gain. This is due to its current-feedback topology. Settling time also remains excellent at high gain—see "Settling Time vs Gain."

NOISE PERFORMANCE

The INA2128 provides very low noise in most applications. Low frequency noise is approximately 0.2μVp-p measured from 0.1 to 10Hz (G ≥ 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.

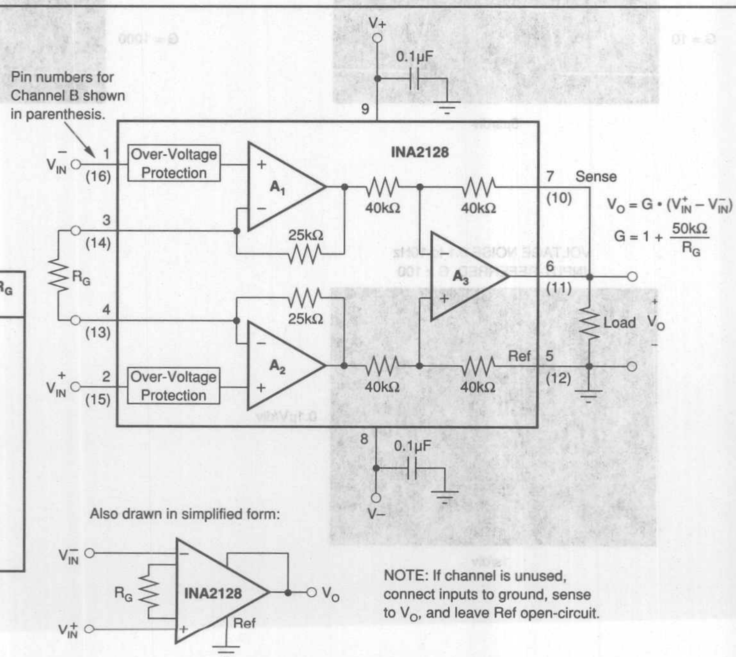


FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA2128 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

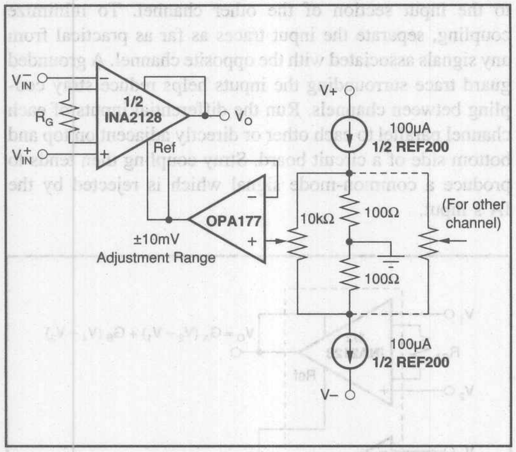


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA2128 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA2128 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA2128 is from approximately 1.4V below the positive supply voltage to 1.7V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output

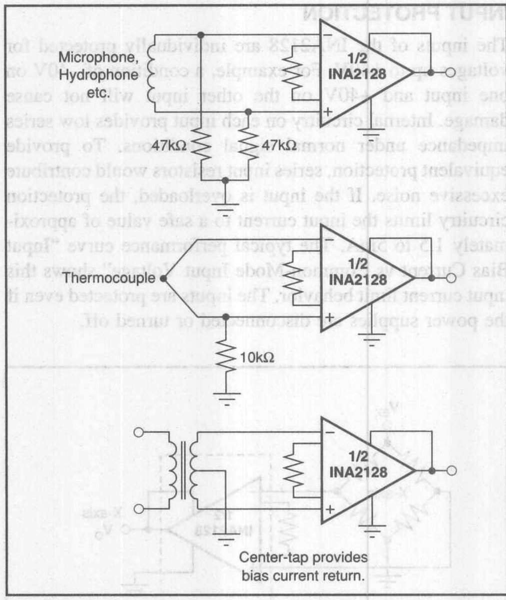


FIGURE 3. Providing an Input Common-Mode Current Path.

voltage swing of amplifiers A_1 and A_2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage."

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA2128 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA2128 can be operated on power supplies as low as ±2.25V. Performance remains excellent with power supplies ranging from ±2.25V to ±18V. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for ±15V, ±5V, and ±2.5V supplies.

The inputs of the INA2128 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5mA. The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

The two channels of the INA2128 are completely independent, including all bias circuitry. At DC and low frequency there is virtually no signal coupling between channels. Crosstalk increases with frequency and is dependent on circuit gain, source impedance and signal characteristics.

As source impedance increases, careful circuit layout will help achieve lowest channel crosstalk. Most crossstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Run the differential inputs of each channel parallel to each other or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal which is rejected by the IA's input.

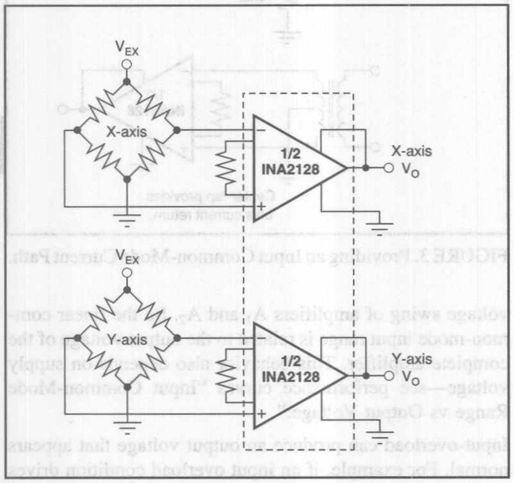


FIGURE 4. Two-Axis Bridge Amplifier.

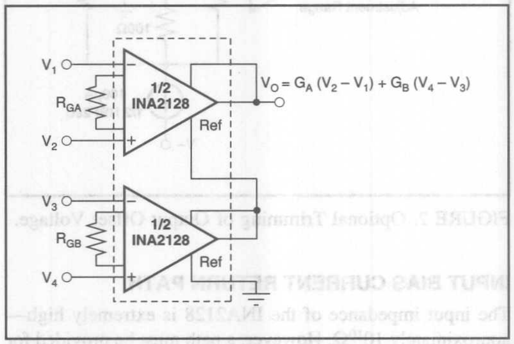


FIGURE 5. Sum of Differences Amplifier.

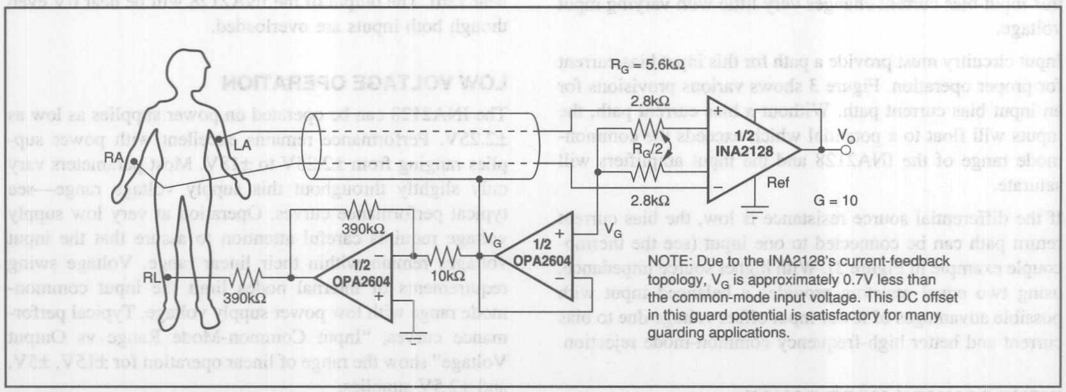
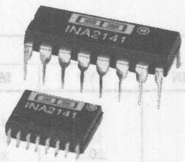


FIGURE 6. ECG Amplifier With Right-Leg Drive.



Dual, Low Power, G = 10, 100 INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.5μV/°C max
- EXCELLENT GAIN ACCURACY: ±0.05% max at G = 10
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 117dB min (G = 100)
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±2.25V to ±18V
- LOW QUIESCENT CURRENT: 750μA/IA
- 16-PIN PLASTIC DIP, SOL-16

APPLICATIONS

- SENSOR AMPLIFIER
  THERMOCOUPLE, RTD, BRIDGE
- MEDICAL INSTRUMENTATION
- MULTIPLE CHANNEL SYSTEMS

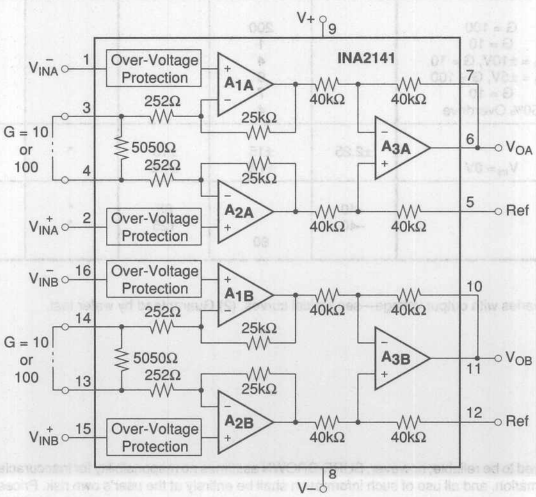
DESCRIPTION

The INA2141 is a low power, dual instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

Simple pin connections set an accurate gain of 10 or 100V/V without external resistors. Internal input protection can withstand up to ±40V without damage.

The INA2141 is laser trimmed for very low offset voltage (50μV), drift (0.5μV/°C) and high common-mode rejection (117dB at G = 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 750μA per amplifier—ideal for battery operated systems.

Packages are 16-pin plastic DIP, and SOL-16 surface-mount, specified for the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

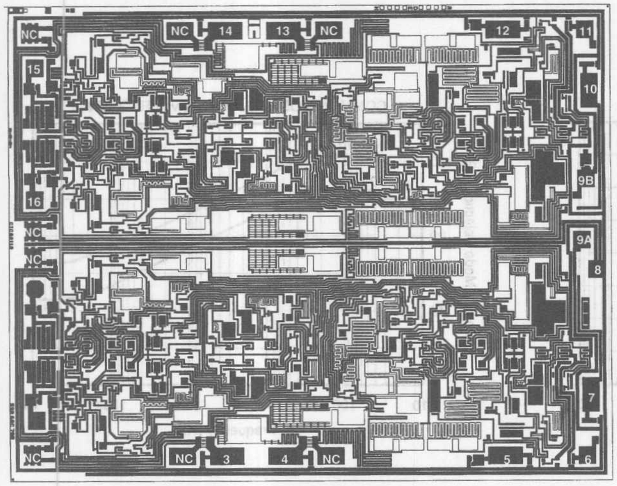
At T_A = +25°C, V_S = ±15V, and R_L = 10kΩ unless otherwise noted.

		INA2141P, U			INA2141PA, UA			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT								
Offset Voltage, RTI	G = 100		±20	±50		*	±125	μV
	G = 10		±50	±100		*	±250	μV
vs Temperature	G = 100		±0.2	±0.5		*	±1.5	μV/°C
	G = 10(2)		±0.5	±2		*	±5	μV/°C
vs Power Supply	V_S = ±2.25 to ±18V, G = 100		±1	±2		*	±5	μV/V
	G = 10		±2	±10		*	±20	μV/V
Long-Term Stability	G = 100		0.2			*		μV/mo
	G = 10		0.5			*		μV/mo
Impedance, Differential			10^{10} || 2			*		Ω || pF
Common-Mode			10^{10} || 9			*		Ω || pF
Common-Mode Voltage Range(1)	V_O = 0V	(V+) – 2	(V+) – 1.4		*	*		V
		(V–) + 2	(V–) + 1.7		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = ±13V, ΔR_S = 1kΩ							
	G = 100	117	125		110	120		dB
	G = 10	97	106		93	100		dB
BIAS CURRENT			±2	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
Offset Current			±1	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
NOISE VOLTAGE, RTI								
f = 10Hz	G = 100, R_S = 0Ω		10			*		nV/√Hz
f = 100Hz			8			*		nV/√Hz
f = 1kHz			8			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.2			*		μVp-p
f = 10Hz	G = 10, R_S = 0Ω		22			*		nV/√Hz
f = 100Hz			13			*		nV/√Hz
f = 1kHz			12			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.6			*		μVp-p
Noise Current								
f = 10Hz			0.9			*		pA/√Hz
f = 1kHz			0.3			*		pA/√Hz
f_B = 0.1Hz to 10Hz			30			*		pAp-p
GAIN								
Gain Error	V_O = ±13.6V, G = 100		±0.03	±0.075		*	±0.15	%
	G = 10		±0.01	±0.05		*	±0.15	%
Gain vs Temperature(2)	G = 10, 100		±2	±10		*	*	ppm/°C
Nonlinearity	G = 100		±0.0005	±0.002		*	±0.004	% of FSR
	G = 10		±0.0003	±0.001		*	±0.002	% of FSR
OUTPUT								
Voltage: Positive	R_L = 10kΩ	(V+) – 1.4	(V+) – 0.9		*	*		V
Negative	R_L = 10kΩ	(V–) + 1.4	(V–) + 0.9		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+6/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 100		200			*		kHz
	G = 10		1			*		MHz
Slew Rate	V_O = ±10V, G = 10		4			*		V/μs
Settling Time, 0.01%	V_O = ±5V, G = 100		9			*		μs
	G = 10		7			*		μs
Overload Recovery	50% Overdrive		4			*		μs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current, Total	V_{IN} = 0V		±1.5	±1.6		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as INA2141P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.

DICE INFORMATION



INA2141 DIE TOPOGRAPHY

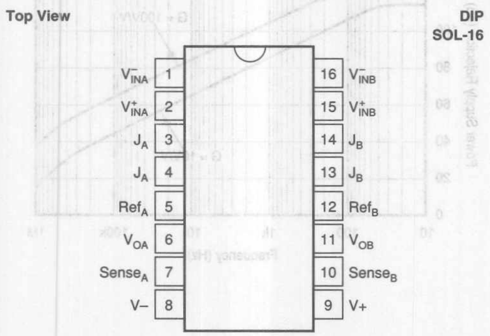
PAD	FUNCTION	PAD	FUNCTION
1	V^-_{INA}	9A, 9B(1)	V+
2	V^+_{INA}	10	$Sense_B$
3	J_A	11	V_{OB}
4	J_A	12	Ref_B
5	Ref_A	13	J_B
6	V_{OA}	14	J_B
7	$Sense_A$	15	$^+V_{INB}$
8	V–	16	$^-V_{INB}$

NC = No Connection.
NOTES: (1) Connect both indicated pads.
Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	163 x 130 ±5	4.14 x 3.30 ±0.13
Die Thickness	18 ±3	0.45 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

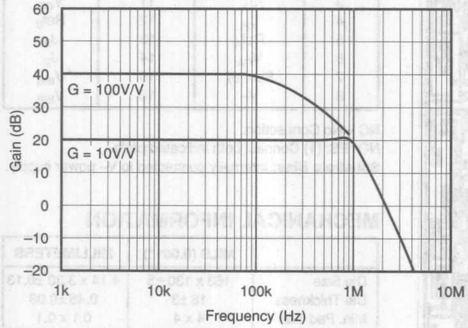
ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
INA2141PA	16-Pin Plastic DIP	180	–40°C to +85°C
INA2141P	16-Pin Plastic DIP	180	–40°C to +85°C
INA2141UA	SOL-16 Surface-Mount	211	–40°C to +85°C
INA2141U	SOL-16 Surface-Mount	211	–40°C to +85°C

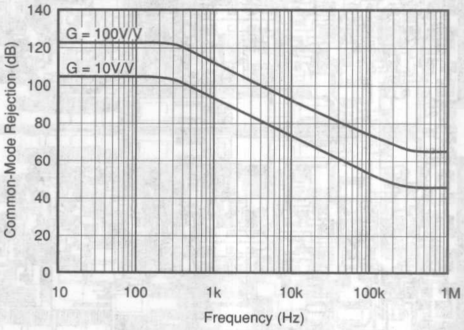
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

At $T_A = +25°C$, and $V_S = ±15V$ unless otherwise noted.

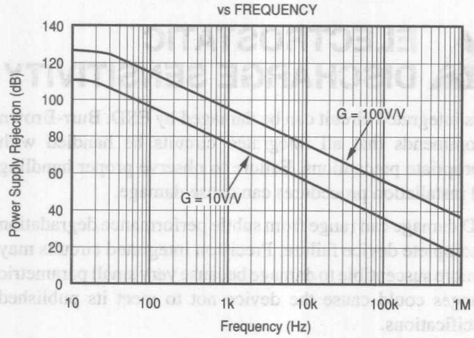
GAIN vs FREQUENCY



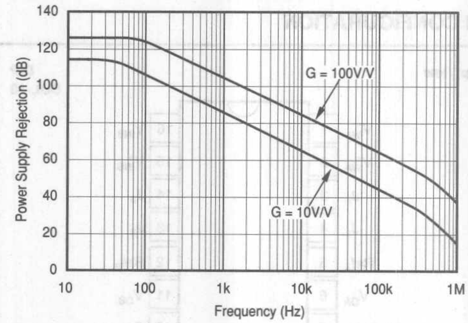
COMMON-MODE REJECTION vs FREQUENCY



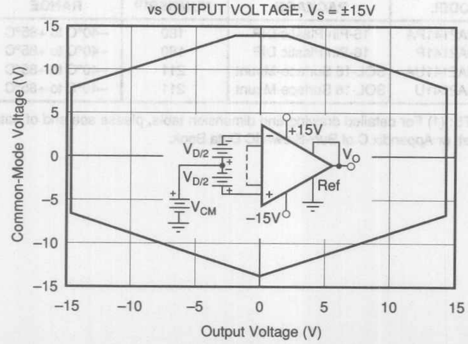
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



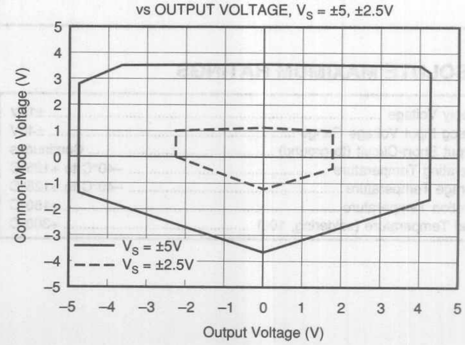
NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



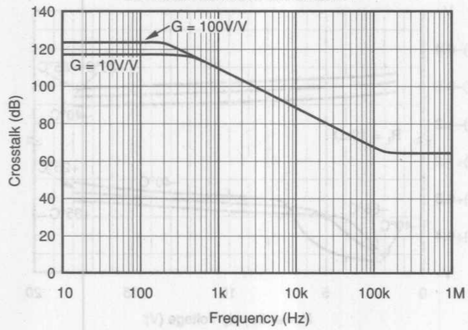
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, $V_S = ±15V$



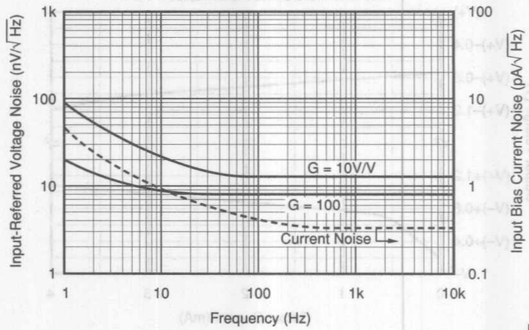
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, $V_S = ±5, ±2.5V$



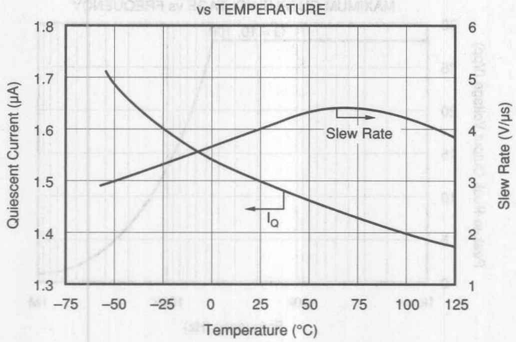
CROSSTALK vs FREQUENCY



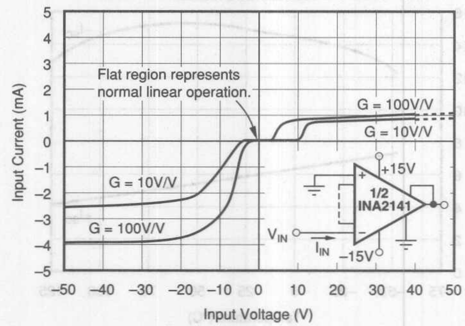
INPUT- REFERRED NOISE vs FREQUENCY



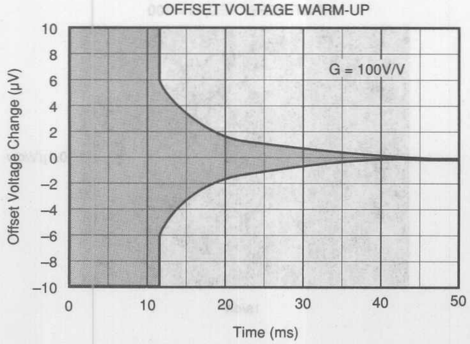
QUIESCENT CURRENT and SLEW RATE vs TEMPERATURE



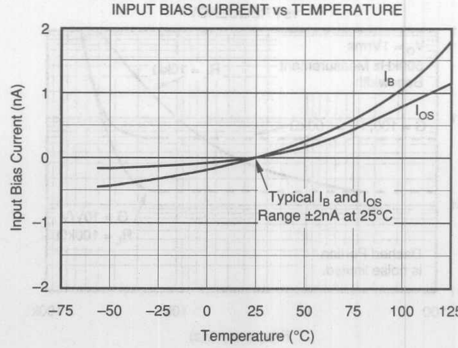
INPUT OVER-VOLTAGE V/I CHARACTERISTICS



OFFSET VOLTAGE WARM-UP

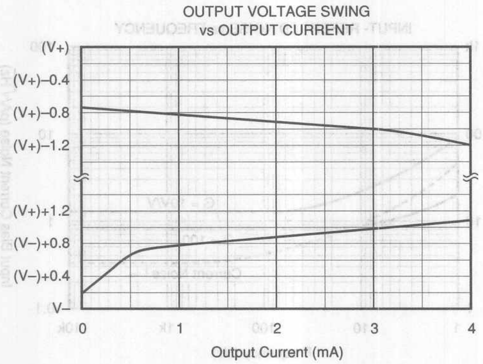


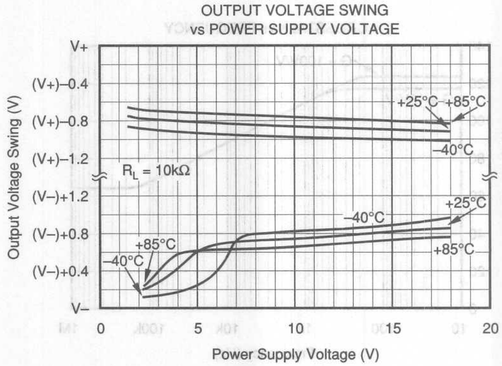
INPUT BIAS CURRENT vs TEMPERATURE

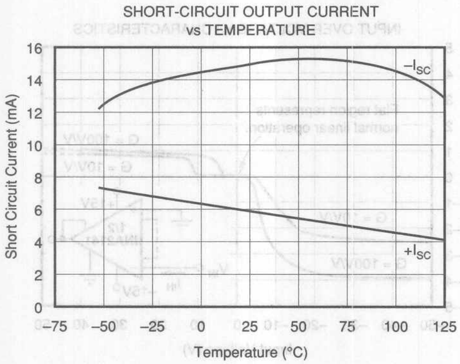


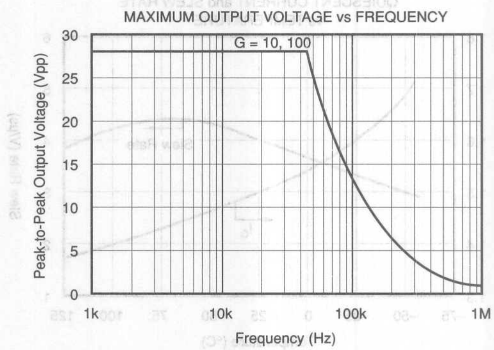
TYPICAL PERFORMANCE CURVES (CONT)

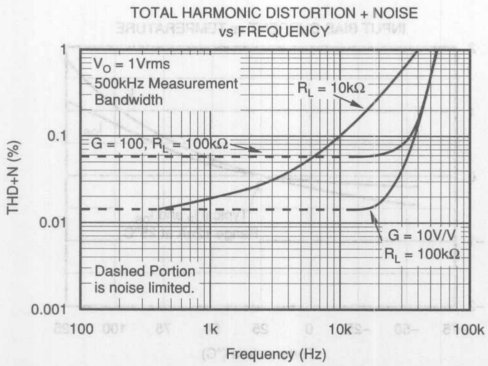
At $T_A = +25°C$, and $V_S = \pm15V$ unless otherwise noted.

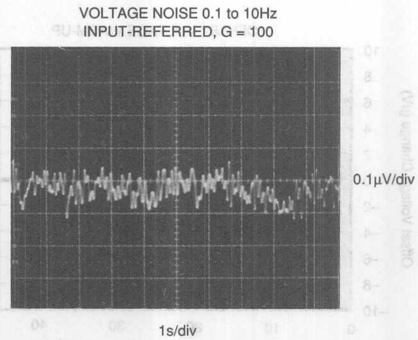












TYPICAL PERFORMANCE CURVES (CONT)

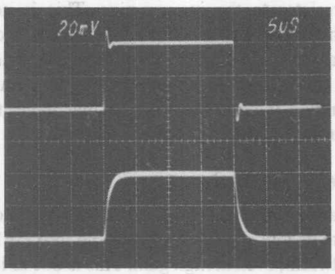
At $T_A = +25°C$, and $V_S = \pm15V$ unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE

G = 10

20mV/div

G = 100



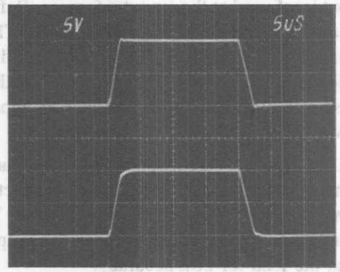
5μs/div

LARGE-SIGNAL STEP RESPONSE

G = 10

5V/div

G = 100



5μs/div

INA2141

4

INSTRUMENTATION AMPLIFIERS

Figure 1 shows the basic connections required for operation of the INA2141. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminals (Ref_A and Ref_B) which are normally grounded. These must be low-impedance connections to assure good common-mode rejection. A resistance of 8Ω in series with a Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

The INA2141 has a separate output sense feedback connections $Sense_A$ and $Sense_B$. These must be connected to their respective output terminals for proper operation. The output sense connection can be used to sense the output voltage directly at the load for best accuracy.

SETTING THE GAIN

Gain of each IA can be independently selected with a jumper connection as shown in Figure 1. G = 10V/V with no jumper installed. With a jumper installed G = 100V/V. To preserve good gain accuracy, this jumper must have low series resistance. A resistance of 0.5Ω in series with the jumper will decrease the gain by 0.1%.

Internal resistor ratios are laser trimmed to assure excellent gain accuracy. Actual resistor values can vary by approximately ±25% from the nominal values shown.

Gains between 10 and 100 can be achieved by connecting an external resistor to the jumper pins. This is not recommended, however, because the ±25% variation of internal resistor values makes the required external resistor value uncertain. A companion model, INA2128, features accurately trimmed internal resistors so that gains from 1 to 10,000 can be set with an external resistor.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that despite its low quiescent current, the INA2141 achieves wide bandwidth, even at high gain. This is due to its current-feedback topology. Settling time also remains excellent at high gain.

NOISE PERFORMANCE

The INA2141 provides very low noise in most applications. Low frequency noise is approximately 0.2μVp-p measured from 0.1 to 10Hz (G = 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

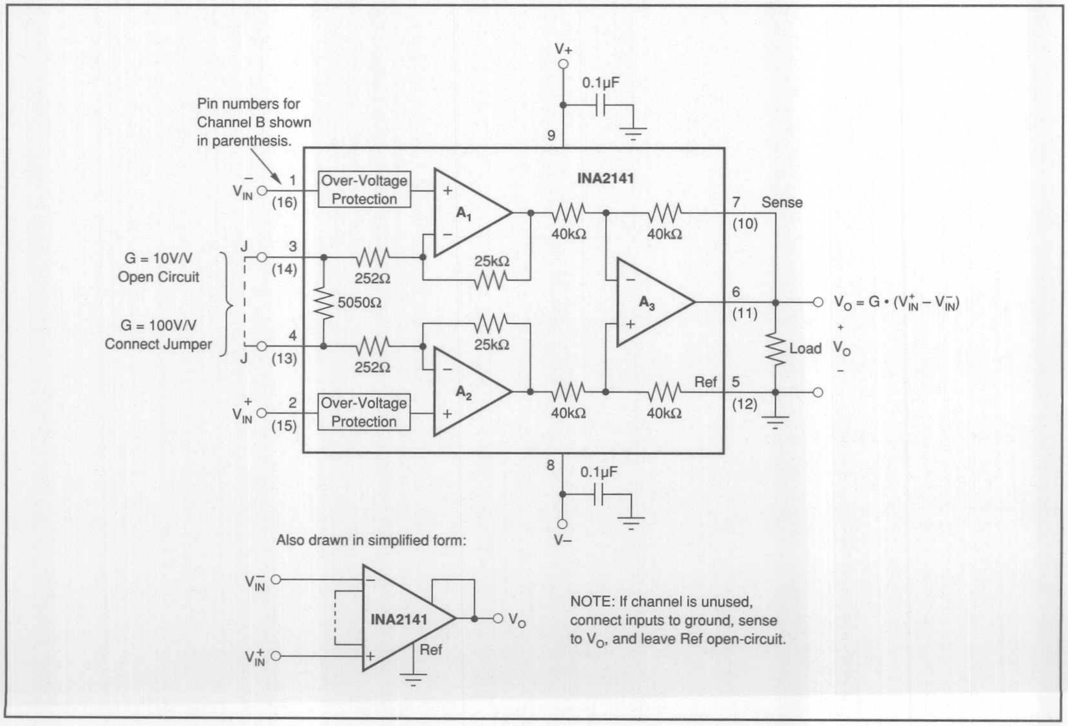


FIGURE 1. Basic Connections.

The INA2141 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

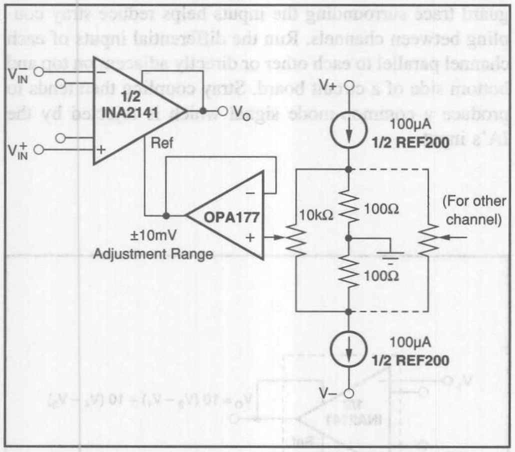


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA2141 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA2141 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA2141 is from approximately 1.4V below the positive supply voltage to 1.7V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output voltage swing of amplifiers A_1 and A_2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage".

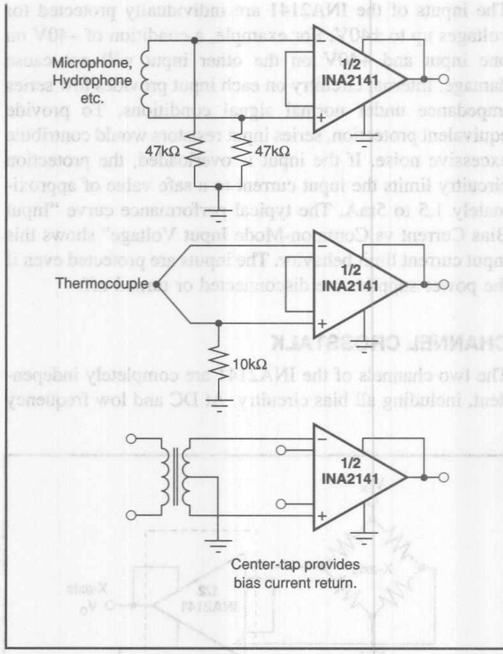


FIGURE 3. Providing an Input Common-Mode Current Path.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA2141 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA2141 can be operated on power supplies as low as ±2.25V. Performance remains excellent with power supplies ranging from ±2.25V to ±18V. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for ±15V, ±5V, and ±2.5V supplies.

INPUT PROTECTION

The inputs of the INA2141 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5mA. The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

CHANNEL CROSSTALK

The two channels of the INA2141 are completely independent, including all bias circuitry. At DC and low frequency there is virtually no signal coupling between channels. Crosstalk increases with frequency and is dependent on circuit gain, source impedance and signal characteristics.

As source impedance increases, careful circuit layout will help achieve lowest channel crosstalk. Most crossstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Run the differential inputs of each channel parallel to each other or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal which is rejected by the IA's input.

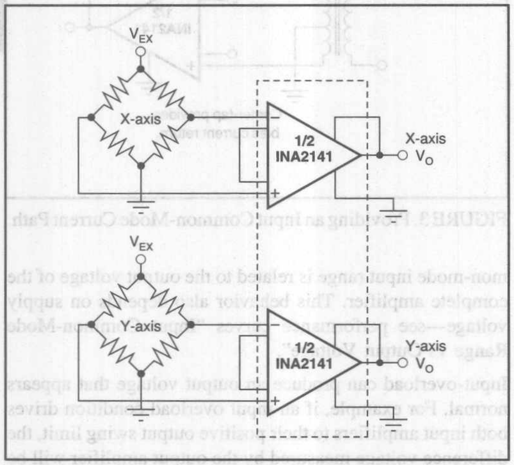


FIGURE 4. Two-Axis Bridge Amplifier.

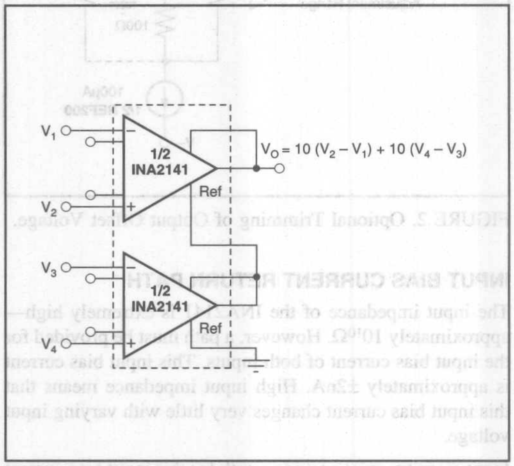


FIGURE 5. Sum of Differences Amplifier.

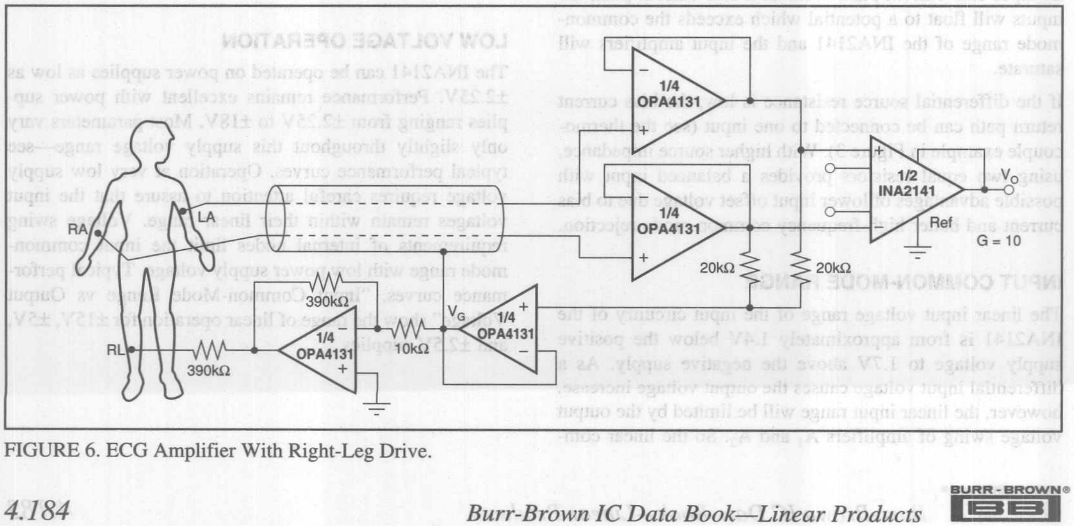
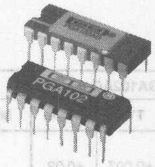


FIGURE 6. ECG Amplifier With Right-Leg Drive.

BURR - BROWN®



PGA102

ABRIDGED DATA SHEET
For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 10579

High Speed
PROGRAMMABLE GAIN AMPLIFIER

FEATURES

- **DIGITALLY PROGRAMMABLE GAIN: G = 1, 10, 100**
- **LOW GAIN ERROR: 0.025% max**
- **FAST SETTLING: 2.8μs to 0.01%**
- **16-PIN PLASTIC AND CERAMIC DIP**

APPLICATIONS

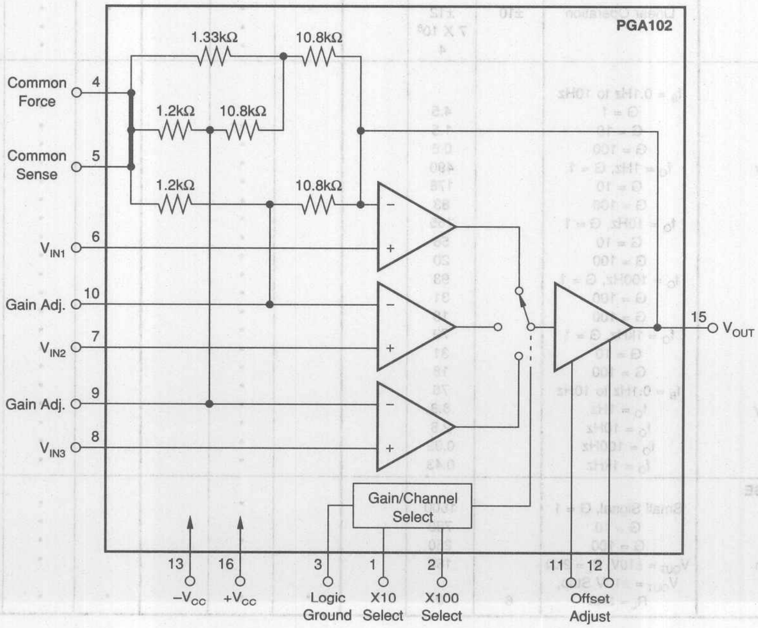
- **DATA ACQUISITION AMPLIFIER**
- **FIXED-GAIN AMPLIFIER**
- **AUTOMATIC GAIN SCALING**

DESCRIPTION

The PGA102 is a high speed, digitally programmable-gain amplifier. CMOS/TTL-compatible inputs select gains of 1, 10 or 100V/V. Each gain has an independent input terminal, providing an input multiplexer function.

On-chip metal film gain-set resistors are laser-trimmed to provide excellent gain accuracy. High speed input circuitry allows multiplexing of high speed signals.

The PGA102 is available in 16-pin plastic and ceramic DIP packages. Commercial, industrial and military temperature range models are available.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At +25°C, $\pm V_{CC}$ = 15VDC unless otherwise specified.

		PGA102AG			PGA102BG, SG			PGA102KP			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN											
Inaccuracy(1)	R_L = 2kΩ, G = 1		±0.007	±0.02		±0.003	±0.01		*	*	%
	G = 10		±0.015	±0.03		±0.01	±0.02		*	±0.05	%
	G = 100		±0.02	±0.05		±0.015	±0.025		*	±0.06	%
vs Temperature	G = 1		±0.4	±5		*	*		*	*	ppm/°C
	G = 10		±2	±7		*	*		*	*	ppm/°C
	G = 100		±7	±20		*	*		±9	*	ppm/°C
Nonlinearity	R_L = 2kΩ, G = 1		0.001	0.003		*	*		*	*	% of FS
	G = 10		0.002	0.005		*	*			*	% of FS
	G = 100		0.003	0.01		*	*			*	% of FS
RATED OUTPUT											
Voltage	R_L = 2kΩ	±10	±12.5		*	*		*	*		V
Current	V_{OUT} = 10V	±5	±10		*	*		*	*		mA
Short Circuit Current		±10	±25		*	*		*	*		mA
Output Resistance			0.01			*			*		Ω
Load Capacitance	For Stable Operation		2000			*			*		pF
INPUT OFFSET VOLTAGE											
Initial(2)	G = 1		±200	±500		±100	±250		*	±1500	μV
	G = 10		±70	±200		±50	±100		*	±600	μV
	G = 100		±70	±200		±50	±100		*	±600	μV
vs Temperature	G = 1		±5	±20		*	*		±7	±50	μV/°C
	G = 10		±1	±7		*	*		±3	±10	μV/°C
	G = 100		±0.5	±3		*	*		±2	±7	μV/°C
vs Supply Voltage	$\pm 5 < V_{CC} < \pm 18V$										
	G = 1		±30	±70		*	*		*	*	μV/V
	G = 10		±8	±30		*	*		*	*	μV/V
	G = 100		±8	±30		*	*		*	*	μV/V
INPUT BIAS CURRENT											
Initial	T_A = +25°C		±20	±50		*	*		*	*	nA
Over Temperature	$T_{A\,MIN}$ to $T_{A\,MAX}$		±25	±60		*	*		*	*	nA
ANALOG INPUT CHARACTERISTICS											
Voltage Range	Linear Operation	±10	±12		*	*		*	*		V
Resistance			7×10^8			*			*		Ω
Capacitance			4			*			*		pF
INPUT NOISE											
Voltage Noise	f_B = 0.1Hz to 10Hz										
	G = 1		4.5			*			*		μVp-p
	G = 10		1.5			*			*		μVp-p
	G = 100		0.6			*			*		μVp-p
Voltage Noise Density	f_O = 1Hz, G = 1		490			*			*		nV/√Hz
	G = 10		178			*			*		nV/√Hz
	G = 100		83			*			*		nV/√Hz
	f_O = 10Hz, G = 1		155			*			*		nV/√Hz
	G = 10		56			*			*		nV/√Hz
	G = 100		20			*			*		nV/√Hz
	f_O = 100Hz, G = 1		93			*			*		nV/√Hz
	G = 100		31			*			*		nV/√Hz
	G = 100		18			*			*		nV/√Hz
	f_O = 1kHz, G = 1		79			*			*		nV/√Hz
	G = 10		31			*			*		nV/√Hz
	G = 100		18			*			*		nV/√Hz
Current Noise	f_B = 0.1Hz to 10Hz		76			*			*		pAp-p
Current Noise Density	f_O = 1Hz		8.8			*			*		pA/√Hz
	f_O = 10Hz		2.8			*			*		pA/√Hz
	f_O = 100Hz		0.99			*			*		pA/√Hz
	f_O = 1kHz		0.43			*			*		pA/√Hz
DYNAMIC RESPONSE											
±3dB Bandwidth	Small Signal, G = 1		1500			*			*		kHz
	G = 10		750			*			*		kHz
	G = 100		250			*			*		kHz
Full Power Bandwidth	V_{OUT} = ±10V, R_L = 2kΩ		160			*			*		kHz
Slew Rate	V_{OUT} = ±10V Step, R_L = 2kΩ	6	9		*	*		*	*		V/μs

SPECIFICATIONS (CONT)

ELECTRICAL

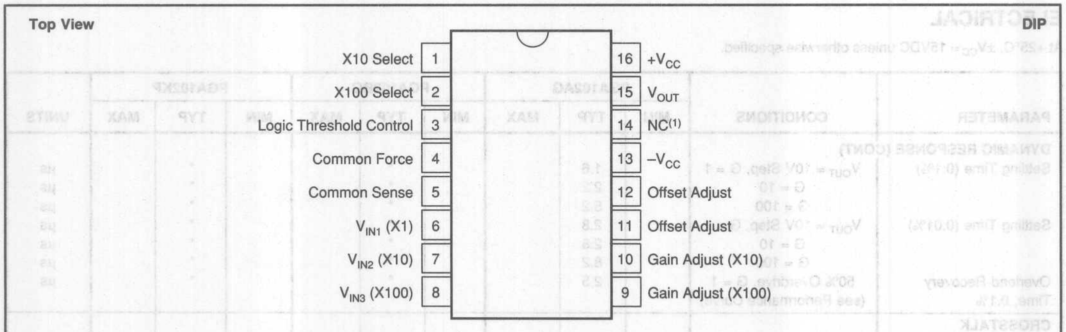
At +25°C, $\pm V_{CC}$ = 15VDC unless otherwise specified.

PARAMETER	CONDITIONS	PGA102AG			PGA102BG			PGA102KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE (CONT)											
Settling Time (0.1%)	V_{OUT} = 10V Step, G = 1		1.6			*			*		µs
	G = 10		2.2			*			*		µs
	G = 100		5.2			*			*		µs
Settling Time (0.01%)	V_{OUT} = 10V Step, G = 1		2.8			*			*		µs
	G = 10		2.8			*			*		µs
	G = 100		8.2			*			*		µs
Overload Recovery Time, 0.1%	50% Overdrive, G = 1 (see Performance Curve)		2.5			*			*		µs
CROSSTALK											
DC	±10V to Both Off Channels		–155			*			*		dB
60Hz	±10V to Both Off Channels		–144			*			*		dB
DIGITAL INPUT CHARACTERISTICS											
Input "Low" Threshold	V_{IL}(3) on Pin 1 or 2			VLTC+0.8			*			*	V
Input "Low" Current				1			*			*	µA
Input "High" Threshold	V_{IH}(3) on Pin 1 or 2	VLTC+2		1	*		*	*		*	V
Input "High" Current			0.1	1		*	*		*	*	µA
Logic Threshold Control	VLTC on Pin 3	$-V_{CC}$		$V_{CC} - 4$	*		*	*		*	V
Switching Time(4)	Between Channels		1			*			*		µs
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range		±5		±18	*		*	*		*	VDC
Quiescent Current	V_{OUT} = 0V		±2.4	±3.3		*	*		*	*	mA
	No External Load, V_{OUT} = ±10V			±5.3			*			*	mA
TEMPERATURE RANGE											
Specification, KP Grade	$T_{A\ MIN}$ to $T_{A\ MAX}$							0		+70	°C
AG and BG Grades		–25		+85	*		*				°C
SG Grade					–55		+125				°C
Operating		–55		+125	*		*	–25		+85	°C
Storage		–65		+150	*		*	–55		+125	°C
Thermal Resistance	θ_{JA}		100			*			*		°C/W

* Specification same as AG grade.

NOTES: (1) Gain inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero for gains of 10 and 100. (2) Offset voltage can be adjusted for any one channel. Adjustment affects temperature drift by approximately ±0.3µV/°C for each 100µV of offset adjusted. (3) Voltage on the logic threshold control pin, VLTC, adjusts the threshold for "Low" and "High" logic levels. (4) Total time to settle equals switching time plus settling time of the newly selected gain.

PIN CONFIGURATION



NOTE: (1) No Internal Connection.

ABSOLUTE MAXIMUM RATINGS

Power Supply	±18V
Input Voltage Range: Analog	$\pm V_{CC}$
Digital	$(V_{PIN\ 3} - 5.6V)$ to $+V_{CC}$
Storage Temperature Range: G Package	–65°C to +150°C
P Package	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration	Continuous to Common
Junction Temperature: G Package	+175°C
P Package	+110°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PGA102AG	16-Pin Hermetic DIP	109
PGA102BG	16-Pin Hermetic DIP	109
PGA102SG	16-Pin Hermetic DIP	109
PGA102KP	16-Pin Plastic DIP	180

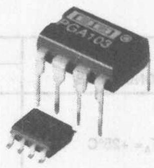
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
PGA102AG	16-Pin Hermetic DIP	–25°C to +85°C
PGA102BG	16-Pin Hermetic DIP	–25°C to +85°C
PGA102SG	16-Pin Hermetic DIP	–55°C to +125°C
PGA102KP	16-Pin Plastic DIP	0°C to +70°C

BURR - BROWN®

PGA103



Programmable Gain AMPLIFIER

FEATURES

- DIGITALLY PROGRAMABLE GAINS: G=1, 10, 100V/V
- CMOS/TTL-COMPATIBLE INPUTS
- LOW GAIN ERROR: ±0.05% max, G=10
- LOW OFFSET VOLTAGE DRIFT: 2μV/°C
- LOW QUIESCENT CURRENT: 2.6mA
- LOW COST
- 8-PIN PLASTIC DIP, SO-8 PACKAGES

APPLICATIONS

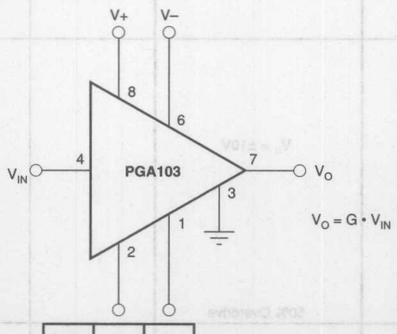
- DATA ACQUISITION SYSTEMS
- GENERAL PURPOSE ANALOG BOARDS
- MEDICAL INSTRUMENTATION

DESCRIPTION

The PGA103 is a programmable-gain amplifier for general purpose applications. Gains of 1, 10, or 100 are digitally selected by two CMOS/TTL-compatible inputs. The PGA103 is ideal for systems that must handle wide dynamic range signals.

The PGA103's high speed circuitry provides fast settling time, even at G=100 (8μs to 0.01%). Bandwidth is 250kHz at G=100, yet quiescent current is only 2.6mA. It operates from ±4.5V to ±18V power supplies.

The PGA103 is available in 8-pin plastic DIP and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.



GAIN	A_1	A_0
1	0	0
10	0	1
100	1	0

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

$T_A = +25°C$, $V_S = ±15V$, $R_L = 2kΩ$ unless otherwise specified.

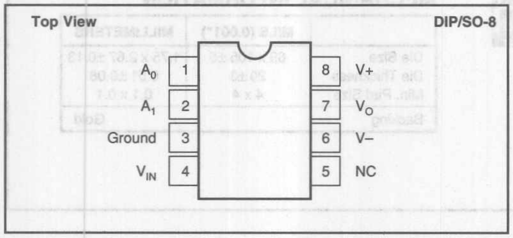
		PGA103P, U			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT					
Offset Voltage, RTI					
G = 1	$T_A = +25°C$		±200	±1500	µV
G = 10			±100	±500	µV
G = 100			±100	±500	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}				
G = 1			±5		µV/°C
G = 10			±2		µV/°C
G = 100			±2		µV/°C
vs Power Supply	$V_S = ±4.5V$ to $±18V$				
G = 1			30	70	µV/V
G = 10			10	35	µV/V
G = 100			10	35	µV/V
Impedance			$10^8 \parallel 2$		Ω ‖ pF
INPUT BIAS CURRENT					
Initial Bias Current			±50	±150	nA
vs Temperature			±100		pA/°C
NOISE VOLTAGE, RTI	G = 100, $R_S = 0Ω$				
f = 10Hz			16		$nV/\sqrt{Hz}$
f = 100Hz			11		$nV/\sqrt{Hz}$
f = 1kHz			11		$nV/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz			0.6		µVp-p
NOISE CURRENT					
f = 10Hz			2.8		$pA/\sqrt{Hz}$
f = 1kHz			0.3		$pA/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz			76		pAp-p
GAIN					
Gain Error					
G = 1			±0.005	±0.02	%
G = 10			±0.02	±0.05	%
G = 100			±0.04	±0.2	%
Gain vs Temperature					
G = 1			±2		ppm/°C
G = 10			±10		ppm/°C
G = 100			±30		ppm/°C
Nonlinearity					
G = 1			±0.001	±0.003	% of FSR
G = 10			±0.002	±0.005	% of FSR
G = 100			±0.004	±0.01	% of FSR
OUTPUT					
Voltage, Positive		(V+) –3.5	(V+) –2.5		V
Negative		(V–) +3.5	(V–) +2.5		V
Load Capacitance, max			1000		pF
Short-Circuit Current			±25		mA
FREQUENCY RESPONSE					
Bandwidth, –3dB					
G = 1			1.5		MHz
G = 10			750		kHz
G = 100			250		kHz
Slew Rate	$V_O = ±10V$		9		V/µs
Settling Time, 0.1%					
G = 1			2		µs
G = 10			2.2		µs
G = 100			6.5		µs
Settling Time, 0.01%					
G = 1			2.5		µs
G = 10			2.5		µs
G = 100			8		µs
Overload Recovery	50% Overdrive		2.5		µs
DIGITAL LOGIC INPUTS					
Digital Low Voltage		–5.6		0.8	V
Digital Low or High Current			1		µA
Digital High Voltage		2		V+	V

ELECTRICAL

$T_A = +25°C$, $V_S = ±15V$, $R_L = 2kΩ$ unless otherwise specified.

PARAMETER	CONDITIONS	PGA103P, U MIN	TYP	MAX	UNITS
POWER SUPPLY					
Voltage Range		±4.5	±15	±18	V
Current	V_{IN} = 0V		±2.6	±3.5	mA
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operating		–40		+125	°C
θ_{JA}: P or U Package			100		°C/W

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	V– to V+
Logic Input Voltage Range	V– to V+
Output Short Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering,10s)	+300°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
PGA103P	8-Pin Plastic DIP	006
PGA103U	SO-8 Surface-Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

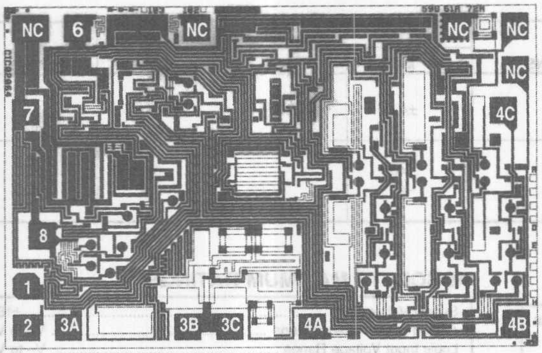
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
PGA103P	8-Pin Plastic DIP	–40°C to +85°C
PGA103U	SO-8 Surface-Mount	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.



PGA103 DIE TOPOGRAPHY

PAD	FUNCTION
1	A_0
2	A_1
3A, 3B, 3C(1)	Ground
4A, 4B, 4C(2)	V_{IN}
6	V–
7	V_O
8	V+

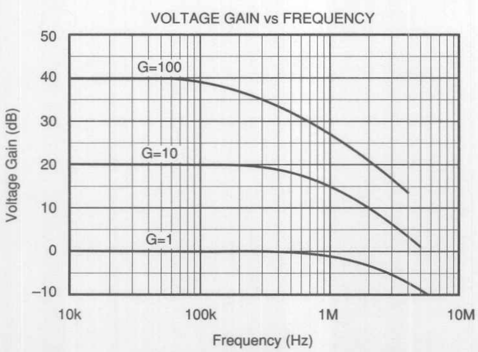
NC: No Connection
NOTES: (1) Connect all three indicated pads. (2) Connect all three indicated pads.
Substrate Bias: Internally connected to V– power supply.

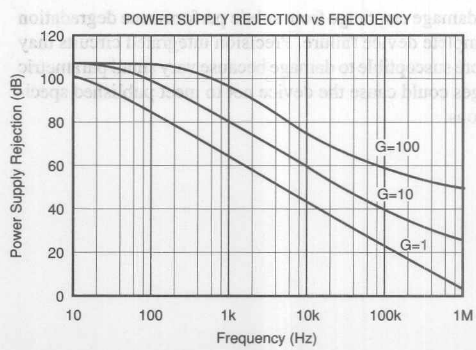
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	69 x 105 ±5	1.75 x 2.67 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

TYPICAL PERFORMANCE CURVES

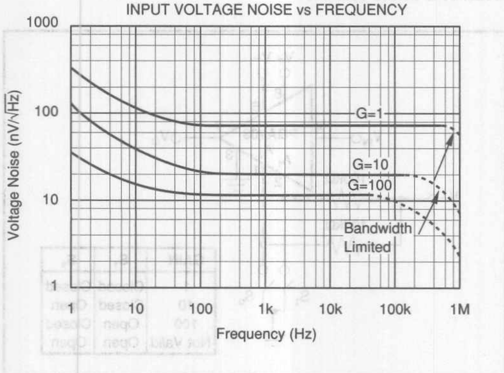
T_A = +25°C, V_S = ±15V unless otherwise noted.

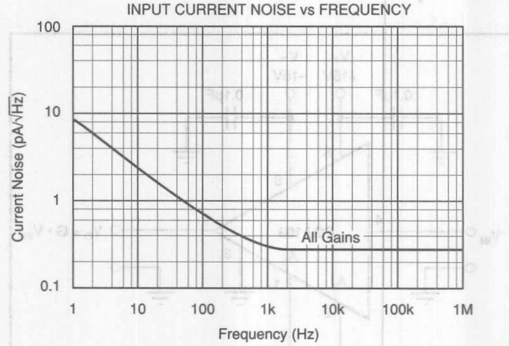


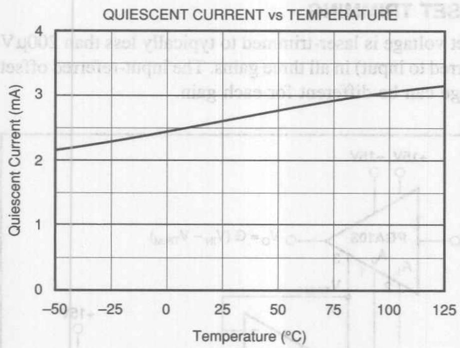


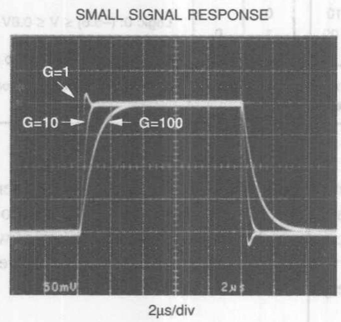
TYPICAL PERFORMANCE CURVES (CONT)

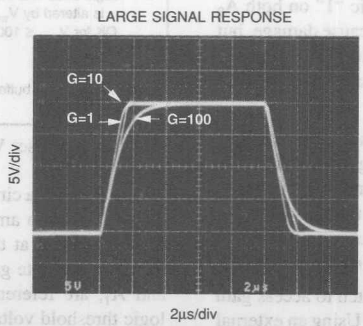
$T_A = +25°C$, $V_S = \pm15V$ unless otherwise noted.





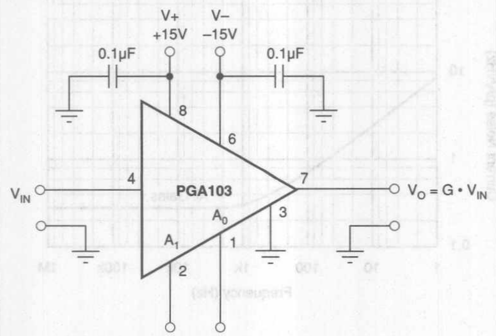






APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA103. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.



GAIN	A_1	A_0
1	0	0
10	0	1
100	1	0
Not Valid	1	1

Logic 0: (–5.6) ≤ V ≤ 0.8V
Logic 1: 2V ≤ V ≤ (V+)
Logic voltages referred to pin 3.

NOTE: (1) Low impedance ground connection required for good gain accuracy—see text.

FIGURE 1. Basic Connections.

The input and output are referred to the ground terminal, pin 3. This must be a low-impedance connection to assure good gain accuracy. A resistance of 0.1Ω in series with the ground pin will cause the gain in G=100 to decrease by approximately 0.2%.

DIGITAL INPUTS

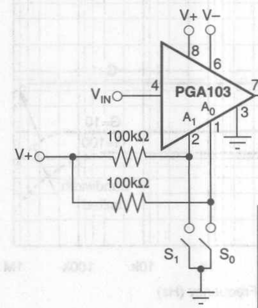
The digital inputs, A_0 and A_1, select the gain according to the logic table in Figure 1. The digital inputs interface directly to common CMOS and TTL logic components. The logic inputs are referenced to the ground terminal, pin 3.

The logic table in Figure 1 shows that logic "1" on both A_0 and A_1 is invalid. This logic code will not cause damage, but the amplifier output will not be predictable while this code is selected. The output will recover when a valid code is selected.

The digital inputs are not latched, so a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately 0.5μs. The time to respond to gain change is equal to the switching time plus the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to access gain control signals from a high speed data bus. Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the latch circuitry as far as practical from analog circuitry to avoid coupling digital noise into the analog circuitry.

Some applications select gain of the PGA103 with switches or jumpers. Figure 2 shows pull-up resistors connected to assure a noise-free logic "1" when the switch or jumper is off or open. Fixed-gain applications can connect the logic inputs directly to V+ or ground (or other valid logic level) without a series resistor.

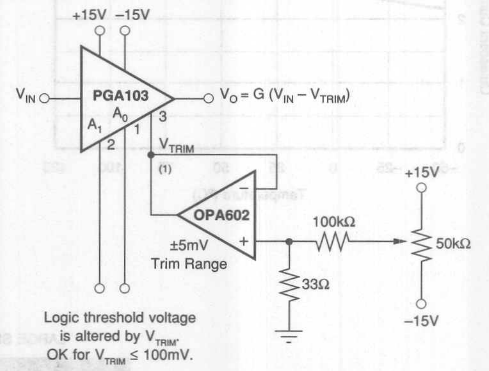


GAIN	S_1	S_0
1	Closed	Closed
10	Closed	Open
100	Open	Closed
Not Valid	Open	Open

FIGURE 2. Switch or Jumper-Selected Gains.

OFFSET TRIMMING

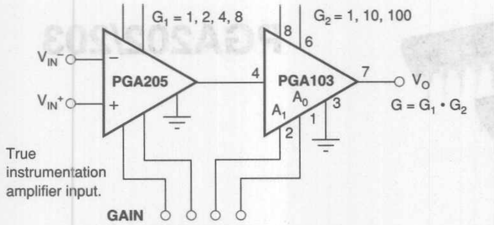
Offset voltage is laser-trimmed to typically less than 200μV (referred to input) in all three gains. The input-referred offset voltage can be different for each gain.



NOTE: (1) Op amp buffer is required to preserve good gain accuracy—see text.

FIGURE 3. Offset Voltage Trim Circuit.

Figure 3 shows a circuit used to trim the offset voltage of the PGA103. An op amp buffers the trim voltage to provide a low impedance at the ground terminal. This is required to maintain accurate gain. Remember that the logic inputs, A_0 and A_1, are referenced to this ground connection, so the logic threshold voltage will be affected by the trim voltage. This is insignificant if the offset adjustment is used only to trim offset voltage. If a large offset is used (greater than 0.1V), be sure that the logic input signals provide valid logic levels when referred to the voltage at the ground terminal, pin 3.



GAIN				
1	0	0	0	0
2	0	1	0	0
4	1	0	0	0
8	1	1	0	0
10	0	0	0	1
20	0	1	0	1
40	1	0	0	1
80	1	1	0	1
100	0	0	1	0
200	0	1	1	0
400	1	0	1	0
800	1	1	1	0

FIGURE 4. Programmable Gain Instrumentation Amplifier.

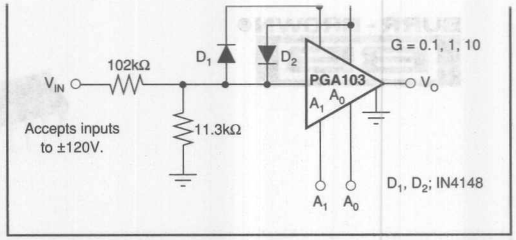


FIGURE 5. Wide Input Voltage Range Amplifer.

MODEL	CHARACTERISTICS
INA103	Low Noise, 1nV/√Hz IA
INA105	G = 1 Difference Amp
INA106	G = 10 Difference Amp
INA114	Resistor-Programmed Gain, Precision
INA117	±200V C-M Input Range Difference Amp
INA111	FET Input, High Speed IA
INA131	Precision, G = 100 IA

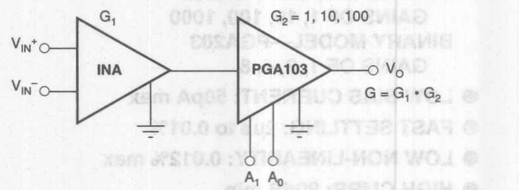
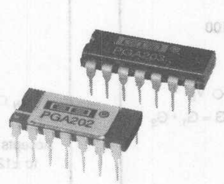


FIGURE 6. Instrumentation Amplifier with Programmable Gain Output Amp.

BURR - BROWN®



PGA202/203

Digitally Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

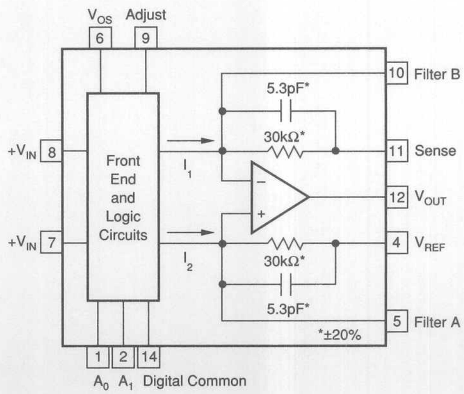
- DIGITALLY PROGRAMMABLE GAINS:
  DECADE MODEL—PGA202
  GAINS OF 1, 10, 100, 1000
  BINARY MODEL—PGA203
  GAINS OF 1, 2, 4, 8
- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 2µs to 0.01%
- LOW NON-LINEARITY: 0.012% max
- HIGH CMRR: 80dB min
- NEW TRANSCONDUCTANCE CIRCUITRY
- LOW COST

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- AUTO-RANGING CIRCUITS
- DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION
- TEST EQUIPMENT

DESCRIPTION

The PGA202 is a monolithic instrumentation amplifier with digitally controlled gains of 1, 10, 100, and 1000. The PGA203 provides gains of 1, 2, 4, and 8. Both have TTL or CMOS-compatible inputs for easy microprocessor interface. Both have FET inputs and a new transconductance circuitry that keeps the bandwidth nearly constant with gain. Gain and offsets are laser trimmed to allow use without any external components. Both amplifiers are available in ceramic or plastic packages. The ceramic package is specified over the full industrial temperature range while the plastic package covers the commercial range.



Covered by U.S. PATENT #4,883,422

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

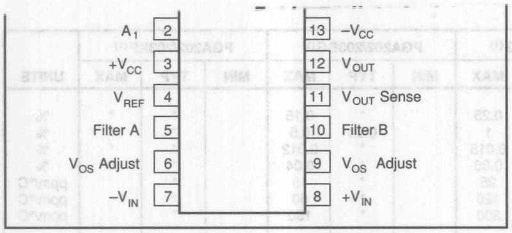
ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted.

		PGA202/203AG(1)			PGA202/203BG(1)			PGA202/203KP(1)			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN											
Error (2)	G < 1000		0.05	0.25		*	0.15		*	*	%
	G = 1000		0.1	1		0.08	0.5		*	*	%
Nonlinearity	G < 1000		0.002	0.015		*	0.012		*	*	%
	G = 1000		0.02	0.06		*	0.04		*	*	%
Gain vs Temperature	G < 100		3	25		*	15		*		ppm/°C
	G = 100		40	120		*	60		*		ppm/°C
	G = 1000		100	300		*	150		*		ppm/°C
RATED OUTPUT											
Voltage	$\lvert I_{OUT}\rvert \le$ 5mA	±10	±12		*	*		*	*		V
Over Specified Temperature	See Typical Perf. Curve		±9			*			±10		V
Current	$\lvert V_{OUT}\rvert \le$ 10V	±5	±10		*	*		*	*		mA
Impedance			0.5			*			*		Ω
ANALOG INPUTS											
Common-Mode Range		±10	±13		*	*		*	*		V
Absolute Max Voltage(3)	No Damage			$\pm V_{CC}$			*			*	V
Impedance, Differential			10 ∥ 3			*			*		GΩ ∥ pF
Common-Mode			10 ∥ 1			*			*		GΩ ∥ pF
OFFSET VOLTAGE (RTI)											
Initial Offset at 25°C (4)			±(0.5 + 5/G)	±(2 + 24/G)		*	±(1 + 12/G)		*	*	mV
vs Temperature			±(3 + 50/G)	±(24 + 240/G)		*	±(12 + 120/G)		*		µV/°C
Offset vs Time			50			*					µV/Month
Offset vs Supply	10 ≤ V_{CC} ≤ 15		10 + 250/G	100 + 900/G		*	50 + 450/G		*	*	µV/V
INPUT BIAS CURRENT											
Initial Bias Current: at 25°C			10	50		*	*		*	*	pA
at 85°C			640	3200		*	*		*	*	pA
Initial Offset Current: at 25°C			5	25		*	*		*	*	pA
at 85°C			320	1600		*	*		*	*	pA
COMMON-MODE REJECTION RATIO											
	G = 1	80	100		*	*		*	*		dB
	G = 10	86	110		*	*		*	*		dB
	G = 100	92	120		*	*		*	*		dB
	G = 1000	94	120		*	*		*	*		dB
INPUT NOISE											
Noise Voltage 0.1 to 10Hz			1.7			*			*		µVp-p
Noise Density at 10kHz (5)			12			*			*		nV/√Hz
OUTPUT NOISE											
Noise Voltage 0.1 to 10Hz			32			*			*		µVp-p
Density at 1kHz (5)			400			*			*		nV/√Hz
DYNAMIC RESPONSE											
Frequency Response	G < 1000		1000			*			*		kHz
	G = 1000		250			*			*		kHz
Full Power Bandwidth	G < 1000		400			*			*		kHz
	G = 1000		100			*			*		kHz
Slew Rate		10	20		15	*		*	*		V/µs
Settling Time (0.01%)(7)	G < 1000		2			*			*		µs
	G = 1000		10			*			*		µs
Overload Recovery Time(7)	G < 1000		5			*			*		µs
	G = 1000		10			*			*		µs
DIGITAL INPUTS											
Digital Common Range		$-V_{CC}$		V_{CC} – 8	*		*	*		*	V
Input Low Threshold(6)				0.8			*			*	V
Input Low Current				10			*			*	µA
Input High Voltage		2.4			*			*			V
Input High Current				10			*			*	µA
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±6		±18	*		*	*		*	V
Quiescent Current			6.5			*			*		mA
TEMPERATURE RANGE											
Specification		–25		85	*		*	0		70	°C
Operating		–55		125	*		*	–25		85	°C
Storage		–65		150	*		*	–40		100	°C
θ_{JA}			100			*			*		°C/W

* Same as the PGA202/203AG

NOTES: (1) All specifications apply to both the PGA202 and the PGA203. Values given for a gain of 10 are the same for a gain of 8 and other values may be interpolated. (2) Measured with a 10k load. (3) The analog inputs are internally diode clamped. (4) Adjustable to zero. (5) $V_{NOISE\ (RTI)} = \sqrt{(V_{N\ INPUT})^2 + (V_{N\ OUTPUT}/Gain)^2}$. (6) Threshold voltages are referenced to Digital Common. (7) From input change or gain change.



Analog and Digital Inputs	$\pm(V_{CC} + 0.5V)$
Operating Temperature Range:	
G Package	–55°C to +125°C
P Package	–40°C to +100°C
Lead Temperature (soldering, 10s)	300°C
Output Short Circuit Duration	Continuous
Junction Temperature	175°C

PACKAGE INFORMATION

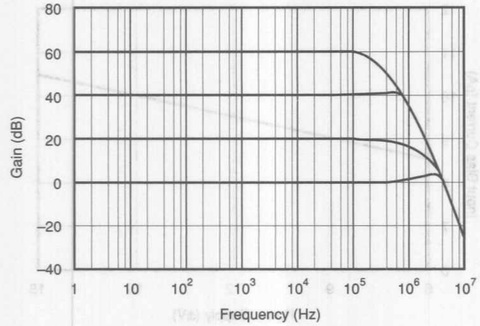
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PGA202KP	14-Pin Plastic DIP	010
PGA202AG	14-Pin Ceramic DIP	169
PGA202BG	14-Pin Ceramic DIP	169
PGA203KP	14-Pin Plastic DIP	010
PGA203AG	14-Pin Ceramic DIP	169
PGA203BG	14-Pin Ceramic DIP	169

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

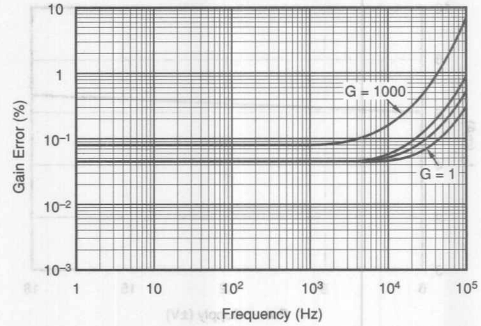
ORDERING INFORMATION

MODEL	GAINS	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (mV)
PGA202KP	1, 10, 100, 1000	Plastic DIP	0°C to +70°C	±(2 + 24/G)
PGA202AG	1, 10, 100, 1000	Ceramic DIP	–25°C to +85°C	±(2 + 24/G)
PGA202BG	1, 10, 100, 1000	Ceramic DIP	–25°C to +85°C	±(1 + 12/G)
PGA203KP	1, 2, 4, 8	Plastic DIP	0°C to +70°C	±(2 + 24/G)
PGA203AG	1, 2, 4, 8	Ceramic DIP	–25°C to +85°C	±(2 + 24/G)
PGA203BG	1, 2, 4, 8	Ceramic DIP	–25°C to +85°C	±(1 + 12/G)

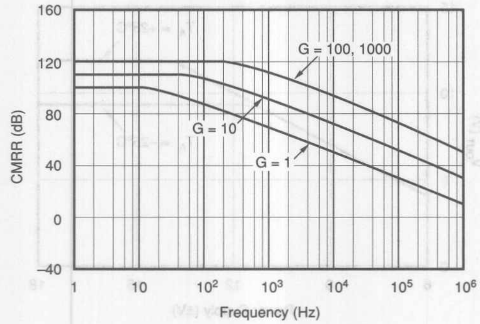
GAIN vs FREQUENCY



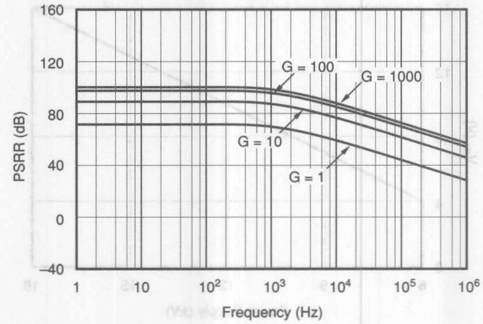
GAIN ERROR vs FREQUENCY



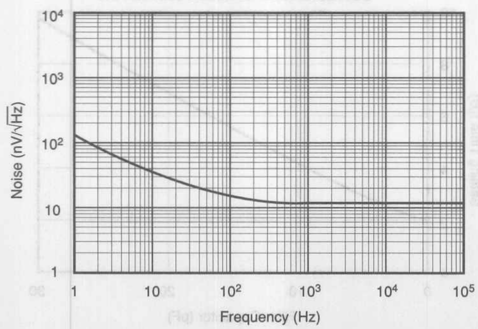
CMRR vs FREQUENCY



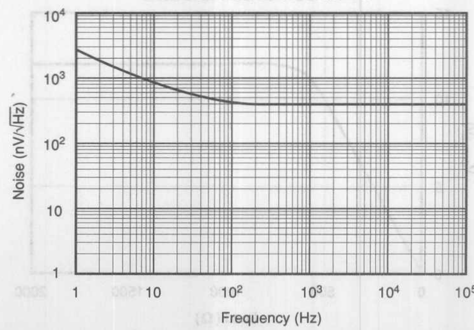
PSRR vs FREQUENCY



INPUT NOISE vs FREQUENCY



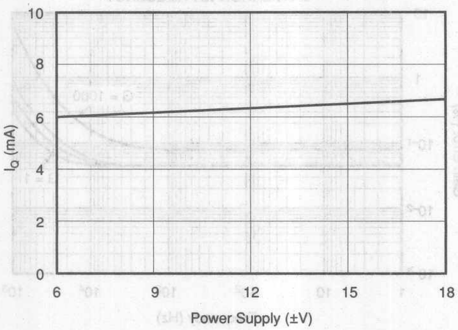
OUTPUT NOISE vs FREQUENCY



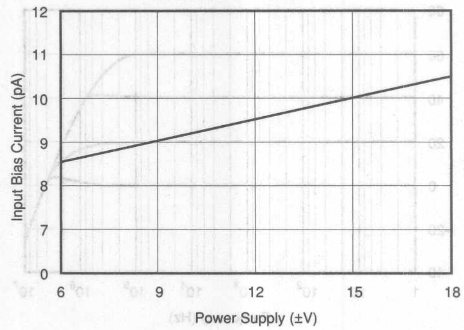
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm15V$ unless otherwise noted.

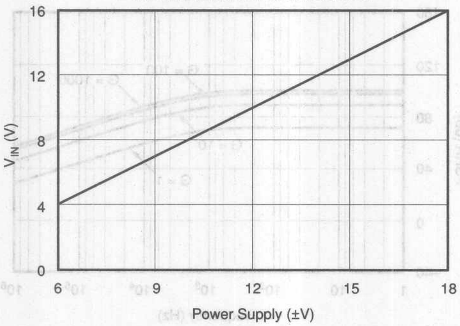
QUIESCENT CURRENT vs POWER SUPPLY



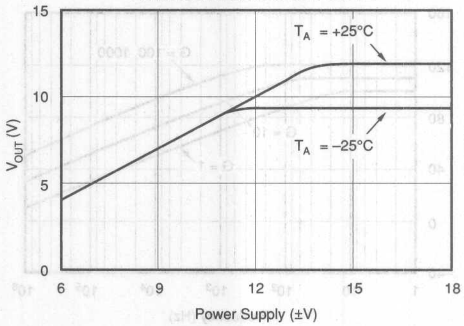
INPUT BIAS CURRENT vs POWER SUPPLY



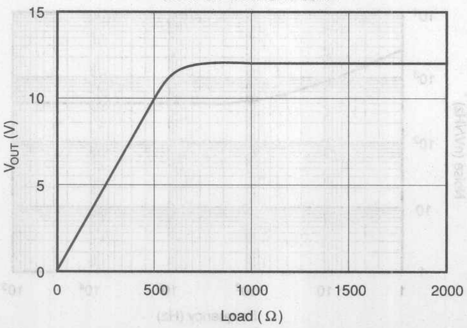
INPUT RANGE vs POWER SUPPLY



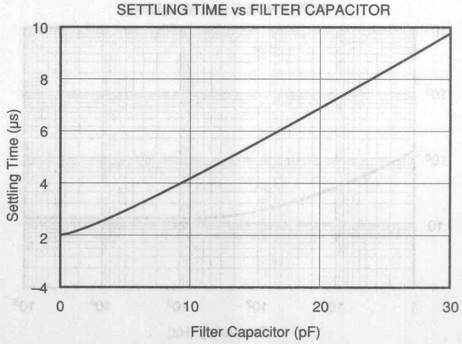
OUTPUT SWING vs POWER SUPPLY



OUTPUT SWING vs LOAD



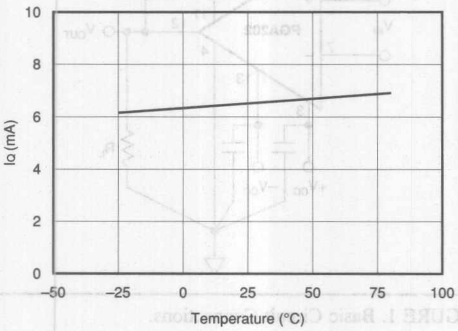
SETTLING TIME vs FILTER CAPACITOR



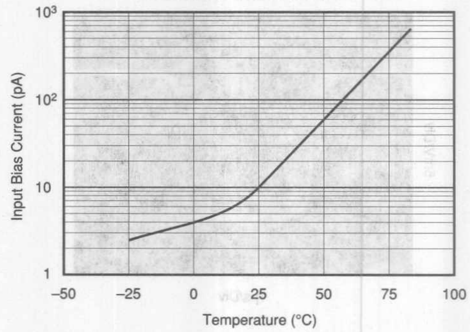
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

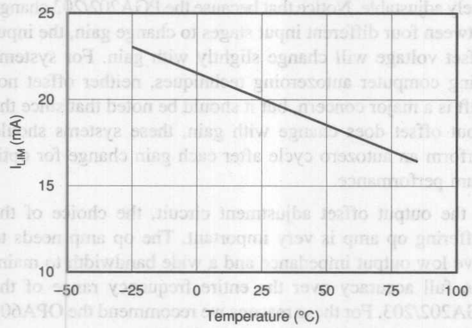
QUIESCENT CURRENT vs TEMPERATURE



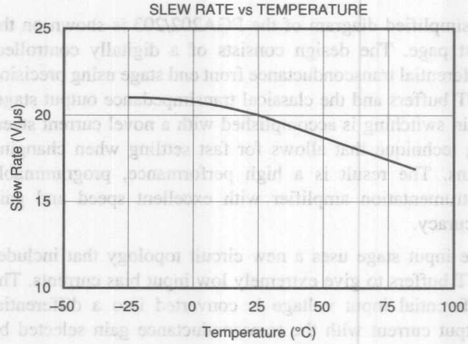
INPUT BIAS CURRENT vs TEMPERATURE



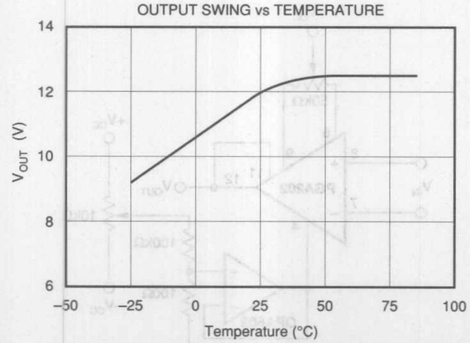
CURRENT LIMIT vs TEMPERATURE



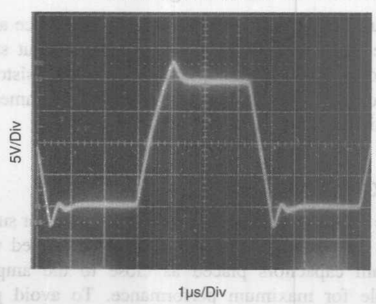
SLEW RATE vs TEMPERATURE



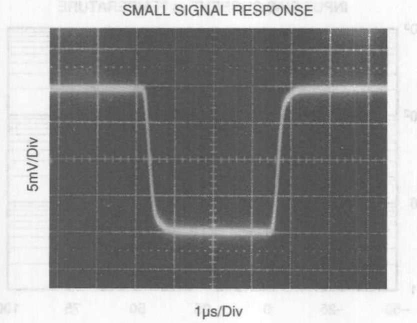
OUTPUT SWING vs TEMPERATURE



LARGE SIGNAL RESPONSE



$T_A = +25°C$, $V_{CC} = \pm15V$ unless otherwise noted.



DISCUSSION OF PERFORMANCE

A simplified diagram of the PGA202/203 is shown on the first page. The design consists of a digitally controlled, differential transconductance front end stage using precision FET buffers and the classical transimpedance output stage. Gain switching is accomplished with a novel current steering technique that allows for fast settling when changing gains. The result is a high performance, programmable instrumentation amplifier with excellent speed and gain accuracy.

The input stage uses a new circuit topology that includes FET buffers to give extremely low input bias currents. The differential input voltage is converted into a differential output current with the transconductance gain selected by steering the input stage bias current between four identical input stages differing only in the value of the gain setting resistor. Each input stage is individually laser-trimmed for input offset, offset drift, and gain.

The output stage is a differential transimpedance amplifier. Unlike the classical difference amplifier output stage, the common-mode rejection is not limited by the resistor matching. However, the output resistors are laser-trimmed to help minimize the output offset and drift.

BASIC CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. The power supplies should be decoupled with 1μF tantalum capacitors placed as close to the amplifier as possible for maximum performance. To avoid gain and CMR errors introduced by the external components, you should connect the grounds as indicated. Any resistance in the sense line (pin 11) or the V_{REF} line (pin 4) will lead to a gain error, so these lines should be kept as short as possible. To also maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

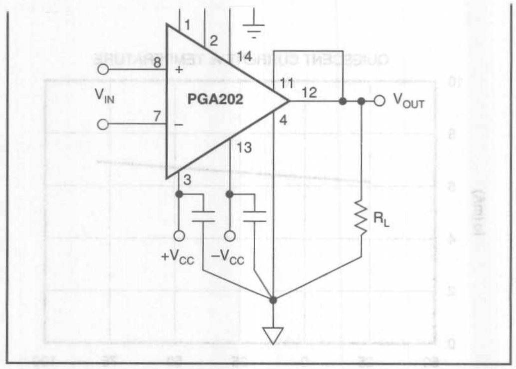


FIGURE 1. Basic Circuit Connections.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuits for the PGA202/203. The input offset and the output offset are both separately adjustable. Notice that because the PGA202/203 change between four different input stages to change gain, the input offset voltage will change slightly with gain. For systems using computer autozeroing techniques, neither offset nor drift is a major concern, but it should be noted that since the input offset does change with gain, these systems should perform an autozero cycle after each gain change for optimum performance.

In the output offset adjustment circuit, the choice of the buffering op amp is very important. The op amp needs to have low output impedance and a wide bandwidth to maintain full accuracy over the entire frequency range of the PGA202/203. For these reasons we recommend the OPA602 as an excellent choice for this application.

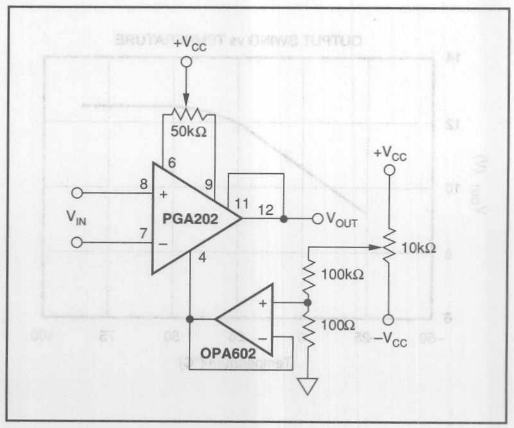


FIGURE 2. Offset Adjustment Circuits.

for the different possible values of the digital input word. The logic inputs are referred to their own separate digital common pin, which can be connected to any voltage between the minus supply and 8V below the positive supply. The gains are all internally trimmed to an initial accuracy of better than 0.1%, so no external gain adjustment is required. However, if necessary the gains can be increased by the use of an external attenuator around the output stage as shown in Figure 3. Recommended resistor values for certain selected output gains are given in Table II.

		PGA202		PGA203	
A_1	A_0	GAIN	ERROR	GAIN	ERROR
0	0	1	0.05%	1	0.05%
0	1	10	0.05%	2	0.05%
1	0	100	0.05%	4	0.05%
1	1	1000	0.10%	8	0.05%

TABLE I. Software Gain Selection.

OUTPUT GAIN	R_1	R_2
2	5kΩ	5kΩ
5	2kΩ	8kΩ
10	1kΩ	9kΩ

TABLE II. Output Stage Gain Control.

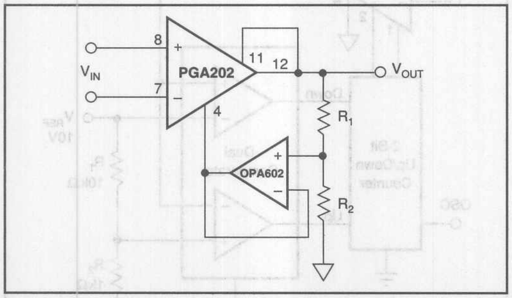


FIGURE 3. Gain Increase with Buffered Attenuator.

COMMON-MODE INPUT RANGE

Unlike the classical three op amp type of circuit, the input common-mode range of the PGA202/203 does not depend on the differential input and the gain. In the standard three op amp circuit, the input common-mode signal must be kept below the maximum output voltage of the input amplifier minus 1/2 the final output voltage. If, for example, these amplifiers can swing ±12V, then to get 12V at the output you must restrict the input common-mode voltage to only 6V. The circuitry of the PGA202/203 is such that the common-mode input range applies to either input pin regardless of the output voltage.

the load at the load site, IR drops due to the load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is required, a power booster can be placed in the feedback loop as shown in Figure 4. Buffer errors are minimized by the loop gain of the output amplifier.

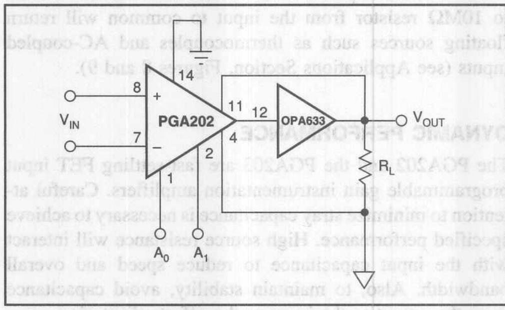


FIGURE 4. Current Boosting the Output.

OUTPUT FILTERING

The summing nodes of the output amplifier have also been made available to allow for output filtering. By placing matched capacitors in parallel with the existing internal capacitors as shown in Figure 5, you can lower the frequency response of the output amplifier. This will reduce the noise of the amplifier, at the cost of a slower response. The nominal frequency responses for some selected values of capacitor are shown in Table III.

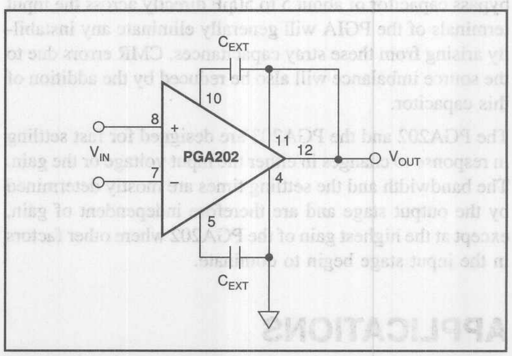


FIGURE 5. Output Filtering.

CUTOFF FREQUENCY	C_1 AND C_2
1MHz	None
100kHz	47pF
10kHz	525pF

TABLE III. Output Frequency vs Filter Capacitors.

INPUT CHARACTERISTICS

Because the PGA202/203 have FET inputs, the bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp currents produce no more than microvolts through megohm sources. The inputs are also internally diode clamped to the supplies. Thus, input filtering and input series protection are easily achievable.

A return path for the input bias currents must always be provided to prevent the charging of any stray capacitance. Otherwise, the amplifier could wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as thermocouples and AC-coupled inputs (see Applications Section, Figures 8 and 9).

DYNAMIC PERFORMANCE

The PGA202 and the PGA203 are fast-settling FET input programmable gain instrumentation amplifiers. Careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with the input capacitance to reduce speed and overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

Applications with balanced source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the stability of the circuit. If, however, the impedance in the positive input is greater, then the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback will, of course, depend on the source impedance imbalance as well as the board layout and the operating gain. The addition of a small bypass capacitor of about 5 to 50pF directly across the input terminals of the PGIA will generally eliminate any instability arising from these stray capacitances. CMR errors due to the source imbalance will also be reduced by the addition of this capacitor.

The PGA202 and the PGA203 are designed for fast settling in response to changes in either the input voltage or the gain. The bandwidth and the settling times are mostly determined by the output stage and are therefore independent of gain, except at the highest gain of the PGA202 where other factors in the input stage begin to dominate.

APPLICATIONS

In addition to general purpose applications, the PGA202/203 are designed to handle two important and demanding classes of applications: inputs with high source impedances, and rapid scanning data acquisition systems requiring fast settling time. Because the user has access to output sense and output common pins, current sources can also be constructed with a minimum of external components. Some basic application circuits are shown in Figures 6 through 12.

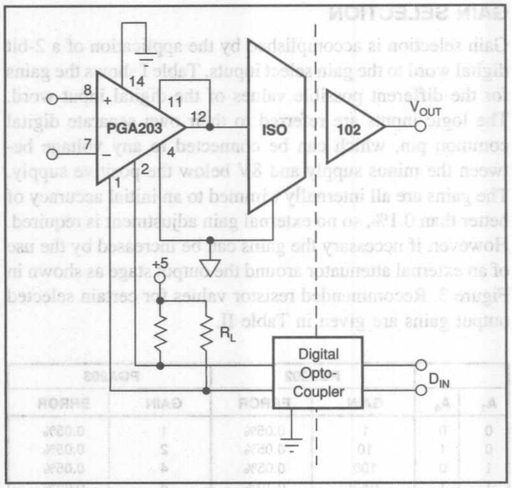


FIGURE 6. Isolated Programmable Gain Instrumentation Amplifier.

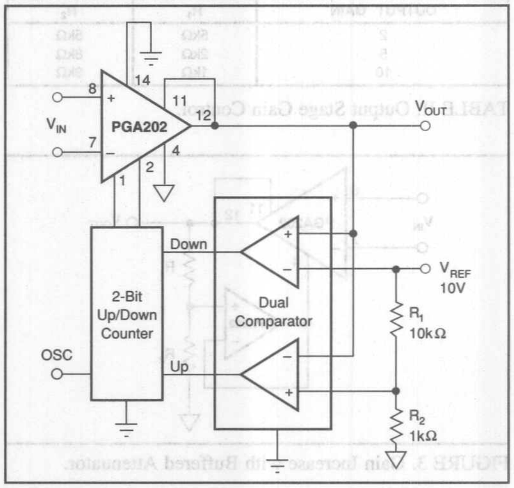


FIGURE 7. Auto Gain Ranging.

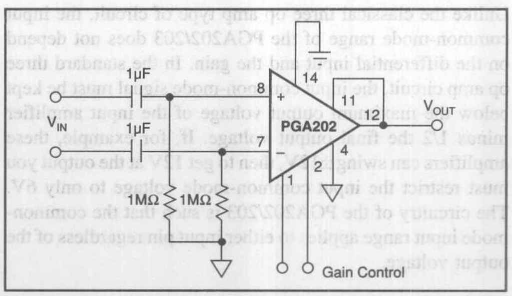


FIGURE 8. AC-Coupled Differential Amplifier for Frequencies Above 0.16Hz.

BURR-BROWN®

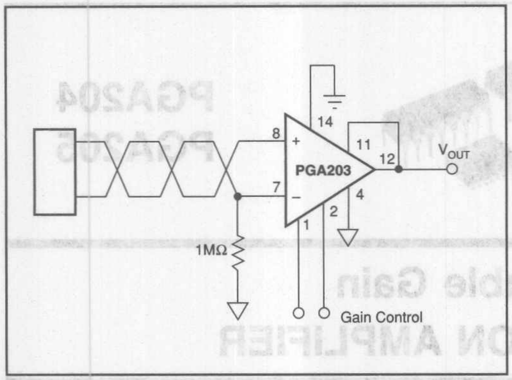


FIGURE 9. Floating Source Programmable Gain Instrumentation Amplifier.

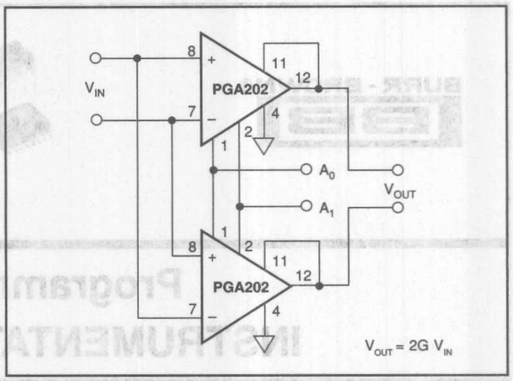


FIGURE 11. Programmable Differential In/Differential Out Amplifier.

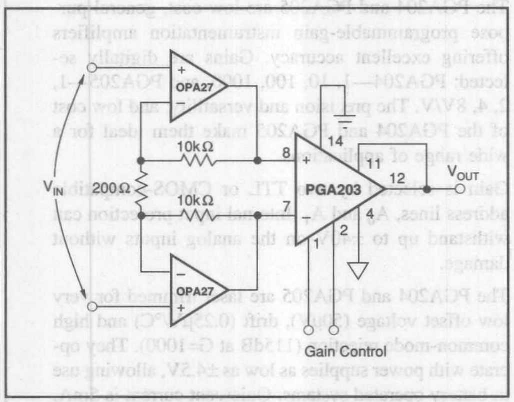


FIGURE 10. Low Noise Differential Amplifier with Gains of 100, 200, 400, 800.

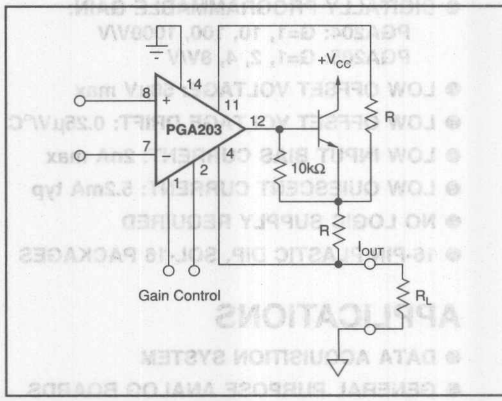
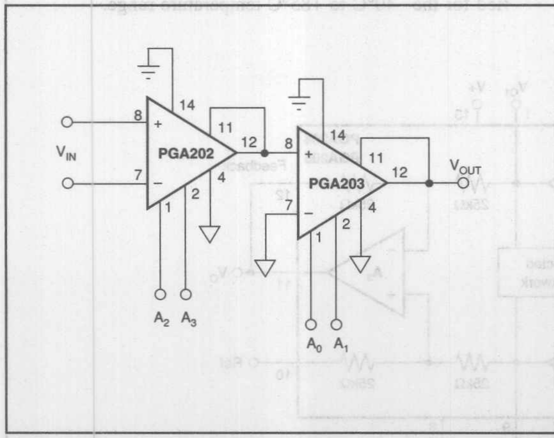


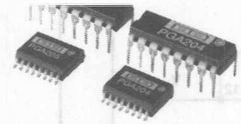
FIGURE 12. Programmable Current Source.



A_3	A_2	A_1	A_0	GAIN
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	10
0	1	0	1	20
0	1	1	0	40
0	1	1	1	80
1	0	0	0	100
1	0	0	1	200
1	0	1	0	400
1	0	1	1	800
1	1	0	0	1000
1	1	0	1	2000
1	1	1	0	4000
1	1	1	1	8000

FIGURE 13. Cascaded Amplifiers.

BURR - BROWN®



PGA204
PGA205

Programmable Gain
INSTRUMENTATION AMPLIFIER

FEATURES

- **DIGITALLY PROGRAMMABLE GAIN:**
  PGA204: G=1, 10, 100, 1000V/V
  PGA205: G=1, 2, 4, 8V/V
- **LOW OFFSET VOLTAGE: 50µV max**
- **LOW OFFSET VOLTAGE DRIFT: 0.25µV/°C**
- **LOW INPUT BIAS CURRENT: 2nA max**
- **LOW QUIESCENT CURRENT: 5.2mA typ**
- **NO LOGIC SUPPLY REQUIRED**
- **16-PIN PLASTIC DIP, SOL-16 PACKAGES**

APPLICATIONS

- **DATA ACQUISITION SYSTEM**
- **GENERAL PURPOSE ANALOG BOARDS**
- **MEDICAL INSTRUMENTATION**

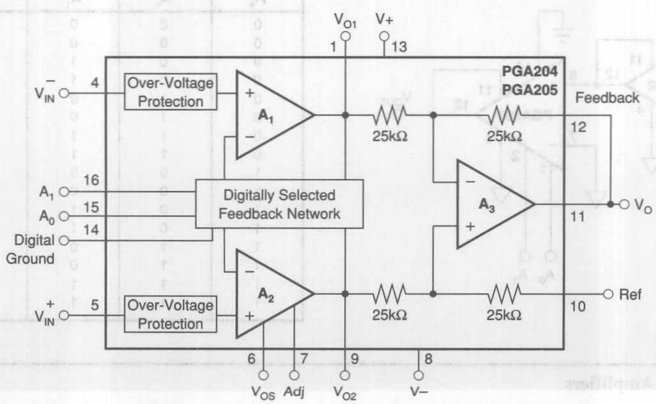
DESCRIPTION

The PGA204 and PGA205 are low cost, general purpose programmable-gain instrumentation amplifiers offering excellent accuracy. Gains are digitally selected: PGA204—1, 10, 100, 1000, and PGA205—1, 2, 4, 8V/V. The precision and versatility, and low cost of the PGA204 and PGA205 make them ideal for a wide range of applications.

Gain is selected by two TTL or CMOS-compatible address lines, A_0 and A_1. Internal input protection can withstand up to ±40V on the analog inputs without damage.

The PGA204 and PGA205 are laser trimmed for very low offset voltage (50µV), drift (0.25µV/°C) and high common-mode rejection (115dB at G=1000). They operate with power supplies as low as ±4.5V, allowing use in battery operated systems. Quiescent current is 5mA.

The PGA204 and PGA205 are available in 16-pin plastic DIP, and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ unless otherwise noted.

		PGA204BP, BU			PGA204AP, AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
Offset Voltage, RTI	T_A=+25°C		±10+20/G	±50+100/G		±25+30/G	±125+500/G	μV
vs Temperature	T_A=T_{MIN} to T_{MAX}		±0.1+0.5/G	±0.25+5/G		±0.25+5/G	±1+10/G	μV/°C
vs Power Supply	V_S=±4.5V to ±18V		0.5+2/G	3+10/G		*	*	μV/V
Long-Term Stability			±0.2+0.5/G			*		μV/mo
Impedance, Differential			10^{10}‖6			*		Ω ‖ pF
Common-Mode			10^{10}‖6			*		Ω ‖ pF
Input Common-Mode Range	V_O=0V (see text)	±10.5	±12.7		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM}=±10V, ΔR_S=1kΩ							
	G=1	80	99		75	90		dB
	G=10	96	114		90	106		dB
	G=100	110	123		106	110		dB
	G=1000	115	123		106	110		dB
BIAS CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
Offset Current			±0.5	±2		*	*	nA
vs Temperature			±8			*		pA/°C
NOISE, Voltage, RTI(1): f=10Hz	G≥100, R_S=0Ω		16			*		nV/√Hz
f=100Hz	G≥100, R_S=0Ω		13			*		nV/√Hz
f=1kHz	G≥100, R_S=0Ω		13			*		nV/√Hz
f_B=0.1Hz to 10Hz	G≥100, R_S=0Ω		0.4			*		μVp-p
Noise Current								
f=10Hz			0.4			*		pA/√Hz
f=1kHz			0.2			*		pA/√Hz
f_B=0.1Hz to 10Hz			18			*		pAp-p
GAIN, Error	G=1		±0.005	±0.024		*	±0.05	%
	G=10		±0.01	±0.024		*	±0.05	%
	G=100		±0.01	±0.024		*	±0.05	%
	G=1000		±0.02	±0.05		*	±0.1	%
Gain vs Temperature	G=1 to 1000		±2.5	±10		*	*	ppm/°C
Nonlinearity	G=1		±0.0004	±0.001		*	±0.002	% of FSR
	G=10		±0.0004	±0.002		*	±0.004	% of FSR
	G=100		±0.0004	±0.002		*	±0.004	% of FSR
	G=1000		±0.0008	±0.01		*	±0.02	% of FSR
OUTPUT								
Voltage, Positive(2)	I_O=5mA, T_{MIN} to T_{MAX}	(V+)–1.5	(V+)–1.3		*	*		V
Negative(2)	I_O=–5mA, T_{MIN} to T_{MAX}	(V–)+1.5	(V–)+1.3		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+23/–17			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G=1		1			*		MHz
	G=10		80			*		kHz
	G=100		10			*		kHz
	G=1000		1			*		kHz
Slew Rate	V_O=±10V, G=10	0.3	0.7		*	*		V/μs
Settling Time(3), 0.1%	G=1		22			*		μs
	G=10		23			*		μs
	G=100		100			*		μs
	G=1000		1000			*		μs
0.01%	G=1		23			*		μs
	G=10		28			*		μs
	G=100		140			*		μs
	G=1000		1300			*		μs
Overload Recovery	50% Overdrive		70			*		μs
DIGITAL LOGIC								
Digital Ground Voltage, V_{DG}		V–		(V+)–4	*		*	V
Digital Low Voltage		V–		V_{DG}+0.8V	*		*	V
Digital Input Current			1			*		μA
Digital High Voltage		V_{DG} +2		V+	*		*	V
POWER SUPPLY, Voltage		±4.5	±15	±18	*	*	*	V
Current	V_{IN}=0V		+5.2/–4.2	±6.5		*	±7.5	mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operating		–40		+125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as PGA204BP.

NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for ±10V min on ±11.4V power supplies. (3) Includes time to switch to a new gain.

SPECIFICATIONS

ELECTRICAL — PGA205 G=1, 2, 4, 8V/V

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ unless otherwise noted.

		PGA205BP, BU			PGA205AP, AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
Offset Voltage, RTI	T_A=+25°C		±10+20/G	±50+100/G		±25+30/G	±125+500/G	µV
vs Temperature	T_A=T_{MIN} to T_{MAX}		±0.1+0.5/G	±0.25+5/G		±0.25+5/G	±1+10/G	µV/°C
vs Power Supply	V_S=±4.5V to ±18V		0.5+2/G	3+10/G		*	*	µV/V
Long-Term Stability			±0.2+0.5/G			*		µV/mo
Impedance, Differential			10^{10}||6			*		Ω||pF
Common-Mode			10^{10}||6			*		Ω||pF
Input Common-Mode Range	V_O=0V (see text)	±10.5	±12.7		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM}=±10V, ΔR_S=1kΩ							
	G=1	80	94		75	88		dB
	G=2	85	100		80	94		dB
	G=4	90	106		85	100		dB
	G=8	95	112		89	106		dB
BIAS CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
Offset Current			±0.5	±2		*	*	nA
vs Temperature			±8			*		pA/°C
Noise Voltage, RTI(1): f=10Hz	G=8, R_S=0Ω		19			*		nV/√Hz
f=100Hz	G=8, R_S=0Ω		15			*		nV/√Hz
f=1kHz	G=8, R_S=0Ω		15			*		nV/√Hz
f_B=0.1Hz to 10Hz	G=8, R_S=0Ω		0.5			*		µVp-p
Noise Current								
f=10Hz			0.4			*		pA/√Hz
f=1kHz			0.2			*		pA/√Hz
f_B=0.1Hz to 10Hz			18			*		pAp-p
GAIN, Error	G=1		±0.005	±0.024		*	±0.05	%
	G=2		±0.01	±0.024		*	±0.05	%
	G=4		±0.01	±0.024		*	±0.05	%
	G=8		±0.01	±0.024		*	±0.05	%
Gain vs Temperature	G=1 to 8		±2.5	±10		*	*	ppm/°C
Nonlinearity	G=1		±0.00024	±0.001		*	±0.002	% of FSR
	G=2		±0.00024	±0.002		*	±0.004	% of FSR
	G=4		±0.00024	±0.002		*	±0.004	% of FSR
	G=8		±0.00024	±0.002		*	±0.004	% of FSR
OUTPUT								
Voltage, Positive(2)	I_O=5mA, T_{MIN} to T_{MAX}	(V+)–1.5	(V+)–1.3		*	*		V
Negative(2)	I_O=–5mA, T_{MIN} to T_{MAX}	(V–)+1.5	(V–)+1.3		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+23/–17			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G=1		1			*		MHz
	G=2		400			*		kHz
	G=4		200			*		kHz
	G=8		100			*		kHz
Slew Rate	V_O=±10V, G=8	0.3	0.7		*	*		V/µs
Settling Time(3), 0.1%	G=1		22			*		µs
	G=2		22			*		µs
	G=4		23			*		µs
	G=8		23			*		µs
0.01%	G=1		23			*		µs
	G=2		23			*		µs
	G=4		25			*		µs
	G=8		28			*		µs
Overload Recovery	50% overdrive		70			*		µs
DIGITAL LOGIC INPUTS								
Digital Ground Voltage, V_{DG}		V–		(V+)–4	*		*	V
Digital Low Voltage		V–		V_{DG}+0.8V	*		*	V
Digital Low Current			1			*		µA
Digital High Voltage		V_{DG}+2		V+	*		*	V
POWER SUPPLY, Voltage		±4.5	±15	±18	*	*	*	V
Current	V_{IN}=0V		+5.2/–4.2	±6.5		*	±7.5	mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operating		–40		+125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as PGA204BP.

NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for ±10V min on ±11.4V power supplies. (3) Includes time to switch to a new gain.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PGA204AP	16-Pin Plastic DIP	180
PGA204BP	16-Pin Plastic DIP	180
PGA204AU	SOL-16 Surface Mount	211
PGA204BU	SOL-16 Surface Mount	211
PGA205AP	16-Pin Plaseic DIP	180
PGA205BP	16-Pin Plastic DIP	180
PGA205AU	SOL-16 Surface Mount	211
PGA205BU	SOL-16 Surface Mount	211

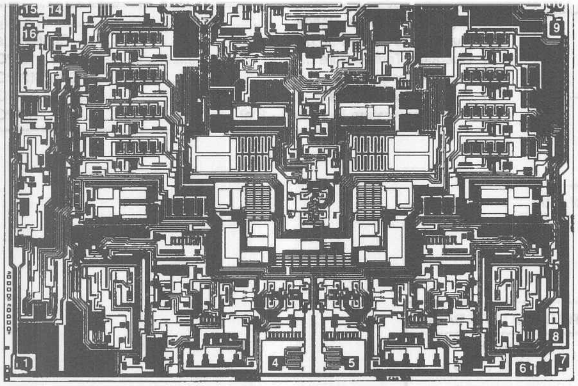
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Logic Input Voltage Range	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering –10s)	+300°C

ORDERING INFORMATION

MODEL	GAINS	PACKAGE	TEMPERATURE RANGE
PGA204AP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	–40 to +85°C
PGA204BP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	–40 to +85°C
PGA204AU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	–40 to +85°C
PGA204BU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	–40 to +85°C
PGA205AP	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40 to +85°C
PGA205BP	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40 to +85°C
PGA205AU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40 to +85°C
PGA205BU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40 to +85°C



PGA204/205 DIE TOPOGRAPHY

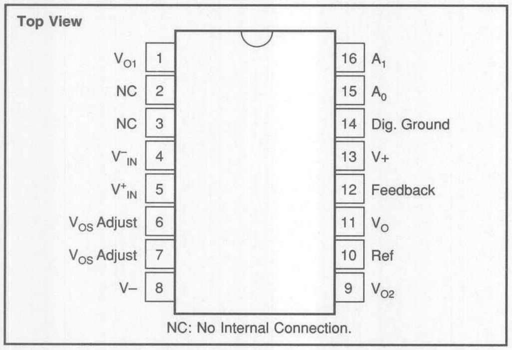
PAD	FUNCTION	PAD	FUNCTION
1	V_{O1}	9	V_{O2}
2	—	10	Ref
3	—	11	V_O
4	V^-_{IN}	12	Feedback
5	V^+_{IN}	13	V+
6	V_{OS} Adj	14	Dig. Ground
7	V_{OS} Adj	15	A_0
8	V–	16	A_1

Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	186 x 130 ±5	4.72 x 3.30 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

PIN CONFIGURATION



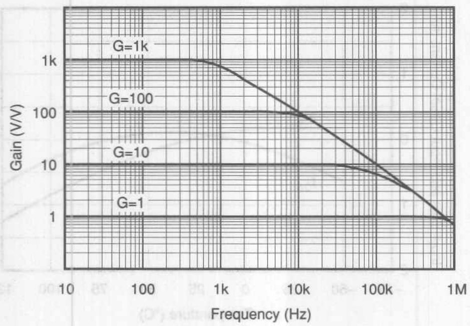
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

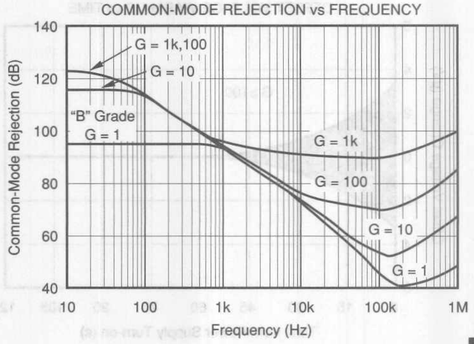
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

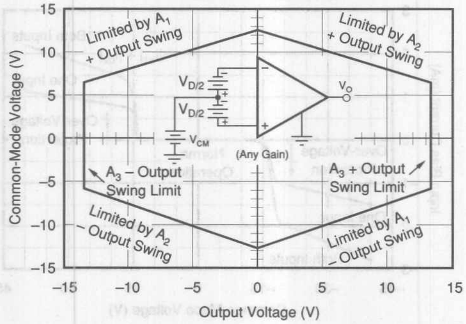
GAIN vs FREQUENCY



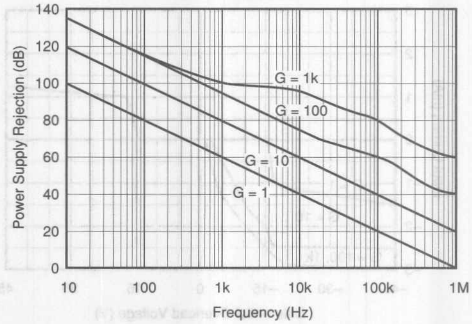
COMMON-MODE REJECTION vs FREQUENCY



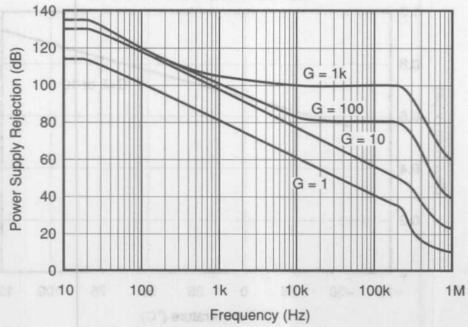
INPUT COMMON-MODE VOLTAGE RANGE
vs OUTPUT VOLTAGE



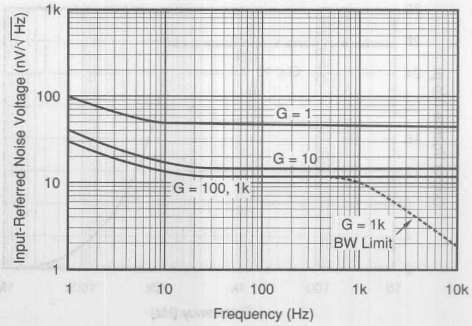
POSITIVE POWER SUPPLY REJECTION
vs FREQUENCY



NEGATIVE POWER SUPPLY REJECTION
vs FREQUENCY



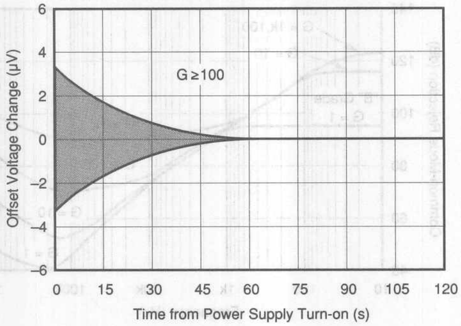
INPUT- REFERRED NOISE VOLTAGE
vs FREQUENCY



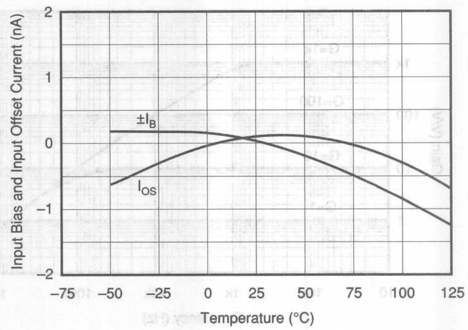
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

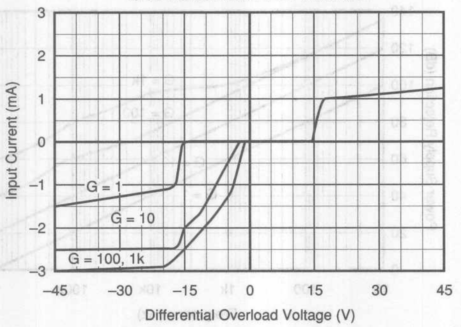
INPUT-REFERRED
OFFSET VOLTAGE WARM-UP vs TIME



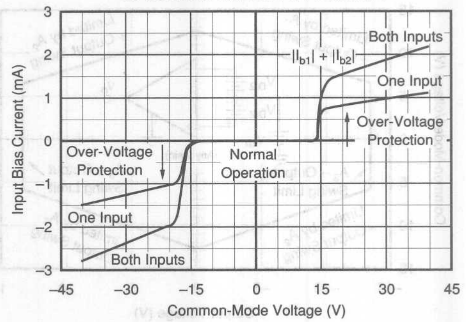
INPUT BIAS AND INPUT OFFSET CURRENT
vs TEMPERATURE



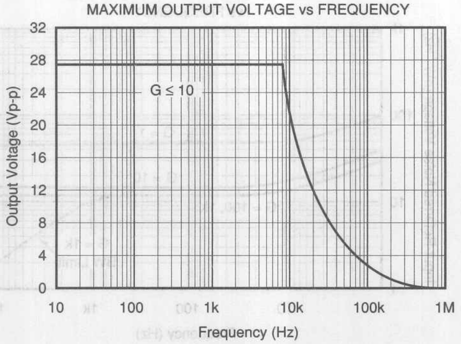
INPUT BIAS CURRENT
vs DIFFERENTIAL INPUT VOLTAGE



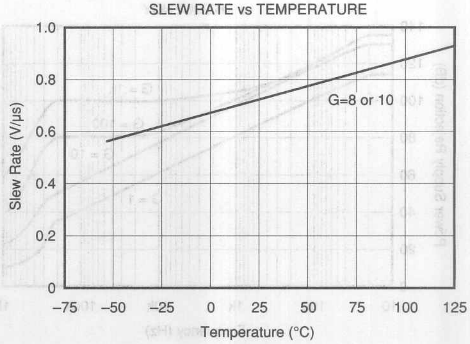
INPUT BIAS CURRENT
vs COMMON-MODE INPUT VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

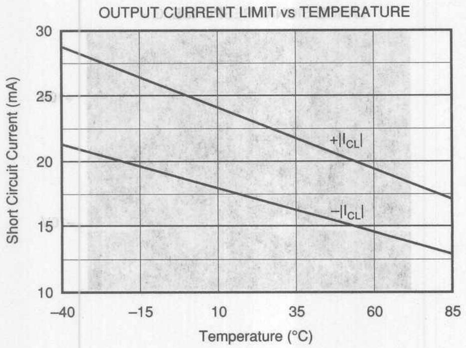


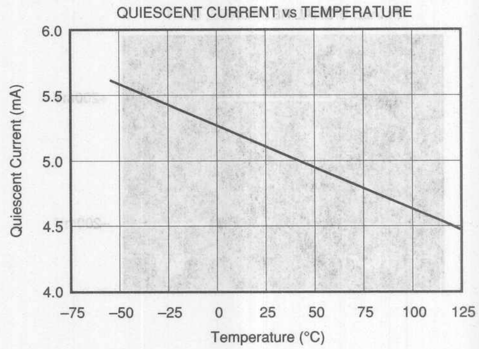
SLEW RATE vs TEMPERATURE

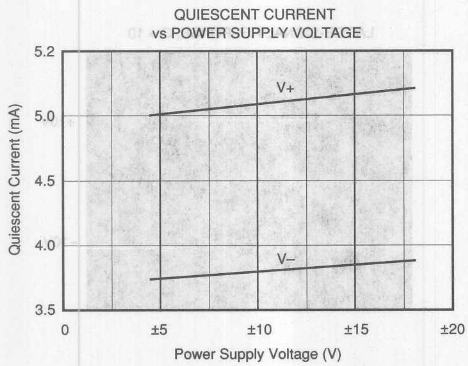


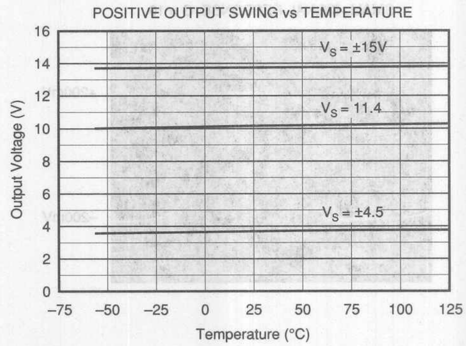
TYPICAL PERFORMANCE CURVES (CONT)

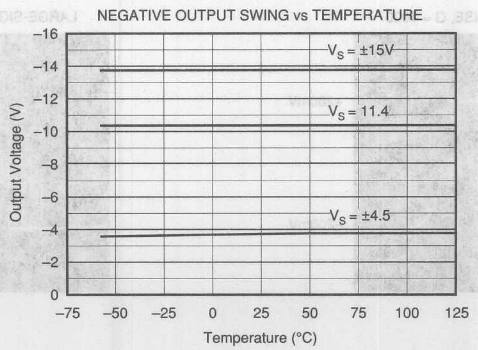
At T_A = +25°C, and V_S = ±15V, unless otherwise noted.



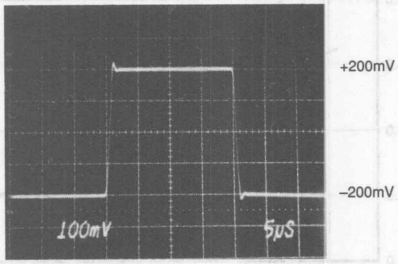




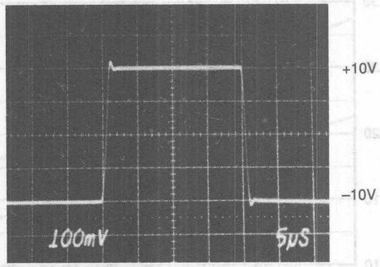




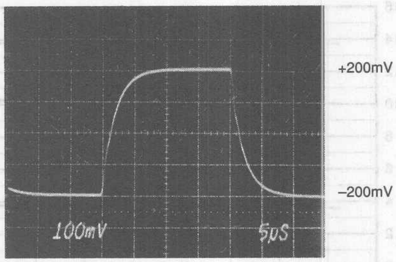
SMALL-SIGNAL RESPONSE, G = 1



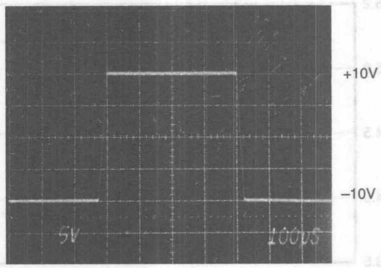
LARGE-SIGNAL RESPONSE, G = 1



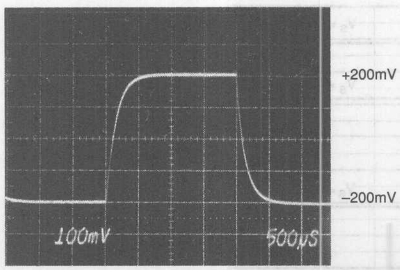
SMALL-SIGNAL RESPONSE, G = 10



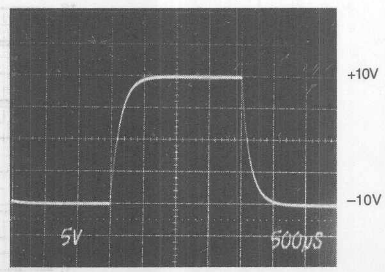
LARGE-SIGNAL RESPONSE, G = 10



SMALL-SIGNAL RESPONSE, G = 1000

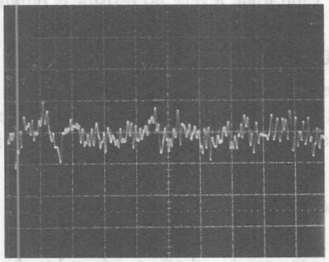


LARGE-SIGNAL RESPONSE, G = 1000

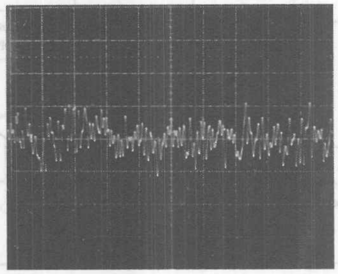


At $T_A = +25°C$, and $V_S = \pm15V$, unless otherwise noted.

INPUT-REFERRED NOISE,
0.1 TO 10Hz, G = 1000



NOISE, 0.1 TO 10Hz, G = 1



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA204/205. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

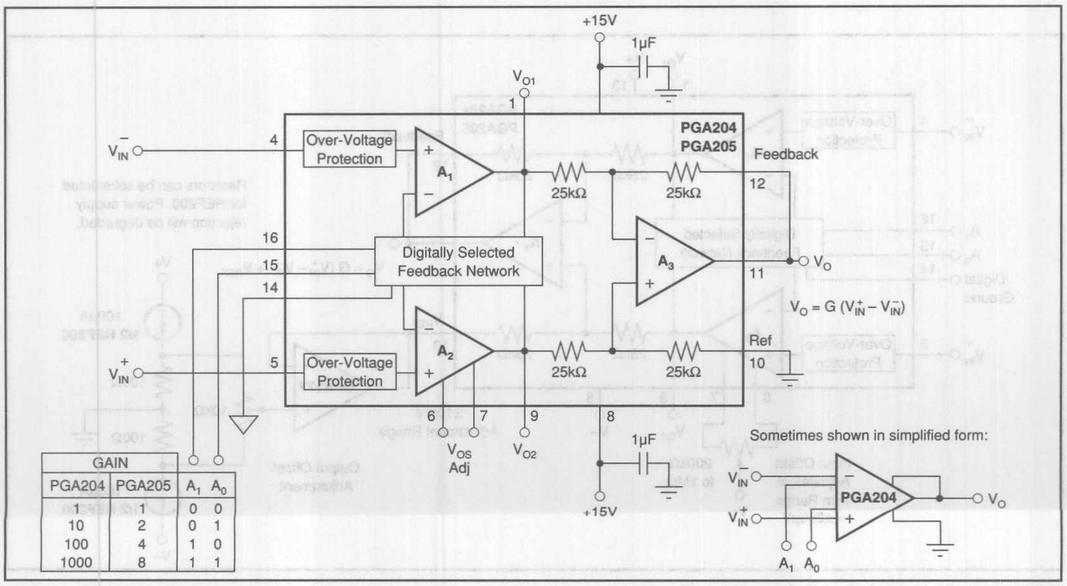
The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G=1).

The PGA204/205 has an output feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. The output Feedback connection can be used to sense the output voltage directly at the load for best accuracy.

DIGITAL INPUTS

The digital inputs A_0 and A_1 select the gain according to the logic table in Figure 1. Logic "1" is defined as a voltage greater than 2V above digital ground potential (pin 14). Digital ground can be connected to any potential from the V– power supply to 4V less than V+. Digital ground is normally connected to ground. The digital inputs interface directly CMOS and TTL logic components.

Approximately 1µA flows out of the digital input pins when a logic "0" is applied. Logic input current is nearly zero with a logic "1" input. A constant current of approximately



GAIN			
PGA204	PGA205	A_1	A_0
1	1	0	0
10	2	0	1
100	4	1	0
1000	8	1	1

FIGURE 1. Basic Connections.

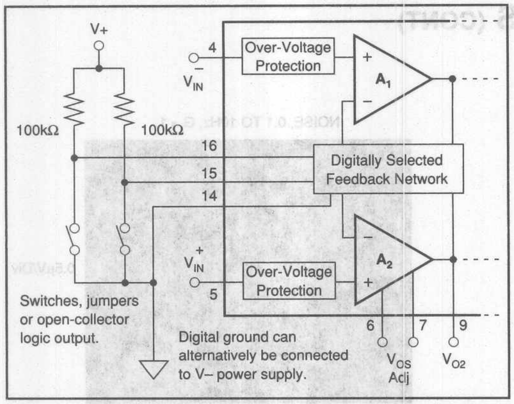


FIGURE 2. Switch or Jumper-Selected Digital Inputs.

1.3mA flows in the digital ground pin. It is good practice to return digital ground through a separate connection path so that analog ground is not affected by the digital ground current.

The digital inputs, A_0 and A_1, are not latched; a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately 1µs. The time to respond to gain change is effectively the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to access gain control data from a high speed data bus (see Figure 7). Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the latch circuitry as far as practical from analog circuitry.

Some applications select gain of the PGA204/205 with switches or jumpers. Figure 2 shows pull-up resistors connected to assure a noise-free logic "1" when the switch, jumper or open-collector logic is open or off. Fixed-gain applications can connect the logic inputs directly to V+ or V– (or other valid logic level); no resistor is required.

OFFSET VOLTAGE

Voltage offset of the PGA204/205 consists of two components—input stage offset and output stage offset. Both components are specified in the specification table in equation form:

$$V_{OS} = V_{OSI} + V_{OSO} / G \quad (1)$$

where:

V_{OS} total is the combined offset, referred to the input.

V_{OSI} is the offset voltage of the input stage, A_1 and A_2.

V_{OSO} is the offset voltage of the output difference amplifier, A_3.

V_{OSI} and V_{OSO} do not change with gain. The composite offset voltage V_{OS} changes with gain because of the gain term in equation 1. Input stage offset dominates in high gain (G≥100); both sources of offset may contribute at low gain (G=1 to 10).

OFFSET TRIMMING

Both the input and output stages are laser trimmed for very low offset voltage and drift. Many applications require no external offset adjustment.

Figure 3 shows an optional input offset voltage trim circuit. This circuit should be used to adjust only the input stage offset voltage of the PGA204/205. Do this by programming

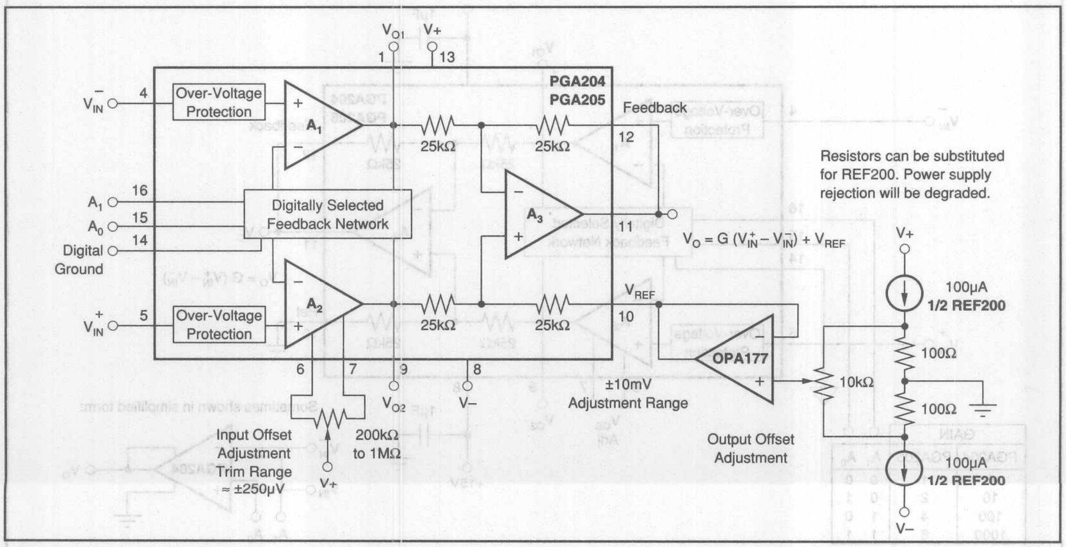


FIGURE 3. Optional Offset Voltage Trim Circuit.

it to its highest gain and trimming the output voltage to zero with the inputs grounded. Drift performance usually improves slightly when the input offset is nulled with this procedure.

Do not use the input offset adjustment to trim system offset or offset produced by a sensor. Nulling offset that is not produced by the input amplifiers will increase temperature drift by approximately 3.3μV/°C per 1mV of offset adjustment.

Many applications that need input stage offset adjustment do not need output stage offset adjustment. Figure 3 also shows a circuit for adjusting output offset voltage. First, adjust the input offset voltage as discussed above. Then program the device for G=1 and adjust the output to zero. Because of the interaction of these two adjustments at G=8, the PGA205 may require iterative adjustment.

The output offset adjustment can be used to trim sensor or system offsets without affecting drift. The voltage applied to the Ref terminal is summed with the output signal. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering the trim voltage with an op amp as shown.

NOISE PERFORMANCE

The PGA204/205 provides very low noise in most applications. Low frequency noise is approximately 0.4μVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of "low noise" chopper-stabilized amplifiers.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the PGA204/205 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the PGA204/205 is to operate properly. Figure 4 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the PGA204/205 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 4). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 4). These applications do not require additional resistor(s) for proper operation.

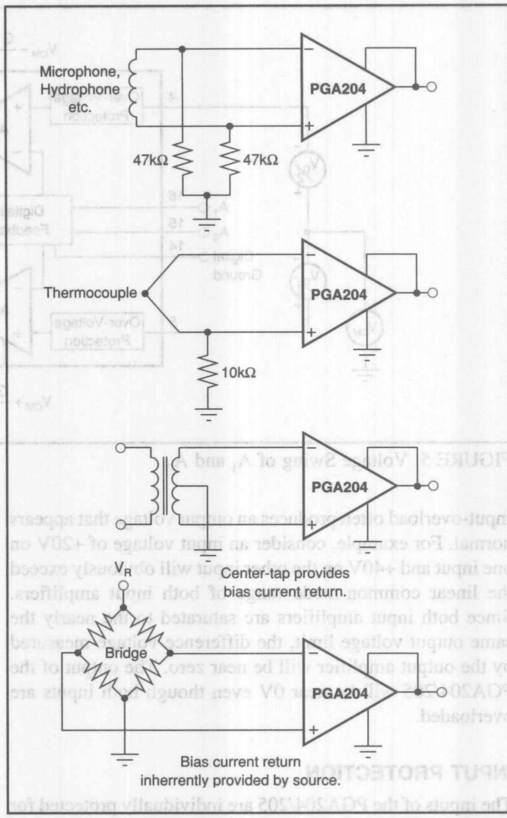


FIGURE 4. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the PGA204/205 is approximately ±12.7V (or 2.3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2. The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage."

A combination of common-mode and differential input voltage can cause the output of A_1 or A_2 to saturate. Figure 5 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3. For applications where input common-mode range must be maximized, limit the output voltage swing by selecting a lower gain of the PGA204/205 (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the PGA204/205 to increase the voltage swing.

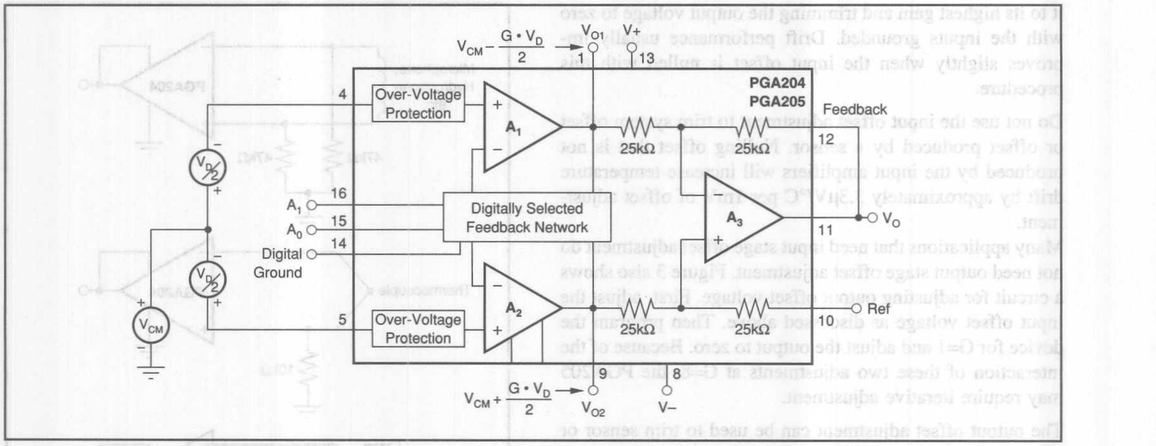
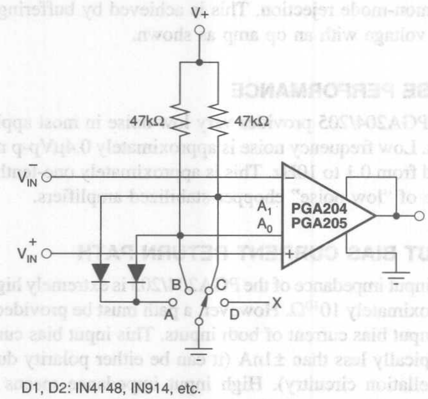


FIGURE 5. Voltage Swing of A_1 and A_2.

Input-overload often produces an output voltage that appears normal. For example, consider an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the PGA204/205 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the PGA204/205 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.



SWITCH POSITION	GAIN	
	PGA204	PGA205
A	1	1
B	10	2
C	100	4
D	1000	8

FIGURE 6. Switch-Selected PGIA.

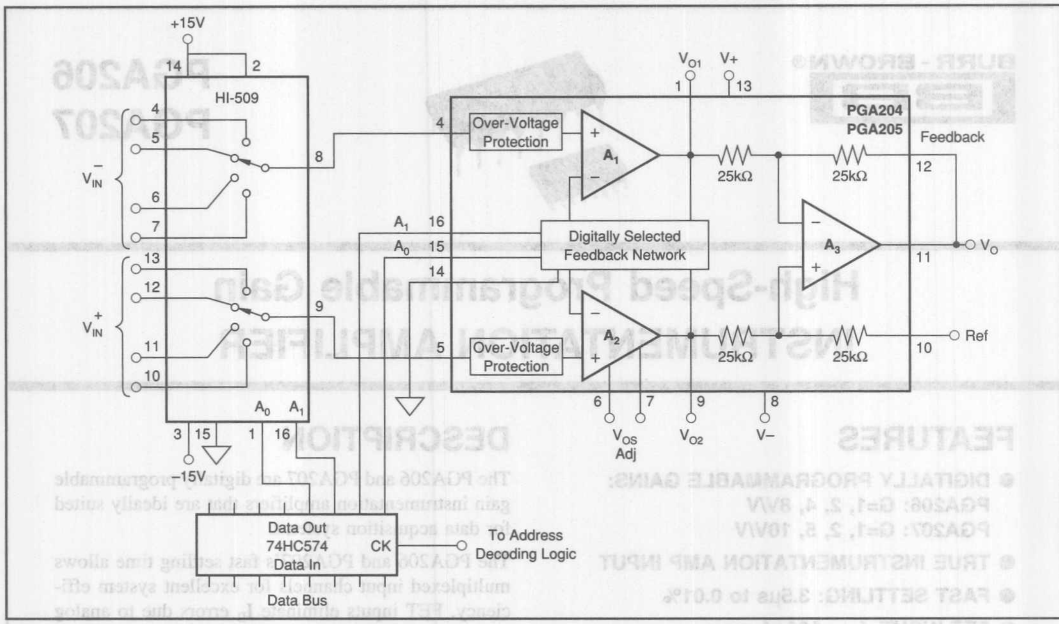


FIGURE 7. Multiplexed-Input Programmable Gain IA.

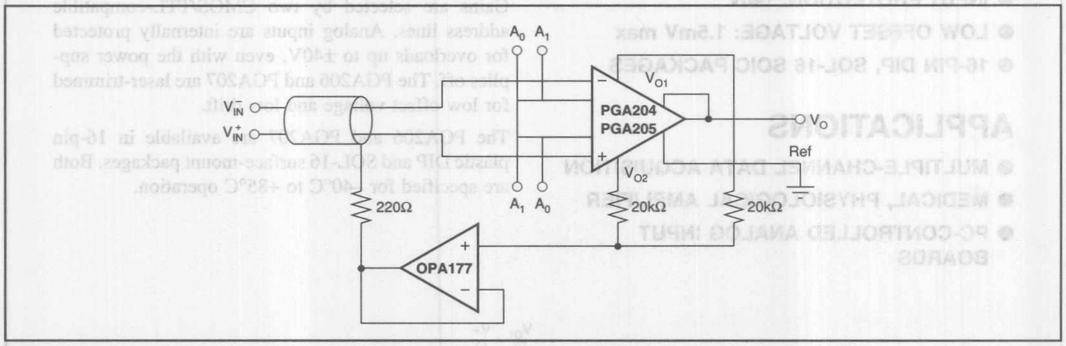
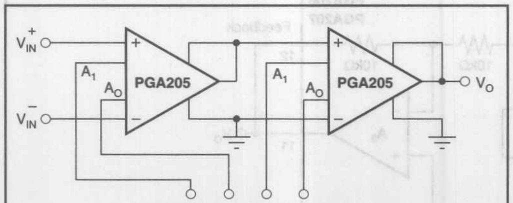


FIGURE 8. Shield Drive Circuit.



GAIN	A_3	A_2	A_1	A_0
1	0	0	0	0
2	0	1	0	0
4	1	0	0	0
8	1	1	0	0
16	1	1	0	1
32	1	1	1	0
64	1	1	1	1

FIGURE 9. Binary Gain Steps, G=1 to G=64.

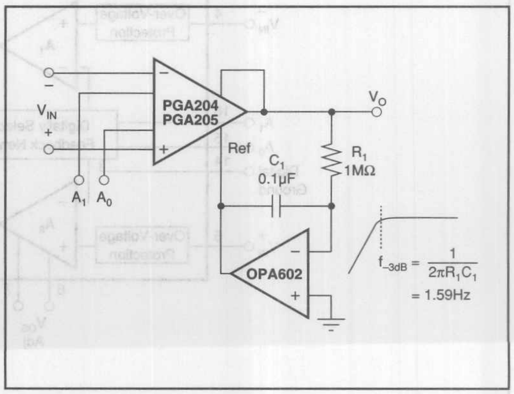


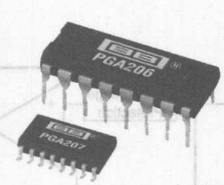
FIGURE 10. AC-Coupled PGIA.

PGA204/205

4

INSTRUMENTATION AMPLIFIERS

BURR - BROWN®



PGA206
PGA207

High-Speed Programmable Gain
INSTRUMENTATION AMPLIFIER

FEATURES

- DIGITALLY PROGRAMMABLE GAINS:
  PGA206: G=1, 2, 4, 8V/V
  PGA207: G=1, 2, 5, 10V/V
- TRUE INSTRUMENTATION AMP INPUT
- FAST SETTLING: 3.5μs to 0.01%
- FET INPUT: I_B = 100pA max
- INPUT PROTECTION: ±40V
- LOW OFFSET VOLTAGE: 1.5mV max
- 16-PIN DIP, SOL-16 SOIC PACKAGES

APPLICATIONS

- MULTIPLE-CHANNEL DATA ACQUISITION
- MEDICAL, PHYSIOLOGICAL AMPLIFIER
- PC-CONTROLLED ANALOG INPUT BOARDS

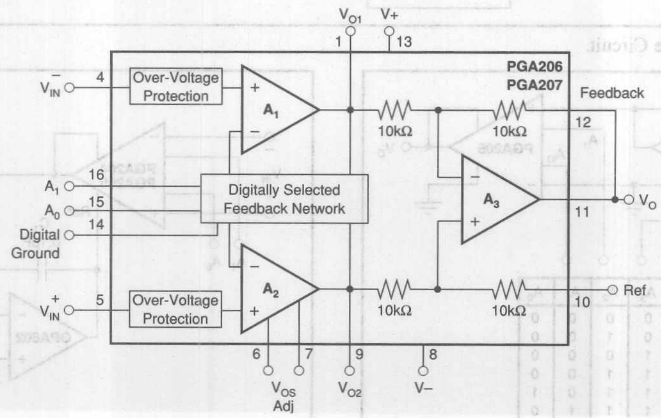
DESCRIPTION

The PGA206 and PGA207 are digitally programmable gain instrumentation amplifiers that are ideally suited for data acquisition systems.

The PGA206 and PGA207's fast settling time allows multiplexed input channels for excellent system efficiency. FET inputs eliminate I_B errors due to analog multiplexer series resistance.

Gains are selected by two CMOS/TTL-compatible address lines. Analog inputs are internally protected for overloads up to ±40V, even with the power supplies off. The PGA206 and PGA207 are laser-trimmed for low offset voltage and low drift.

The PGA206 and PGA207 are available in 16-pin plastic DIP and SOL-16 surface-mount packages. Both are specified for –40°C to +85°C operation.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1241A

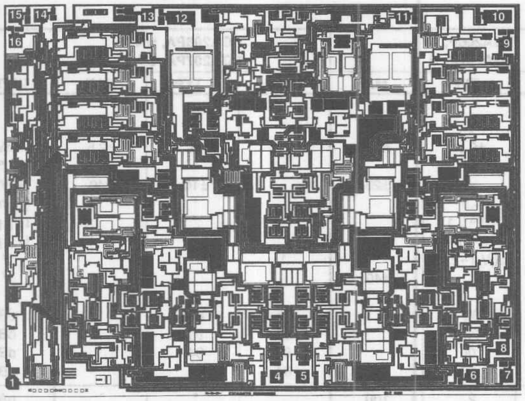
SPECIFICATIONS

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	PGA206P, U PGA207P, U MIN	TYP	MAX	PGA206PA, UA PGA207PA, UA MIN	TYP	MAX	UNITS
INPUT								
Offset Voltage, RTI	All Gains							
Initial	T_A = +25°C		±0.5	±1.5		±1	±2.5	mV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}, G = 8, 10		±2			*		µV/°C
vs Power Supply	V_S = ±4.5V to ±18V		±5	±20		±10	±40	µV/V
Long-Term Stability			4.5			*		µV/mo
Impedance, Differential			10^{13} || 1			*		Ω || pF
Common-Mode			10^{12} || 4			*		Ω || pF
Common-Mode Voltage Range(1)	V_O = 0V	±(|V_S|–4)	±(|V_S| –2.5)		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = ±11V, ΔR_S = 1kΩ							
	G = 1	80	92		75	86		dB
	G = 2	85	96		80	90		dB
	G = 4 or 5	90	100		84	94		dB
	G = 8 or 10	95	100		84	94		dB
INPUT BIAS CURRENT	V_{IN} = 0		2	100		*	*	pA
vs Temperature			See Typical Curve			*		
Offset Current			1	100		*	*	pA
vs Temperature			See Typical Curve			*		
NOISE VOLTAGE, RTI	G = 8,10; R_S = 0Ω							
f = 10Hz			30			*		nV/√Hz
f = 100Hz			20			*		nV/√Hz
f = 1kHz			18			*		nV/√Hz
f_B = 0.1Hz to 10Hz			1			*		µVp-p
Noise Current								
f = 1kHz			1.5			*		fA/√Hz
GAIN	All Gains, V_O = ±11V							
Gain Error			±0.01	±0.05		*	±0.1	%
Gain vs Temperature(2)			±1	±10		*	*	ppm/°C
Nonlinearity			±0.0003	±0.002		*	±0.005	% of FSR
OUTPUT								
Voltage, Positive		(V+) –4	(V+) –2.3		*	*		V
Negative		(V–) +4	(V–) +1.5		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			±17			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		5			*		MHz
	G = 2		4			*		MHz
	G = 4, 5		1.3			*		MHz
	G = 8, 10		600			*		kHz
Slew Rate	V_O = ±10V, G = 1 to 10		25			*		V/µs
Settling Time, 0.1%	20V Step, All Gains		2			*		µs
0.01%	20V Step, All Gains		3.5			*		µs
Output Overload Recovery	50% Overdrive		1.5			*		µs
DIGITAL LOGIC INPUTS								
Digital Ground Voltage, V_{DG}		V–		(V+) –4	*		*	V
Digital Low Voltage		V–		V_{DG} + 0.8V	*		*	V
Digital Input Current			1			*		pA
Digital High Voltage		V_{DG}+2		V+	*		*	V
Gain Switching Time			500			*		ns
POWER SUPPLY								
Voltage Range		±4.5	±15	±18	*		*	V
Current	V_{IN} = 0V		+12.4/–11.2	±13.5		*		mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operating		–40		+125	*		*	°C
Thermal Resistance, θ_{JA}			80			*		°C/W

* Specification same as PGA206P or PGA207P.

NOTES: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.



PGA206 and PGA207 DIE TOPOGRAPHY

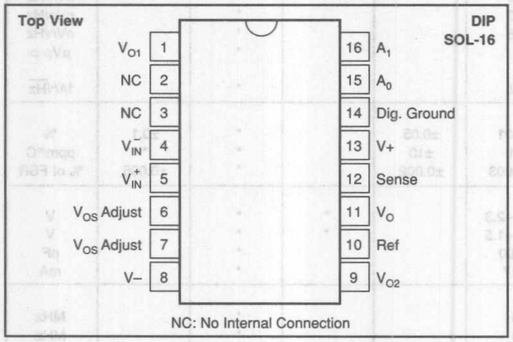
PAD	FUNCTION	PAD	FUNCTION
1	V_{O1}	9	V_{O2}
2	—	10	Ref
3	—	11	V_O
4	V_{IN}^-	12	Sense
5	V_{IN}^+	13	V+
6	V_{OS} Adjust	14	Dig. Ground
7	V_{OS} Adjust	15	A_0
8	V–	16	A_1

Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	182 x 140 ±5	4.65 x 3.56 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Logic Input Voltage Range	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering –10s)	+300°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
PGA206PA	16-Pin Plastic DIP	180
PGA206P	16-Pin Plastic DIP	180
PGA206UA	SOL-16 Surface Mount	211
PGA206U	SOL-16 Surface Mount	211
PGA207PA	16-Pin Plastic DIP	180
PGA207P	16-Pin Plastic DIP	180
PGA207UA	SOL-16 Surface Mount	211
PGA207U	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	GAINS	PACKAGE	TEMPERATURE RANGE
PGA206PA	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA206P	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA206UA	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA206U	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA207PA	1, 2, 5, 10V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA207P	1, 2, 5, 10V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA207UA	1, 2, 5, 10V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA207U	1, 2, 5, 10V/V	SOL-16 Surface-Mount	–40°C to +85°C

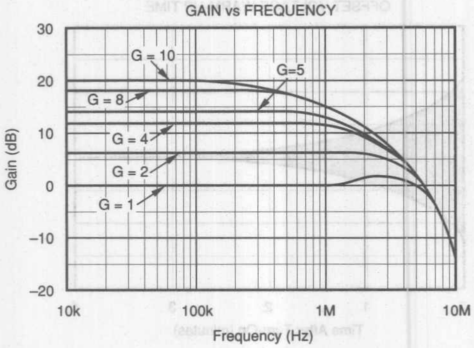
ELECTROSTATIC DISCHARGE SENSITIVITY

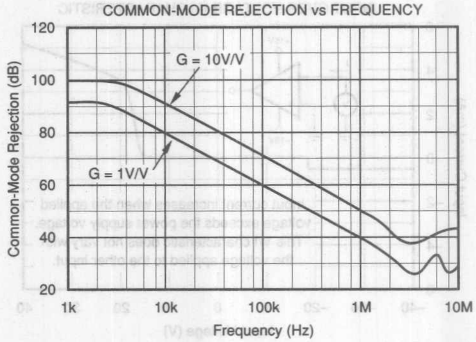
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

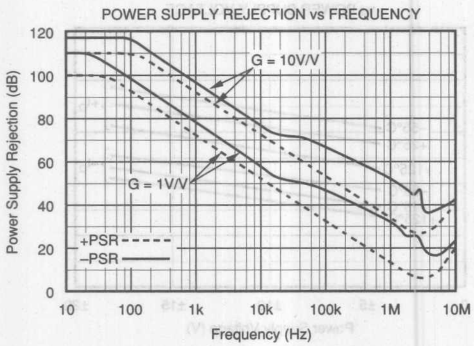
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

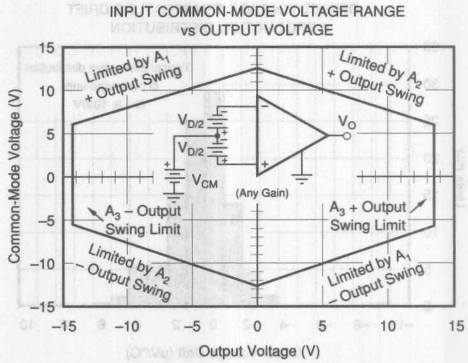
TYPICAL PERFORMANCE CURVES

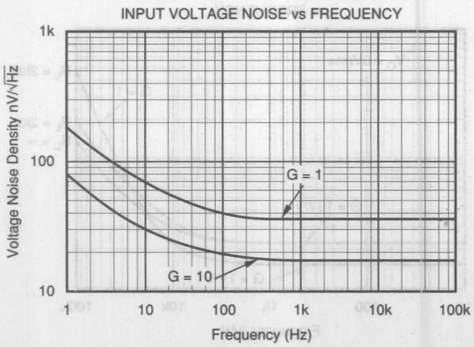
At $T_A = +25°C$, and $V_S = \pm15V$, unless otherwise noted.

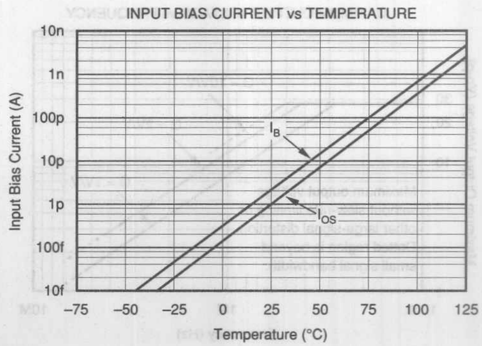












PGA206/207

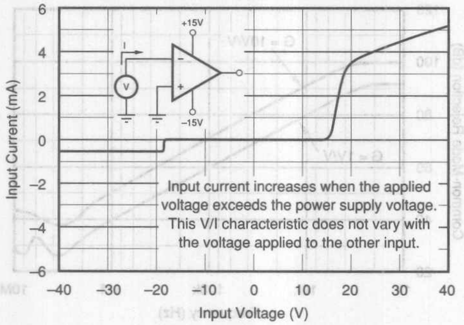
4

INSTRUMENTATION AMPLIFIERS

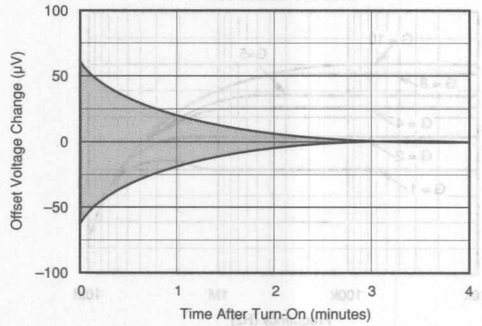
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

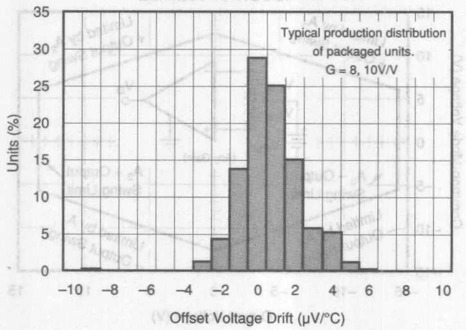
INPUT OVER-VOLTAGE V/I CHARACTERISTIC



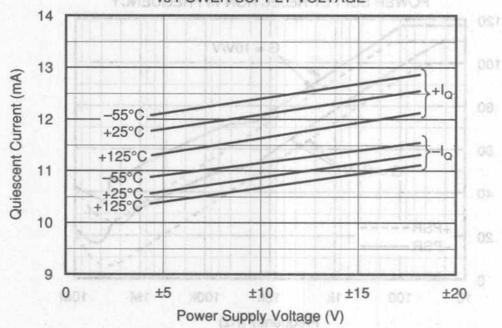
OFFSET VOLTAGE WARM-UP TIME



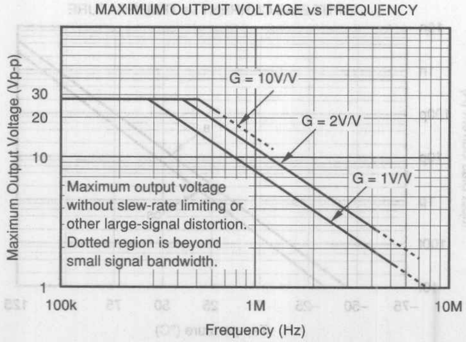
OFFSET VOLTAGE TEMPERATURE DRIFT PRODUCTION DISTRIBUTION



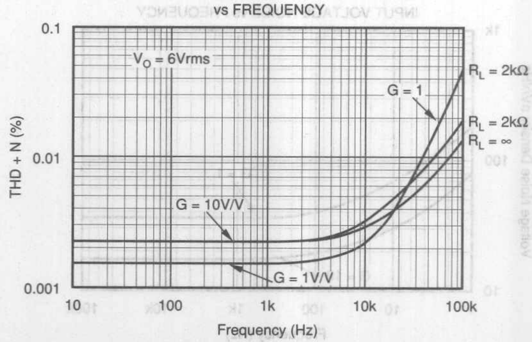
QUIESCENT CURRENT vs POWER SUPPLY VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



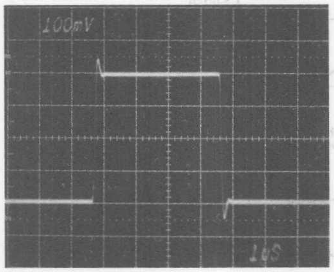
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



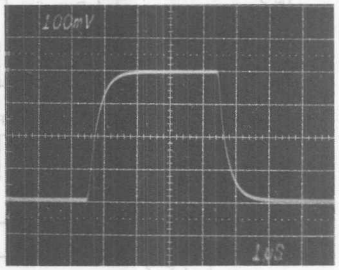
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

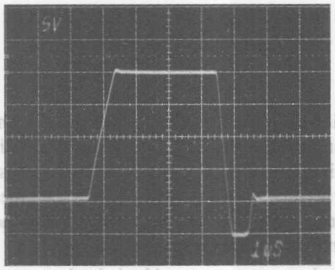
SMALL SIGNAL RESPONSE
G = 1, C_L = 50pF



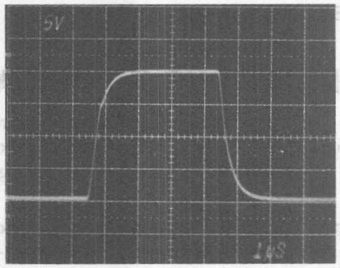
SMALL SIGNAL RESPONSE
G = 10, C_L = 50pF

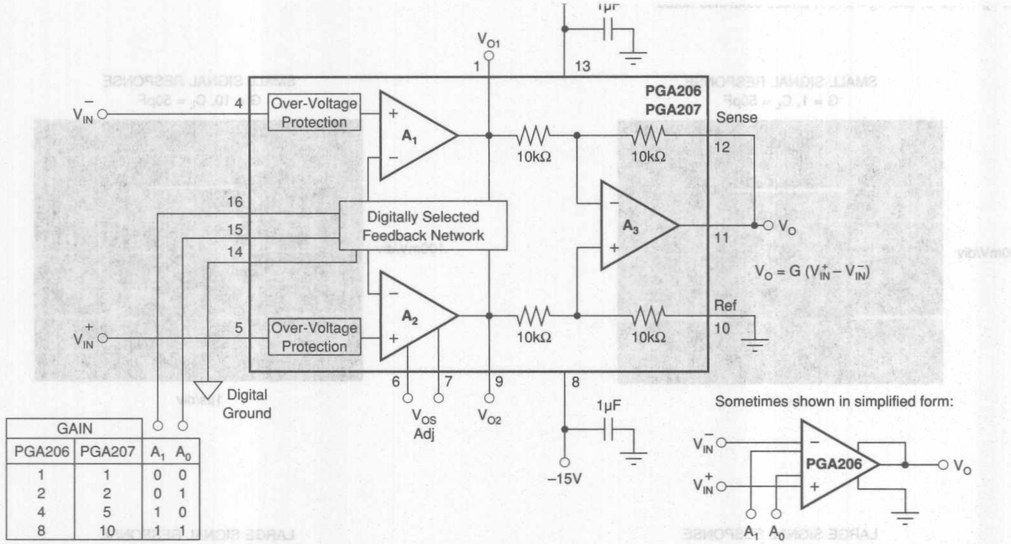


LARGE SIGNAL RESPONSE
G = 1, C_L = 50pF



LARGE SIGNAL RESPONSE
G = 10, C_L = 50pF





GAIN			
PGA206	PGA207	A_1	A_0
1	1	0	0
2	2	0	1
4	5	1	0
8	10	1	1

FIGURE 1. Basic Connections.

APPLICATIONS INFORMATION

Figure 1 shows the circuit diagram for basic operation of the PGA206 or PGA207. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 2Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

The output sense connection (pin 12) must be connected to the output terminal (pin 11) for proper operation. This connection can be made at the load for best accuracy.

DIGITAL INPUTS

The digital inputs A_0 and A_1 select the gain according to the logic table in Figure 1. Logic "1" is defined as a voltage greater than 2V above digital ground potential (pin 14). Digital ground can be connected to any potential ranging from the V– power supply to 4V less than V+. Digital ground is usually equal to analog ground potential and the two grounds are connected at the power supply. The digital inputs interface directly to CMOS and TTL logic.

A nearly constant current of approximately 1.2mA flows in the digital ground pin. It is good practice to return digital ground through a separate connection path so that analog ground is not affected by the digital ground current.

The digital inputs, A_0 and A_1, are not latched. A change in logic input immediately selects a new gain. Switching time of the logic is approximately 500ns. The time to respond to gain change is equal to switching time, plus the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to acquire gain control data from a high speed digital bus. Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the digital latch as far as practical from analog circuitry to avoid coupling digital noise into analog input circuitry.

OFFSET VOLTAGE ADJUSTMENT

The PGA206 and PGA207 are laser trimmed for very low offset voltage and drift. Many applications require no external offset adjustment. Multiplexed data acquisition systems generally correct offset by grounding the inputs of one channel to measure offset voltage. Stored offset values for each gain are then subtracted from subsequent readings of other channels.

Figure 2 shows optional offset voltage trim circuits. Offset voltage changes with the selected gain. To adjust for low offset voltage in all gains, both input and output offsets must be trimmed.

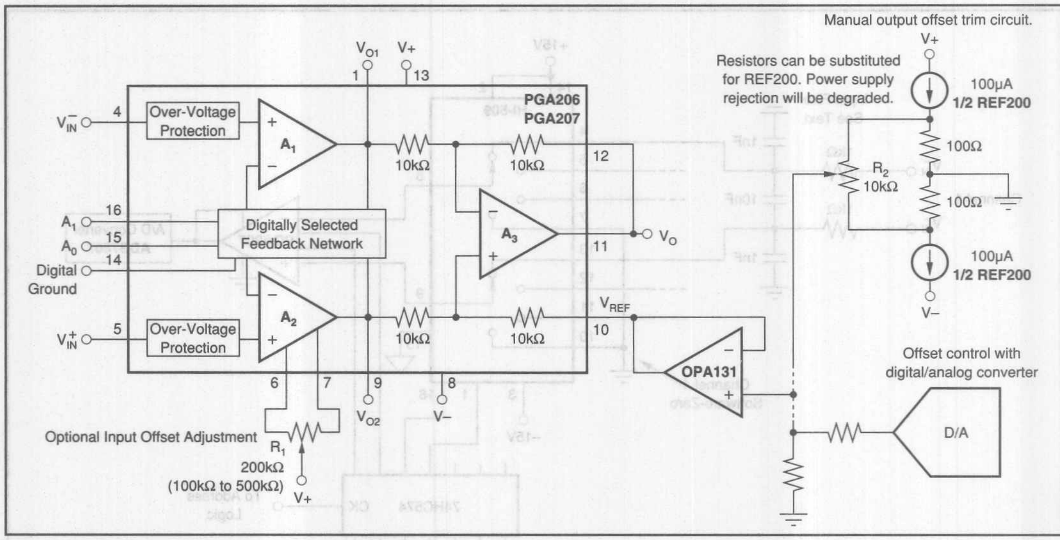


FIGURE 2. Optional Offset Voltage Trim Circuits.

R_1 adjusts the offset of the input amplifiers. Output stage offset is adjusted with R_2. A buffer op amp is required in the output offset adjustment circuit, as shown, to assure that the Ref pin is driven by a low source impedance. To adjust for low offset voltage in all gains, first adjust the input stage offset in the highest gain. Then adjust the output stage offset (R_2) in G = 1. Iterate the adjustments for lowest offset in all gains.

Offset can also be adjusted under processor control with a D/A converter as shown in Figure 2. The D/A's output voltage can be reduced with a resistor divider for better adjustment resolution, but an op amp buffer following the divider is required to provide a low source impedance to the ref terminal. A different offset value is required for each amplifier gain.

INPUT BIAS CURRENT RETURN PATH

The FET inputs of the PGA206 and PGA207 provide extremely high input impedance. Still, a path must be provided for the bias current of each input. Figure 3 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the linear input voltage range and the input amplifiers will saturate.

If the differential source resistance is low, a bias current return path can be connected to only one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 3). These applications do not require additional resistor(s) for proper operation.

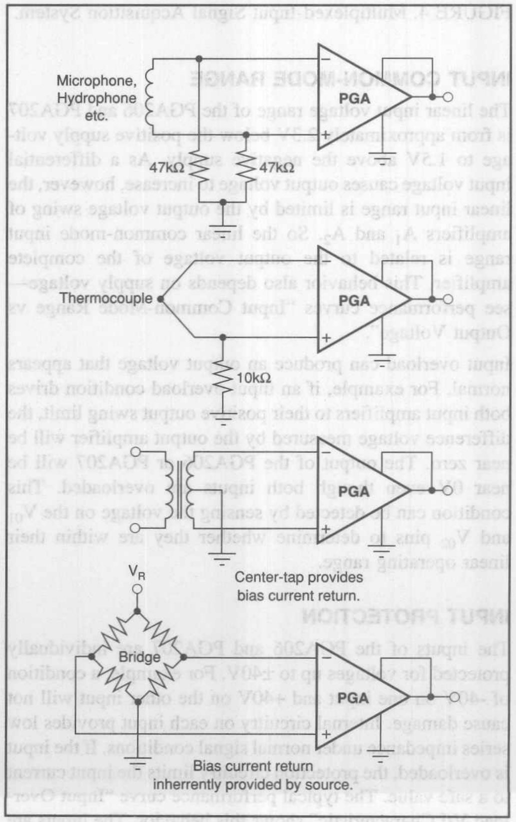


FIGURE 3. Providing an Input Bias Current Path.

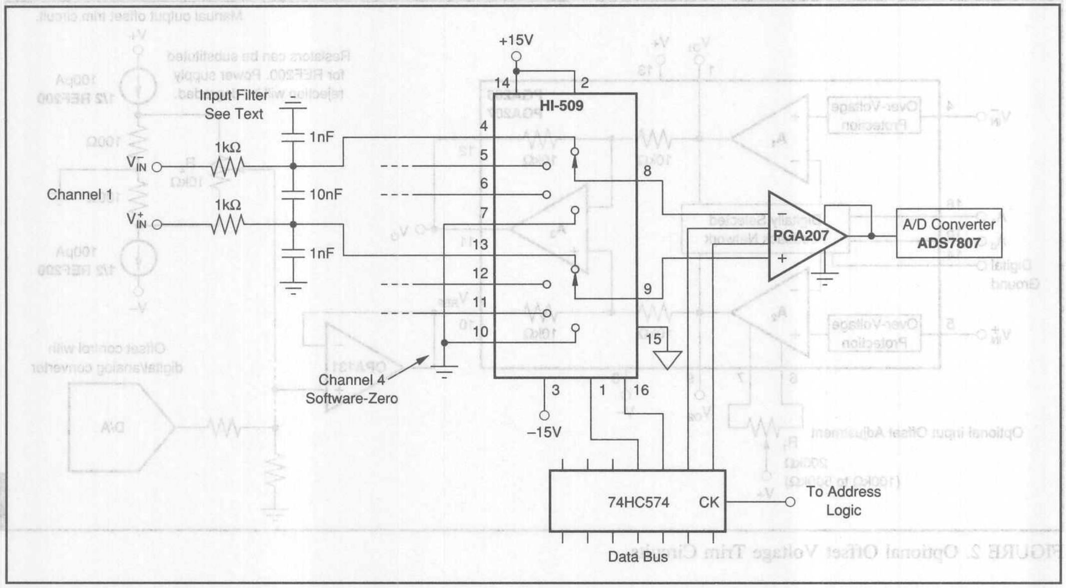


FIGURE 4. Multiplexed-Input Signal Acquisition System.

INPUT COMMON-MODE RANGE

The linear input voltage range of the PGA206 and PGA207 is from approximately 2.3V below the positive supply voltage to 1.5V above the negative supply. As a differential input voltage causes output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage".

Input overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the PGA206 or PGA207 will be near 0V even though both inputs are overloaded. This condition can be detected by sensing the voltage on the V_{01} and V_{02} pins to determine whether they are within their linear operating range.

INPUT PROTECTION

The inputs of the PGA206 and PGA207 are individually protected for voltages up to ±40V. For example, a condition of -40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value. The typical performance curve "Input Overload V/I Characteristic" shows this behavior. The inputs are protected even if no power supply voltage is applied.

MULTIPLEXED INPUTS

The PGA206 and PGA207 are ideally suited for multiple channel data acquisition. Figure 4 shows a typical application with an analog multiplexer used to connect one of four differential input signals to a single PGA207.

Careful circuit layout will help preserve accuracy of multiplexed signals. Run the inverting and non-inverting connections of each channel parallel to each other over a ground plane, or directly adjacent on top and bottom of the circuit board. Grounded guard traces between channels help reduce stray signal pick-up.

Multiplexed signals from high impedance sources require special care. As inputs are switched by the multiplexer, charge can be injected into the source, disturbing the input signal. Since many such sources involve slow signals, a simple R/C filter at the input can be used to dramatically reduce this effect. The arrangement shown filters both the differential signal and common-mode noise.

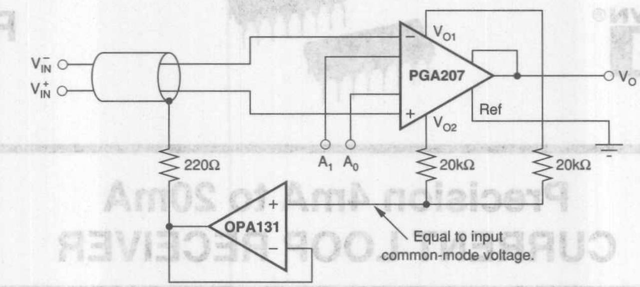
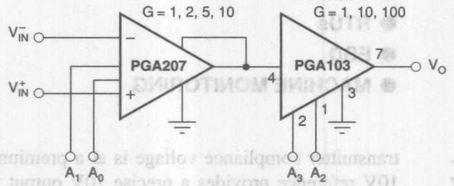


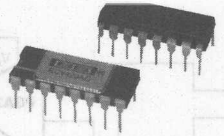
FIGURE 5. Shield Drive Circuit.



GAIN (V/V)	A_1	A_0	A_3	A_2
1	0	0	0	0
2	0	1	0	0
5	1	0	0	0
10	1	1	0	0
20	0	1	0	1
50	1	0	0	1
100	1	1	0	1
200	0	1	1	0
500	1	0	1	0
1000	1	1	1	0

FIGURE 6. Wide Gain Range Programmable IA.

BURR - BROWN®



RCV420

Precision 4mA to 20mA CURRENT LOOP RECEIVER

FEATURES

- COMPLETE 4-20mA TO 0-5V CONVERSION
- INTERNAL SENSE RESISTORS
- PRECISION 10V REFERENCE
- BUILT-IN LEVEL-SHIFTING
- ±40V COMMON-MODE INPUT RANGE
- 0.1% OVERALL CONVERSION ACCURACY
- HIGH NOISE IMMUNITY: 86dB CMR

APPLICATIONS

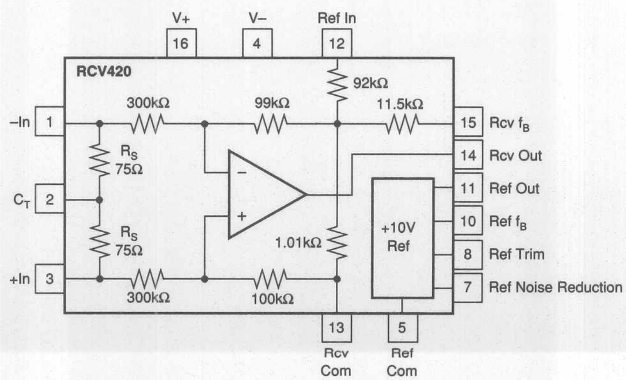
- PROCESS CONTROL
- INDUSTRIAL CONTROL
- FACTORY AUTOMATION
- DATA ACQUISITION
- SCADA
- RTUs
- ESD
- MACHINE MONITORING

DESCRIPTION

The RCV420 is a precision current-loop receiver designed to convert a 4–20mA input signal into a 0–5V output signal. As a monolithic circuit, it offers high reliability at low cost. The circuit consists of a premium grade operational amplifier, an on-chip precision resistor network, and a precision 10V reference. The RCV420 features 0.1% overall conversion accuracy, 86dB CMR, and ±40V common-mode input range.

The circuit introduces only a 1.5V drop at full scale, which is useful in loops containing extra instrument burdens or in intrinsically safe applications where transmitter compliance voltage is at a premium. The 10V reference provides a precise 10V output with a typical drift of 5ppm/°C.

The RCV420 is completely self-contained and offers a highly versatile function. No adjustments are needed for gain, offset, or CMR. This provides three important advantages over discrete, board-level designs: 1) lower initial design cost, 2) lower manufacturing cost, and 3) easy, cost-effective field repair of a precision circuit.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 741-4395 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

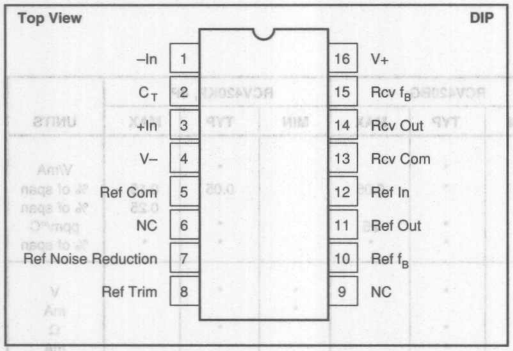
T = +25°C and V_S = ±15V unless otherwise noted.

	RCV420AG			RCV420BG			RCV420KP, JP			
CHARACTERISTICS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN										
Initial		0.3125			*			*		V/mA
Error		0.025	0.1		*	0.05		0.05	0.15	% of span
Error—JP Grade									0.25	% of span
vs Temp		15	50		*	25		*		ppm/°C
Nonlinearity(1)		0.0002	0.002		*	*		*	*	% of span
OUTPUT										
Rated Voltage (I_O = +10mA, –5mA)	10	12		*	*		*	*		V
Rated Current (E_O = 10V)	+10, –5			*			*			mA
Impedance (Differential)		0.01			*			*		Ω
Current Limit (To Common)		+49, –13			*			*		mA
Capacitive Load		1000			*			*		pF
(Stable Operation)										
INPUT										
Sense Resistance	74.25	75	75.75	*	*	*	*	*	*	Ω
Input Impedance (Common-Mode)		200			*			*		kΩ
Common-Mode Voltage			±40			*			*	V
CMR(2)	72	80		86	94		70	*		dB
vs Temp (DC) (T_A = T_{MIN} to T_{MAX})	66	76		80	90			*		dB
AC 60Hz		80			94			*		dB
OFFSET VOLTAGE (RTO)(3)										
Initial			1			*			*	mV
vs Temp		10	50		*	25		*		µV/°C
vs Supply (±11.4V to ±18V)	74	90		80	*		*	*		dB
vs Time		200			*			*		µV/mo
ZERO ERROR(4)										
Initial		0.01	0.05		*	0.025		0.025	0.075	% of span
Initial—JP Grade									0.15	% of span
vs Temp		10	50		*	25		*		ppm of
									span/°C	
OUTPUT NOISE VOLTAGE										
f_B = 0.1Hz to 10Hz		50			*			*		µVp-p
f_O = 10kHz		800			*			*		$nV/\sqrt{Hz}$
DYNAMIC RESPONSE										
Gain Bandwidth		150			*			*		kHz
Full Power Bandwidth		30			*			*		kHz
Slew Rate		1.5			*			*		V/µs
Settling Time (0.01%)		10			*			*		µs
VOLTAGE REFERENCE										
Initial	9.995		10.005	*		*	9.99		10.01	V
Trim Range(5)		±4			*			*		%
vs Temp(6)		5	20		*	*		*		ppm/°C
vs Supply (±11.4V to ±18V)		0.0002			*			*		%/V
vs Output Current (I_O = 0 to +10mA)		0.0002			*			*		%/mA
vs Time		15			*			*		ppm/kHr
Noise (0.1Hz to 10Hz)		5			*			*		µVp-p
Output Current	+10, –2			*			*			mA
POWER SUPPLY										
Rated		±15			*			*		V
Voltage Range(7)	–5, +11.4		±18	*		*	*		*	V
Quiescent Current (V_O = 0V)		3	4		*	*		*	*	mA
TEMPERATURE RANGE										
Specification	–25		+85	*		*	0		+70	°C
Operation	–55		+125	*		*	–25		+85	°C
Storage	–65		+150	*		*	–40		+85	°C

*Specification same as RCV420AG.

NOTES: (1) Nonlinearity is the max peak deviation from best fit straight line. (2) With 0 source impedance on Rcv Com pin. (3) Referred to output with all inputs grounded including Ref In. (4) With 4mA input signal and Voltage Reference connected (includes V_{OS}, Gain Error, and Voltage Reference Errors). (5) External trim slightly affects drift. (6) The "box method" is used to specify output voltage drift vs temperature. (7) I_O Ref = 5mA, I_O Rcv = 2mA.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply	±22V
Input Current, Continuous	40mA
Input Current Momentary, 0.1s	250mA, 1% Duty Cycle
Common-Mode Input Voltage, Continuous	±40V
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common (Rcv and Ref)	Continuous

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
RCV420AG	16-Pin Hermetic DIP	109
RCV420BG	16-Pin Hermetic DIP	109
RCV420KP	16-Pin Plastic DIP	180
RCV420JP	16-Pin Plastic DIP	180

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

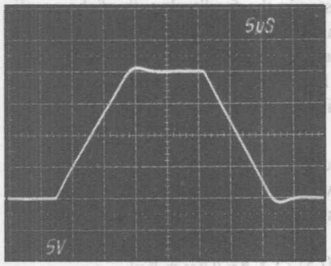
ORDERING INFORMATION

MODEL	PERFORMANCE GRADE	PACKAGE
RCV420AG	–25°C to +85°C	16-Pin Hermetic DIP
RCV420BG	–25°C to +85°C	16-Pin Hermetic DIP
RCV420KP	0°C to +70°C	16-Pin Plastic DIP
RCV420JP	0°C to +70°C	16-Pin Plastic DIP

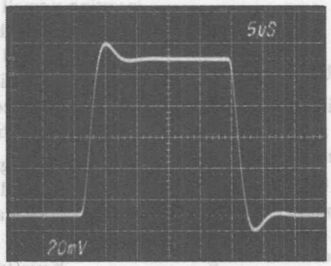
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

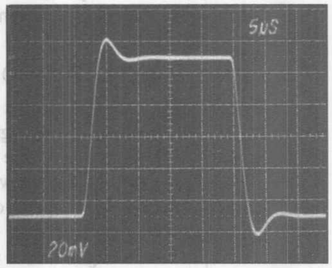
STEP RESPONSE
NO LOAD



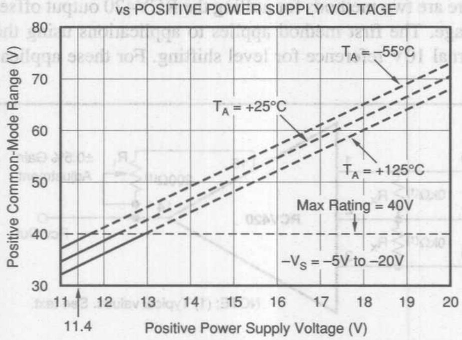
SMALL SIGNAL RESPONSE
NO LOAD



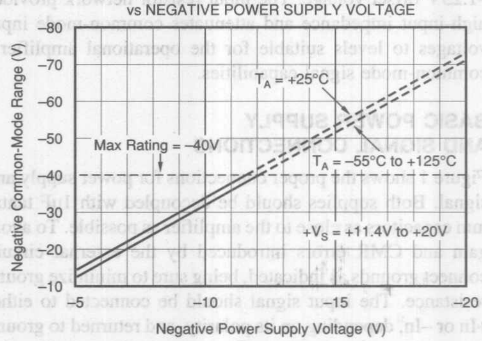
SMALL SIGNAL RESPONSE
R_L = ∞, C_L = 1000pF



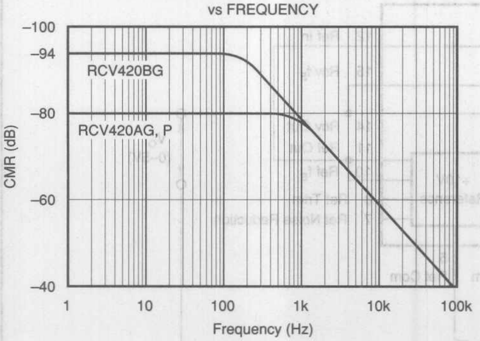
POSITIVE COMMON-MODE VOLTAGE RANGE
vs POSITIVE POWER SUPPLY VOLTAGE



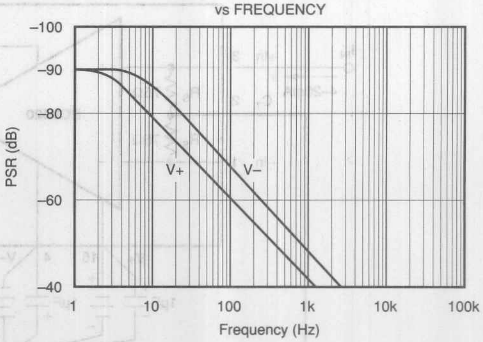
NEGATIVE COMMON-MODE VOLTAGE RANGE
vs NEGATIVE POWER SUPPLY VOLTAGE



COMMON-MODE REJECTION
vs FREQUENCY



POWER-SUPPLY REJECTION
vs FREQUENCY



RCV420

4

INSTRUMENTATION AMPLIFIERS

Refer to the figure on the first page. For 0–5V output with 4–20mA input, the required transimpedance of the circuit is:

$$V_{OUT}/I_{IN} = 5V/16mA = 0.3125V/mA.$$

To achieve the desired output (0V for 4mA and 5V for 20mA), the output of the amplifier must be offset by an amount:

$$V_{OS} = -(4mA)(0.3125V/mA) = -1.25V.$$

The input current signal is connected to either +In or –In, depending on the polarity of the signal, and returned to ground through the center tap, C_T. The balanced input—two matched 75Ω sense resistors, R_S—provides maximum rejection of common-mode voltage signals on C_T and true differential current-to-voltage conversion. The sense resistors convert the input current signal into a proportional voltage, which is amplified by the differential amplifier. The voltage gain of the amplifier is:

$$A_D = 5V/(16mA)(75\Omega) = 4.1667V/V.$$

The tee network in the feedback path of the amplifier provides a summing junction used to generate the required –1.25V offset voltage. The input resistor network provides high-input impedance and attenuates common-mode input voltages to levels suitable for the operational amplifier's common-mode signal capabilities.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Both supplies should be decoupled with 1μF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. The input signal should be connected to either +In or –In, depending on its polarity, and returned to ground through the center tap, C_T. The output of the voltage reference, Ref Out, should be connected to Ref In for the

GAIN AND OFFSET ADJUSTMENT

Figure 2 shows the circuit for adjusting the RCV420 gain. Increasing the gain of the RCV420 is accomplished by inserting a small resistor in the feedback path of the amplifier. Increasing the gain using this technique results in CMR degradation, and therefore, gain adjustments should be kept as small as possible. For example, a 1% increase in gain is typically realized with a 125Ω resistor, which degrades CMR by about 6dB.

A decrease in gain can be achieved by placing matched resistors in parallel with the sense resistors, also shown in Figure 2. The adjusted gain is given by the following expression

$$V_{OUT}/I_{IN} = 0.3125 \times R_X/(R_X + R_S).$$

A 1% decrease in gain can be achieved with a 7.5kΩ resistor. It is important to match the parallel resistance on each sense resistor to maintain high CMR. The TCR mismatch between the two external resistors will effect gain error drift and CMR drift.

There are two methods for nulling the RCV420 output offset voltage. The first method applies to applications using the internal 10V reference for level shifting. For these applica-

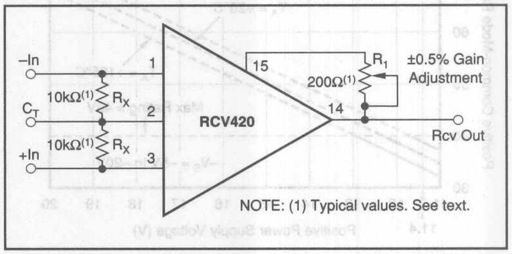


FIGURE 2. Optional Gain Adjustment.

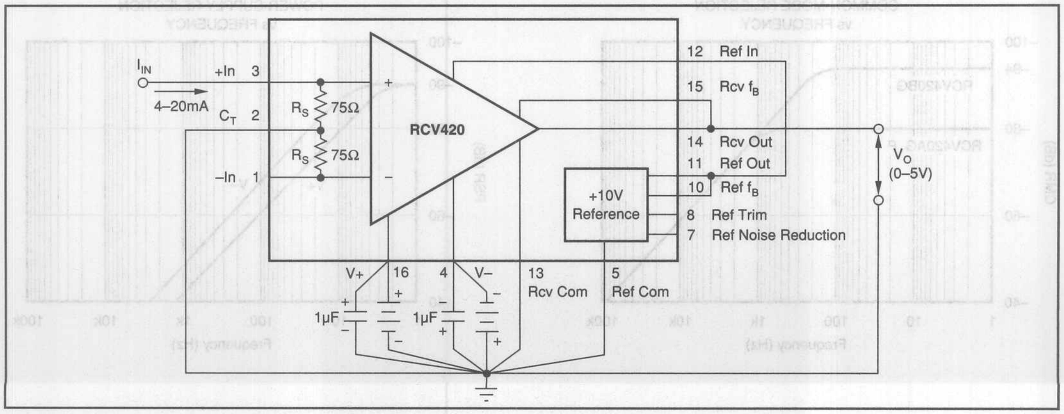


FIGURE 1. Basic Power Supply and Signal Connections.

tions, the voltage reference output trim procedure can be used to null offset errors at the output of the RCV420. The voltage reference trim circuit is discussed under "Voltage Reference."

When the voltage reference is not used for level shifting or when large offset adjustments are required, the circuit in Figure 3 can be used for offset adjustment. A low impedance on the Rcv Com pin is required to maintain high CMR.

ZERO ADJUSTMENT

Level shifting the RCV420 output voltage can be achieved using either the Ref In pin or the Rcv Com pin. The disadvantage of using the Ref In pin is that there is an 8:1 voltage attenuation from this pin to the output of the RCV420. Thus, use the Rcv Com pin for large offsets, because the voltage on this pin is seen directly at the output. Figure 4 shows the circuit used to level-shift the output of the RCV420 using the Rcv Com pin. It is important to use a low-output impedance amplifier to maintain high CMR. With this method of zero adjustment, the Ref In pin must be connected to the Rcv Com pin.

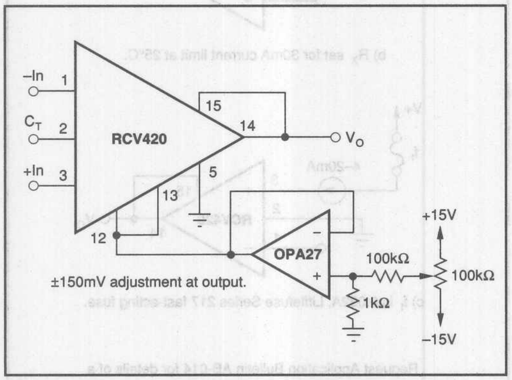


FIGURE 3. Optional Output Offset Nulling Using External Amplifier.

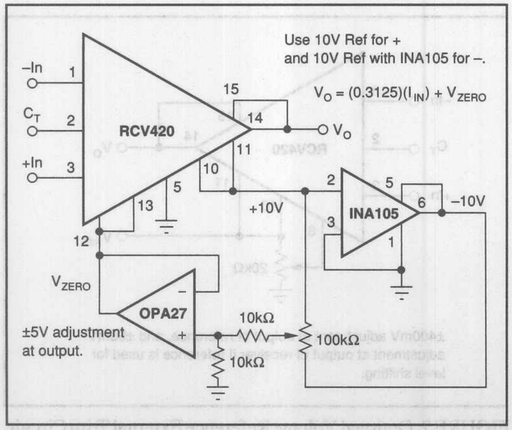


FIGURE 4. Optional Zero Adjust Circuit.

MAINTAINING COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: (1) resistor matching and tracking (the internal resistor network does this) and (2) source impedance. CMR depends on the accurate matching of several resistor ratios. The high accuracies needed to maintain the specified CMR and CMR temperature coefficient are difficult and expensive to reliably achieve with discrete components. Any resistance imbalance introduced by external circuitry directly affects CMR. These imbalances can occur by: mismatching sense resistors when gain is decreased, adding resistance in the feedback path when gain is increased, and adding series resistance on the Rcv Com pin.

The two sense resistors are laser-trimmed to typically match within 0.01%; therefore, when adding parallel resistance to decrease gain, take care to match the parallel resistance on each sense resistor. To maintain high CMR when increasing the gain of the RCV420, keep the series resistance added to the feedback network as small as possible. Whether the Rcv Com pin is grounded or connected to a voltage reference for level shifting, keep the series resistance on this pin as low as possible. For example, a resistance of 20Ω on this pin degrades CMR from 86dB to approximately 80dB. For applications requiring better than 86dB CMR, the circuit shown in Figure 5 can be used to adjust CMR.

PROTECTING THE SENSE RESISTOR

The 75Ω sense resistors are designed for a maximum continuous current of 40mA, but can withstand as much as 250mA for up to 0.1s (see absolute maximum ratings). There are several ways to protect the sense resistor from

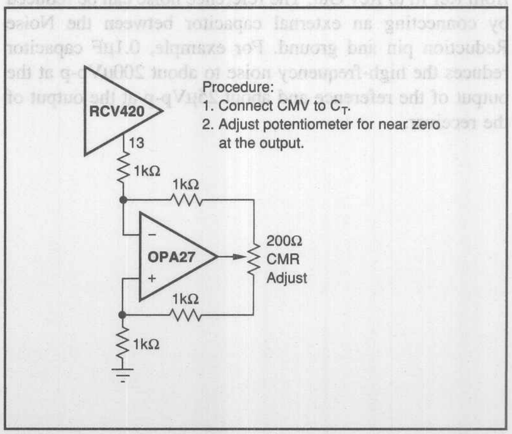


FIGURE 5. Optional Circuit for Externally Trimming CMR.

overcurrent conditions exceeding these specifications. Refer to Figure 6. The simplest and least expensive method is a resistor as shown in Figure 6a. The value of the resistor is determined from the expression

$$R_X = V_{CC}/40mA - 75\Omega$$

and the full scale voltage drop is

$$V_{RX} = 20mA \times R_X.$$

For a system operating off of a 32V supply $R_X = 725\Omega$ and $V_{RX} = 14.5V$. In applications that cannot tolerate such a large voltage drop, use circuits 6b or 6c. In circuit 6b a power JFET and source resistor are used as current limit. The 200Ω potentiometer, R_X, is adjusted to provide a current limit of approximately 30mA. This circuit introduces a 1-4V drop at full scale. If only a very small series voltage drop at full scale can be tolerated, then a 0.032A series 217 fast-acting fuse should be used, as shown in Figure 6c.

For automatic fold-back protection, use the circuit shown in Figure 15.

VOLTAGE REFERENCE

The RCV420 contains a precision 10V reference. Figure 8 shows the circuit for output voltage adjustment. Trimming the output will change the voltage drift by approximately 0.007ppm/°C per mV of trimmed voltage. Any mismatch in TCR between the two sides of the potentiometer will also affect drift, but the effect is divided by approximately 5. The trim range of the voltage reference using this method is typically ±400mV. The voltage reference trim can be used to trim offset errors at the output of the RCV420. There is an 8:1 voltage attenuation from Ref In to Rcv Out, and thus the trim range at the output of the receiver is typically ±50mV.

The high-frequency noise (to 1MHz) of the voltage reference is typically 1mVp-p. When the voltage reference is used for level shifting, its noise contribution at the output of the receiver is typically 125μVp-p due to the 8:1 attenuation from Ref In to Rcv Out. The reference noise can be reduced by connecting an external capacitor between the Noise Reduction pin and ground. For example, 0.1μF capacitor reduces the high-frequency noise to about 200μVp-p at the output of the reference and about 25μVp-p at the output of the receiver.

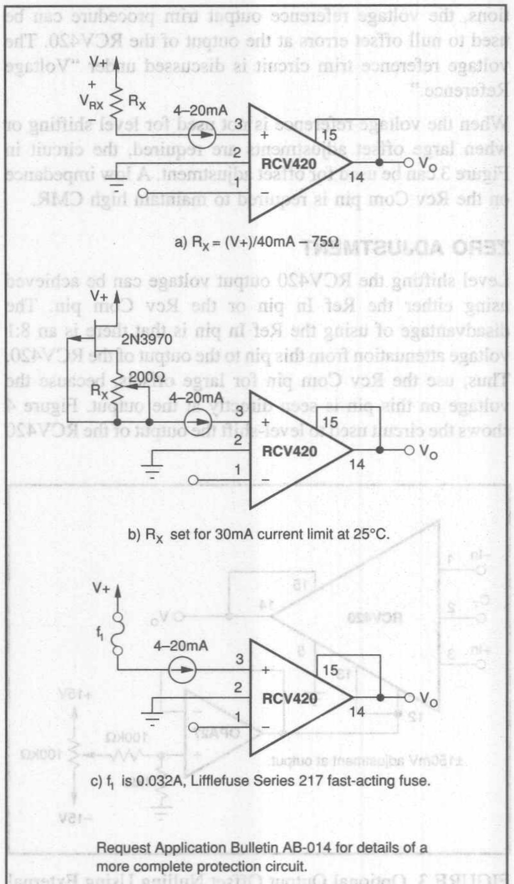


FIGURE 6. Protecting the Sense Resistors.

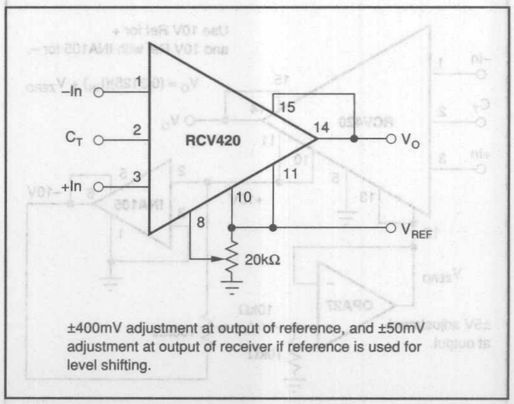


FIGURE 7. Optional Voltage Reference External Trim Circuit.

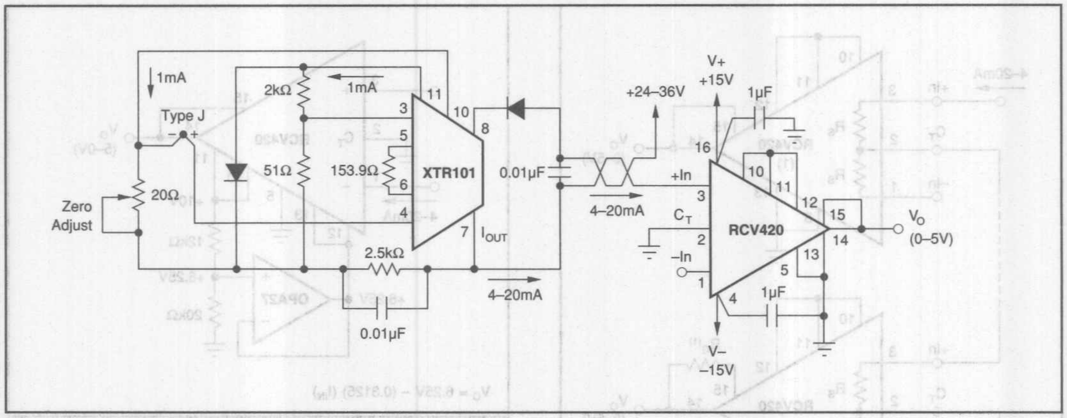


FIGURE 8. RCV420 Used in Conjunction with XTR101 to Form a Complete Solution for 4-20mA Loop.

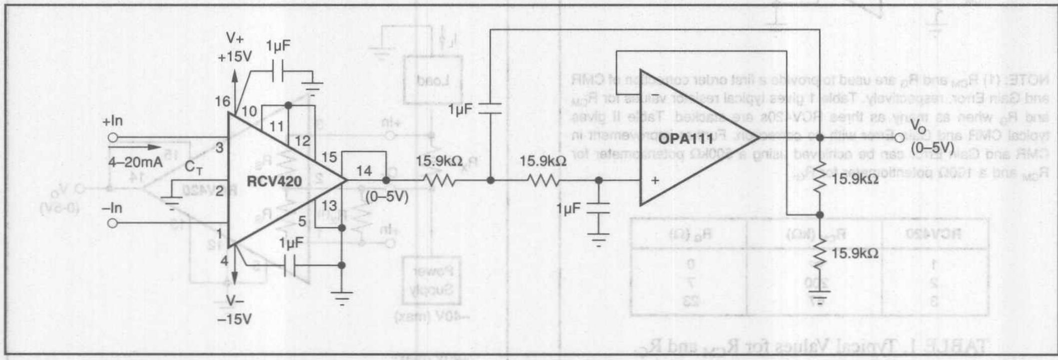


FIGURE 9. 4-20mA to 0-10V Conversion With Second-Order Active Low-Pass Filtering (f_{-3dB} = 10Hz).

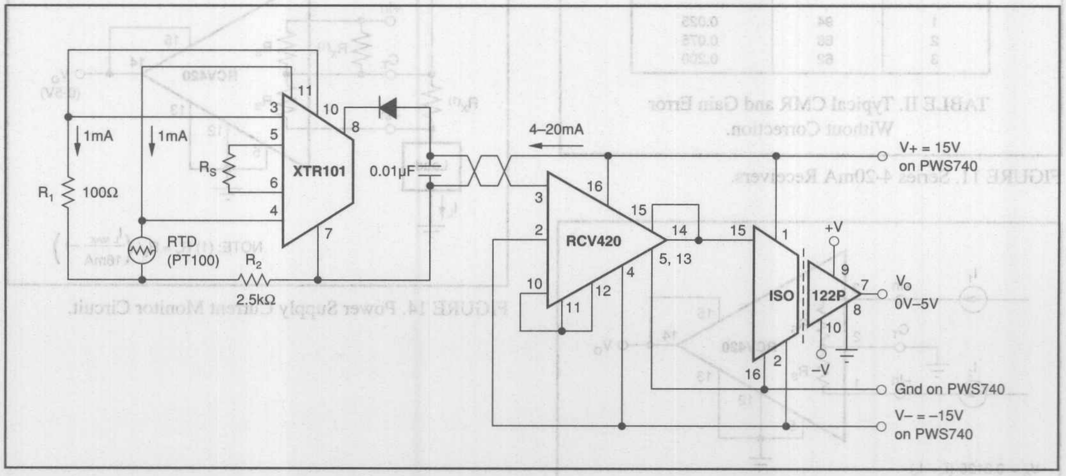
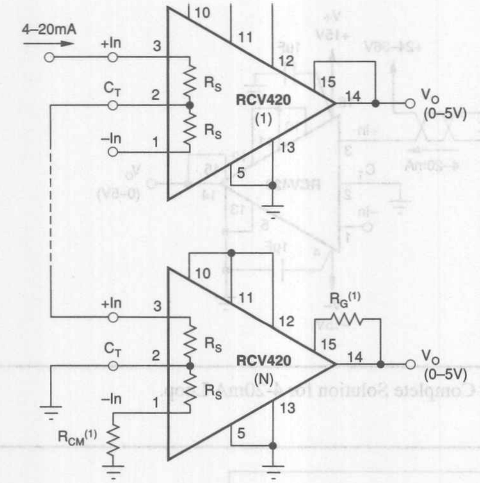


FIGURE 10. Isolated 4-20mA Instrument Loop (RTD shown).



NOTE: (1) R_{CM} and R_G are used to provide a first order correction of CMR and Gain Error, respectively. Table 1 gives typical resistor values for R_{CM} and R_G when as many as three RCV420s are stacked. Table II gives typical CMR and Gain Error with no correction. Further improvement in CMR and Gain Error can be achieved using a 500kΩ potentiometer for R_{CM} and a 100Ω potentiometer for R_G.

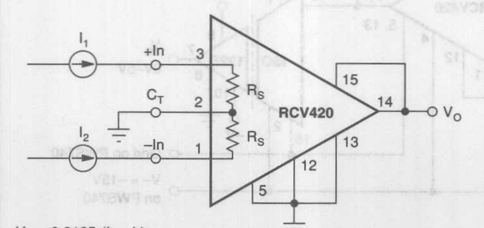
RCV420	R_{CM} (kΩ)	R_G (Ω)
1	∞	0
2	200	7
3	67	23

TABLE 1. Typical Values for R_{CM} and R_G.

RCV420	CMR (dB)	GAIN ERROR %
1	94	0.025
2	68	0.075
3	62	0.200

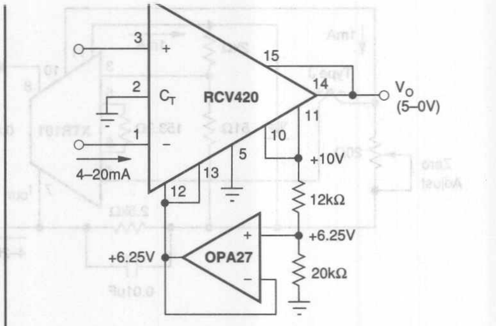
TABLE II. Typical CMR and Gain Error Without Correction.

FIGURE 11. Series 4-20mA Receivers.



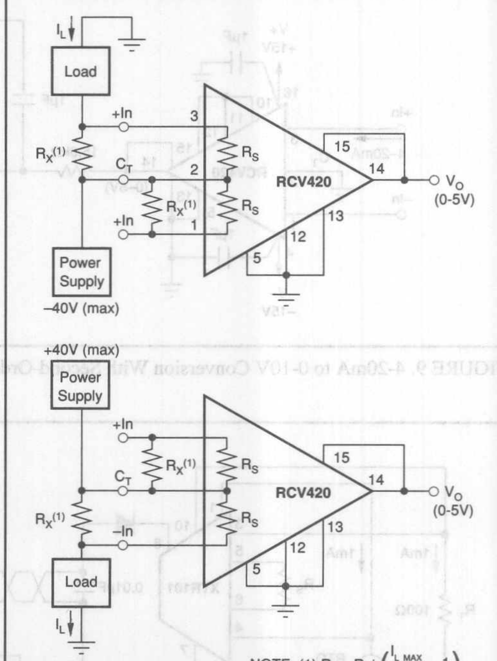
$V_O = 0.3125\,(I_1 - I_2)$
Max Gain Error = 0.1% (RCV420BG)

FIGURE 12. Differential Current-to-Voltage Converter.



$V_O = 6.25V - (0.3125)\,(I_{IN})$

FIGURE 13. 4-20mA to 5-0V Conversion.



NOTE: (1) $R_x = R_s / \left(\frac{I_{L\,MAX}}{16mA} - 1\right)$

FIGURE 14. Power Supply Current Monitor Circuit.

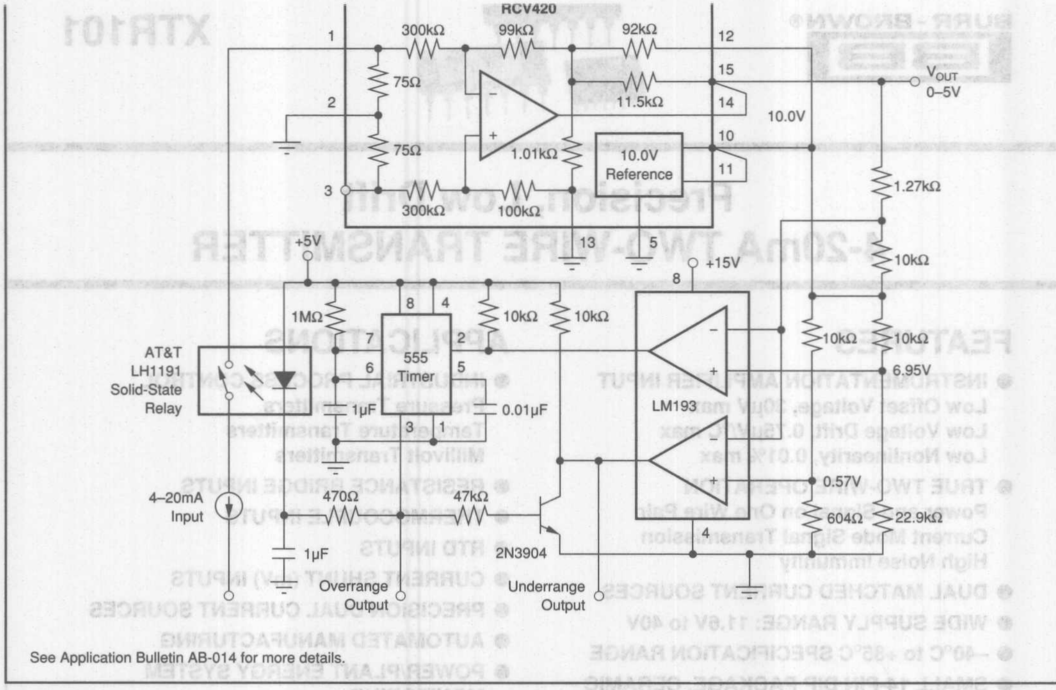


FIGURE 15. 4-20mA Current Loop Receiver with Input Overload Protection.

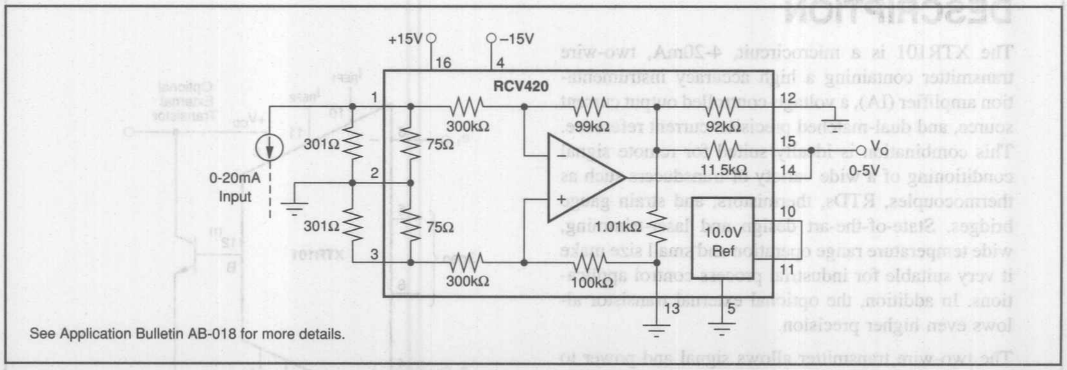
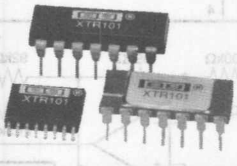


FIGURE 16. 0-20mA/0-5V Receiver Using RCV420.

BURR - BROWN®



XTR101

Precision, Low Drift 4-20mA TWO-WIRE TRANSMITTER

FEATURES

- **INSTRUMENTATION AMPLIFIER INPUT**
  Low Offset Voltage, 30μV max
  Low Voltage Drift, 0.75μV/°C max
  Low Nonlinearity, 0.01% max
- **TRUE TWO-WIRE OPERATION**
  Power and Signal on One Wire Pair
  Current Mode Signal Transmission
  High Noise Immunity
- **DUAL MATCHED CURRENT SOURCES**
- **WIDE SUPPLY RANGE: 11.6V to 40V**
- **–40°C to +85°C SPECIFICATION RANGE**
- **SMALL 14-PIN DIP PACKAGE, CERAMIC AND PLASTIC**

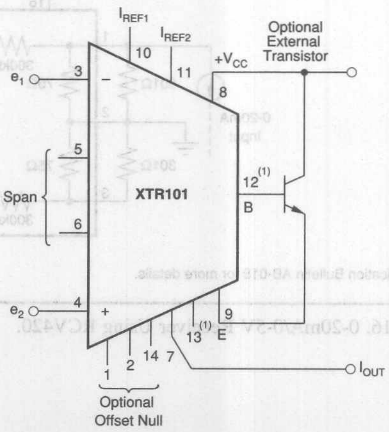
APPLICATIONS

- **INDUSTRIAL PROCESS CONTROL**
  Pressure Transmitters
  Temperature Transmitters
  Millivolt Transmitters
- **RESISTANCE BRIDGE INPUTS**
- **THERMOCOUPLE INPUTS**
- **RTD INPUTS**
- **CURRENT SHUNT (mV) INPUTS**
- **PRECISION DUAL CURRENT SOURCES**
- **AUTOMATED MANUFACTURING**
- **POWER/PLANT ENERGY SYSTEM MONITORING**

DESCRIPTION

The XTR101 is a microcircuit, 4-20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, and dual-matched precision current reference. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTDs, thermistors, and strain gauge bridges. State-of-the-art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications. In addition, the optional external transistor allows even higher precision.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers.



NOTE: (1) Pins 12 and 13 are used for optional BW control.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

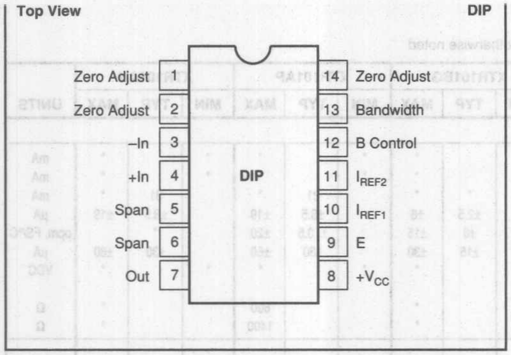
ELECTRICAL

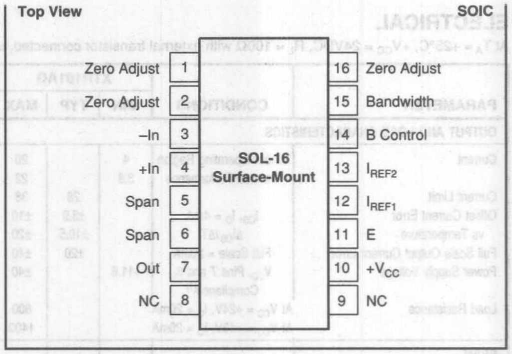
At T_A = +25°C, $+V_{CC}$ = 24VDC, R_L = 100Ω with external transistor connected, unless otherwise noted

PARAMETER	CONDITIONS	XTR101AG MIN	XTR101AG TYP	XTR101AG MAX	XTR101BG MIN	XTR101BG TYP	XTR101BG MAX	XTR101AP MIN	XTR101AP TYP	XTR101AP MAX	XTR101AU MIN	XTR101AU TYP	XTR101AU MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS														
Current	Linear Operating Region	4		20	*		*	*		*	*		*	mA
	Derated Performance	3.8		22	*		*	*		*	*		*	mA
Current Limit			28	38		*	*		31	*		31	*	mA
Offset Current Error	I_{OS}, I_O = 4mA		±3.9	±10		±2.5	±6		±8.5	±19		±8.5	±19	µA
vs Temperature	$\Delta I_{OS}/\Delta T$		±10.5	±20		±8	±15		±10.5	±20		*		ppm, FS/°C
Full Scale Output Current Error	Full Scale = 20mA		±20	±40		±15	±30		±30	±60		±30	±60	µA
Power Supply Voltage	V_{CC}, Pins 7 and 8, Compliance(1)	+11.6		±40	*		*	*		*	*		*	VDC
Load Resistance	At V_{CC} = +24V, I_O = 20mA			600			*			600			*	Ω
	At V_{CC} = +40V, I_O = 20mA			1400			*			1400			*	Ω
SPAN														
Output Current Equation	R_S in Ω, e_1 and e_2 in V				i_O = 4mA + [0.016Ω + (40/R_S)] ($e_2 - e_1$)									
Span Equation	R_S in Ω				S = [0.016Ω + (40/R_S)]									A/V
vs Temperature	Excluding TCR of R_S		±30	±100		*	*		*	*		*	*	ppm/°C
Untrimmed Error(2)	ε_{SPAN}	–5	–2.5	0	*	*	*	*	*	*	*	*	*	%
Nonlinearity	$\varepsilon_{NONLINEARITY}$			0.01			*			*			*	%
Hysteresis			0			*			*			*		%
Dead Band			0			*			*			*		%
INPUT CHARACTERISTICS														
Impedance: Differential			0.4 || 3			*			*			*		GΩ || pF
Common-Mode			10 || 3			*			*			*		GΩ || pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)$(3)	0		1	*		*	*		*	*		*	V
Offset Voltage	V_{OS}		±30	±60		±20	±30		*	±100		*	±100	µV
vs Temperature	$\Delta V_{OS}/\Delta T$		±0.75	±1.5		±0.35	±0.75		*	*		*	*	µV/°C
Power Supply Rejection	ΔV_{CC}/PSRR = V_{OS} Error	110	125		*	*		*	122		110	122		dB
Bias Current	I_B		60	150		*	*		*	*		*	*	nA
vs Temperature	$\Delta I_B/\Delta T$		0.30	1		*	*		*	*		*	*	nA/°C
Offset Current	I_{OSI}		10	±30		*	±20		*	*		*	*	nA
vs Temperature	$\Delta I_{OSI}/\Delta T$		0.1	0.3		*	*		*	*		*	*	nA/°C
Common-Mode Rejection(4)	DC	90	100		*	*		*	*		*	*		dB
Common-Mode Range	e_1 and e_2 with Respect to Pin 7	4		6	*		*	*		*	*		*	V
CURRENT SOURCES														
Magnitude			1			*			*			*		mA
Accuracy	V_{CC} = 24V, $V_{PIN\ 8} - V_{PIN\ 10,11}$ = 19V R_2 = 5kΩ, Fig. 5		±0.06	±0.17		±0.025	±0.075		±0.2	±0.37		±0.2	±0.37	%
vs Temperature			±50	±80		±30	±50		*	*		*	*	ppm/°C
vs V_{CC}			±3			*			*			*		ppm/V
vs Time			±8			*			*			*		ppm/month
Compliance Voltage	With Respect to Pin 7	0		V_{CC} – 3.5	*		*	*		*	*		*	V
Ratio Match	Tracking													
Accuracy	$(1 - I_{REF1}/I_{REF2})$ X 100%		±0.014	±0.06		±0.009	±0.04		±0.031	±0.088		±0.031	±0.088	%
vs Tempeature				±15			10			*			*	ppm/°C
vs V_{CC}			±10						*			*		ppm/V
vs Time			±1						*			*		ppm/month
Output Impedance		10	20		*			*	15		*	15		MΩ
TEMPERATURE RANGE														
Specification		–40		+85	*		*	–40		+85	*		*	°C
Operating		–55		+125	*		*	–40		+85	–40		+85	°C
Storage		–55		+165	*		*	–55		+125	–55		+125	°C

*Same as XTR101AG.

NOTES: (1) See Typical Performance Curves. (2) Span error shown is untrimmed and may be adjusted to zero. (3) e_1 and e_2 are signals on the –In and +In terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR101A and XTR101B grades respectively. 2mV FS is also possible with the B grade, but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise. (4) Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Application Information section.



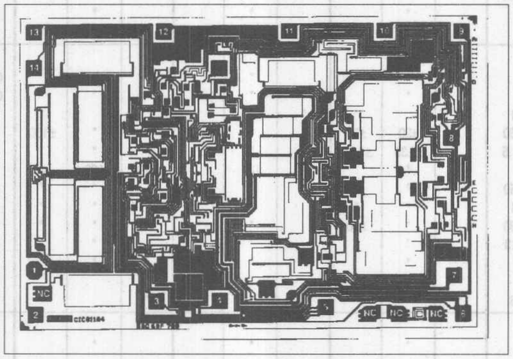


DICE INFORMATION

PAD	FUNCTION	PAD	FUNCTION
1	Zero Adjust	8	$+V_{CC}$
2	Zero Adjust	9	E
3	–In	10	I_{REF1}
4	+In	11	I_{REF2}
5	Span	12	B Control
6	Span	13	Bandwidth
7	Out	14	Zero Adjust

NC: No Connection

Substrate Bias: Electrically connected to V– supply.



XTR101 DIE TOPOGRAPHY

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	150 x 105 ±5	3.81 x 2.67 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

ABSOLUTE MAXIMUM RATINGS

Power Supply, $+V_{CC}$	40V
Input Voltage, e_1 or e_2	$\geq V_{OUT}$, $\leq +V_{CC}$
Storage Temperature Range, Ceramic	–55°C to +165°C
Plastic	–55°C to +125°C
Lead Temperature (soldering 10s) G, P	+300°C
(wave soldering, 3s) U	+260°C
Output Short-Circuit Duration	Continuous $+V_{CC}$ to I_{OUT}
Junction Temperature	+165°C

PACKAGE INFORMATION

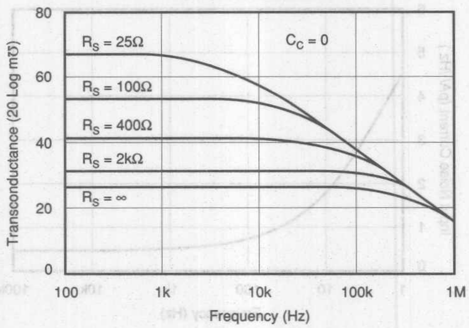
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
XTR101AG	14-Pin Ceramic DIP	169
XTR101BG	14-Pin Ceramic DIP	169
XTR101AP	14-Pin Plastic DIP	010
XTR101AU	16-Pin SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

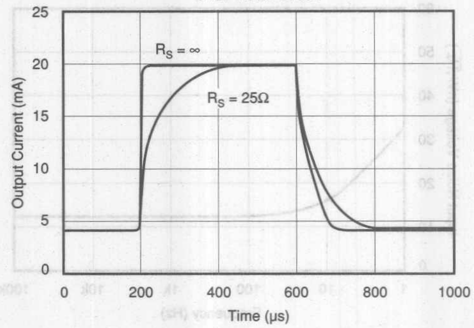
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
XTR101AG	14-Pin Ceramic DIP	–40°C to +85°C
XTR101BG	14-Pin Ceramic DIP	–40°C to +85°C
XTR101AP	14-Pin Plastic DIP	–40°C to +85°C
XTR101AU	16-Pin SOIC	–40°C to +85°C

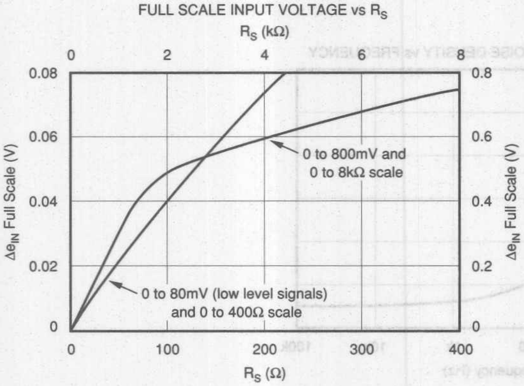
SPAN vs FREQUENCY



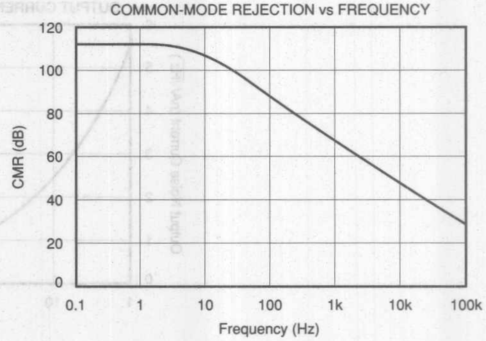
STEP RESPONSE



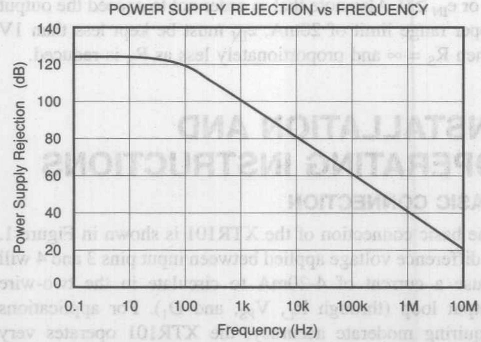
FULL SCALE INPUT VOLTAGE vs R_S



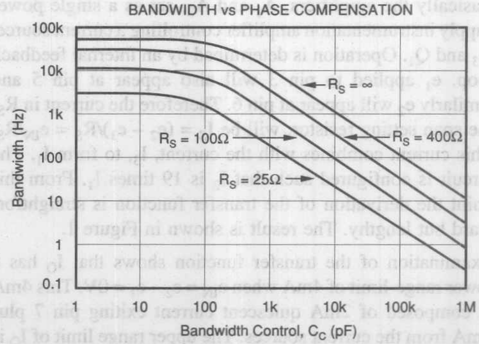
COMMON-MODE REJECTION vs FREQUENCY



POWER SUPPLY REJECTION vs FREQUENCY

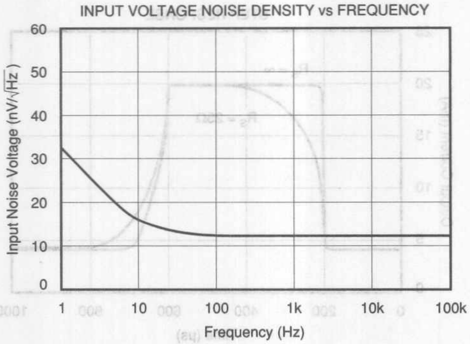


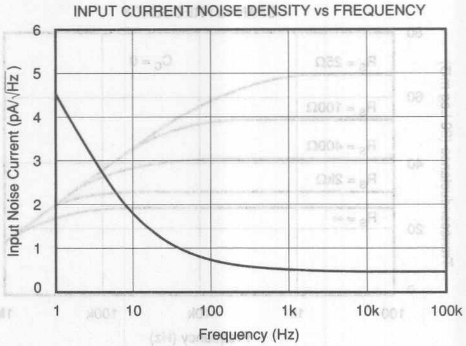
BANDWIDTH vs PHASE COMPENSATION

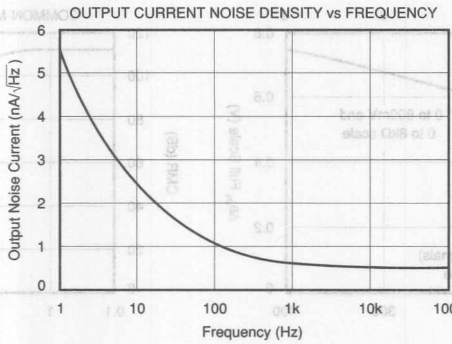


TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $+V_{CC}$ = 24VDC unless otherwise noted.







THEORY OF OPERATION

A simplified schematic of the XTR101 is shown in Figure 1. Basically the amplifiers, A_1 and A_2, act as a single power supply instrumentation amplifier controlling a current source, A_3 and Q_1. Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S, the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3, to form I_1. The circuit is configured such that I_2 is 19 times I_1. From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0V$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN}. Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., (0.016℧+ 40/R_S)(e_{IN} full scale) = 16mA. Note that since I_O is unipolar e_2 must be kept larger than e_1; i.e., $e_2 \geq e_1$ or $e_{IN} \geq 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR101 is shown in Figure 1. A difference voltage applied between input pins 3 and 4 will cause a current of 4-20mA to circulate in the two-wire output loop (through R_L, V_{PS}, and D_1). For applications requiring moderate accuracy, the XTR101 operates very cost-effectively with just its internal drive transistor. For more demanding applications (high accuracy in high gain) an external NPN transistor can be added in parallel with the internal one. This keeps the heat out of the XTR101 package

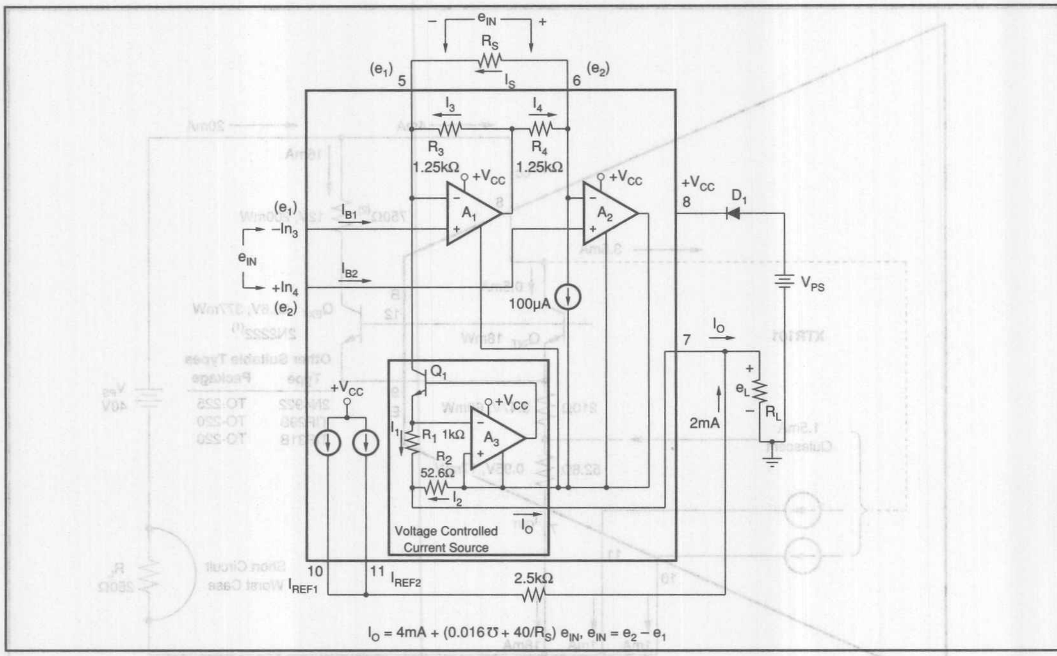


FIGURE 1. Simplified Schematic of the XTR101.

and minimizes thermal feedback to the input stage. Also in such applications where e_{IN} full scale is small (<50mV) and R_{SPAN} is small (<150Ω), caution should be taken to consider errors from the external span circuit plus high amplification of offset drift and noise.

OPTIONAL EXTERNAL TRANSISTOR

The optional external transistor, when used, is connected in parallel with the XTR101's internal transistor. The purpose is to increase accuracy by reducing heat change inside the XTR101 package as the output current spans from 4-20mA. Under normal operating conditions, the internal transistor is never completely turned off as shown in Figure 2. This maintains frequency stability with varying external transistor characteristics and wiring capacitance. The actual "current sharing" between internal and external transistors is dependent on two factors: (1) relative geometry of emitter areas and (2) relative package dissipation (case size and thermal conductivity). For best results, the external device should have a larger base-emitter area and smaller package. It will, upon turn on, take about [0.95 (I_O – 3.3mA)]mA. However, it will heat faster and take a greater share after a few seconds.

Although any NPN of suitable power rating will operate with the XTR101, two readily available transistors are recommended.

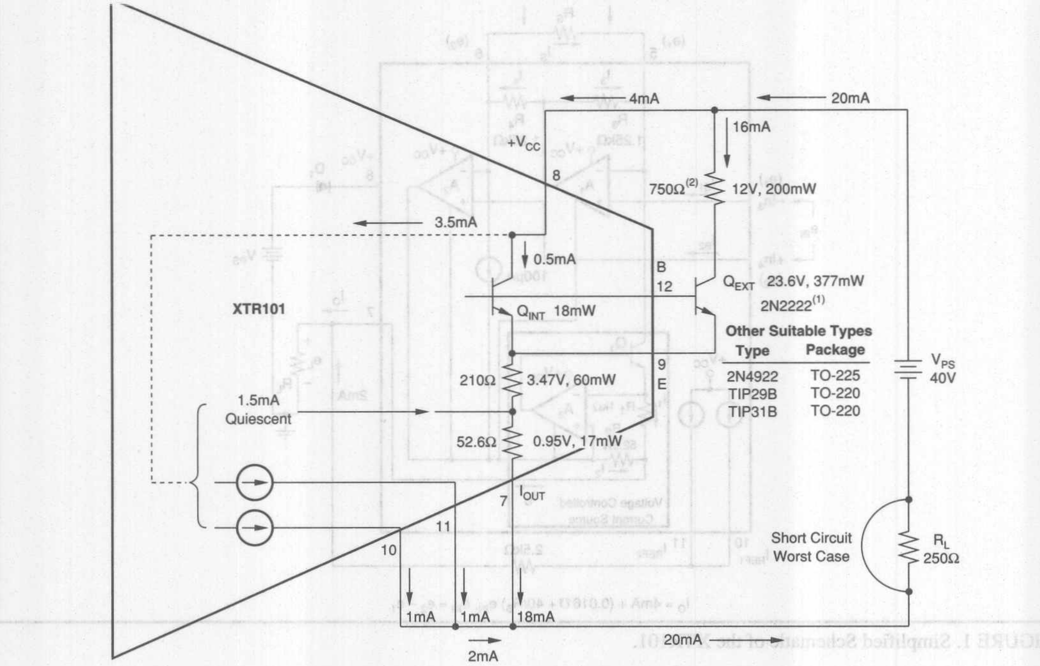
1. 2N2222 in the TO-18 package. For power supply voltages above 24V, a 750Ω, 1/2W resistor should be connected in series with the collector. This will limit the power dissipation to 377mW under the worst-case conditions shown in Figure 2. Thus the 2N2222 will safely operate below its 400mW rating at the upper temperature of +85°C. Heat sinking the 2N2222 will result in greatly reduced accuracy improvement and is not recommended.
2. TIP29B in the TO-220 package. This transistor will operate over the specified temperature and output voltage range without a series collector resistor. Heat sinking the TIP29B will result in slightly less accuracy improvement. It can be done, however, when mechanical constraints require it.

ACCURACY WITH AND WITHOUT EXTERNAL TRANSISTOR

The XTR101 has been tested in a circuit using an external transistor. The relative difference in accuracy with and without an external transistor is shown in Figure 3. Notice that a dramatic improvement in offset voltage change with supply voltage is evident for any value of load resistor.

MAJOR POINTS TO CONSIDER WHEN USING THE XTR101

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. $+V_{CC}$ should be bypassed with a 0.01µF capacitor as close to the unit as possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation, +4V to +6V (e_1 and e_2 measured with respect to pin 7).



NOTES: (1) An external transistor is used in the maufacturing test circuit for testing electrical specifications.
(2) This resistor is required for the 2N2222 with V_{PS} > 24V to limit power dissipation.

FIGURE 2. Power Calculation of XTR101 with External Transistor.

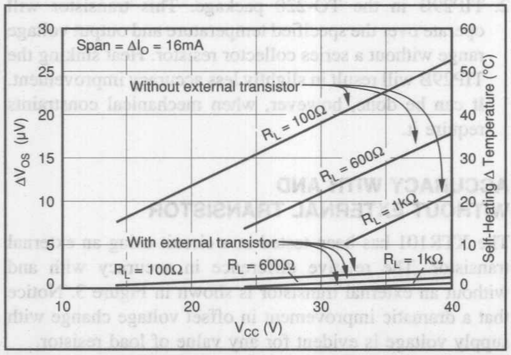


FIGURE 3. Thermal Feedback Due to Change in Output Current.

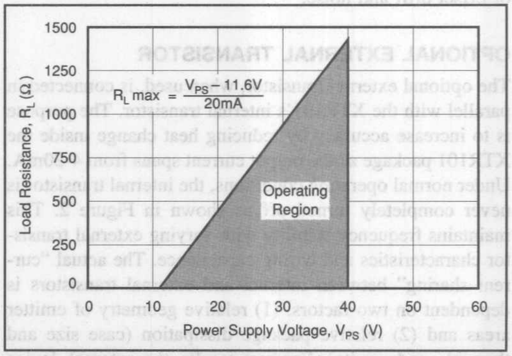


FIGURE 4. Power Supply Operating Range.

4. The maximum input signal level (e_{INFS}) is 1V with $R_S = \infty$ and proportionally less as R_S decreases.

5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation, connect them together to pin 7. Each reference must have between 0V and $+(V_{CC} - 4V)$ with respect to pin 7.

6. Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 ($+V_{CC}$) remains within the 11.6V to 40V range as the output changes between the 4-20mA range (see Figure 4).

7. It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR101 caused by a momentary (e.g., transient) or long term application of the wrong polarity of voltage between pins 7 and 8.

8. Consider PC board layout which minimizes parasitic capacitance, especially in high gain.

SELECTING R_S

R_{SPAN} is chosen to that a given full scale input span e_{INFS} will result in the desired full scale output span of ΔI_{OFS},

$$[(0.016\mho) + (40/R_S)]\ \Delta e_{IN} = \Delta I_O = 16\text{mA}.$$

Solving for R_S:

$$R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016\mho} \qquad (1)$$

For example, if $\Delta e_{INFS} = 100\text{mV}$ for $\Delta I_{OFS} = 16\text{mA}$,

$$R_S = \frac{40}{16\text{mA}/100\text{mV}) - 0.016} = \frac{40}{0.16 - 0.016}$$

$$= \frac{40}{0.144} = 278\Omega$$

See Typical Performance Curves for a plot of R_S vs Δe_{INFS}. Note that in order not to exceed the 20mA upper range limit, e_{IN} must be less than 1V when $R_S = \infty$ and proportionately smaller as R_S decreases.

BIASING THE INPUTS

Because the XTR operates from a single supply both e_1 and e_2 must be biased approximately 5V above the voltage at pin 7 to assure linear response. This is easily done by using one or both current sources and an external resistor R_2. Figure 5 shows the simplest case— a floating voltage source e'_2. The 2mA from the current sources flows through the 2.5kΩ value of R_2 and both e_1 and e_2 are raised by the required 5V with respect to pin 7. For linear operation the constraint is

$$+4\text{V} \le e_1 \le +6\text{V}$$
$$+4\text{V} \le e_2 \le +6\text{V}$$

The offset adjustment is used to remove the offset voltage of the input amplifier. When the input differential voltage (e_{IN}) equals zero, adjust for 4mA output.

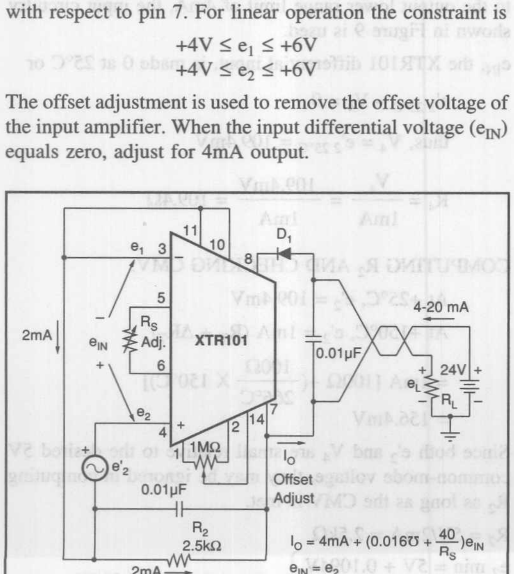


FIGURE 5. Basic Connection for Floating Voltage Source.

Figure 6 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources. Also, the offset adjustment has higher resolution compared to Figure 5.

CMV AND CMR

The XTR101 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications.

If the inputs are biased at some other CMV then an input offset error term is (CMV – 5)/CMRR; CMR is in dB, CMRR is in V/V.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR101 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 7 and 8(a). In this example the sensor voltage is derived from R_T (a thermistor, RTD, or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 8(b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2 and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20µV) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by ±0.3µV/°C per 100µV or induced offset.

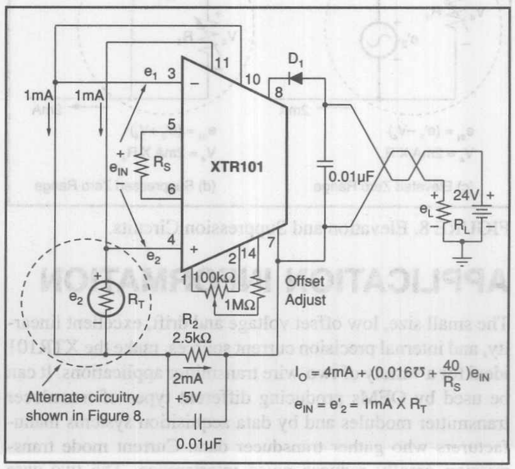


FIGURE 6. Basic Connection for Resistive Source.

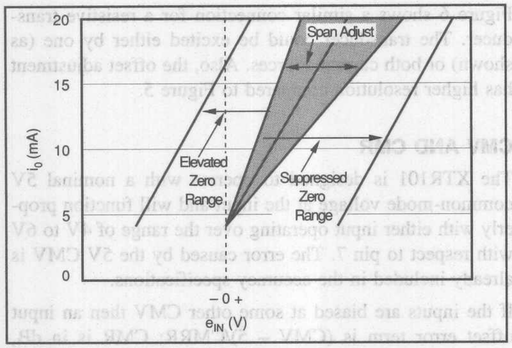


FIGURE 7. Elevation and Suppression Graph.

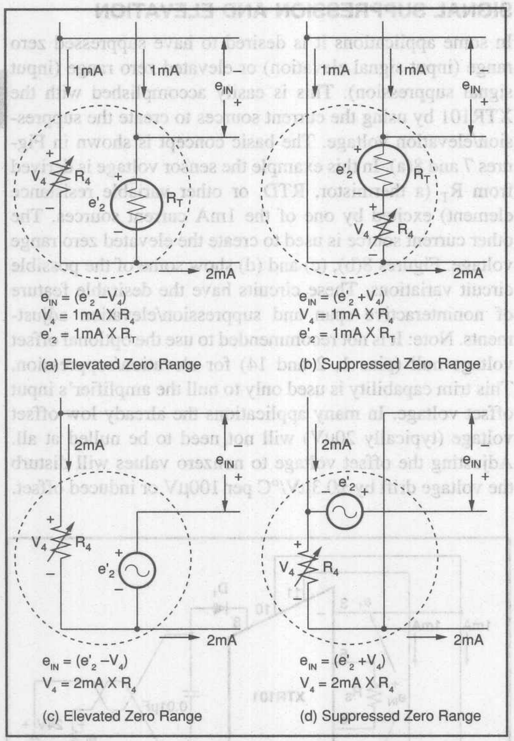


FIGURE 8. Elevation and Suppression Circuits.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR101 ideal for a variety of two-wire transmitter applications. It can be used by OEMs producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR101 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1

RTD Transducer shown in Figure 9.

Given a process with temperature limits of +25°C and +150°C, configure the XTR101 to measure the temperature with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

COMPUTING R_S:

The sensitivity of the RTD is $\Delta R/\Delta T$ = 100Ω/266°C. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span), the span of e_{IN} is 1mA X (100Ω/266°C) X 125°C = 47mV = Δe_{IN}.

From equation 1, $R_S = \dfrac{40}{\Delta I_O/\Delta e_{IN} - 0.016\Omega}$

$$R_S = \frac{40}{16\text{mA}/47\text{mV} - 0.016℧} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S.

COMPUTING R_4:

At +25°C, e'_2 = 1mA ($R_T + \Delta R_T$)

$$= 1\text{mA}\ [100\Omega + \frac{100\Omega}{266°\text{C}} \times 25°\text{C}]$$

$$= 1\text{mA}\ (109.4\Omega) = 109.4\text{mV}$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA, the input circuitry shown in Figure 9 is used.

e_{IN}, the XTR101 differential input, is made 0 at 25°C or

$e'_{2\ 25°C} - V_4 = 0$

thus, $V_4 = e'_{2\ 25°C}$ = 109.4mV

$$R_4 = \frac{V_4}{1\text{mA}} = \frac{109.4\text{mV}}{1\text{mA}} = 109.4\Omega$$

COMPUTING R_2 AND CHECKING CMV:

At +25°C, e'_2 = 109.4mV

At +150°C, e'_2 = 1mA ($R_T + \Delta R_T$)

$$= 1\text{mA}\ [100\Omega + (\frac{100\Omega}{266°\text{C}} \times 150°\text{C})]$$

= 156.4mV

Since both e'_2 and V_4 are small relative to the desired 5V common-mode voltage, they may be ignored in computing R_2 as long as the CMV is met.

R_2 = 5V/2mA = 2.5kΩ

$$\left.\begin{array}{l} e_2 \text{ min} = 5\text{V} + 0.1094\text{V} \\ e_2 \text{ max} = 5\text{V} + 0.1564\text{V} \\ e_1 = 5\text{V} + 0.1094\text{V} \end{array}\right\} \text{The +4V to +6V CMV requirement is met.}$$

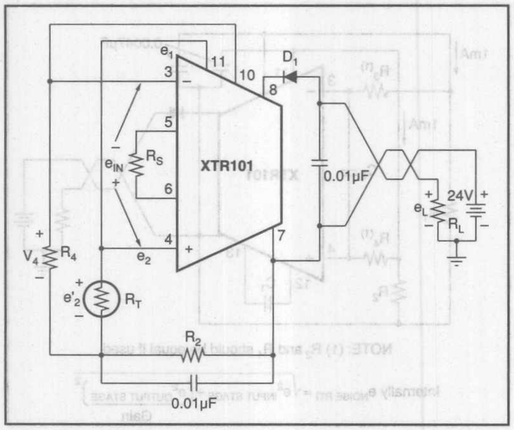


FIGURE 9. Circuit for Example 1.

EXAMPLE 2

Thermocouple Transducer shown in Figure 10.

Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the XTR101 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, V_{R6}, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of +25°C this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2.

ESTABLISHING R_S:

The input full scale span is 58mV (Δe_{INFS} = 58mV).

R_S is found from equation (1)

$$R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016\mho}$$

$$= \frac{40}{16\text{mA}/58\text{mV} - 0.016\mho} = \frac{40}{0.2599} = 153.9\Omega$$

SELECTING R_4:

R_4 is chosen to make the output 4mA at T_{TC} = 0°C (V_{TC}= –1.28mV) and T_D = +25°C (V_D = 0.6V). A circuit is shown in Figure 10.

V_{TC} will be –1.28mV when T_{TC} = 0°C and the reference junction is at +25°C. e_1 must be computed for the condition of T_D = +25°C to make e_{IN} = 0V.

$$V_{D\,25°C} = 600\text{mV}$$

$$e_{1\,25°C} = 600\text{mV}\,(51/2051) = 14.9\text{mV}$$

$$e_{IN} = e_2 - e_1 = V_{TC} + V_4 - e_1$$

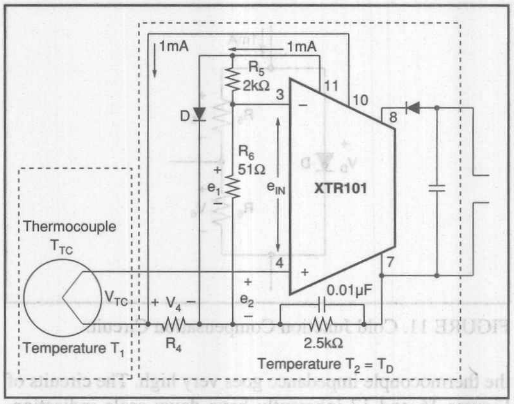


FIGURE 10. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

With e_{IN} = 0 and V_{TC} = –1.28mV,

$$V_4 = e_1 + e_{IN} - V_{TC}$$

$$= 14.9\text{mV} + 0\text{V} - (-1.28\text{mV})$$

$$1\text{mA}\,(R_4) = 16.18\text{mV}$$

$$R_4 = 16.18\Omega$$

COLD JUNCTION COMPENSATION:

The temperature reference circuit is shown in Figure 11. The diode voltage has the form

$$V_D = \frac{KT}{q} \ln \frac{I_{DIODE}}{I_{SAT}}$$

Typically at T_2 = +25°C, V_D = 0.6V and $\Delta V_D/\Delta T$ = –2mV/°C. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta_V D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At +25°C this is approximately 52μV/°C (obtained from standard thermocouple table); therefore,

$$\Delta T_C/\Delta T = \Delta_V D/\Delta T \left[\frac{R_6}{R_5 + R_6}\right] \quad (2)$$

$$52\mu\text{V}/°\text{C} = 2000\mu\text{V}/°\text{C} \left[\frac{R_6}{R_5 + R_6}\right]$$

R_5 is chosen as 2kΩ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω.

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when

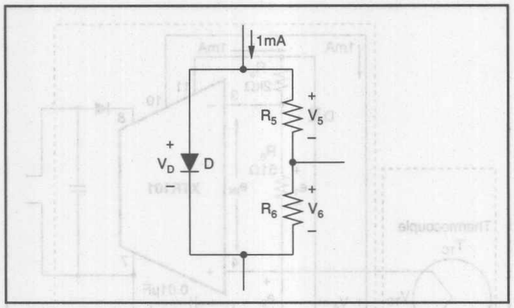


FIGURE 11. Cold Junction Compensation Circuit.

the thermocouple impedance goes very high. The circuits of Figures 16 and 17 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the + input (large impedance) will cause I_O to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 18 should be used. When the T_C opens the output will go to its upper range limit value (about 25mA or higher).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR101 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltages (30µV max for the B grade, 60µV max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2 and 14 as shown in Figures 5 and 6. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommended where possible and can be done by either one of two techniques shown in Figure 12. C_2 connected to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by,

$$f_{CO} = \frac{15.9}{(R_1 + R_2 + R_3 + R_4)\,(C_2 + 3\text{pF})}$$

This method has the disadvantage of having f_{CO} vary with R_1, R_2, R_3, R_4, and it may require large values of R_3 and R_4. The other method, using C_1, will use smaller values of capacitance and is not a function of the input resistors. It is, however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{CO} is shown in the Typical Performance Curves.

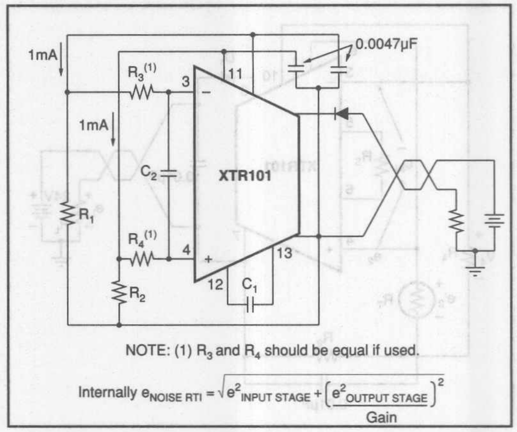


FIGURE 12. Optional Filtering.

APPLICATION CIRCUITS

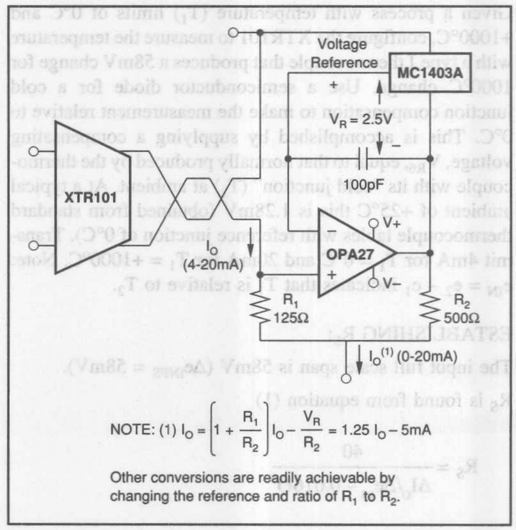


FIGURE 13. 0-20mA Output Converter.

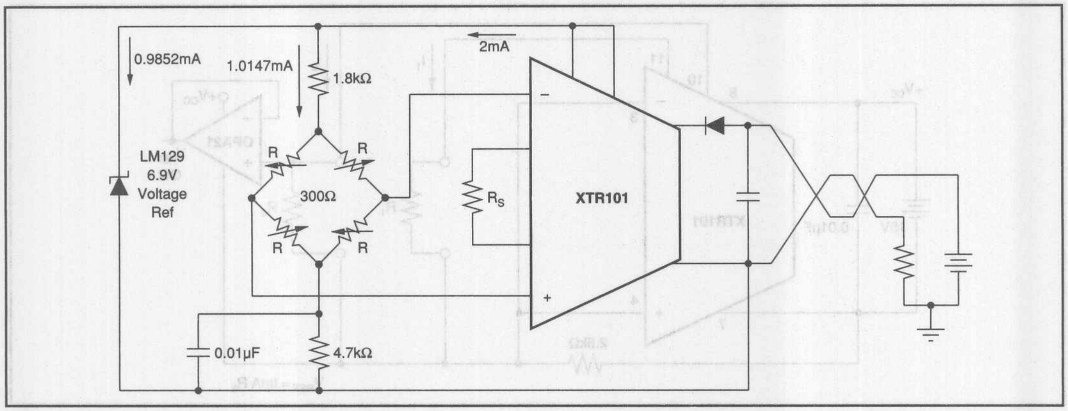


FIGURE 14. Bridge Input, Voltage Excitation.

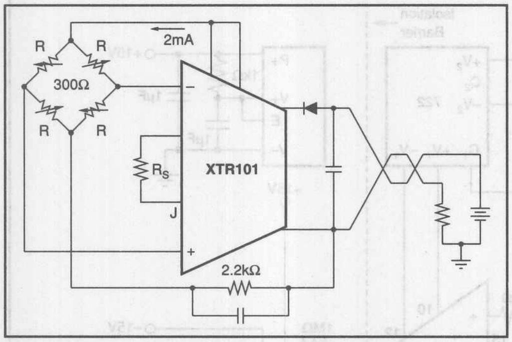


FIGURE 15. Bridge Input, Current Excitation.

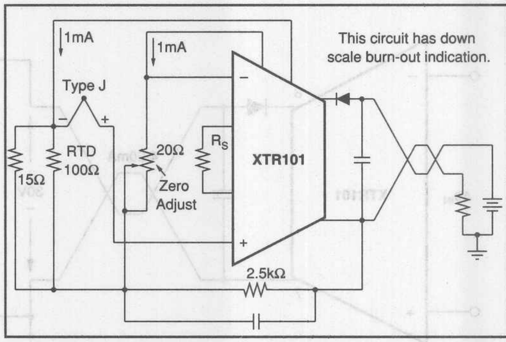


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

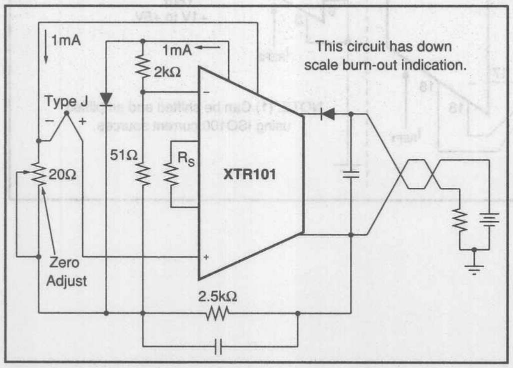


FIGURE 17. Thermocouple Input with Diode Cold Junction Compensation.

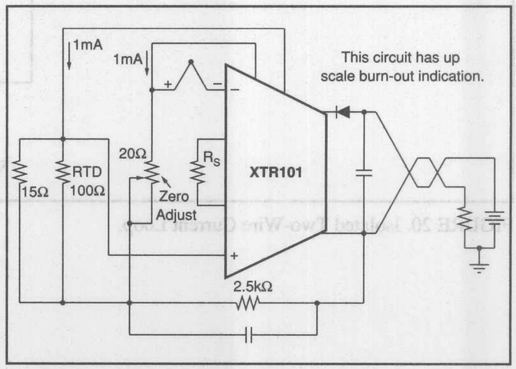


FIGURE 18. Thermocouple Input with RTD Cold Junction Compensation.

XTR101

4

INSTRUMENTATION AMPLIFIERS

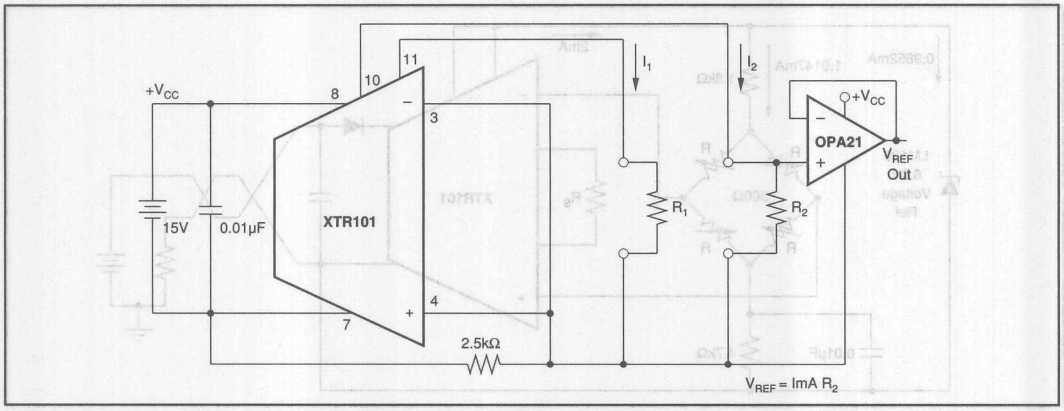


FIGURE 19. Dual Precision Current Sources Operated From One Supply.

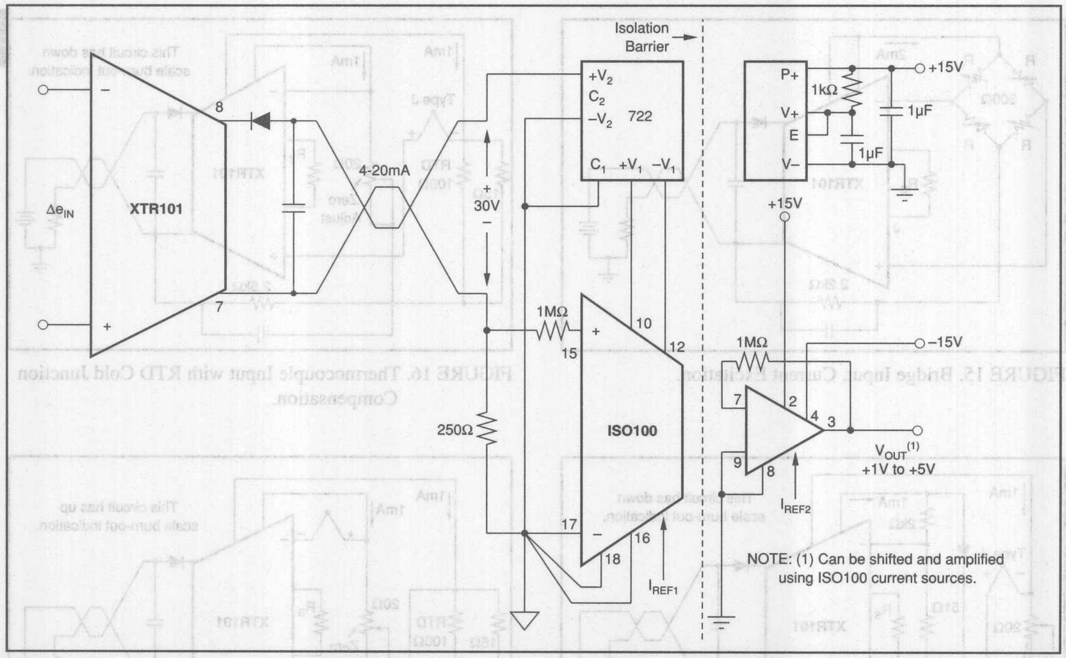


FIGURE 20. Isolated Two-Wire Current Loop.

DETAILED ERROR ANALYSIS

The ideal output current is

$$i_{O\ IDEAL} = 4mA + K\ e_{IN}$$

K is the span (gain) term, $(0.016\Omega + (40/R_S))$ (3)

In the XTR101 there are three major components of error:

1. σ_O = errors associated with the output stage.
2. σ_S = errors associated with span adjustment.
3. σ_I = errors associated with the input stage.

The transfer function including these errors is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\,(1 + \sigma_S)(e_{IN} + \sigma_I) \quad (4)$$

When this expression is expanded, second order terms $(\sigma_S\ \sigma_1)$ dropped, and terms collected, the result is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ e_{IN} + K\sigma_I + K\sigma_S\ e_{IN}$$

(5)

The error in the output current is $i_{O\ ACTUAL} - i_{O\ IDEAL}$ and can be found by subtracting equations (5) and (3).

$$i_{O\ ERROR} = \sigma_O + K\sigma_1 + K\sigma_S\ e_{IN} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR101 and the particular circuit in which it is applied. The circuit of Figure 9 will be used to illustrate the principles.

1. $\sigma_O = I_{OS\ RTO}$ (7)
2. $\sigma_S = \varepsilon_{NONLINEARITY} + \varepsilon_{SPAN}$ (8)
3. (9)

$$\sigma_I = V_{OSI} + (I_{B1} + R_4 - I_{B2}\ R_T) + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR}$$

The term in parentheses may be written in terms of offset current and resistor mismatches as $I_{B1}\ \Delta R + I_{OS}'\ R_4$.

V_{OSI}*	= input offset voltage
I_{B1}*, I_{B2}*	= input bias current
I_{OSI}*	= input offset current
$I_{OS\ RTO}$*	= output offset current error
ΔR	= $R_T - R_4$ = mismatch in resistor
ΔV_{CC}	= change supply voltage between pins 7 and 8 away from 24V nominal
PSRR*	= power supply rejection ratio
CMRR*	= common-mode rejection ratio
ε_{NONLIN}*	= span nonlinearity
ε_{SPAN}*	= span equation error. Untrimmed error = 5% max. May be trimmed to zero.

Items marked with an asterisk (*) can be found in the Electrical Specifications.

EXAMPLE 3

The circuit in Figure 9 with the XTR101BG specifications and the following conditions: $R_T = 109.4\Omega$ at 25°C, $R_T = 156.4\Omega$ at 150°C, $I_O = 4mA$ at 25°C, $I_O = 20mA$ at 150°C, $R_S = 123.3\Omega$, $R_4 = 109\Omega$, $R_L = 250\Omega$, $R_{LINE} = 100\Omega$, $V_{DI} = 0.6V$, $V_{PS} = 24V \pm 0.5\%$. Determine the % error at the upper and lower range values.

A. AT THE LOWER RANGE VALUE (T = +25°C).

$$\sigma_O = I_{OS\ RTO} = \pm 6\mu A$$

$$\sigma_I = V_{OSI} + (I_{B1}\ \Delta R + I_{OSI}\ R_4) + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR}$$

$$\Delta R = R_{T\ 25°C} - R_4 = 109.4 - 109 \approx 0$$

$$\Delta V_{CC} = (24 \times 0.005) + 4mA\ (250\Omega + 100\Omega) + 0.6V = 120mV + 1400mV + 600mV = 2120mV$$

$$e_1 = (2mA \times 2.5k\Omega) + (1mA \times 109\Omega) = 5.109V$$

$$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 109.4\Omega) = 5.1094V$$

$$(e_1 + e_2)/2 - 5 = 0.1092V$$

PSRR= 3.16×10^5 for 110dB

CMRR = 31.6×10^3 for 90dB

$$\sigma_1 = 30\mu V + (150nA \times 0 + 20nA \times 109\Omega) + \frac{2120mV}{3.16 \times 10^5} + \frac{0.1092V}{3.16 \times 10^3} \quad (10)$$

$$= 30\mu V + 2.18\mu V + 6.7\mu V + 3.46\mu V = 42.34\mu V$$

$$\sigma_S = \varepsilon_{NONLIN} + \varepsilon_{SPAN} = 0.0001 + 0 \text{ (assumes trim of } R_S)$$

$$I_O \text{ error} = \sigma_O + K\ \sigma_I + K\ \sigma_S\ e_{IN}$$

$$K = 0.016 + \frac{40}{R_s} = 0.016 + \frac{40}{123.3\Omega} = 0.340\mho$$

$$e_{IN} = e_2 - V_4 = I_{REF1}\ R_{T\ 25°C} - I_{REF2}\ R_4$$

since $R_{T\ 25°C} = R_4$,

$$e_{IN} = (I_{REF1} - I_{REF2})\ R_4 = 0.4\mu A \times 109\Omega = 43.6\mu V$$

Since the maximum mismatch of the current references is 0.04% of 1mA = 0.4µA,

$$I_O \text{ error} = 6\mu A + (0.34\mho \times 42.34\mu V) + (0.34\mho \times 0.0001 \times 43.6\mu V) = 6\mu A + 14.40\mu A + 0.0015\mu A = 20.40\mu A$$

$$\% \text{ error} = \frac{20.40\mu A}{16mA} \times 100\%$$

0.13% of span at lower range value.

B. AT THE UPPER RANGE VALUE (T = +150°C).

$$\Delta R = R_{T\ 150°C} - R_4 = 156.4 - 109.4 = 47\Omega$$

$$\Delta V_{CC} = (24 \times 0.005) + 20mA\ (250\Omega + 100\Omega) + 0.6V = 7720mV$$

$$e_1 = 5.109V$$

$$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 156.4\Omega) = 5.156V$$

$$(e_1 + e_2)/2 - 5V = 0.1325V$$

$$+\frac{7720\text{mV}}{3.16 \times 10^5}+\frac{0.1325\text{V}}{3.16 \times 10^3}$$

$$= 30\mu\text{V} + 9.23\mu\text{V} + 24\mu\text{V} + 4.19\mu\text{V}$$
$$= 67.42\mu\text{V}$$

$$\sigma_S = 0.0001$$

$$e_{IN} = e'_2 - V_4 = I_{REF1}\, R_{T\,150°C} - I_{REF2}\, R_4$$
$$= (1\text{mA} \times 156.4\Omega) - (1\text{mA} \times 109\Omega) = 47\text{mV}$$

$$I_O \text{ error} = \sigma_O + K\,\sigma_I + K\,\sigma_S\, e_{IN} = 6\mu\text{A} + (0.34℧ \times 67.42\mu\text{V}) + (0.34℧ \times 0.0001 \times 47000\mu\text{V}) = 6\mu\text{A} + 22.92\mu\text{A} + 1.60\mu\text{A}$$
$$= 30.52\mu\text{A}$$

$$\%\text{ error} = \frac{30.52\mu\text{A}}{16\text{mA}} \times 100\%$$

= 0.19% of span at upper range value.

CONCLUSIONS

Lower Range: From equation (10) it is observed that the predominant error term is the input offset voltage (30µV for the B grade). This is of little consequence in many applications. $V_{OS\ RTI}$ can, however, be nulled using the pot shown in Figures 5 and 6. The result is an error of 0.06% of span instead of 0.13% if span.

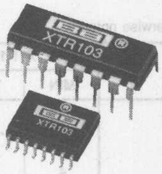
the result is an error of 0.09% of span instead of 0.19% span.

RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice, we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove the static-generating materials, such as untreated plastic, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporat ing microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% recommended).

BURR - BROWN®



XTR103

4-20mA Current Transmitter with RTD EXCITATION AND LINEARIZATION

FEATURES

- LESS THAN ±1% TOTAL ADJUSTED ERROR, –40°C TO +85°C
- RTD EXCITATION AND LINEARIZATION
- TWO OR THREE-WIRE RTD OPERATION
- WIDE SUPPLY RANGE: 9V to 40V
- HIGH PSR: 110dB min
- HIGH CMR: 80dB min

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA

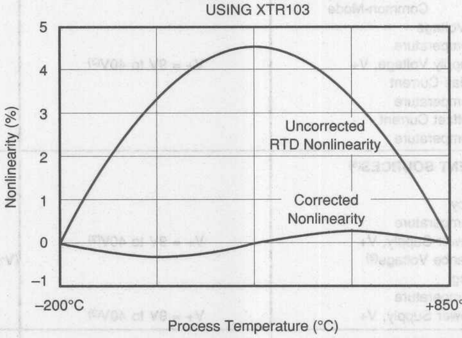
DESCRIPTION

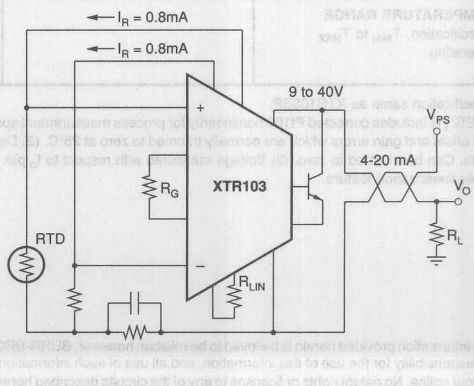
The XTR103 is a monolithic 4-20mA, two-wire current transmitter designed for Platinum RTD temperature sensors. It provides complete RTD current excitation, instrumentation amplifier, linearization, and current output circuitry on a single integrated circuit. Versatile linearization circuitry provides a 2nd-order correction to the RTD, typically achieving a 40:1 improvement in linearity.

Instrumentation amplifier gain can be configured for a wide range of temperature measurements. Total adjusted error of the complete current transmitter, including the linearized RTD is less than ±1% over the full –40 to +85°C operating temperature range. This includes zero drift, span drift and nonlinearity. The XTR103 operates on loop power supply voltages down to 9V.

The XTR103 is available in 16-pin plastic DIP and SOL-16 surface-mount packages specified for the –40°C to +85°C temperature range.

Pt100 NONLINEARITY CORRECTION USING XTR103





International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

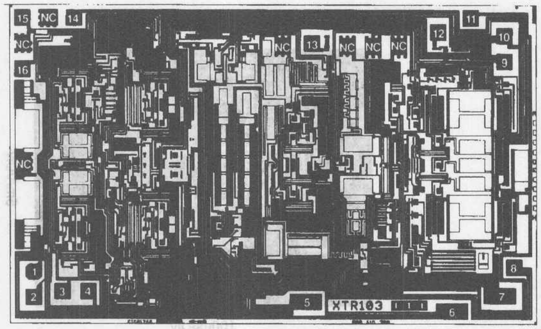
T_A = +25°C, V+ = 24V, and 2N6121 external transistor, unless otherwise noted.

PARAMETER	CONDITIONS	XTR103BP/BU MIN	XTR103BP/BU TYP	XTR103BP/BU MAX	XTR103AP/AU MIN	XTR103AP/AU TYP	XTR103AP/AU MAX	UNITS
OUTPUT								
Output Current Equation		$I_O = V_{IN} \cdot (0.016 + 40/R_G) + 4mA$, V_{IN} in Volts, R_G in Ω						A
Total Adjusted Error(1)	T_{MIN} to T_{MAX}			±1			±2	% of FS
Output Current, Specified Range		4		20	*		*	mA
Over-Scale Limit			34	40		*	*	mA
Under Scale-Limit			3.6	3.8		*	*	mA
Full Scale Output Error	V_{IN} = 1V, R_G = ∞		±15	±50		*	±100	µA
Noise: 0.1Hz to 1kHz	R_G = 40Ω		8			*		µAp-p
ZERO OUTPUT(2)	V_{IN} = 0, R_G = ∞		4			*		mA
Initial Error			±5	±50		*	±100	µA
vs Temperature			±0.2	±0.5		*	±1	µA/°C
vs Supply Voltage, V+	V+ = 9V to 40V(3)		0.5	2		*	*	µA/V
vs Common-Mode Voltage	V_{CM} = 2V to 4V(3)		0.1	2		*	*	µA/V
SPAN								
Span Equation (Transconductance)		$S = 0.016 + 40/R_G$				*		A/V
Untrimmed Error	R_G ≥ 75Ω		±0.1	±1		*	*	%
vs Temperature(4)			±20	±50		*	±100	ppm/°C
Nonlinearity: Ideal Input				0.01			*	%
RTD Input	Pt100: –200°C to +850°C, R_{LIN} = 1127Ω		0.1				*	%
INPUT								
Differential Range	R_G = ∞			1			*	V
Input Voltage Range(3)		2		4	*		*	V
Common-Mode Rejection	V_{IN} = 2V to 4V(3)	80	100		*	*		dB
Impedance: Differential			3			*		GΩ
Common-Mode			0.5			*		GΩ
Offset Voltage			±0.5	±2.5		*	*	mV
vs Temperature			±1	±2.5		±2	±5	µV/°C
vs Supply Voltage, V+	V+ = 9V to 40V(3)	110	130		*	*		dB
Input Bias Current			100	250		*	*	nA
vs Temperature			0.1	2		*	*	nA/°C
Input Offset Current			2	20		*	*	nA
vs Temperature			0.01	0.25		*	*	nA/°C
CURRENT SOURCES(5)								
Current			0.8			*		mA
Accuracy			±0.25	±0.5		*	±1	%
vs Temperature			±25	±50		±50	±100	ppm/°C
vs Power Supply, V+	V+ = 9V to 40V(3)		50			*		ppm/V
Compliance Voltage(3)		$(V^-_{IN}) - 0.2$		(V+) – 5	*		*	V
Matching				±0.5			*	%
vs Temperature			±10	±25		*	±50	ppm/°C
vs Power Supply, V+	V+ = 9V to 40V(3)		10			*		ppm/V
POWER SUPPLY								
Voltage Range(3), V+		9		40	*		*	V
TEMPERATURE RANGE								
Specification, T_{MIN} to T_{MAX}		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as XTR103BP.

NOTES: (1) Includes corrected Pt100 nonlinearity for process measurement spans greater than 100°C, and over-temperature zero and span effects. Does not include initial offset and gain errors which are normally trimmed to zero at 25°C. (2) Describes accuracy of the 4mA low-scale offset current. Does not include input amplifier effects. Can be trimmed to zero. (3) Voltage measured with respect to I_O pin. (4) Does not include TCR of gain-setting resistor, R_G. (5) Measured with R_{LIN} = ∞ to disable linearization feature.

DICE INFORMATION



XTR103 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Zero Adj.	9	R_{LIN}
2	Zero Adj.	10	V+
3	V^-_{IN}	11	E (Emitter)
4	V^+_{IN}	12	I_{R1}
5	R_G	13	I_{R2}
6	R_G	14	E_{INT} (Int. Emit.)
7	I_O	15	B (Base)
8	R_{LIN}	16	Zero Adj.

NC: No Connection
Substrate Bias: Internally connected to the I_O terminal (#7).

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	168 x 104 ±5	4.27 x 2.64 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATION

TOP VIEW

Pin	Function	Pin	Function
1	Zero Adjust	16	Zero Adjust
2	Zero Adjust	15	B (Base)
3	V^-_{IN}	14	E_{INT} (Internal Emitter)
4	V^+_{IN}	13	I_{R2}
5	R_G	12	I_{R1}
6	R_G	11	E (Emitter)
7	I_O	10	V+
8	R_{LIN}	9	R_{LIN}

ABSOLUTE MAXIMUM RATINGS

Power Supply, V+ (referenced to I_O pin)	40V
Input Voltage, V^+_{IN}, V^-_{IN} (referenced to I_O pin)	0V to V+
Storage Temperature Range	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Current Limit	Continuous
Junction Temperature	+165°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION

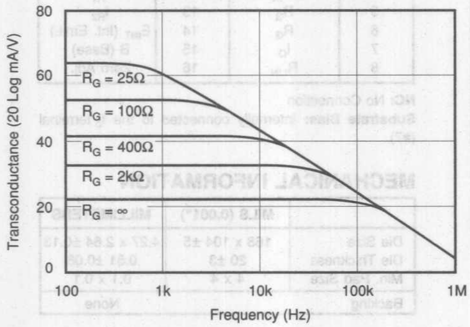
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
XTR103AP	16-pin Plastic DIP	180
XTR103BP	16-pin Plastic DIP	180
XTR103AU	SOL-16 Surface Mount	211
XTR103BU	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

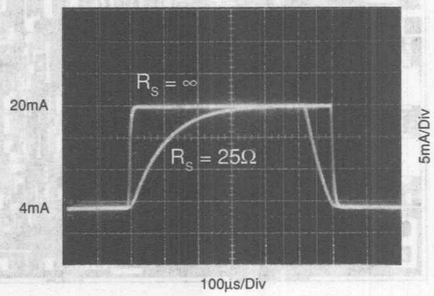
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
XTR103AP	16-pin Plastic DIP	–40°C to +85°C
XTR103BP	16-pin Plastic DIP	–40°C to +85°C
XTR103AU	SOL-16 Surface Mount	–40°C to +85°C
XTR103BU	SOL-16 Surface Mount	–40°C to +85°C

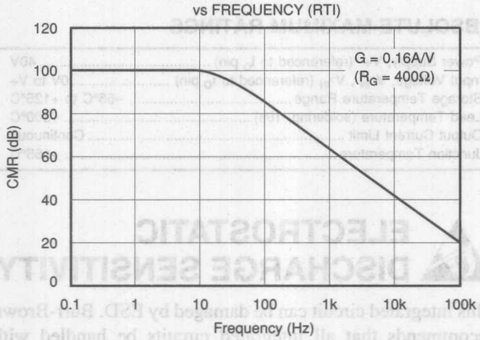
TRANSCONDUCTANCE vs FREQUENCY



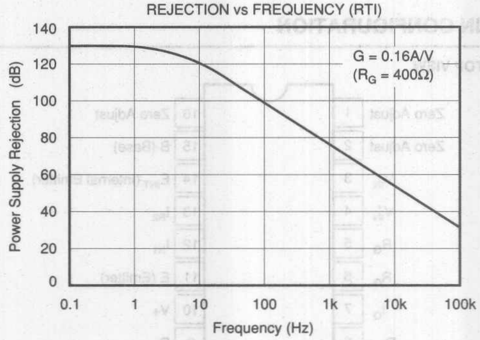
STEP RESPONSE



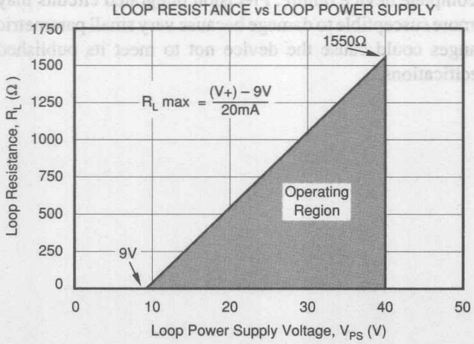
COMMON-MODE REJECTION vs FREQUENCY (RTI)



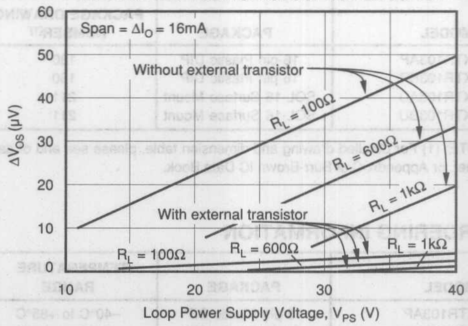
POWER SUPPLY REJECTION vs FREQUENCY (RTI)



LOOP RESISTANCE vs LOOP POWER SUPPLY

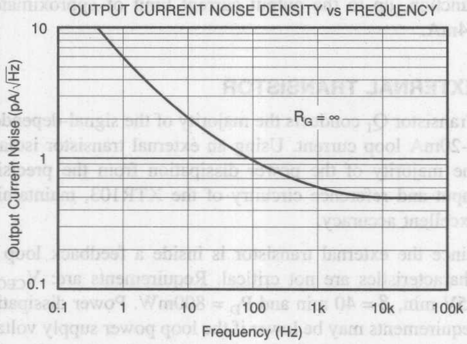


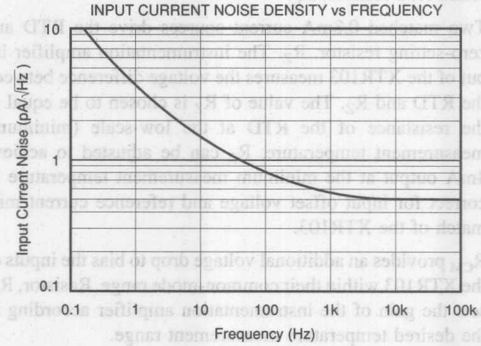
INPUT OFFSET VOLTAGE vs LOOP POWER SUPPLY

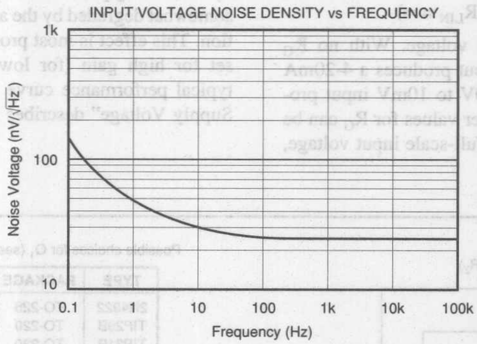


TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, +V = 24VDC, unless otherwise noted.







XTR103

4

INSTRUMENTATION AMPLIFIERS

APPLICATION INFORMATION

Figure 1 shows the basic connection diagram for the XTR103. The loop power supply, V_{PS} provides power for all circuitry. Output loop current is measured as a voltage across the series load resistor, R_L.

Two matched 0.8mA current sources drive the RTD and zero-setting resistor, R_Z. The instrumentation amplifier input of the XTR103 measures the voltage difference between the RTD and R_Z. The value of R_Z is chosen to be equal to the resistance of the RTD at the low-scale (minimum) measurement temperature. R_Z can be adjusted to achieve 4mA output at the minimum measurement temperature to correct for input offset voltage and reference current mismatch of the XTR103.

R_{CM} provides an additional voltage drop to bias the inputs of the XTR103 within their common-mode range. Resistor, R_G, sets the gain of the instrumentation amplifier according to the desired temperature measurement range.

The transfer function through the complete instrumentation amplifier and voltage-to-current converter is:

$$I_O = V_{IN} \bullet (0.016 + 40/R_G) + 4\text{mA},$$

$$(V_{IN} \text{ in volts, } R_G \text{ in ohms, } R_{LIN} = \infty)$$

where V_{IN} is the differential input voltage. With no R_G connected ($R_G = \infty$), a 0V to 1V input produces a 4-20mA output current. With $R_G = 25\Omega$, a 0V to 10mV input produces a 4-20mA output current. Other values for R_G can be calculated according to the desired full-scale input voltage, V_{FS}, with the formula in Figure 1.

Negative input voltage, V_{IN}, will cause the output current to be less than 4mA. Increasingly negative V_{IN} will cause the output current to limit at approximately 3.6mA.

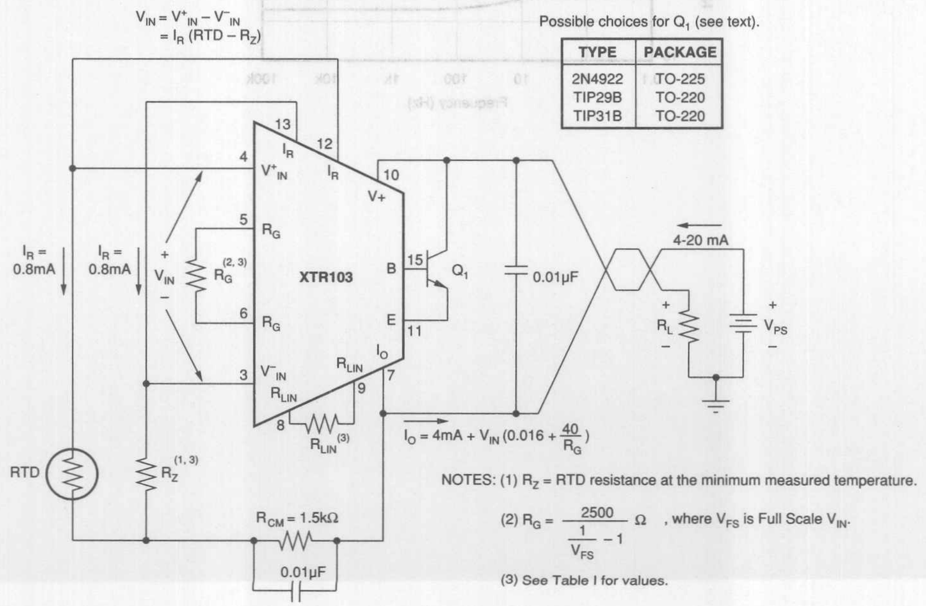
Increasingly positive input voltage (greater than V_{FS}) will produce increasing output current according to the transfer function, up to the output current limit of approximately 34mA.

EXTERNAL TRANSISTOR

Transistor Q_1 conducts the majority of the signal-dependent 4-20mA loop current. Using an external transistor isolates the majority of the power dissipation from the precision input and reference circuitry of the XTR103, maintaining excellent accuracy.

Since the external transistor is inside a feedback loop its characteristics are not critical. Requirements are: V_{CEO} = 45V min, β = 40 min and P_D = 800mW. Power dissipation requirements may be lower if the loop power supply voltage is less than 40V. Some possible choices for Q_1 are listed in Figure 1.

The XTR103 can be operated without this external transistor by connecting pin 11 to 14 (see Figure 2). Accuracy will be somewhat degraded by the additional internal power dissipation. This effect is most pronounced when the input stage is set for high gain (for low full-scale input voltage). The typical performance curve "Input Offset Voltage vs Loop Supply Voltage" describes this behavior.



Possible choices for Q_1 (see text).

TYPE	PACKAGE
2N4922	TO-225
TIP29B	TO-220
TIP31B	TO-220

NOTES: (1) R_Z = RTD resistance at the minimum measured temperature.

(2) $R_G = \dfrac{2500}{\dfrac{1}{V_{FS}} - 1}\ \Omega$, where V_{FS} is Full Scale V_{IN}.

(3) See Table I for values.

FIGURE 1. Basic RTD Temperature Measurement Circuit.

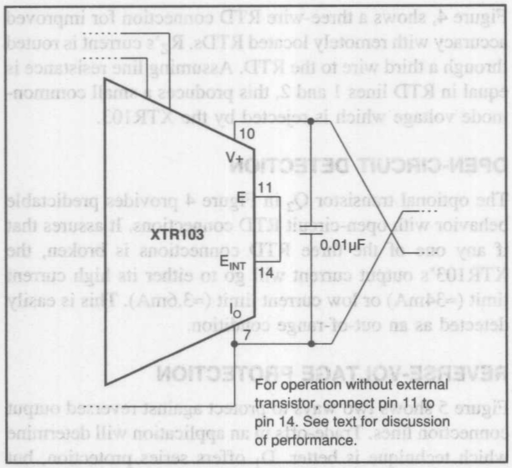


FIGURE 2. Operation Without External Transistor.

LOOP POWER SUPPLY

The voltage applied to the XTR103, V+, is measured with respect to the I_O connection, pin 7. V+ can range from 9V to 40V. The loop supply voltage, V_{PS}, will differ from the voltage applied to the XTR103 according to the voltage drop on the current sensing resistor, R_L (plus any other voltage drop in the line).

If a low loop supply voltage is used, R_L must be made a relatively low value to assure that V+ remains 9V or greater for the maximum loop current of 20mA. It may, in fact, be prudent to design for V+ equal or greater than 9V with loop currents up to 34mA to allow for out-of-range input conditions. The typical performance curve "Loop Resistance vs Loop Power Supply" shows the allowable sense resistor values for full-scale 20mA.

The low operating voltage (9V) of the XTR103 allows operation directly from personal computer power supplies (12V ±5%). When used with the RCV420 Current Loop Receiver (Figure 8), load resistor voltage drop is limited to 1.5V.

LINEARIZATION

On-chip linearization circuitry creates a signal-dependent variation in the two matching current sources. Both current sources are varied equally according to the following equation:

$$I_{R1} = I_{R2} = 0.8 + \frac{500 \cdot V_{IN}}{R_{LIN}}$$

(I_R in mA, V_{IN} in volts, R_{LIN} in ohms)
(maximum I_R = 1.0mA)

This varying excitation provides a 2nd-order term to the transfer function (including the RTD) which can correct the RTD's nonlinearity. The correction is controlled by resistor R_{LIN} which is chosen according to the desired temperature measurement range. Table I provides the R_G, R_Z and R_{LIN} resistor values for a Pt100 RTD.

If no linearity correction is desired, do not connect a resistor to the R_{LIN} pins ($R_{LIN} = \infty$). This will cause the excitation current sources to remain a constant 0.8mA.

ADJUSTING INITIAL ERRORS

Most applications will require adjustment of initial errors. Offset errors can be corrected by adjustment of the zero resistor, R_Z.

Figure 3 shows another way to adjust zero errors using the output current adjustment pins of the XTR103. This provides a minimum of ±300µA (typically ±500µA) adjustment around the initial low-scale output current. This is an output current adjustment which is independent of the input stage gain set

MEASUREMENT TEMPERATURE SPAN ΔT (°C)

T_{MIN}	100°C	200°C	300°C	400°C	500°C	600°C	700°C	800°C	900°C	1000°C
–200°C	18/90 653	18/185 838	18/286 996	18/396 1087	18/515 1131	18/645 1152	18/788 1159	18/946 1158	18/1120 1154	18/1317 1140
–100°C	60/84 1105	60/173 1229	60/270 1251	60/374 1249	60/487 1231	60/610 1207	60/746 1181	60/895 1155	60/1061 1128	
0°C	100/81 1287	100/167 1258	100/260 1229	100/361 1201	100/469 1173	100/588 1145	100/718 1117	100/860 1089		
100°C	138/78 1211	138/162 1183	138/252 1155	138/349 1127	138/453 1100	138/567 1073	138/691 1046			
200°C	175/76 1137	175/157 1110	175/244 1083	175/337 1056	175/437 1030	175/546 1003				
300°C	212/73 1066	212/152 1039	212/235 1013	212/325 987	212/422 962					
400°C	247/71 996	247/146 971	247/227 946	247/313 921						
500°C	280/68 930	280/141 905	280/219 881							
600°C	313/66 865	313/136 841								
700°C	345/64 803									
800°C	375/61 743									

R_Z/R_G
R_{LIN}
(Values are in Ω.)

NOTE: Values shown are for a Pt100 RTD.
Double (x2) all values for Pt200.

TABLE I. R_Z, R_G, and R_{LIN} Resistor Values for Pt100 RTD.

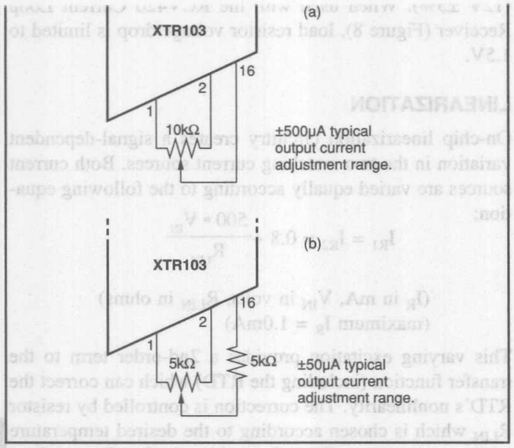


FIGURE 3. Low-Scale Output Current Adjustment.

with R_G. If the input stage is set for high gain (as required with narrow temperature measurement spans) the output current adjustment may not provide sufficient range. In these cases, offset can be nulled by adjusting the value of R_Z.

TWO-WIRE AND THREE-WIRE RTD CONNECTIONS

In Figure 1, the RTD can be located remotely simply by extending the two connections to the RTD. With this two-wire connection to the RTD, line resistance will introduce error. This error can be partially corrected by adjusting the values of R_Z, R_G, and R_{LIN}.

through a third wire to the RTD. Assuming line resistance is equal in RTD lines 1 and 2, this produces a small common-mode voltage which is rejected by the XTR103.

OPEN-CIRCUIT DETECTION

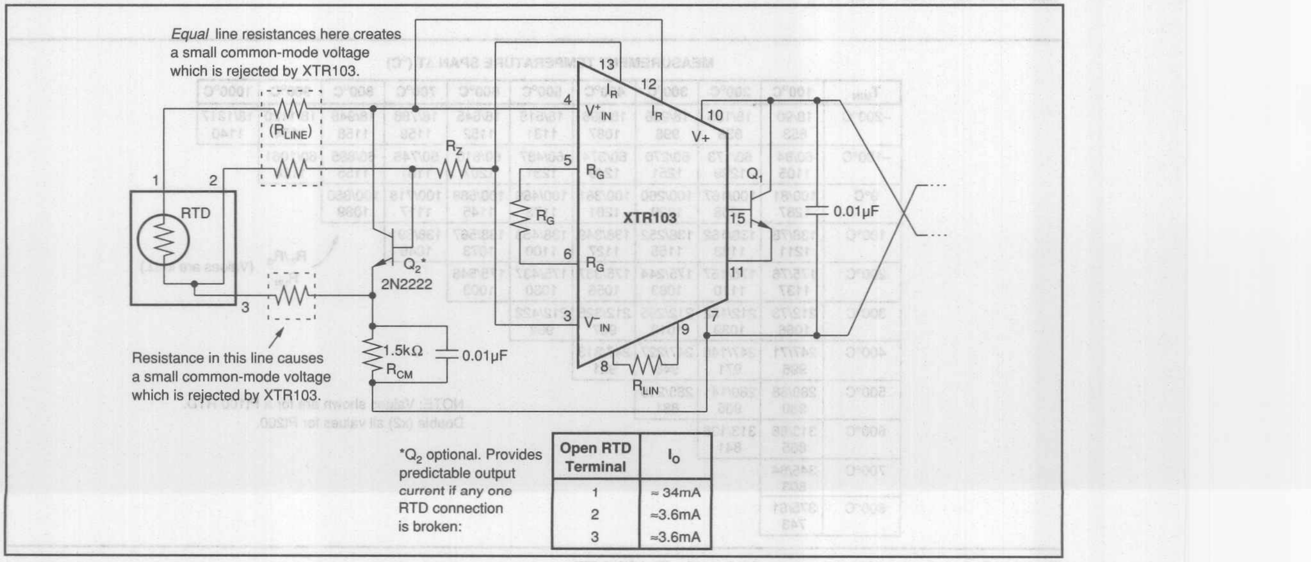
The optional transistor Q_2 in Figure 4 provides predictable behavior with open-circuit RTD connections. It assures that if any one of the three RTD connections is broken, the XTR103's output current will go to either its high current limit (≈34mA) or low current limit (≈3.6mA). This is easily detected as an out-of-range condition.

REVERSE-VOLTAGE PROTECTION

Figure 5 shows two ways to protect against reversed output connection lines. Trade-offs in an application will determine which technique is better. D_1 offers series protection, but causes a 0.7V loss in loop supply voltage. This may be undesirable if V+ can approach the 9V limit. Using D_2 (without D_1) has no voltage loss, but high current will flow in the loop supply if the leads are reversed. This could damage the power supply or the sense resistor, R_L. A diode with a higher current rating is needed for D_2 to withstand the highest current that could occur with reversed lines.

SURGE PROTECTION

Long lines are subject to voltage surges which can damage semiconductor components. To avoid damage, the maximum applied voltage rating for the XTR103 is 40V. A zener diode may be used for D_2 (Figure 6) to clamp the voltage applied to the XTR103 to a safe level. The loop power supply voltage must be lower than the voltage rating of the zener diode.



Open RTD Terminal	I_O
1	≈ 34mA
2	≈3.6mA
3	≈3.6mA

FIGURE 4. Three-Wire Connection for Remotely Located RTDs.

There are special zener diode types specifically designed to provide a very low impedance clamp and withstand large energy surges. These devices normally have a diode characteristic in the forward direction which also protects against reversed loop connections. As noted earlier, reversed loop connections would produce a large loop current, possibly damaging R_L.

RADIO FREQUENCY INTERFERENCE

The long wire lengths of current loops invite radio frequency interference. RF can be rectified by the sensitive input circuitry of the XTR103 causing errors. This generally appears as an unstable output current that varies with the position of loop supply or input wiring.

If the RTD sensor is remotely located, the interference may enter at the input terminals. For integrated transmitter assemblies with short connection to the sensor, the interference more likely comes from the current loop connections.

Bypass capacitors on the input often reduce or eliminate this interference. Connect these bypass capacitors to the I_O terminal as shown in Figure 7. Although the DC voltage at the I_O terminal is not equal to 0V (at the loop supply, V_{PS}) this circuit point can be considered the transmitter's "ground."

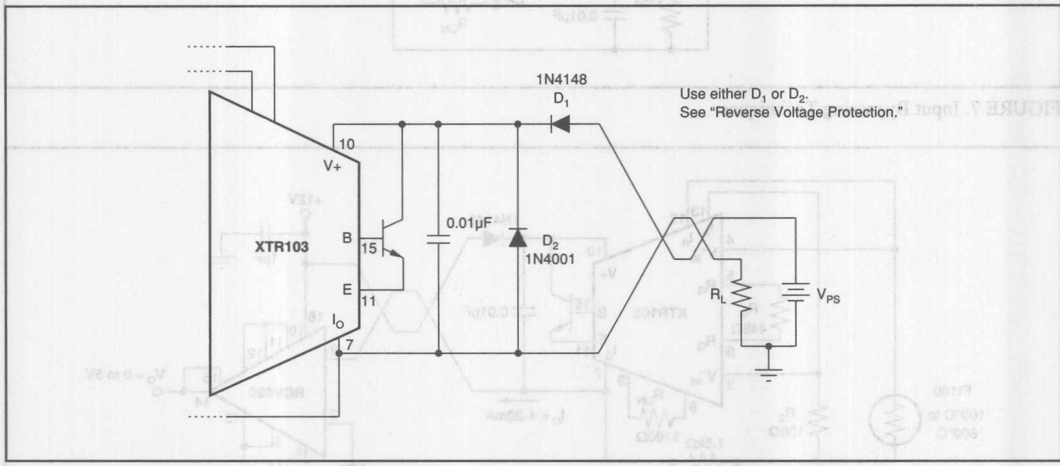


FIGURE 5. Reverse Voltage Protection.

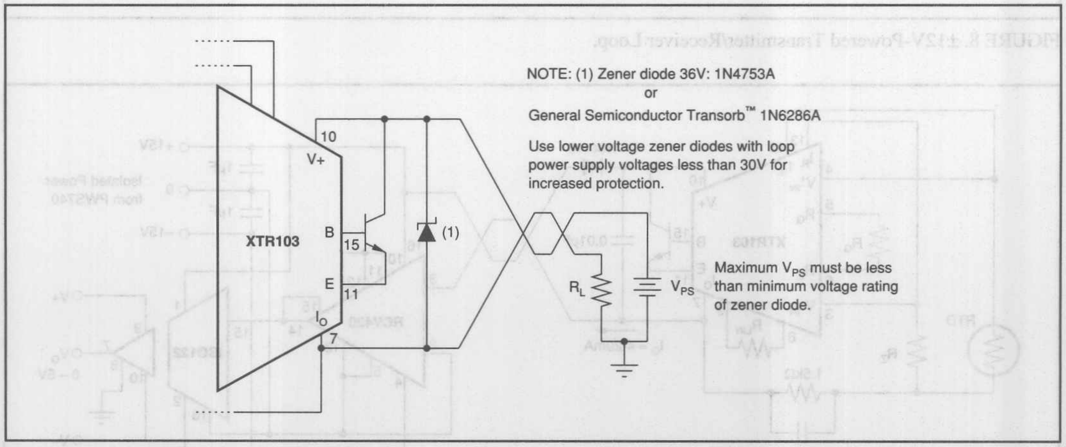


FIGURE 6. Over-Voltage Surge Protection.

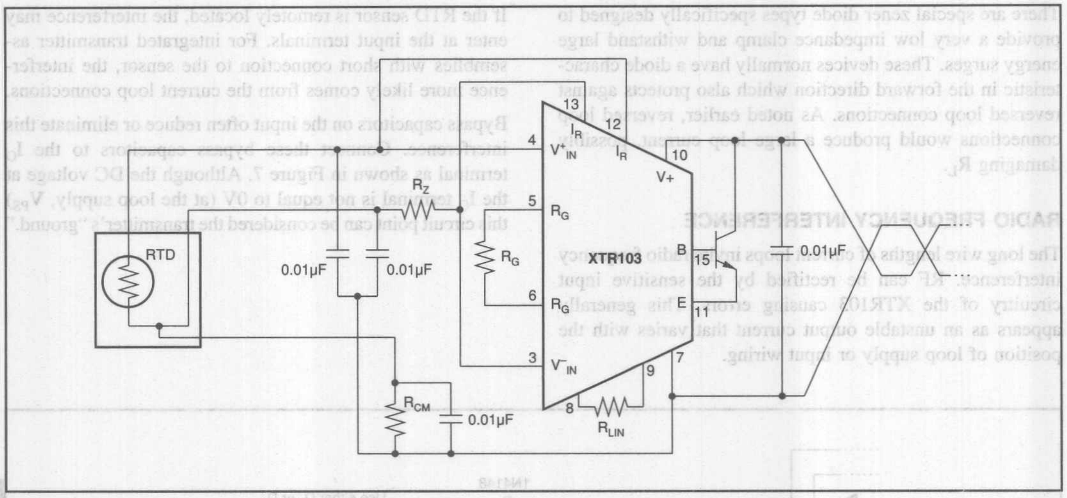


FIGURE 7. Input Bypassing Techniques.

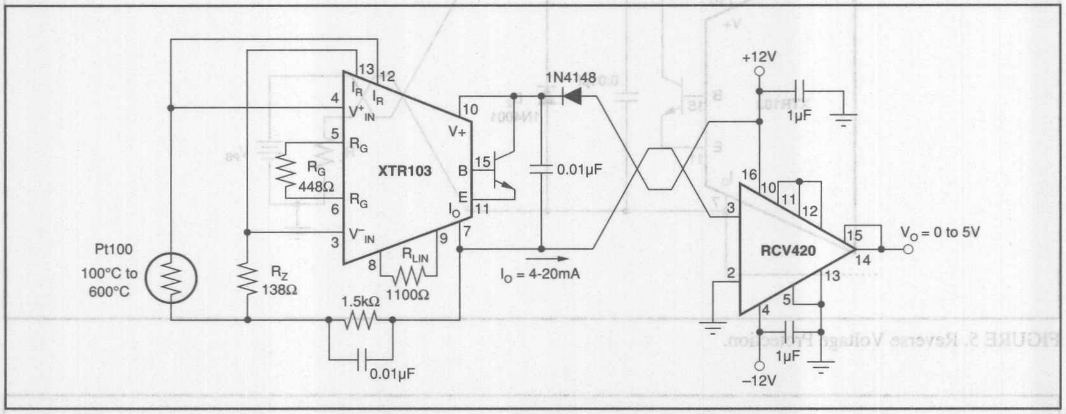


FIGURE 8. ±12V-Powered Transmitter/Receiver Loop.

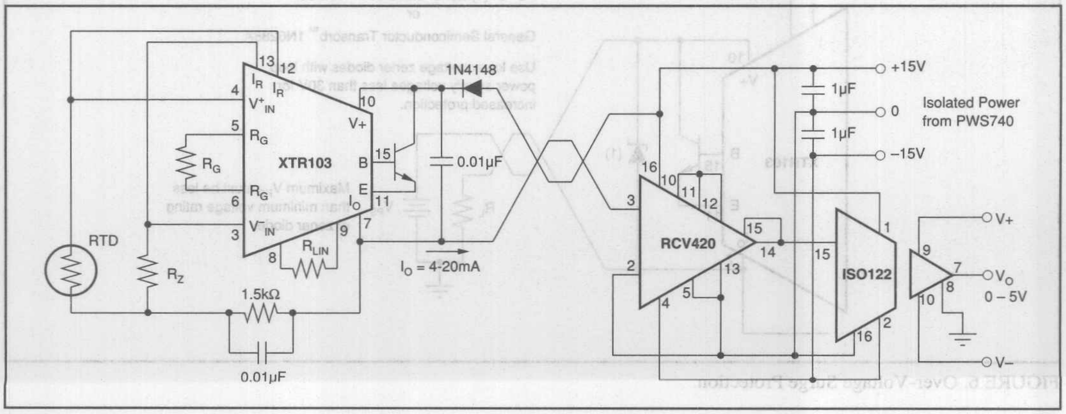
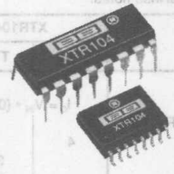


FIGURE 9. Isolated Transmitter/Receiver Loop.

BURR - BROWN®



XTR104

4-20mA Current Transmitter with BRIDGE EXCITATION AND LINEARIZATION

FEATURES

- LESS THAN ±1% TOTAL ADJUSTED ERROR, –40°C TO +85°C
- BRIDGE EXCITATION AND LINEARIZATION
- WIDE SUPPLY RANGE: 9V to 40V
- LOW SPAN DRIFT: 50ppm/°C max
- HIGH PSR: 110dB min
- HIGH CMR: 80dB min

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA
- WEIGHTING SYSTEMS
- ACCELEROMETERS

DESCRIPTION

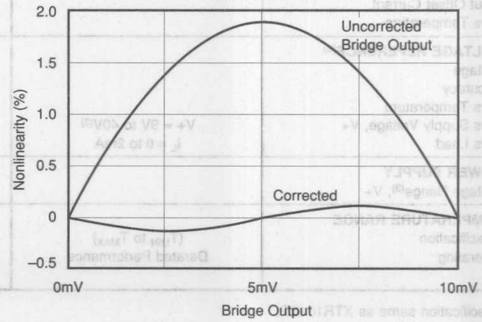
The XTR104 is a monolithic 4-20mA, two-wire current transmitter integrated circuit designed for bridge input signals. It provides complete bridge excitation, instrumentation amplifier, linearization, and current output circuitry necessary for high impedance strain gage sensors.

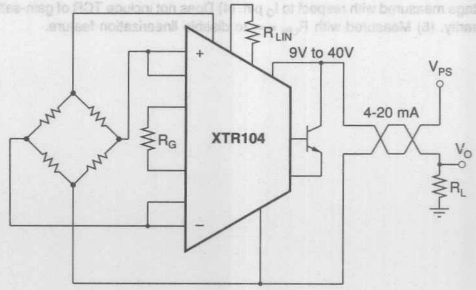
The instrumentation amplifier can be used over a wide range of gain, accommodating a variety of input signals and sensors. Total adjusted error of the complete current transmitter, including the linearized bridge is less than ±1% over the full –40°C to +85°C temperature range. This includes zero drift, span drift and non-linearity for bridge outputs as low as 10mV. The XTR104 operates on loop power supply voltages down to 9V.

Linearization circuitry consists of a second, fully independent instrumentation amplifier that controls the bridge excitation voltage. It provides second-order correction to the transfer function, typically achieving a 20:1 improvement in nonlinearity, even with low cost transducers.

The XTR104 is available in 16-pin plastic DIP and SOL-16 surface-mount packages specified for the –40°C to +85°C temperature range.

BRIDGE NONLINEARITY CORRECTION USING XTR104



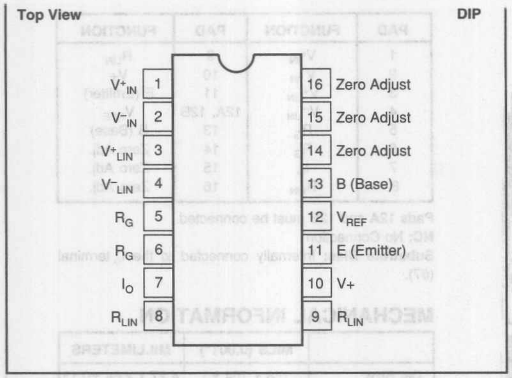


International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PARAMETER	CONDITIONS	XTR104BP, BU MIN	XTR104BP, BU TYP	XTR104BP, BU MAX	XTR104AP, AU MIN	XTR104AP, AU TYP	XTR104AP, AU MAX	UNITS
OUTPUT								
Output Current Equation		$I_O = V_{IN} \cdot (0.016 + 40/R_G) + 4mA$			V_{IN} in Volts, R_G in Ω			A
Total Adjusted Error(1)	T_{MIN} to T_{MAX}, $V_{FS} \geq 10mV$, $R_B = 5k\Omega$			±1			±2	% of FS
Current, Specified Range		4		20	*		*	mA
Over-Scale Limit			34	40		*	*	mA
Under Scale-Limit			3.6	3.8		*	*	mA
Full Scale Output Error	$V_{IN} = 1V$, $R_G = \infty$		±15	±50		*	±100	µA
Noise: 0.1Hz to 1kHz	$R_G = 40\Omega$		8			*		µAp-p
ZERO OUTPUT(2)	$V_{IN} = 0V$, $R_G = \infty$		4			*		mA
Initial Error			±5	±50		*	±100	µA
vs Temperature			±0.2	±0.5		*	±1	µA/°C
vs Supply Voltage, V+	V+ = 9V to 40V(3)		0.5	2		*	*	µA/V
vs Common-Mode Voltage	V_{CM} = 2V to 3V(3)		0.1	2		*	*	µA/V
SPAN								
Span Equation (Transconductance)		$S = 0.016 + 40/R_G$				*		A/V
Untrimmed Error	$R_G \geq 75\Omega$		±0.1	±1		*	*	%
vs Temperature(4)			±20	±50		*	±100	ppm/°C
Nonlinearity: Ideal Input				0.01			*	%
Bridge Input(5)			0.1			*		%
INPUT								
Differential Range				1			*	V
Input Voltage Range(3)		2		3	*		*	V
Common-Mode Rejection	V_{IN} = 2V to 3V(3)	80	100		*	*		dB
Impedance: Differential			3			*		GΩ
Common-Mode			0.5			*		GΩ
Offset Voltage			±0.5	±2.5		*	*	mV
vs Temperature			1	2.5		2	5	µV/°C
vs Supply Voltage, V+	V+ = 9V to 40V(3)	110	130		*	*		dB
Input Bias Current			100	250		*	*	nA
vs Temperature			0.1	2		*	*	nA/°C
Input Offset Current			2	20		*	*	nA
vs Temperature			0.01	0.25		*	*	nA/°C
VOLTAGE REFERENCE(6)								
Voltage			5			*		V
Accuracy			±0.25	±0.5		*	±1	%
vs Temperature			±10	±50		*	±100	ppm/°C
vs Supply Voltage, V+	V+ = 9V to 40V(3)		5			*		ppm/V
vs Load	I_L = 0 to 2mA		50			*		ppm/mA
POWER SUPPLY								
Voltage Range(3), V+		9		40	*		*	V
TEMPERATURE RANGE								
Specification	(T_{MIN} to T_{MAX})	–40		85	*		*	°C
Operating	Derated Performance	–40		125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as XTR104BP.

NOTES: (1) Includes corrected second-order nonlinearity of bridge, and over-temperature zero and span effects. Does not include initial offset and span errors which are normally trimmed to zero at 25°C. (2) Describes accuracy of the 4mA low-scale current. Does not include input amplifier effects. Can be trimmed to zero. (3) Voltage measured with respect to I_O pin. (4) Does not include TCR of gain-setting resistor, R_G. (5) When configured to correct for ≤2% second-order bridge sensor nonlinearity. (6) Measured with $R_{LIN} = \infty$ to disable linearization feature.



Power Supply, V+ (referenced to I_O pin) ....
Input Voltage, V^+_{IN}, V^-_{IN}, V^+_{LIN}, V^-_{LIN} (referenced to I_O pin) ..... 0V to V+
Storage Temperature Range .... –55°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
Output Current Limit .... Continuous
Junction Temperature .... +165°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
XTR104AP	16-Pin Plastic DIP	180
XTR104BP	16-Pin Plastic DIP	180
XTR104AU	SOL-16 Surface Mount	211
XTR104BU	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

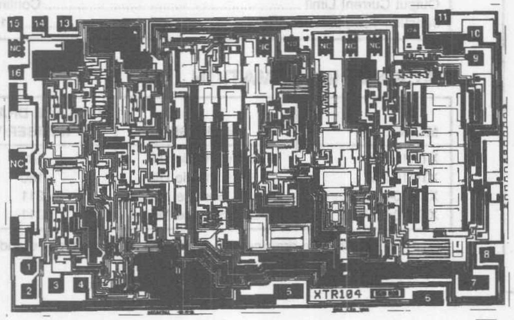
MODEL	PACKAGE	TEMPERATURE RANGE
XTR104AP	16-pin Plastic DIP	–40°C to +85°C
XTR104BP	16-pin Plastic DIP	–40°C to +85°C
XTR104AU	SOL-16 Surface Mount	–40°C to +85°C
XTR104BU	SOL-16 Surface Mount	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

DICE INFORMATION



XTR104 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	V^+_{IN}	9	R_{LIN}
2	V^-_{IN}	10	V+
3	V^+_{LIN}	11	E (Emitter)
4	V^-_{LIN}	12A, 12B	V_{REF}
5	R_G	13	B (Base)
6	R_G	14	Zero Adj.
7	I_O	15	Zero Adj.
8	R_{LIN}	16	Zero Adj.

Pads 12A and 12B must be connected.
NC: No Connection
Substrate Bias: Internally connected to the I_O terminal (#7).

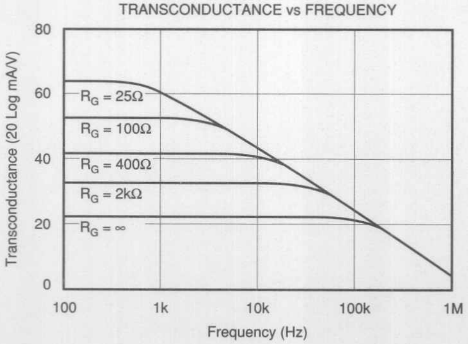
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	168 x 104 ±5	4.27 x 2.64 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

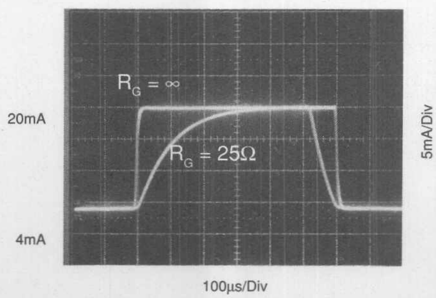
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V+ = 24V, unless otherwise noted.

TRANSCONDUCTANCE vs FREQUENCY



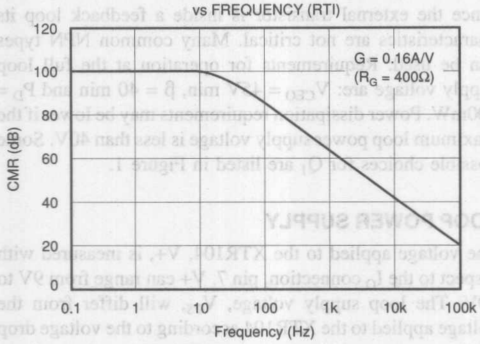
STEP RESPONSE



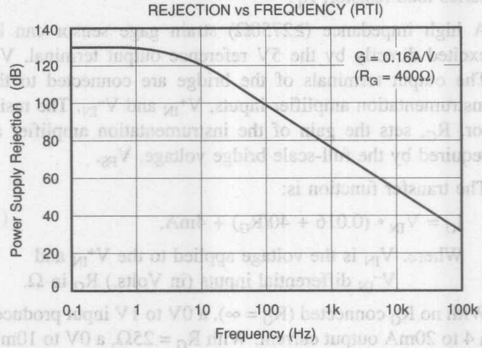
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $+V = 24V$, unless otherwise noted.

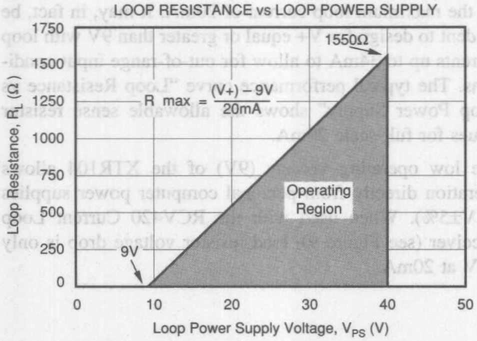
COMMON-MODE REJECTION vs FREQUENCY (RTI)



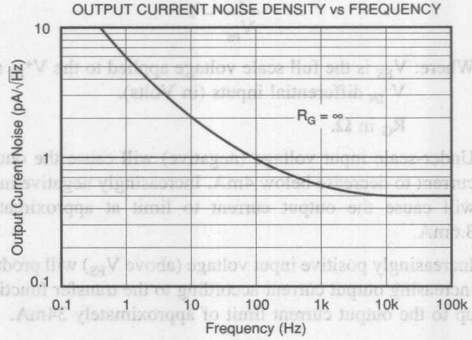
POWER SUPPLY REJECTION vs FREQUENCY (RTI)



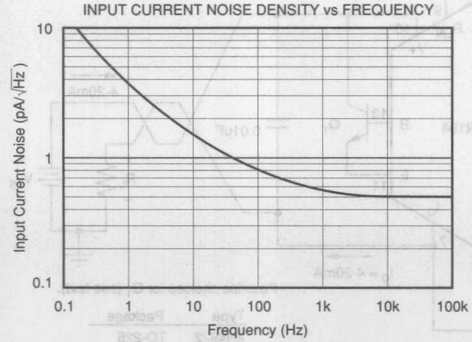
LOOP RESISTANCE vs LOOP POWER SUPPLY



OUTPUT CURRENT NOISE DENSITY vs FREQUENCY



INPUT CURRENT NOISE DENSITY vs FREQUENCY



INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

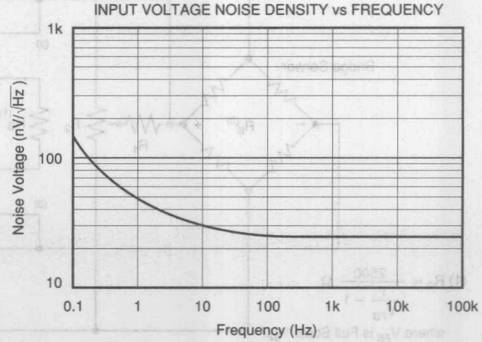


Figure 1 shows the basic connection diagram for the XTR104. The loop power supply, V_{PS}, provides power for all circuitry. Loop current is measured as a voltage across the series load resistor, R_L.

A high impedance (≥2750Ω) strain gage sensor can be excited directly by the 5V reference output terminal, V_R. The output terminals of the bridge are connected to the instrumentation amplifier inputs, V^+_{IN} and V^-_{IN}. The resistor, R_G, sets the gain of the instrumentation amplifier as required by the full-scale bridge voltage, V_{FS}.

The transfer function is:

$$I_O = V_{IN} \cdot (0.016 + 40/R_G) + 4\text{mA}, \qquad (1)$$

Where: V_{IN} is the voltage applied to the V^+_{IN} and V^-_{IN} differential inputs (in Volts.) R_G in Ω.

With no R_G connected ($R_G = \infty$), a 0V to 1V input produces a 4 to 20mA output current. With $R_G = 25\Omega$, a 0V to 10mV input produces a 4 to 20mA output current. Other values for R_G can be calculated as follows:

$$R_G = \frac{2500}{\dfrac{1}{V_{FS}} - 1} \qquad (2)$$

Where: V_{FS} is the full scale voltage applied to the V^+_{IN} and V^-_{IN} differential inputs (in Volts).

R_G in Ω.

Under-scale input voltage (negative) will cause the output current to decrease below 4mA. Increasingly negative input will cause the output current to limit at approximately 3.6mA.

Increasingly positive input voltage (above V_{FS}) will produce increasing output current according to the transfer function, up to the output current limit of approximately 34mA.

Transistor Q_1 conducts the majority of the signal-dependent 4 to 20mA loop current. Using an external transistor isolates the power dissipation from the precision input and reference circuitry of the XTR104, maintaining excellent accuracy.

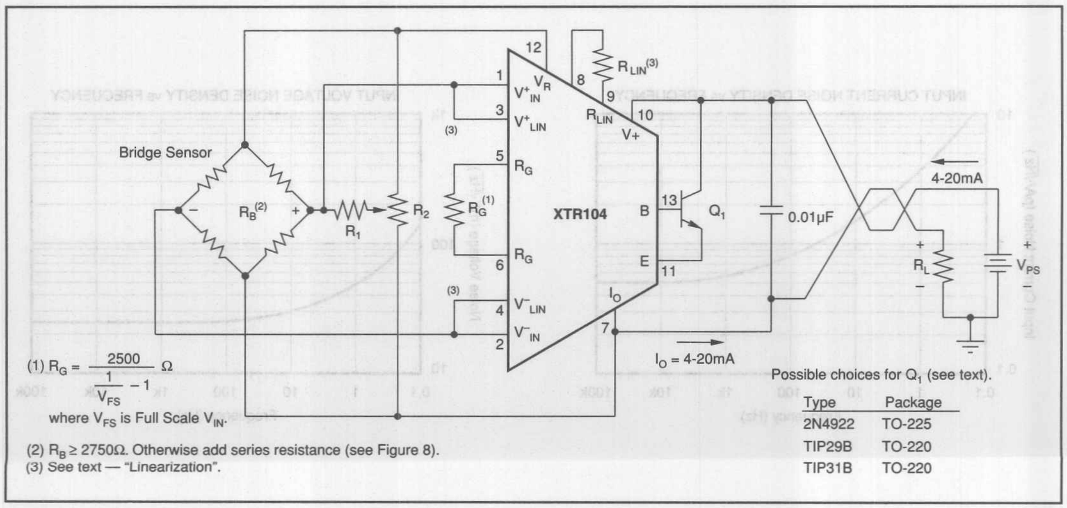
Since the external transistor is inside a feedback loop its characteristics are not critical. Many common NPN types can be used. Requirements for operation at the full loop supply voltage are: V_{CEO} = 45V min, β = 40 min and P_D = 800mW. Power dissipation requirements may be lower if the maximum loop power supply voltage is less than 40V. Some possible choices for Q_1 are listed in Figure 1.

LOOP POWER SUPPLY

The voltage applied to the XTR104, V+, is measured with respect to the I_O connection, pin 7. V+ can range from 9V to 40V. The loop supply voltage, V_{PS}, will differ from the voltage applied to the XTR104 according to the voltage drop on the current sensing resistor, R_L (plus any other voltage drop in the line).

If a low loop supply voltage is used, R_L must be made a relatively low value to assure that V+ remains 9V or greater for the maximum loop current of 20mA. It may, in fact, be prudent to design for V+ equal or greater than 9V with loop currents up to 34mA to allow for out-of-range input conditions. The typical performance curve "Loop Resistance vs Loop Power Supply" shows the allowable sense resistor values for full-scale 20mA.

The low operating voltage (9V) of the XTR104 allows operation directly from personal computer power supplies (12V±5%). When used with the RCV420 Current Loop Receiver (see Figure 9), load resistor voltage drop is only 1.5V at 20mA.



Type	Package
2N4922	TO-225
TIP29B	TO-220
TIP31B	TO-220

FIGURE 1. Bridge Sensor Application, Connected for Positive Nonlinearity.

Figure 1 shows a bridge trim circuit (R_1, R_2). This adjustment can be used to compensate for the initial accuracy of the bridge and/or to trim the offset voltage of the XTR104. The values of R_1 and R_2 depend on the impedance of the bridge, and the trim range required. This trim circuit places an additional load on the V_R output. The effective load of the trim circuit is nearly equal to R_2. Total load on the V_R output terminal must not exceed 2mA. An approximate value for R_1 can be calculated:

$$R_1 \approx \frac{5V \cdot R_B}{4 \cdot V_{TRIM}} \quad (3)$$

Where: R_B is the resistance of the bridge.
V_{TRIM} is the desired ±voltage trim range (in V).

Make R_2 equal or lower in value to R_1.

Figure 2 shows another way to adjust zero errors using the output current adjustment pins of the XTR104. This provides ±500μA (typical) adjustment around the initial low-scale output current. This is an output current adjustment that is independent of the input stage gain set with R_G. If the input stage is set for high gain the output current adjustment may not provide sufficient range.

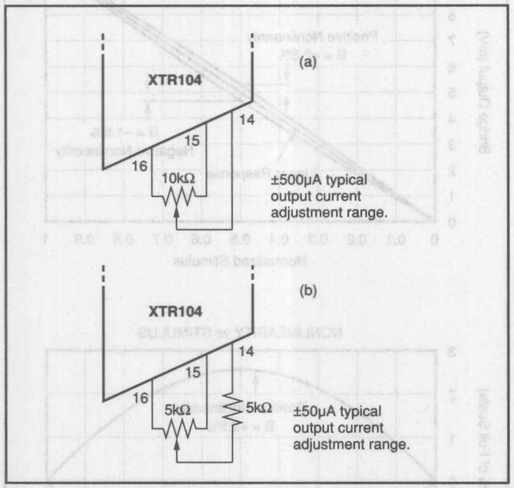


FIGURE 2. Low-scale Output Current Adjustment.

LINEARIZATION

Differential voltage applied to the linearization inputs, V^+_{LIN} and V^-_{LIN}, causes the reference (excitation) voltage, V_R, to vary according to the following equation:

$$V_R = 5V + V_{LIN} \frac{K_{LIN}}{R_{LIN}} \quad (4)$$

Where: V_{LIN} is the voltage applied to the V^+_{LIN} and V^-_{LIN} differential inputs (in V).
R_{LIN} in Ω.
$K_{LIN} \approx 24000$ (approximately ±20% depending on variations in the fabrication of the XTR104).

bridge excitation voltage can be made to vary as much as ±0.5V in response to the bridge output voltage. Be sure that the total load on the V_R output is less than 2mA at the maximum excitation voltage, $V_R = 5.5V$.

Signal-dependent variation of the bridge excitation voltage provides a second-order term to the complete transfer function (including the bridge). This can be tailored to correct for bridge sensor nonlinearity. Either polarity of nonlinearity (bowing up or down) can be compensated by proper connection of the V_{LIN} inputs. Connecting V^+_{LIN} to V^+_{IN} and V^-_{LIN} to V^-_{IN} (Figure 1) causes V_R to increase with bridge output which compensates for a positive bow in the bridge response. Reversing the connections (Figure 3) causes V_R to decrease with increasing bridge output, to compensate for negative-bowing nonlinearity.

To determine the required value for R_{LIN} you must know the nonlinearity of the bridge sensor with constant excitation voltage. The linearization circuitry can only compensate for the parabolic portion of a sensor's nonlinearity. Parabolic nonlinearity has a maximum deviation from linear occurring at mid-scale (see Figure 4). Sensors with nonlinearity curves similar to that shown in Figure 4, but not peaking exactly at mid-scale can be substantially improved. A nonlinearity that is perfectly "S-shaped" (equal positive and negative nonlinearity) cannot be corrected with the XTR104. It may, however, be possible to improve the worst-case nonlinearity of a sensor by equalizing the positive and negative nonlinearity.

The nonlinearity, B (in % of full scale), is positive or negative depending on the direction of the bow. A maximum of ±2.5% nonlinearity can be corrected. An approximate value for R_{LIN} can be calculated by:

$$R_{LIN} = \frac{K_{LIN} \cdot V_{FS}}{0.2 \cdot B} \quad (5)$$

Where: $K_{LIN} \approx 24000$.
V_{FS} is the full-scale bridge output (in Volts) with constant 5V excitation.
B is the parabolic nonlinearity in ±% of full scale.
R_{LIN} in Ω.

Methods for refining this calculation involve determining the actual value of K_{LIN} for a particular device (explained later).

B is a signed number (negative for a downward-bowing nonlinearity). This can produce a negative value for R_{LIN}. In this case, use the resistor value indicated (ignore the sign), but connect V^+_{LIN} to V^-_{IN} and V^-_{LIN} to V^+_{IN} as shown in Figure 3.

This approximate calculation of R_{LIN} generally provides about a 5:1 improvement in bridge nonlinearity.

Example: The bridge sensor depicted by the negative-bowing curve in Figure 4. Its full scale output is 10mV with constant 5V excitation. Its maximum nonlinearity, B, is –1.9% referred to full scale (occurring at mid-scale). Using equation 5:

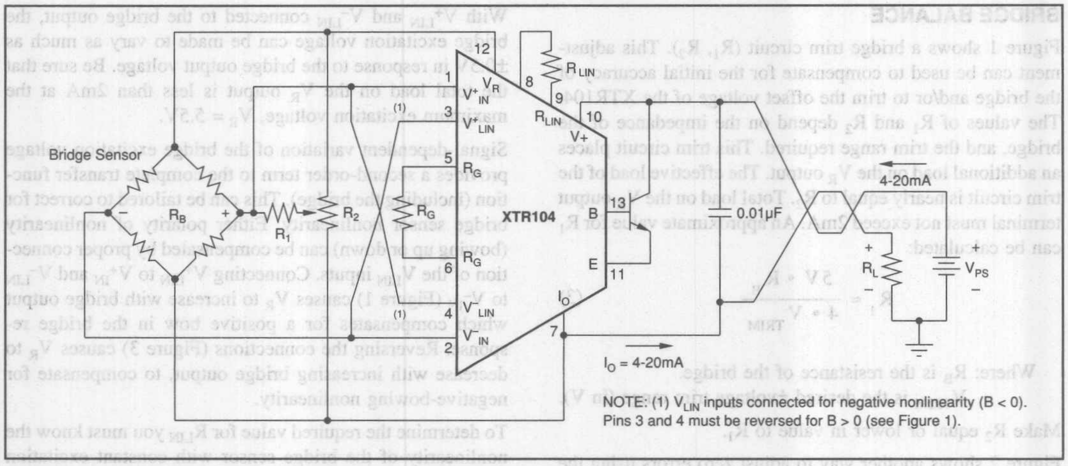


FIGURE 3. Bridge Sensor, V_{LIN} Connected for Negative Nonlinearity.

$$R_{LIN} \approx \frac{24000 \cdot 0.01}{0.2 \cdot (-1.9)} = -632\ \Omega$$

Use $R_{LIN} = 632\Omega$. Because the calculation yields a negative result, connect V^+_{LIN} to V^-_{IN} and V^-_{LIN} to V^+_{IN}.

Gain is affected by the varying the excitation voltage. For each 1% of corrected nonlinearity, the gain must be altered by 4%. As a result, equation 2 will not provide an accurate R_G when nonlinearity correction is used. The following equation calculates the required value for R_G to compensate for this effect.

$$R_G = \frac{2500}{\dfrac{1}{(1 + 0.04 \cdot B)\ V_{FS}} - 1} \tag{6}$$

B must again be a signed number in this calculation—positive for positive bowing nonlinearity, and negative for a negative-bowing nonlinearity.

$R_G = 23.32\Omega$ for the example above.

A more accurate value for R_{LIN} can be determined by first measuring the actual gain constant of the linearization inputs, K_{LIN} (see equation 4). Measure the change in the reference voltage, ΔV_R, in response to a measured voltage change at the linearization inputs, ΔV_{LIN}. Make this measurement with a known, temporary test value for R_{LIN}. These measurements can be made during operation of the circuit by providing stimulus to the bridge sensor, or by temporarily unbalancing the bridge with a fixed resistor in parallel with one of the bridge resistors. Calculate the actual K_{LIN}:

$$K_{LIN} = \frac{\Delta V_R \cdot R_{TEST}}{\Delta V_{LIN}} \tag{7}$$

Where: ΔV_{LIN} is the change in voltage at V_{LIN}.
ΔV_R is the measured change in reference voltage, V_R.
R_{TEST} is a temporary fixed value of R_{LIN} (in Ω).

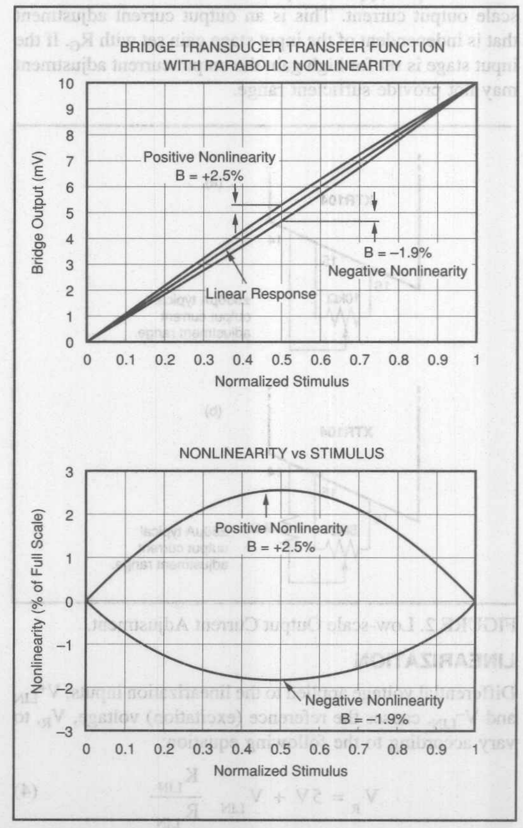


FIGURE 4. Parabolic Nonlinearity.

Then, R_{LIN} can be calculated using equation 5 using the accurate value of K_{LIN} from equation 7. K_{LIN} can be a different value for each XTR104.

It is also possible to make a real-time adjustment of R_{LIN} with a variable resistor (active circuit trimming). This is done by measuring the change in V_R in response to a zero-to-V_{FS} change in voltage applied to the V_{LIN} inputs. To correct for each 1% of nonlinearity, the excitation voltage, V_R, must make a 4% change at full-scale input. So the change in reference voltage, ΔV_R, for a full-scale change in V_{LIN} can be calculated by:

$$\Delta V_R = 0.2 \cdot B \tag{8}$$

Example: A bridge sensor has a –1.9% nonlinearity. Apply the full-scale bride output, V_{FS} (10mV), to the V_{LIN} inputs and adjust R_{LIN} for:

$$V_R'' = 5V + 0.2 \cdot B = 4.62V$$

Note that with all the calculation and adjustment methods described above, the full-scale bridge output is no longer equal to V_{FS} because the excitation voltage at full scale is no longer 5V. All the calculations and adjustment procedures described above assume V_{FS} to be the full-scale bridge output with constant 5V excitation. It is not necessary to iterate the calculations or adjustment procedures using the new full-scale bridge output as a starting point. However, a new value for R_G must be calculated using equation 6.

A refined value for R_{LIN}, arrived at either by active circuit trimming, or by measuring linearization gain (equation 7) will improve linearity. Reduction of the original parabolic nonlinearity of the sensor can approach 40:1. Actual results will depend on higher-order nonlinearity of the sensor.

If no linearity correction is desired, make no connections to the R_{LIN} pins ($R_{LIN} = \infty$). This will cause the V_R output to remain a constant +5V. The V^+_{LIN} and V^-_{LIN} inputs should remain connected to the bridge output to keep these inputs biased in their active region.

OTHER SENSOR TYPES

The XTR104 can be used with a wide variety of inputs. Its high input impedance instrumentation amplifier is versatile and can be configured for differential input voltages from millivolts to a maximum of 1V full scale. The linear common-mode range of the inputs is from 2V to 4V, referenced to the I_O terminal, pin 7.

You can use the linearization feature of the XTR104 with any sensor whose output is ratiometric with an excitation voltage. For example, Figure 5 shows the XTR104 used with a potentiometer position sensor.

REVERSE-VOLTAGE PROTECTION

Figure 6 shows two ways to protect against reversed output connection lines. Trade-offs in an application will determine which technique is better. D_1 offers series protection, but causes a 0.7V loss in loop supply voltage. This may be undesirable if V+ can approach the 9V limit. Using D_2 (without D_1) has no voltage loss, but high current will flow in the loop supply if the leads are reversed. This could damage the power supply or the sense resistor, R_L. A diode with a higher current rating is needed for D_2 to withstand the highest current that could occur with reversed lines.

SURGE PROTECTION

Long lines may be subject to voltage surges which can damage semiconductor components. To avoid damage, the maximum applied voltage rating for the XTR104 is 40V. A zener diode can be used for D_2 (Figure 7) to clamp the voltage applied to the XTR104 to a safe level. The loop power supply voltage must be lower than the voltage rating of the zener diode.

There are special zener diode types (Figure 7) specifically designed to provide a very low impedance clamp and withstand large energy surges. These devices normally have a diode characteristic in the forward direction which also

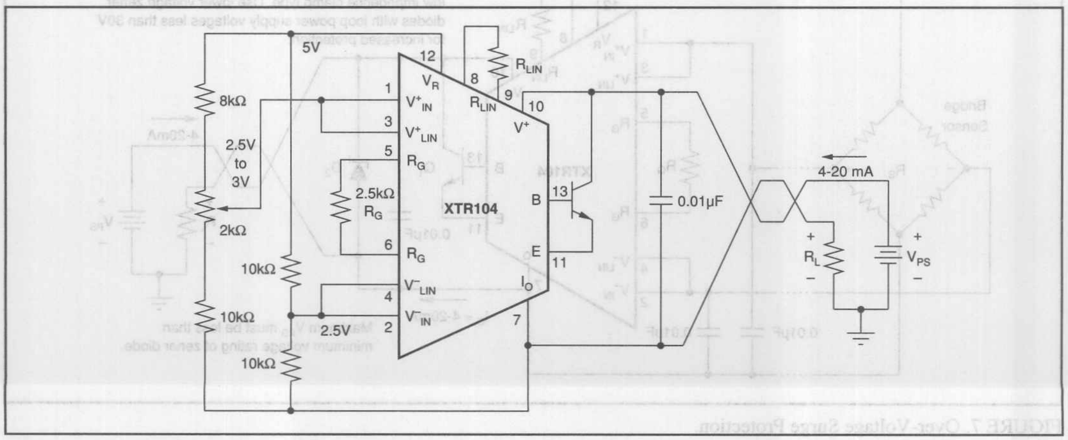


FIGURE 5. Potentiometer Sensor Application.

rent, possibly damaging R_L.

RADIO FREQUENCY INTERFERENCE

The long wire lengths of current loops invite radio frequency interference. RF can be rectified by the sensitive input circuitry of the XTR104 causing errors. This generally appears as an unstable output current that varies with the position of loop supply or input wiring.

If the bridge sensor is remotely located from the XTR104, the interference may enter at the input terminals. For integrated transmitter assemblies with short connections to the sensor, the interference more likely comes from the current loop connections. Connect these bypass capacitors to the I_O terminal (see Figure 7). Although the DC voltage at the I_O terminal is not equal to 0V (at the loop supply, V_{PS}) this circuit point can be considered the transmitter's "ground".

LOW-IMPEDANCE BRIDGES

Low impedance bridges can be used with the XTR104 by adding series resistance to limit excitation current to ≤2mA. Equal resistance should be added to the upper and lower sides of the of the bridge (Figure 8) to keep the bridge output voltage centered at approximately 2.5V. Bridge output is reduced, so a preamplifier, as shown, may be needed to reduce offset and drift.

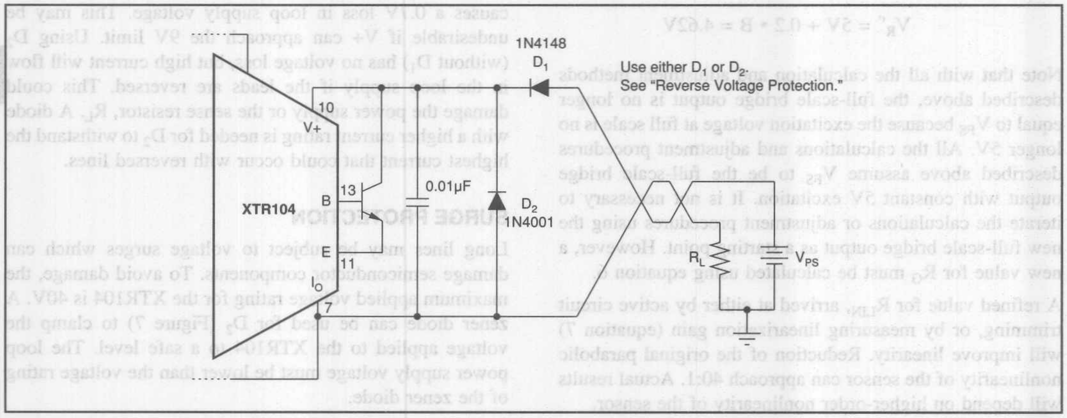


FIGURE 6. Reverse Voltage Protection.

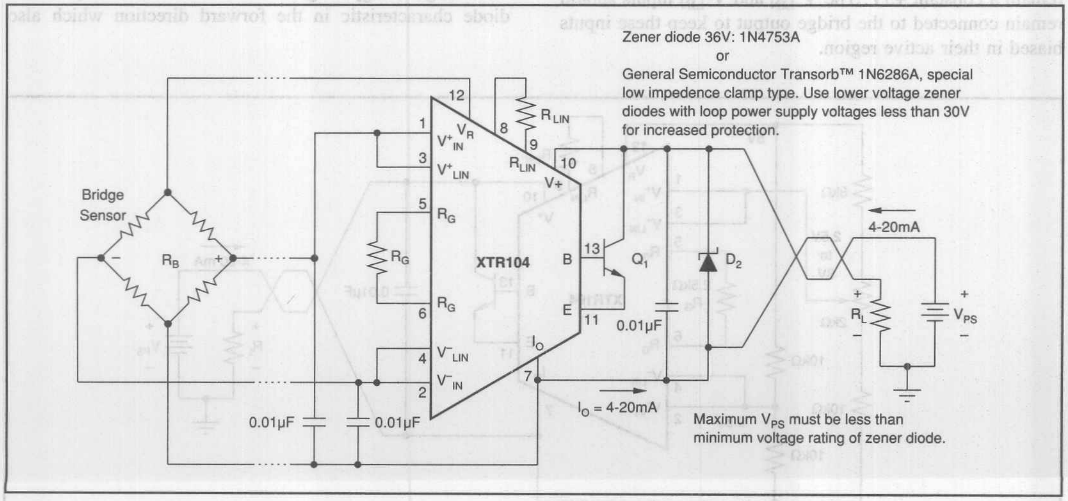


FIGURE 7. Over-Voltage Surge Protection.

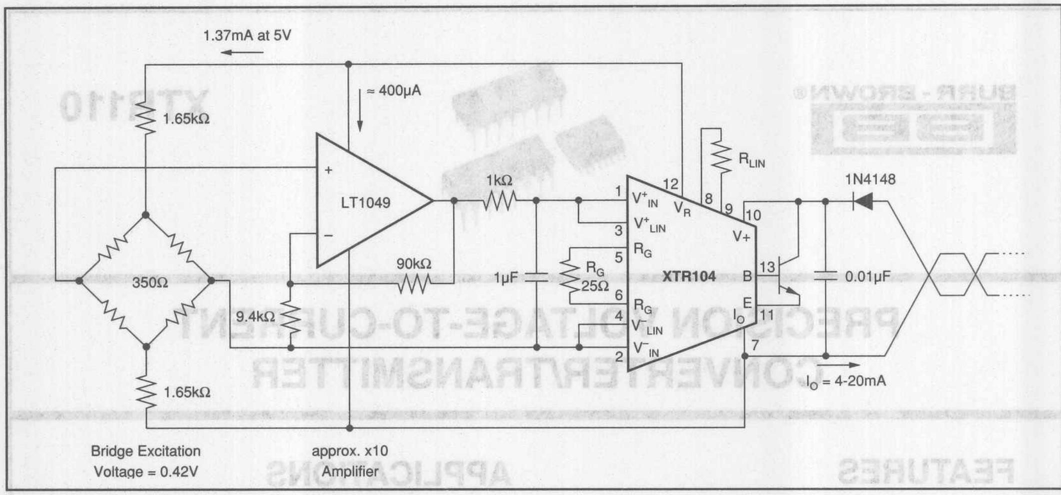


FIGURE 8. 350Ω Bridge With X10 Preamplifier.

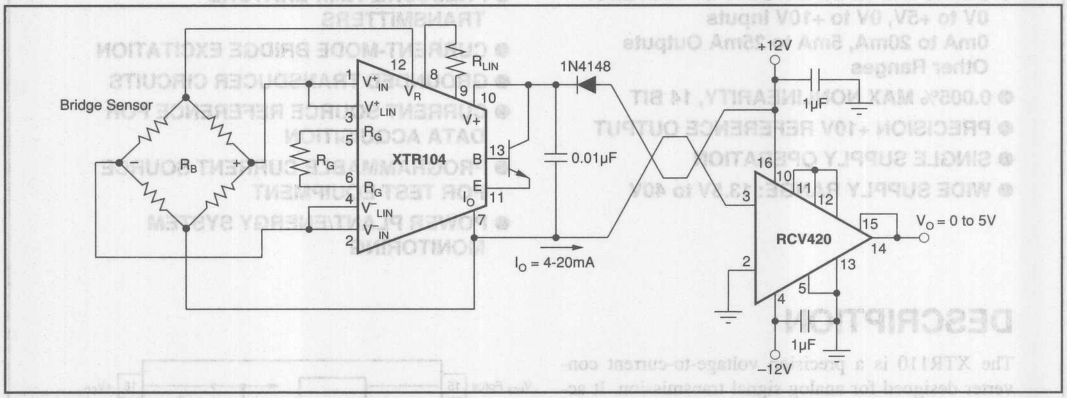


FIGURE 9. ±12V-Powered Transmitter/Receiver Loop.

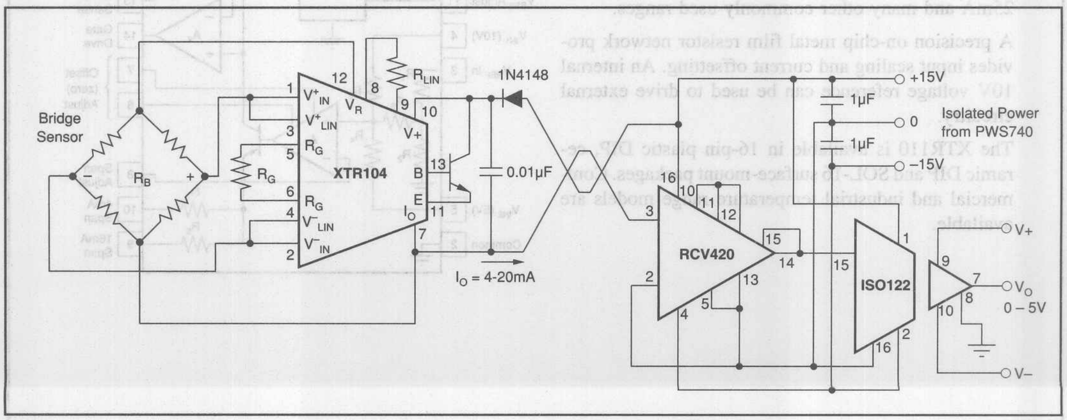
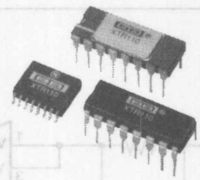


FIGURE 10. Isolated Transmitter/Receiver Loop.

BURR - BROWN®



XTR110

PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
  0V to +5V, 0V to +10V Inputs
  0mA to 20mA, 5mA to 25mA Outputs
  Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE: 13.5V to 40V

APPLICATIONS

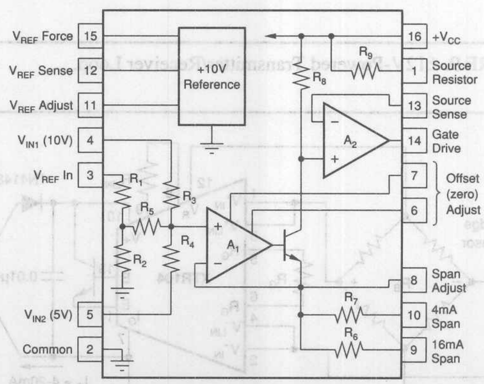
- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR110 is a precision voltage-to-current converter designed for analog signal transmission. It accepts inputs of 0 to 5V or 0 to 10V and can be connected for outputs of 4 to 20mA, 0 to 20mA, 5 to 25mA and many other commonly used ranges.

A precision on-chip metal film resistor network provides input scaling and current offsetting. An internal 10V voltage reference can be used to drive external circuitry.

The XTR110 is available in 16-pin plastic DIP, ceramic DIP and SOL-16 surface-mount packages. Commercial and industrial temperature range models are available.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC} = +24V and R_L = 250Ω**, unless otherwise specified.

PARAMETER	CONDITIONS	XTR110AG, KP, KU MIN	TYP	MAX	XTR110BG MIN	TYP	MAX	UNITS
TRANSMITTER								
Transfer Function			$I_O = 10\,[(V_{REF}\,In/16) + (V_{IN1}/4) + (V_{IN2}/2)]\,/R_{SPAN}$					
Input Range: V_{IN1} (5)	Specified Performance	0		+10	*		*	V
V_{IN2}	Specified Performance	0		+5	*		*	V
Current, I_O	Specified Performance(1)	4		20	*		*	mA
	Derated Performance(1)	0		40	*		*	mA
Nonlinearity	16mA/20mA Span(2)		0.01	0.025		0.002	0.005	% of Span
Offset Current, I_{OS}	I_O = 4mA(1)							
Initial	(1)		0.2	0.4		0.02	0.1	% of Span
vs Temperature	(1)		0.0003	0.005		*	0.003	% of Span/°C
vs Supply, V_{CC}	(1)		0.0005	0.005		*	*	% of Span/V
Span Error	I_O = 20mA							
Initial	(1)		0.3	0.6		0.05	0.2	% of Span
vs Temperature	(1)		0.0025	0.005		0.0009	0.003	% of Span/°C
vs Supply, V_{CC}	(1)		0.003	0.005		*	*	% of Span/V
Output Resistance	From Drain of FET (Q_{EXT})(3)		10×10^9			*		Ω
Input Resistance	V_{IN1}		27			*		kΩ
	V_{IN2}		22			*		kΩ
	V_{REF} In		19			*		kΩ
Dynamic Response								
Settling Time	To 0.1% of Span		15			*		µs
	To 0.01% of Span		20			*		µs
Slew Rate			1.3			*		mA/µs
VOLTAGE REFERENCE								
Output Voltage		+9.95	+10	+10.05	+9.98	*	+10.02	V
vs Temperature			35	50		15	30	ppm/°C
vs Supply, V_{CC}	Line Regulation		0.0002	0.005		*	*	%/V
vs Output Current	Load Regulation		0.0005	0.01		*	*	%/mA
vs Time			100			*		ppm/1k hrs
Trim Range		–0.100		+0.25	*		*	V
Output Current	Specified Performance	10			*			mA
POWER SUPPLY								
Input Voltage, V_{CC}		+13.5		+40	*		*	V
Quiescent Current	Excluding I_O		3	4.5		*	*	mA
TEMPERATURE RANGE								
Specification: AG, BG		–40		+85	*		*	°C
KP, KU		0		+70				°C
Operating: AG, BG		–55		+125	*		*	°C
KP, KU		–25		+85				°C

* Specifications same as AG/KP grades. ** Specifications apply to the range of R_L shown in Typical Performance Curves.

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by $(+V_{CC} - 2V) + V_{DS}$ required for linear operation of the FET. (4) For V_{REF} adjustment circuit see Figure 3. (5) For extended I_{REF} drive circuit see Figure 4. (5) Unit may be damaged. See section, "Input Voltage Range".

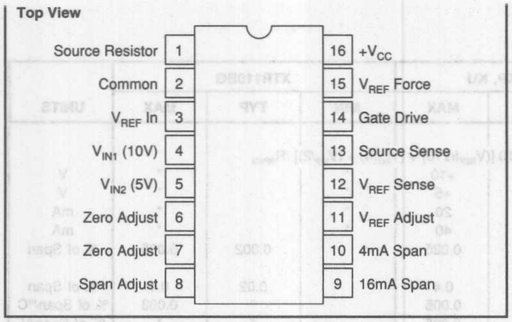
ABSOLUTE MAXIMUM RATINGS

Power Supply, $+V_{CC}$ 40V
Input Voltage, V_{IN1}, V_{IN2}, $V_{REF\ IN}$ .... $+V_{CC}$
See text regarding safe negative input voltage range.
Storage Temperature Range: A, B .... –55°C to +125°C
K, U .... –40°C to +85°C
Lead Temperature
(soldering, 10s) G, P .... 300°C
(wave soldering, 3s) U .... 260°C
Output Short-Circuit Duration, Gate Drive
and V_{REF} Force .... Continuous to common and $+V_{CC}$
Output Current Using Internal 50Ω Resistor 40mA

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.



MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
XTR110AG	16-Pin Ceramic DIP	109
XTR110BG	16-Pin Ceramic DIP	109
XTR110KP	16-Pin Plastic DIP	180
XTR110KU	SOL-16 Surface-Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

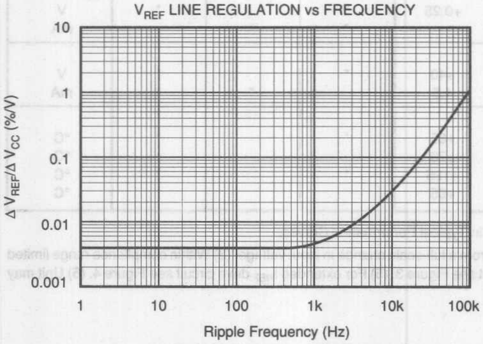
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
XTR110AG	16-Pin Ceramic DIP	–40°C to +85°C
XTR110BG	16-Pin Ceramic DIP	–40°C to +85°C
XTR110KP	16-Pin Plastic DIP	0°C to +70°C
XTR110KU	SOL-16 Surface-Mount	0°C to +70°C

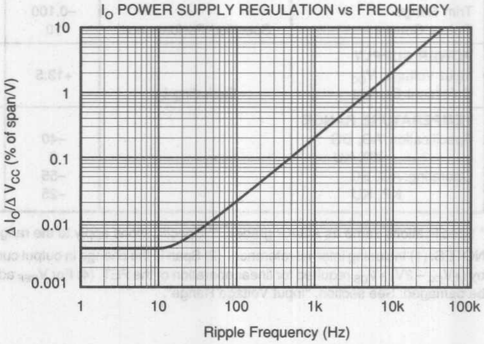
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = 24VDC, R_L = 250Ω, unless otherwise noted.

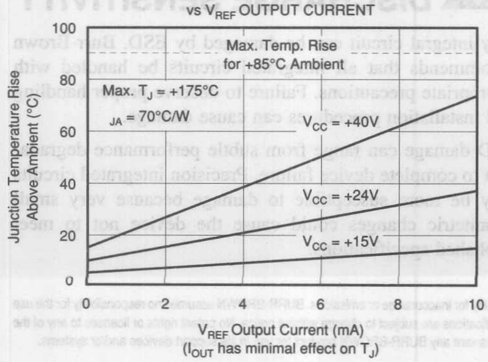
V_{REF} LINE REGULATION vs FREQUENCY



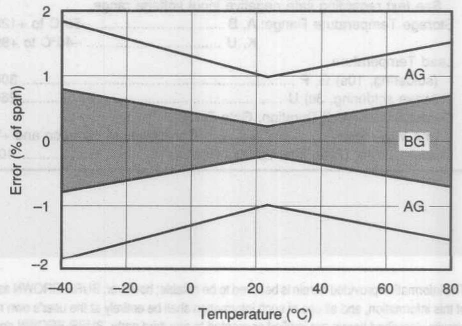
I_O POWER SUPPLY REGULATION vs FREQUENCY



JUNCTION TEMPERATURE RISE vs V_{REF} OUTPUT CURRENT



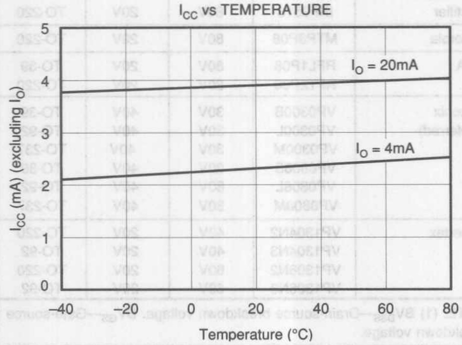
TOTAL OUTPUT ERROR vs TEMPERATURE



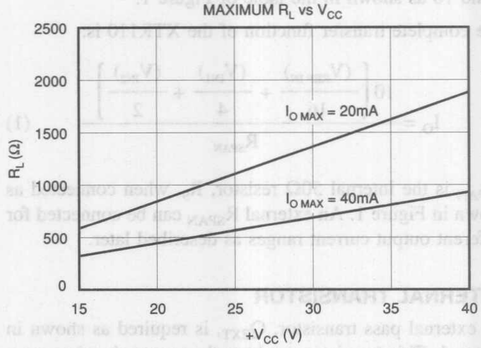
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_{CC} = 24VDC$, $R_L = 250\Omega$, unless otherwise noted.

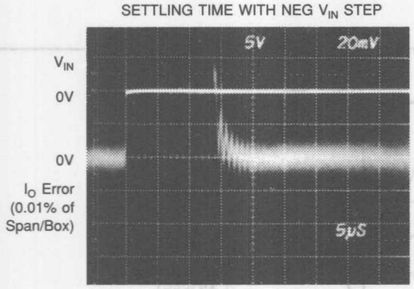
I_{CC} vs TEMPERATURE



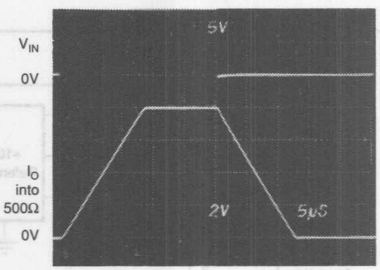
MAXIMUM R_L vs V_{CC}



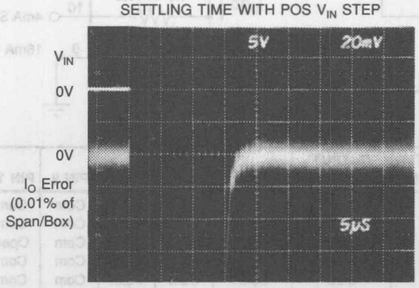
SETTLING TIME WITH NEG V_{IN} STEP



PULSE RESPONSE



SETTLING TIME WITH POS V_{IN} STEP



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for 0 to 10V input and 4 to 20mA output. Other input voltage and output current ranges require changes in connections of pins 3, 4, 5, 9 and 10 as shown in the table of Figure 1.

The complete transfer function of the XTR110 is:

$$I_O = \frac{10\left[\dfrac{(V_{REF\ IN})}{16} + \dfrac{(V_{IN1})}{4} + \dfrac{(V_{IN2})}{2}\right]}{R_{SPAN}} \qquad (1)$$

R_{SPAN} is the internal 50Ω resistor, R_9, when connected as shown in Figure 1. An external R_{SPAN} can be connected for different output current ranges as described later.

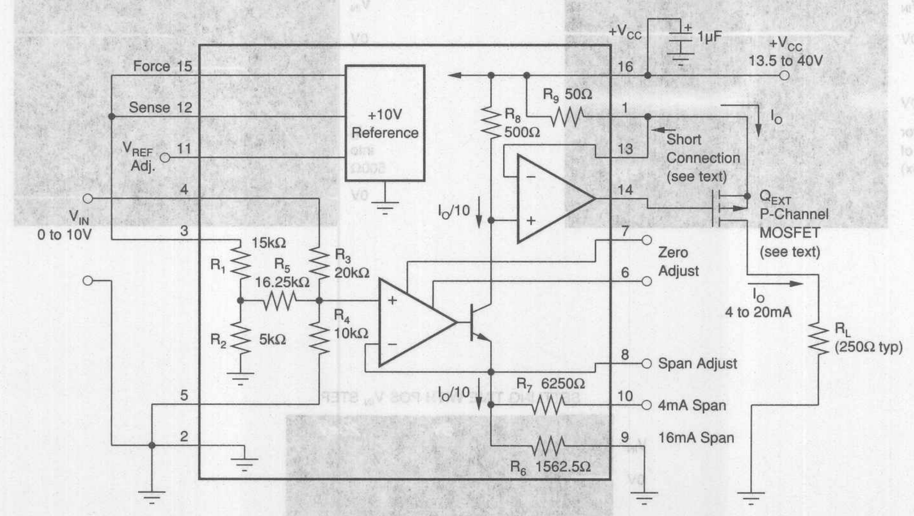
EXTERNAL TRANSISTOR

An external pass transistor, Q_{EXT}, is required as shown in Figure 1. This transistor conducts the output signal current. A P-channel MOSFET transistor is recommended. It must have a voltage rating equal or greater than the maximum power supply voltage. Various recommended types are shown in Table I.

MANUFACTURER	PART NO.	BV_{DSS}(1)	BV_{GS}(1)	PACKAGE
Ferranti	ZVP1304A	40V	20V	TO-92
	ZVP1304B	40V	20V	TO-39
	ZVP1306A	60V	20V	TO-92
	ZVP1306B	60V	20V	TO-39
International Rectifier	IRF9513	60V	20V	TO-220
Motorola	MTP8P08	80V	20V	TO-220
RCA	RFL1P08	80V	20V	TO-39
	RFT2P08	80V	20V	TO-220
Siliconix (preferred)	VP0300B	30V	40V	TO-39
	VP0300L	30V	40V	TO-92
	VP0300M	30V	40V	TO-237
	VP0808B	80V	40V	TO-39
	VP0808L	80V	40V	TO-92
	VP0808M	80V	40V	TO-237
Supertex	VP1304N2	40V	20V	TO-220
	VP1304N3	40V	20V	TO-92
	VP1306N2	60V	20V	TO-220
	VP1306N3	60V	20V	TO-92

NOTE: (1) BV_{DSS}—Drain-source breakdown voltage. BV_{GS}—Gate-source breakdown voltage.

TABLE I. Available P-Channel MOSFETs.



INPUT RANGE (V)	OUTPUT RANGE (mA)	PIN 3	PIN 4	PIN 5	PIN 9	PIN 10
0-10	0-20	Com	Input	Com	Com	Com
2-10	4-20	Com	Input	Com	Com	Com
0-10	4-20	+10V Ref	Input	Com	Com	Open
0-10	5-25	+10V Ref	Input	Com	Com	Com
0-5	0-20	Com	Com	Input	Com	Com
1-5	4-20	Com	Com	Input	Com	Com
0-5	4-20	+10V Ref	Com	Input	Com	Open
0-5	5-25	+10V Ref	Com	Input	Com	Com

FIGURE 1. Basic Circuit Connection.

If the supply voltage, $+V_{CC}$, exceeds the gate-to-source breakdown voltage of Q_{EXT}, and the output connection (drain of Q_{EXT}) is broken, Q_{EXT} could fail. If the gate-to-source breakdown voltage is lower than $+V_{CC}$, Q_{EXT} can be protected with a 12V zener diode connected from gate to source.

Two PNP discrete transistors (Darlington-connected) can be used for Q_{EXT}—see Figure 2. Note that an additional capacitor is required for stability. Integrated Darlington transistors are not recommended because their internal base-emitter resistors cause excessive error.

TRANSISTOR DISSIPATION

Maximum power dissipation of Q_{EXT} depends on the power supply voltage and full-scale output current. Assuming that the load resistance is low, the power dissipated by Q_{EXT} is:

$$P_{MAX} = (+V_{CC})\ I_{FS} \qquad (2)$$

The transistor type and heat sinking must be chosen according to the maximum power dissipation to prevent overheating. See Table II for general recommendations.

PACKAGE TYPE	ALLOWABLE POWER DISSIPATION
TO-92	Lowest: Use minimum supply and at +25°C.
TO-237	Acceptable: Trade-off supply and temperature.
TO-39	Good: Adequate for majority of designs.
TO-220	Excellent: For prolonged maximum stress.
TO-3	Use if hermetic package is required.

TABLE II. External Transistor Package Type and Dissipation.

INPUT VOLTAGE RANGE

The internal op amp A_1 can be damaged if its non-inverting input (an internal node) is pulled more than 0.5V below common (0V). This could occur if input pins 3, 4 or 5 were driven with an op amp whose output could swing negative under abnormal conditions. The voltage at the input of A_1 is:

$$V_{A1} = \frac{(V_{REF\ IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2} \qquad (3)$$

This voltage should not be allowed to go more negative than –0.5V. If necessary, a clamp diode can be connected from the negative-going input to common to clamp the input voltage.

COMMON (Ground)

Careful attention should be directed toward proper connection of the common (grounds). All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the I_{OUT} return. It can be returned to any point where it will not modulate the common at pin 2.

VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 ($V_{REF\ SENSE}$). To preserve accuracy, any load including pin

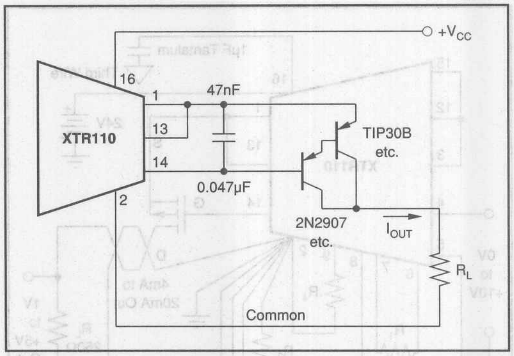


FIGURE 2. Q_{EXT} Using PNP Transistors.

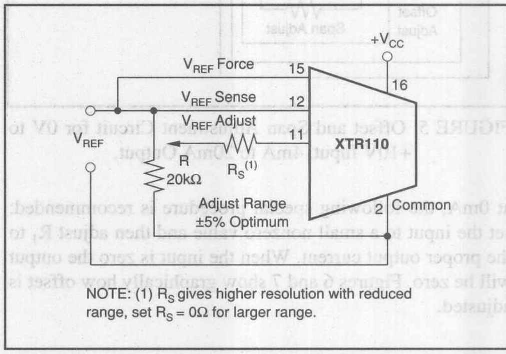


FIGURE 3. Optional Adjustment of Reference Voltage.

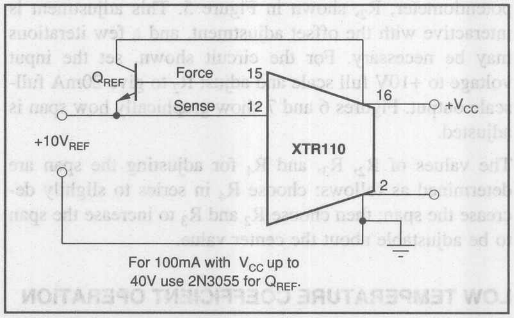


FIGURE 4. Increasing Reference Current Drive.

3 should be connected to this point. The circuit in Figure 3 shows adjustment of the voltage reference.

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 4.

OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer, R_1, shown in Figure 5. Set the input voltage to zero and then adjust R_1 to give 4mA at the output. For spans starting

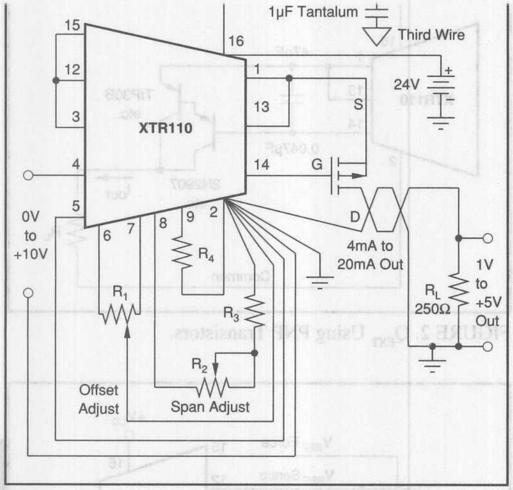


FIGURE 5. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust R_1 to the proper output current. When the input is zero the output will be zero. Figures 6 and 7 show graphically how offset is adjusted.

SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer, R_2, shown in Figure 5. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and adjust R_2 to give 20mA full-scale output. Figures 6 and 7 show graphically how span is adjusted.

The values of R_2, R_3, and R_4 for adjusting the span are determined as follows: choose R_4 in series to slightly decrease the span; then choose R_2 and R_3 to increase the span to be adjustable about the center value.

LOW TEMPERATURE COEFFICIENT OPERATION

Although the precision resistors in the XTR110 track within 1ppm/°C, the output current depends upon the absolute temperature coefficient (TC) of any one of the resistors, R_6, R_7, R_8, and R_9. Since the absolute TC of the output current can have 20ppm/°C, maximum, the TC of the output current can have 20ppm/°C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors (R_6 or R_7) or for the source resistor (R_9) but not both.

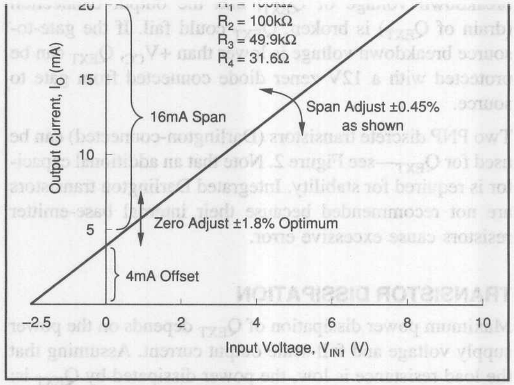


FIGURE 6. Zero and Span of 0V to +10V Input, 4mA to 20mA Output Configuration (see Figure 5).

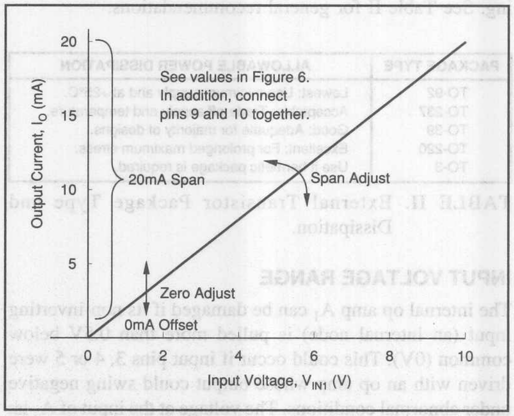


FIGURE 7. Zero and Span of 0V to +10V_{IN}, 0mA to 20mA Output Configuration (see Figure 5).

EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor (R_9) may be replaced by an external resistor connected between pins 13 and 16.

Its value can be calculated as follows:

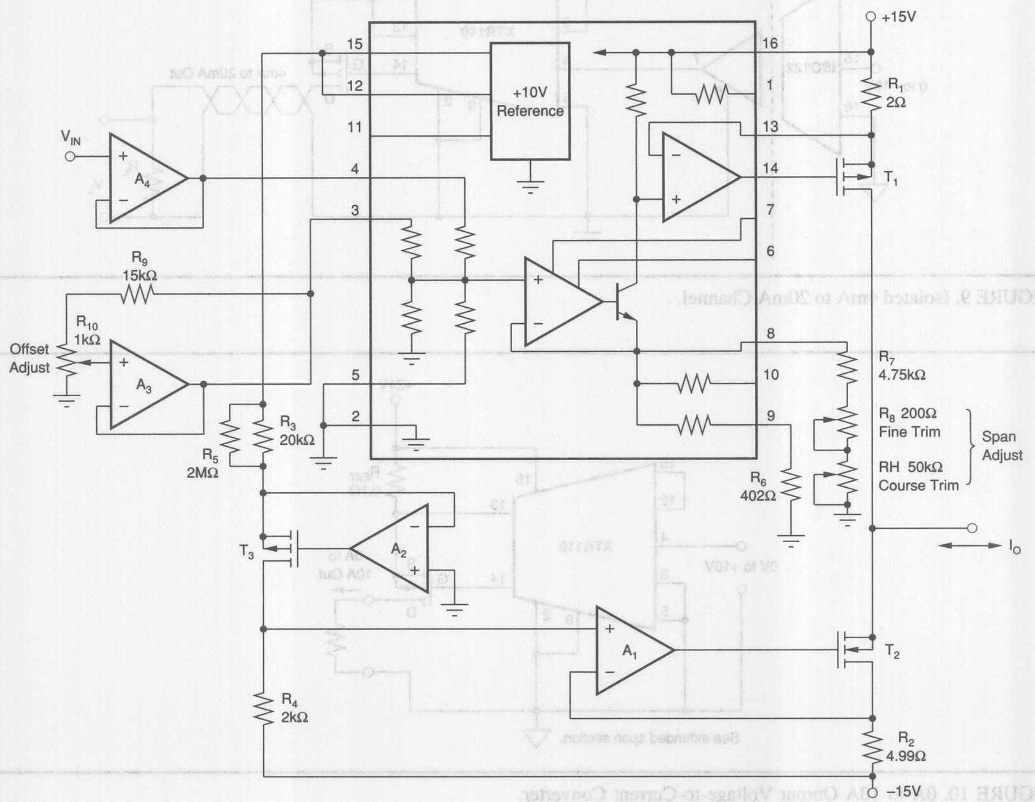
$$R_{EXT} = R_9\ (Span_{OLD}/Span_{NEW})$$

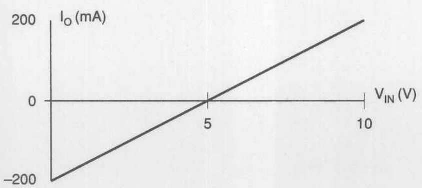
Since the internal thin-film resistors have a 20% absolute value tolerance, measure R_9 before determining the final value of R_{EXT}. Self-heating of R_{EXT} can cause nonlinearity. Therefore, choose one with a low TC and adequate power rating. See Figure 10 for application.

TYPICAL APPLICATIONS

The XTR110 is ideal for a variety of applications requiring high noise immunity current-mode signal transmission. The precision +10V reference can be used to excite bridges and transducers. Selectable ranges make it very useful as a precision programmable current source. The compact design and low price of the XTR110 allow versatility with a minimum of external components and design engineering expense.

Figures 8 through 10 show typical applications of the XTR110.





R_1, R_2: Low TC resistors to dissipate 0.32W continuous power. For other current ranges, scale both resistors proportionately.
R_8, R_{10}, R_{11}: 10-turn trimpots for greatest sensitivity.
R_6, R_7: Low TC resistors.
A_1 - A_4: 1/4 LM324 (powered by ±15V).
T_1: International Rectifier IR9513[(1)].
T_2: International Rectifier IR513[(1)].
T_3: International Rectifier IRFF9113[(1)].

NOTE: (1) Or other adequate power rating MOS transistor.

FIGURE 8. ±200mA Current Pump.

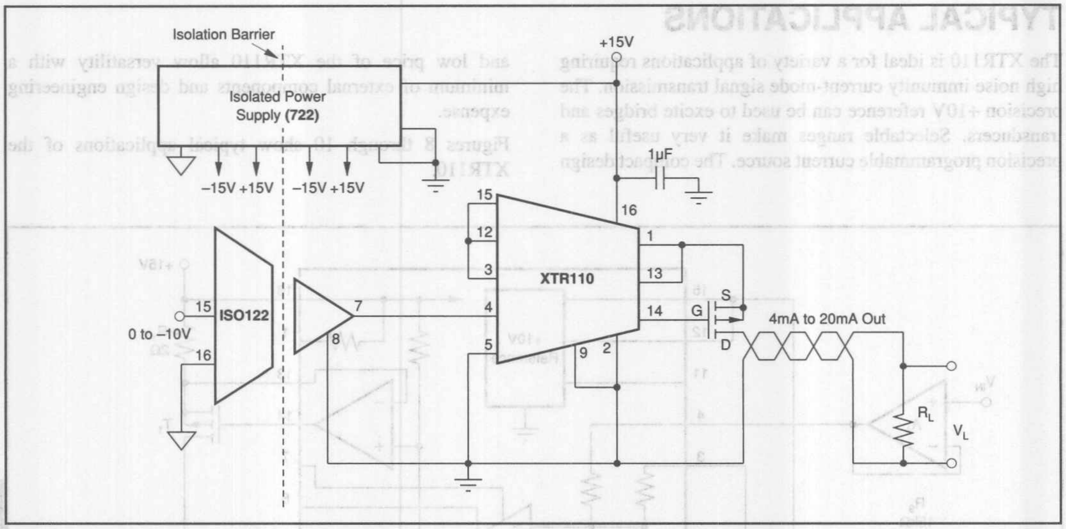


FIGURE 9. Isolated 4mA to 20mA Channel.

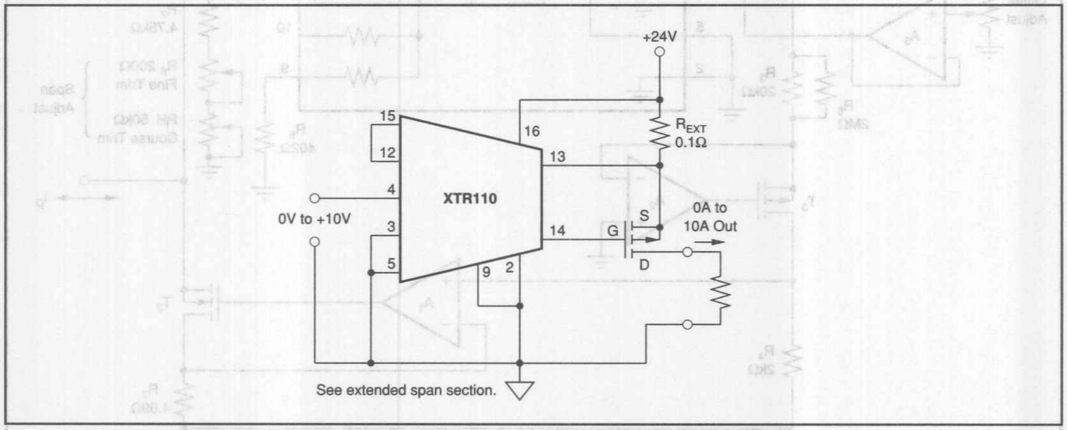


FIGURE 10. 0A to 10A Output Voltage-to-Current Converter.

BURR - BROWN®

XTR501

HIGH CURRENT BRIDGE DRIVER and 4-20mA Transmitter

FEATURES

- SENSOR EXCITATION OF 1W
- VARIABLE EXCITATION VOLTAGE: 1.5V to 5.0V
- SINGLE SUPPLY: 11.4V to 30VDC
- INRUSH CURRENT LIMITING
- 4-20mA TRANSMITTER

APPLICATIONS

- GAS DETECTION SENSORS
- PELLISTOR CATALYTIC DETECTORS
- STRAIN GAGES
- HIGH CURRENT BRIDGES
- LOAD CELLS
- HOT-WIRE ANEMOMETERS

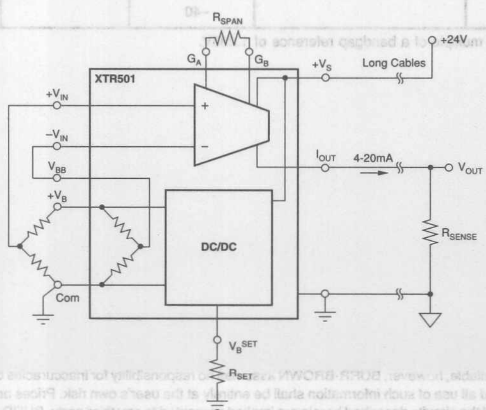
DESCRIPTION

The XTR501 contains a high efficiency DC/DC converter and 4-20mA three wire current transmitter. It provides regulated bridge excitation, optional half bridge, differential inputs and current transmitter necessary for the excitation and signal conditioning of low impedance bridge sensors and high integrity signal transmission.

The DC/DC converter is capable of supplying 1W into a regulated bridge voltage of 1.5V to 5.0V from a supply of 11.4V to 30V. The combination of a low startup current and high efficiency current step-up allows for a combined supply line resistance of up to 100Ω when exciting low impedance sensors.

The instrumentation amplifier of the current transmitter can be used over a wide range of gains, accommodating a variety of input signals and sensors.

The XTR501 is particularly suited to excitation of high current/low impedance sensors used in bridge applications allowing the use of lighter cabling leading to considerable savings on cabling costs.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

$T_A = +25°C$, $V_S = 24V$, $V_{BRIDGE} = 2V$, $I_{LOAD} = 300mA$ unless otherwise specified.

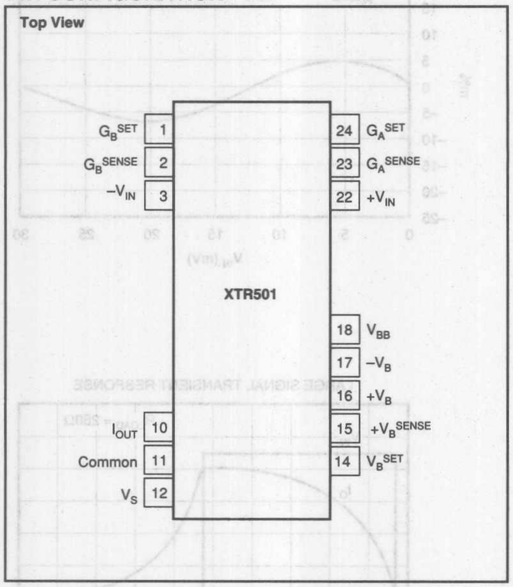
		XTR501			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
INSTRUMENTATION AMPLIFIER/CURRENT TRANSMITTER					
SIGNAL OUTPUT					
Output Current Equation	R_G in Ω, V_{IN} in V		$I_O = 0.004 + 0.016\ [(1 + 50k\Omega/R_G)/4.94]\ V_{IN}$		A
Output Current	Linear Operating Range	4		20	mA
Over-scale Limit		25	27		mA
Under-scale Limit			0		mA
ZERO					
Output Current			4		mA
Offset Error			±50	±100	µA
vs Temperature			0.2		µA/°C
vs Supply Voltage	V_S = 11.4V to 30V		0.5	2	µA/V
SPAN					
Span Equation	R_G in Ω, V_{IN} in V		$Span = 0.016[(1 + 50k\Omega/R_G)/4.94]$		A/V
Untrimmed Error	G = 1		±0.2	±2.5	%
	G = 250		±1.5	±10	%
vs Temperature			50		ppm/°C
Nonlinearity	G = 1, I_O = 4mA to 20mA			±0.025	%
INPUT					
Common-Mode Range		0		4.94[1]	V
Offset Voltage			16		mV
vs Temperature			50		µV/°C
vs Supply Voltage			75		dB
Common-Mode Rejection			85		dB
Impedance; Differential, Common-Mode			$10^{10} \parallel 6$		Ω ‖ pF
DC/DC CONVERTER					
BRIDGE EXCITATION VOLTAGE SOURCE					
Output Voltage		1.5		5	V
vs Temperature	V_{IN} = 0V, G= 1		200		ppm/°C
vs Long Term Stability			100		ppm/1000hrs
Output Power				1	W
Line Voltage Regulation	V_S = 11.4V to 30.0V		0.25		%
Load Voltage Regulation	Load Current 160mA to 340mA Load Voltage 2V		0.25		%
Output Voltage Ripple	Load Current 300mA Load Voltage 2V		150		mV
Output Voltage Ripple Frequency			100		kHz
Output Short-Circuit Current	Limited Duration		2.6		A
Input Current	Output Short-Circuit		150		mA
POWER SUPPLY					
Supply Voltage, V_S		11.4	24	30	V
Supply Current			See Typical Curve		
TEMPERATURE					
Operating		–40		+70	°C
Storage		–40		+85	°C

NOTE: (1) Common-Mode Range is based on a multiple of a bandgap reference of 1.235V.

Input Voltage	10V
Output Power	1W
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	–40°C to +85°C

MODEL	PACKAGE	TEMPERATURE RANGE
XTR501	24-Pin Plastic Module	–40°C to +70°C

PIN CONFIGURATION



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
XTR501	24-Pin Plastic Module	902

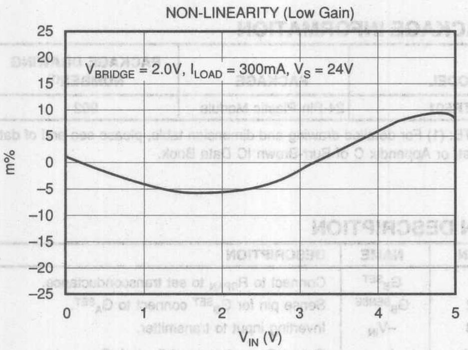
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

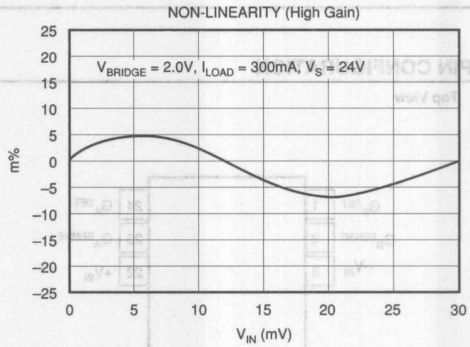
PIN DESCRIPTION

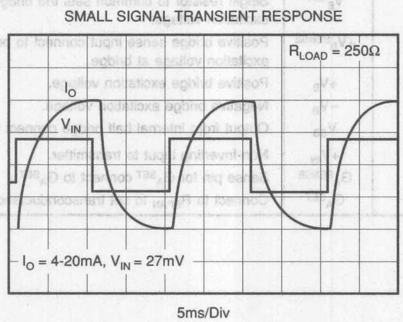
PIN	NAME	DESCRIPTION
1	G_B^{SET}	Connect to R_{SPAN} to set transconductance.
2	G_B^{SENSE}	Sense pin for G_B^{SET} connect to G_A^{SET}.
3	$-V_{IN}$	Inverting input to transmitter.
10	I_{OUT}	Output Current connect through R_{SENSE} to common.
11	Common	Supply return for sense and V_B connectors.
12	V_S	Supply to XTR501 +11.4V to 30.0V.
14	V_B^{SET}	Single resistor to common sets the bridge excitation voltage.
15	$+V_B^{SENSE}$	Positive bridge sense input connect to positive excitation voltage at bridge.
16	$+V_B$	Positive bridge excitation voltage.
17	$-V_B$	Negative bridge excitation voltage.
18	V_{BB}	Output from internal half bridge connect to $-V_{IN}$.
22	$+V_{IN}$	Non-Inverting input to transmitter.
23	G_A^{SENSE}	Sense pin for G_A^{SET} connect to G_A^{SET}.
24	G_A^{SET}	Connect to R_{SPAN} to set transconductance.

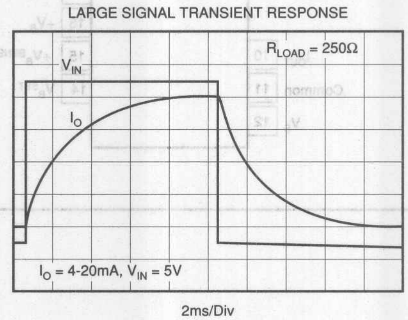
TYPICAL PERFORMANCE CURVES

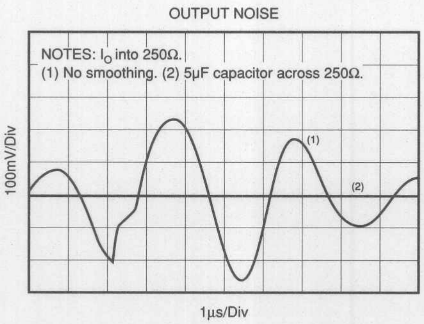
$T_A = +25°C$, $V_S = 24V$, $V_{BRIDGE} = 2V$, $I_{LOAD} = 300mA$ unless otherwise specified.

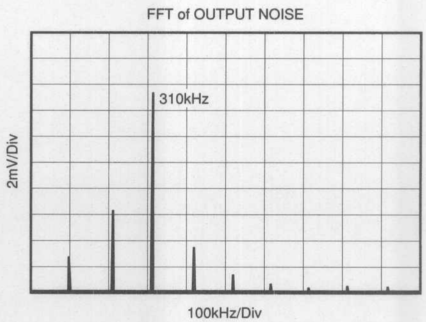






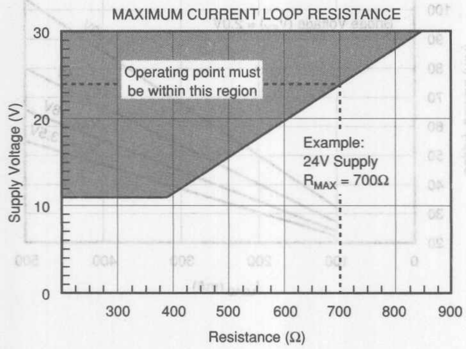


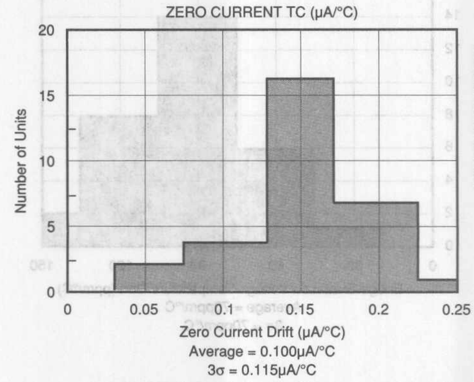


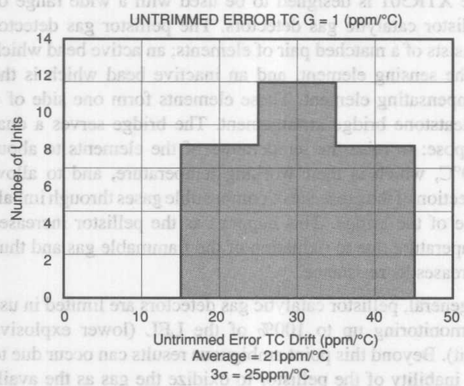


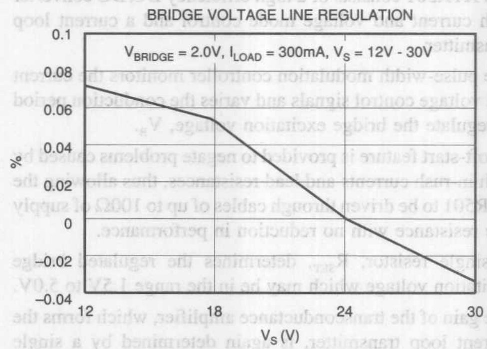
TYPICAL PERFORMANCE CURVES (CONT)

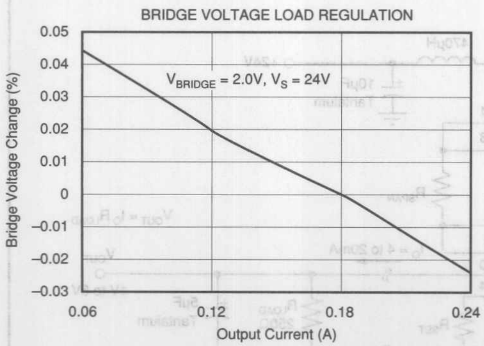
$T_A = +25°C$, $V_S = 24V$, $V_{BRIDGE} = 2V$, $I_{LOAD} = 300mA$ unless otherwise specified.

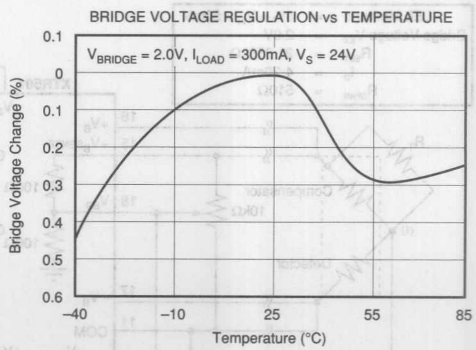












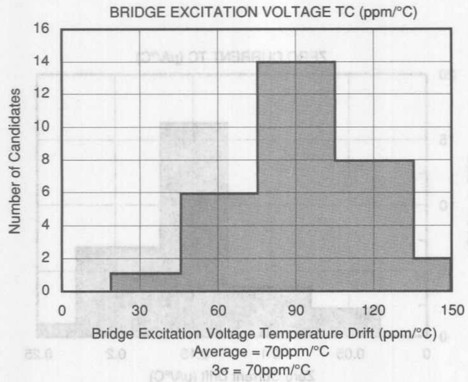
XTR501

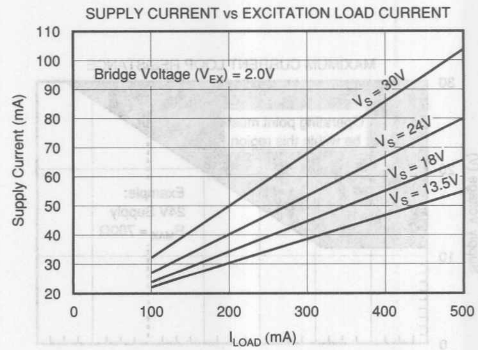
4

INSTRUMENTATION AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = 24V$, $V_{BRIDGE} = 2V$, $I_{LOAD} = 300mA$ unless otherwise specified.





METHOD OF OPERATION

The XTR501 consists of a high efficiency DC/DC converter with current and voltage mode control and a current loop transmitter.

The pulse-width modulation controller monitors the current and voltage control signals and varies the conduction period to regulate the bridge excitation voltage, V_B.

A soft-start feature is provided to negate problems caused by high in-rush currents and lead resistances, thus allowing the XTR501 to be driven through cables of up to 100Ω of supply line resistance with no reduction in performance.

A single resistor, R_{SET}, determines the regulated bridge excitation voltage which may be in the range 1.5V to 5.0V.

The gain of the transconductance amplifier, which forms the current loop transmitter, is again determined by a single resistor R_{SPAN} and allows input voltages from 25mV to drive the 4-20mA current loop.

APPLICATIONS

The XTR501 is designed to be used with a wide range of pellistor catalytic gas detectors. The pellistor gas detector consists of a matched pair of elements; an active bead which is the sensing element, and an inactive bead which is the compensating element. These elements form one side of a Wheatstone bridge arrangement. The bridge serves a dual purpose: to raise the temperature of the elements to about 500°C, which is their working temperature, and to allow detection of the presence of combustible gases through imbalance of the bridge. This happens as the pellistor increases temperature due to oxidation of the flammable gas and thus increases its resistance.

In general, pellistor catalytic gas detectors are limited in use to monitoring up to 100% of the LEL (lower explosive limit). Beyond this point ambiguous results can occur due to the inability of the pellistor to oxidize the gas as the available oxygen decreases (see Figure 3).

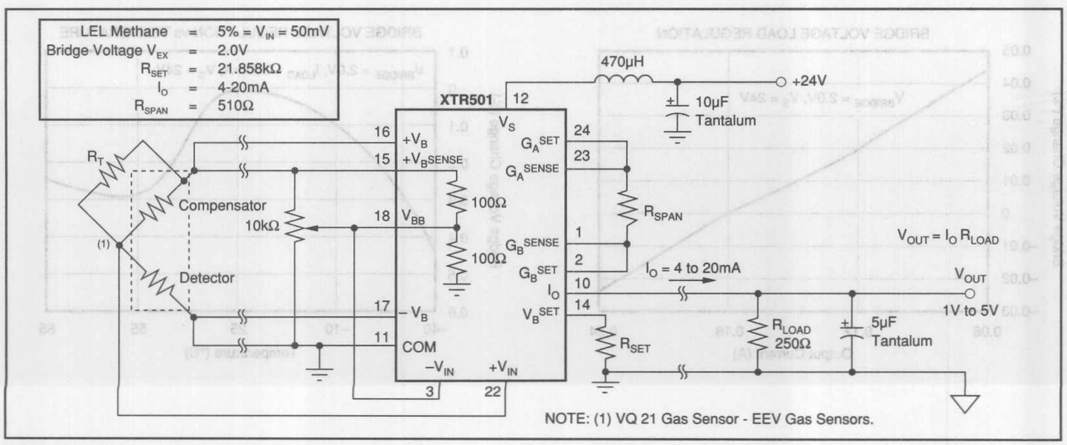


FIGURE 1. Basic Connection

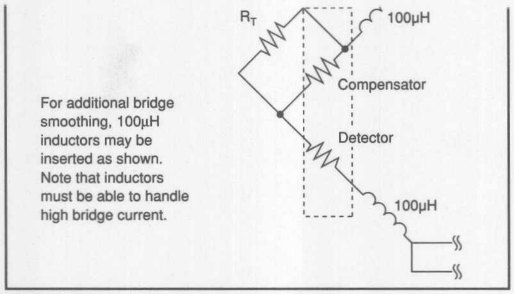


FIGURE 2. Bridge Smoothing.

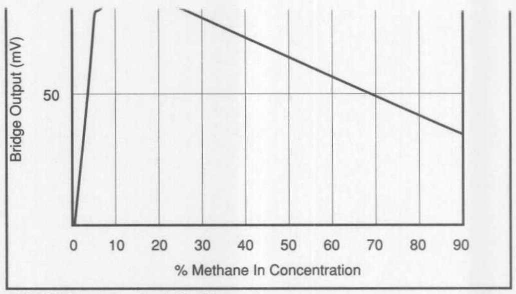


FIGURE 3. Typical Pellistor Response.

An interesting feature of pellistor elements, and those tested in the applications, is that they create a similar bridge output at LEL for almost all hydrocarbons. This feature allows a comparative measurement to be made of one gas when an instrument has been calibrated for another.

e.g. Instrument calibrated for Methane (K=112) measuring Hydrogen (K=85.8).

Actual % of LEL will be 1.31 x meter reading. (112/85.8).

This is an approximation and it is recommended that for exact conversions the instrument should be calibrated using the relevant gases.

Tables of these constants can be sourced through the manufacturers of gas sensing products.

An example of the XTR501 used with a pellistor catalytic gas detector is shown in Figure 1.

To Calculate R_{SET}

See Figure 4. Point (a) will be maintained at 1.235V.

$$\frac{V_B - 1.235}{10k\Omega} = \frac{1.235\,(50k\Omega + R_{SET})}{R_{SET}\;50k\Omega}$$

$$\frac{50k\Omega\,(V_B - 1.235)}{(10k\Omega)\,(1.235)} = \frac{50k\Omega + R_{SET}}{R_{SET}}$$

$$= 1 + \frac{50k\Omega}{R_{SET}}$$

$$\frac{5\,(V_B - 1.235)}{1.235} - 1 = \frac{50k\Omega}{R_{SET}}$$

$$R_{SET} = \frac{(50k\Omega)\,(1.235)}{5\,(V_B - 1.235) - 1.235}$$

Example:

V_B	R_{SET} Calculated
1.5	Open
2.0	21.858kΩ
3.0	7.891kΩ
4.0	4.815kΩ
5.0	3.464kΩ

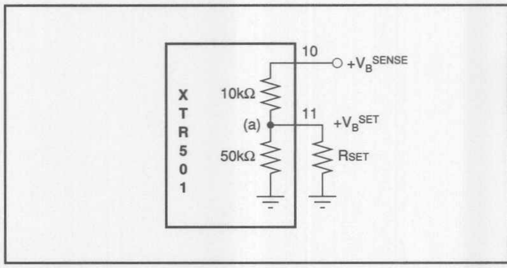


FIGURE 4. Internal Circuit $+V_B^{SET}$.

To Calculate R_{SPAN}

$$I_O = 0.004 + 0.016\left(\frac{1 + 50k\Omega / R_{SPAN}}{4.94}\right)V_{IN}$$

For V_{IN} = 10mV and I_O = 20mA

$$0.02 = 0.004 + 0.016\left(\frac{1 + 50k\Omega / R_{SPAN}}{4.94}\right)0.01$$

$$\frac{0.016}{(0.016)\,(0.01)} = \frac{1 + (50k\Omega / R_{SPAN})}{4.94}$$

$$494 = 1 + 50k\Omega / R_{SPAN}$$

$$R_{SPAN} = \frac{50k\Omega}{493}$$

$$= 101.4$$

i.e

$$\frac{4.94}{V_{IN}} = 1 + \frac{50k\Omega}{R_{SPAN}}$$

$$R_{SPAN} = \frac{50k\Omega}{\frac{4.94}{V_{IN}} - 1}$$

5 Isolation Products

Isolation amplifiers can be used to amplify and measure low level signals in the presence of high common-mode voltages, breakground loops and/or eliminate source ground connections, provide an interface between medical patient monitoring equipment, and provide isolation protection to electronic instruments/equipment.

Our isolation amplifiers feature three different technologies—transformer isolation, capacitor isolation, and opto-isolation. The following selection guides will help you determine the performance and functionality that best fit your requirements.

Choose from the industry's most complete line of isolation solutions including:

ISO130—Provides high isolation-mode rejection, wide bandwidth and low cost in 8-pin DIP and surface-mount packages.

ISO122—Low cost, 1500V isolation available in 16-pin plastic DIP and 28-pin SOIC packages.

ISO120—Industry's first total hermetic isolation amplifier with 0.01% linearity. It is synchronous and offered with specifications over the military temperature range.

ISO103—Unity-gain isolation amp combined with an internal isolated DC/DC converter in a space-saving, 24-pin ceramic DIP.

ISO212—Low cost, uncommitted input amplifier, differential output with an internal isolated DC/DC converter.

ISO100—Versatile, adjustable gain optically-coupled amplifier in a 18-pin DIP.

3656—Transformer-coupled amplifier with an internal isolated DC/DC converter that offers three port isolation.

ISO150—High speed, low cost dual digital transceiver that is TTL- and CMOS-compatible, available in a 24-pin plastic DIP and in a 28-lead SOIC.

ISO164 and ISO174—New, precision, input isolated programmable gain amplifiers. Capable of both fixed and variable gains, they allow flexibility of input stage for use in applications such as IPC and data acquisition systems.

ISO165 and ISO175—New, precision, input isolated instrumentation amplifiers that offer excellent accuracy. A single resistor sets any gain from 1 to 10,000. Available in a 24-pin plastic "skinny" DIP.

ISO250 Family—This new family of precision, 3-port isolated amplifiers consists of a buffer (ISO253), programmable gain (ISO254), instrumentation (ISO255), and operational (ISO256) amplifiers aimed at industrial process control applications.

ISO485 Family—A differential isolated bus transceiver that uses capacitively-coupled isolation technology to achieve high speed and low cost bus isolation. It is RS-485/RS-422 compatible.

ISO800 Family—A new series of 12- and 16-bit isolated sampling A/D converters. Use of state-of-the-art CMOS architectures and high voltage capacitors transfer data digitally across the isolation barrier thereby eliminating signal degradation.

The selection guide also includes our versatile line of isolated DC/DC converters.

ISOLATION PRODUCTS

ANALOG AMPLIFIERS

Without Power
Rated Continuous(1) (Vrms)

- ISO100 (750)
- ISO130 (750)
- ISO102 (1.5k)
- ISO120 (1.5k)
- ISO122 (1.5k)
- **ISO164 (1.5k)**
- **ISO165 (1.5k)**
- **ISO166 (1.5k)**
- **ISO174 (1.5k)**
- **ISO175 (1.5k)**
- **ISO176 (1.5k)**
- ***ISO182 (1.5k)***
- 3650 (2k)
- 3652 (2k)
- ISO106 (3.5k)
- ISO121 (3.5k)

With Power
Rated Continuous(1) (kVrms)

2 PORT
- ISO103 (1.5k)
- ISO113 (1.5k)
- ISO213 (1.5k)
- ISO212 (1.5k)
- ISO107 (2.5k)

3 PORT
- **ISO253 (1.5k)**
- **ISO254 (1.5k)**
- **ISO255 (1.5k)**
- **ISO256 (1.5k)**
- 3656 (3.5k)

Technology
(Gain Range)

OPTICALLY-COUPLED
- ISO100 (Variable Gain)
- 3650 (Variable Gain)
- 3652 (Variable Gain, FET Input)
- ISO130 (G = 8, Differential in and out)

CAPACITIVE-COUPLED
- ISO102 (G = 1)
- ISO103 (G = 1)
- ISO106 (G = 1)
- ISO107 (G = 1)
- ISO113 (G = 1)
- ISO120 (G = 1)
- ISO121 (G = 1)
- ISO122 (G = 1)
- **ISO164 (PGA, G = 1, 10, 100)**
- **ISO165 (INA, Variable Gain)**
- **ISO166 (Variable Gain)**
- **ISO174 (PGA, G = 1, 10, 100)**
- **ISO175 (INA, Variable Gain)**
- **ISO176 (Variable Gain)**
- ***ISO182 (G = 1)***
- **ISO253 (G = 1)**
- **ISO254 (PGA, G = 1, 10, 100, 1000)**
- **ISO255 (INA, Variable Gain)**
- **ISO256 (Variable Gain)**

TRANSFORMER-COUPLED
- ISO212 (Variable Gain)
- 3656 (Variable Gain)

A/D CONVERTERS
Rated Continuous(1), f_S

12-BIT
- **ISO806 (1.5kVrms, 40kHz)**
- **ISO808 (1.5kVrms, 100kHz)**

16-BIT
- **ISO807 (1.5kVrms, 40kHz)**
- **ISO809 (1.5kVrms, 100kHz)**

DC/DC CONVERTERS
Rated Continuous(1) (Vrms)

- PWS745 (750)
- PWS750 (750)
- 724 (1k)
- PWS740 (1.5k)
- PWS725A (1.5k)
- PWS726A (3.5k)
- 722 (3.5k)

DIGITAL COUPLERS
(Function)

- ISO485 (RS-485 Transceiver)
- ISO150 (Transceiver, Dual)

SENSOR CONDITIONING
(Function)

- ISC300 (RTD, Bridge, TC in)
- IXR100 (RTD, 4-20mA, 2 Wire)

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPI

NOTE: (1) All isolation voltages defined at continuous A(

Some specifications have been estimated for compari
purposes. Refer to data sheets for guaranteed specifi

Product	Isolation Voltage Cont Peak (DC) (V)	Isolation Voltage Pulse/Test Peak (V)	Isolation Mode Rejection DC typ (dB)	Isolation Mode Rejection 60Hz typ (dB)	Leakage Current at 240V/60Hz max (μArms)	Gain Non-linearity max (%)	Input Offset Voltage Drift max (±μV/°C)	Bias Current max (nA)	Small Signal Bandwidth typ (kHz)	Temp(1) Range	Description
ISO100	750	2500	146(4)	108(4)	0.3	0.07	2(4)	10	60	Ind	Low Drift Wide BW
ISO102	2121	4000	160	120	1.0	±0.003	250	—	70	Ind(2)	1500Vrms Isolation, Buffer
ISO106	4950	8000	160	130	1.0	±0.025	250	—	70	Ind(2)	3500Vrms Isolation, Buffer
ISO120	2121	2500(3)	160	115	0.5	±0.01	150	—	60	Mil(2)	1500Vrms Isolation, Buffer
ISO121	4950	5600(3)	160	115	0.5	±0.01	150	—	60	Mil(2)	3500Vrms Isolation, Buffer
ISO122	2121	2400(3)	160	140	0.5	±0.02	200*	—	50	Ind	1500Vrms Isolation, Buffer
ISO130	720	960(3)	140	140	—	±0.25	2.1*	670*	85	Ind	High IMR Wide BW, G = 8
ISO164	**2121**	**2500(3)**	**115**	**115 (50Hz)**	**0.8 (50Hz)**	**±0.01**	**155**	**5**	**6**	**Ind**	**1500Vrms Isolation with PGA**
ISO165	**2121**	**2500(3)**	**160**	**115**	**1**	**±0.052**	**1.2**	**±10**	**50**	**XInd**	**1500Vrms, INA**
ISO166	**2121**	**2500(3)**	**160**	**115**	**0.8**	**±0.062**	**150***	**±5**	**6***	**XInd**	**1500Vrms, Op Amp**
ISO174	**2121**	**2500(3)**	**115**	**115 (50Hz)**	**0.8 (50Hz)**	**±0.04**	**505**	**5**	**60**	**Ind**	**1500Vrms Isolation with PGA**
ISO175	**2121**	**2500(3)**	**160**	**115**	**1**	**±0.052**	**1.5**	**±10**	**50**	**XInd**	**1500Vrms, INA**
ISO176	**2121**	**2500(3)**	**160**	**115**	**0.8**	**±0.062**	**500***	**±5**	**60***	**XInd**	**1500Vrms, Op Amp**
ISO182	***2121***	***2400(3)***	***140***	***140***	***0.5***	***±0.01***	***200****	**—**	***160***	***Ind***	***Transient Imunity = 5kV/μs***
3650	2000	5000	140	120	0.35	±0.05	5	40	15	Ind	Balanced Current Input, Buffer
3652	2000	5000	140	120	0.35	±0.1	25	50pA	15	Ind	Balanced

NOTES: All packages are DIPs except ISO130 and ISO122 which are also available in surface mount. (1) Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Hermetic. (3) Partial discharge test voltage. (4) R_{IN} = 10kΩ.

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPME

Some specifications have been estimated for comparisor purposes. Refer to data sheets for guaranteed specificati

ANALOG WITH POWER

Product	Isolation Voltage Cont Peak (V)	Isolation Voltage Pulse/Test Peak (V)	Isolation Mode Rejection typ DC (dB)	Isolation Mode Rejection typ 60Hz (dB)	Leakage Current at 240V/60Hz max (µA)	Gain Non-linearity max (%)	Input Offset Voltage Drift max (±µV/°C)	Bias Current max (nA)	Small Signal Bandwidth typ (kHz)	Temp[(1)] Range	Description
ISO103	2121	5657	160	130	2.0	±0.025	250	—	20	Ind	1500Vrms Isolated Input Power, Buffer, 2 port
ISO107	3500	8000	160	100	2.0	±0.025	400	—	20	Ind	2500Vrms Isolated Input Power, Buffer, 2 port
ISO113	2121	5657	160	130	2.0	±0.02	250	—	20	Ind	1500Vrms Isolated Output Power, Buffer, 2 port
ISO212	2121	2400[(3)]	160	115	2.0	±0.025	(±30/G)	50	1	Com	750Vrms Isolated Input Power, Low Cost, 2 port
ISO213	2120	2500[(3)]	160	115	3.0	±0.025	(5 ±35/G)	10	1	Com	Instrumentation Amplifier, 2 port
ISO253	**1500**	**2500[(3)]**	**160**	**115**	**2.0**	**±0.1**	**150**	**NS**	**50**	**XInd**	**Buffer, 3 port**
ISO254	**1500**	**2500[(3)]**	**160**	**150**	**2.0**	**±0.102**	**± (1 + 520/G)**	**5**	**50**	**XInd**	**Programmable Gain Amplifier, 3 port**
ISO255	**1500**	**2500[(3)]**	**160**	**130**	**2.0**	**±0.102**	**± (4 + 510/G)**	**10**	**50**	**XInd**	**Instrumentation Amplifier, 3 port**
ISO256	**1500**	**2500[(3)]**	**160**	**130**	**2.0**	**±0.1**	**±1.2**	**±5**	**50**	**XInd**	**Operational Amplifier, Input, 3 port**
3656	3500	8000	160	125	0.5[(2)]	±0.05	$(5+ 350/G_1)$	100	30	Ind	High Isolation Voltage, 3 port

NOTES: All packages are DIPs except the package for the ISO212 and ISO213 is a SIP. (1) Ind = –25°C to +85°C, Com = 0°C to +70°C. XInd = –40°C to 85°C. (2) At 120V/60Hz. (3) Partial discharge test voltage, ac Vrms.

A/D CONVERTERS

Product	Resolution (Bits)	Linearity Error max (%FSR)	Input Range (see table, pg 43) (V)	Sampling Rate (kHz)	NMC	THD (dB, max)	Temp Range	Pkg	Description
ISO806	**12**	**±0.022**	**C, D, S**	**40**	**12**	**–90***	**Ind**	**PDIP**	**Serial, Isolated, Rated 1500 Vrms**
ISO807	**16**	**±0.0046**	**C, D, S**	**40**	**15**	**–100***	**Ind**	**PDIP**	**Serial, Isolated, Rated 1500 Vrms**
ISO808	**12**	**±0.022**	**C, D, E, P, R, S**	**100**	**12**	**–90***	**Ind**	**PDIP**	**Serial, Isolated, Rated 1500 Vrms**
ISO809	**16**	**±0.006**	**C, D, E, P, R, S**	**100**	**15**	**–100***	**Ind**	**PDIP**	**Serial, Isolated, Rated 1500 Vrms**

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

DC/DC CONVERTERS

Product	Isolation Voltage Cont Peak (V)	Isolation Voltage Pulse Test Peak (V)	Input Voltage min (VDC)	Input Voltage max (VDC)	Leakage Current 240VAC 60Hz (μA)	Current, Balanced Loads On All Outputs Rated (mA)	Current, Balanced Loads On All Outputs Max(1) (mA)	Sensitivity To Input Change (V/V)	Temp(2) Range	Pkg	Description
PWS725A	2121	4000	7	18	2	±15	±40	1.15	Ind	DIP	Single ±15V Output
PWS726A	4950	8000	7	18	2	±15	±40	1.15	Ind	DIP	Single ±15V Output
PWS740	2121	4000	7	20	1.5	30(3)	60(3)	1.20	Ind	Sys(4)	Multiple Output (1-8)
PWS745(6)	1060	1200(7)	10(5)	18(5)	1.5	±15	30	1.20(5)	Ind	Comp	Multiple Output (1-8)
PWS750	1060	1200(7)	10(5)	18(5)	1.5	±15	30	1.20(5)	Ind	Comp	Multiple Output (1-8)
722	3500	8000	5	16	1	±3-40	±50	1.13	Ind	Mod	Dual ±15V Output
724	1000	3000	5	16	1	±3-16	±60	0.63	Ind	Mod	Quad ±8V Output

NOTES: (1) See complete Product Data Sheet for full specifications, especially regarding output current capabilities. (2) Ind = –25°C to +85°C. (3) Per channel. (4) 1 TO-3 driver per 8 channels, plus 2 DIPs per channel. (5) 15V operation. (6) PWS745-1 driver may also be used with PWS740 components. (7) Partial discharge test voltage, ac Vrms.

DIGITAL COUPLER

Product	Isolation Voltage Cont Peak (Vrms)	Isolation Voltage Pulse Test Peak (V)	Leakage Current 240VAC 60Hz (μA)	Data Rate (MBd)*	Power Consumption Per Channel max (mW)	Ext Power Req	Temp(1)	Pkg	Description
ISO150	1500	2400(2)	0.6	80	25	Yes	XInd	DIP, SOIC	Dual Isolated Transceiver
ISO485	1500	NS	NS	20	180 at 5MBit/s	Yes	XInd	DIP	RS-485 Transceiver

NOTES: (1) XInd = –40°C to +85°C. (2) Partial discharge test voltage, ac Vrms.

SENSOR CONDITIONING

Product	Isolation Voltage Cont Peak (V)	Leakage Current (μArms)	Isolation Impedance	Gain Non-linearity typ	Frequency Response	Reference Voltage	Isolated Power Req	Temp(1) Range	Pkg	Description
ISC300	700	4	2GΩ || 15pF	±0.01%	3.5Hz	Yes	No	Com	Mod	Precision Measured Channel

Product	Isolation Voltage Cont Peak (V)	Span Untrimmed Error, max (%)	Span Non-linearity, typ (%)	Span Temp Drift (ppm/°C)	Input Offset Voltage typ	Input vs Temp max (μV/°C)	CMR vs Supply (dB)	Output Current Range (mA)	Output Current Limit (mA)	Temp(1) Range	Pkg	Description
IXR100	2121	–2.5	0.01 (EMF) 0.1 (RTD)	100	500μV	5	100	4-20	32	Special	Mod	Two-Wire Transmitter

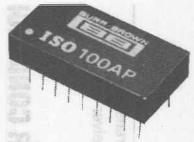
NOTE: (1) Special = –20°C to +70°C, Com = 0°C to 70°C.

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR - BROWN®



ISO100

Optically-Coupled Linear ISOLATION AMPLIFIER

FEATURES

- **EASY TO USE, SIMILAR TO AN OP AMP**
  $V_{OUT}/I_{IN} = R_F$, Current Input
  $V_{OUT}/V_{IN} = R_F/R_{IN}$, Voltage Input
- **100% TESTED FOR BREAKDOWN: 750V Continuous Isolation Voltage**
- **ULTRA-LOW LEAKAGE: 0.3µA, max, at 240V/60Hz**
- **WIDE BANDWIDTH: 60kHz**
- **18-PIN DIP PACKAGE**

APPLICATIONS

- **INDUSTRIAL PROCESS CONTROL**
  Transducer Sensing
  (Thermocouples, RTD, Pressure Bridges)
  4mA to 20mA Loops
  Motor and SCR Control
  Ground Loop Elimination
- **BIOMEDICAL MEASUREMENTS**
- **TEST EQUIPMENT**
- **DATA ACQUISITION**

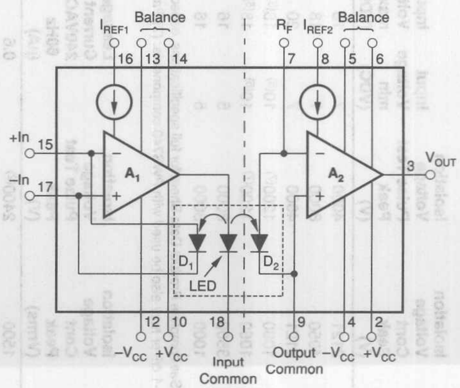
DESCRIPTION

The ISO100 is an optically-coupled isolation amplifier. High accuracy, linearity, and time-temperature stability are achieved by coupling light from an LED back to the input (negative feedback) as well as forward to the output. Optical components are carefully matched and the amplifier is actively laser-trimmed to assure excellent tracking and low offset errors.

The circuit acts as a current-to-voltage converter with a minimum of 750V (2500V test) between input and output terminals. It also effectively breaks the galvanic connection between input and output commons as indicated by the ultra-low 60Hz leakage current of 0.3µA at 250V. Voltage input operation is easily achieved by using one external resistor.

Versatility along with outstanding DC and AC performance provide excellent solutions to a variety of challenging isolation problems. For example, the ISO100 is capable of operating in many modes, including: noninverting (unipolar and bipolar) and inverting (unipolar and bipolar) configurations. Two precision current sources are provided to accomplish bipolar operation. Since these are not required for unipolar operation, they are available for external use (see Applications section).

Designs using the ISO100 are easily accomplished with relatively few external components. Since V_{OUT} of the ISO100 is simply $I_{IN}R_F$, gains can be changed by altering one resistor value. In addition, the ISO100 has sufficient bandwidth (DC to 60kHz) to amplify most industrial and test equipment signals.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

At $T_A = +25°C$ and $\pm V_{CC} = 15VDC$, unless otherwise specified.

		ISO100AP			ISO100BP			ISO100CP			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ISOLATION											
Voltage											
Rated Continuous, AC peak or DC(1)		750			*			*			V
Test Breakdown, DC	10s	2500			*			*			V
Rejection(2) DC			5			*			*		pA/V
	R_{IN} = 10kΩ, Gain = 100		146			*			*		dB
AC	60Hz, 480V, R_F = 1MΩ		400			*			*		pA/V
	R_{IN} = 10kΩ, Gain = 100		108			*			*		dB
Impedance			10^{12}‖2.5			*			*		Ω‖pF
Leakage Current	240Vrms, 60Hz			0.3			*			*	μA, rms
OFFSET VOLTAGE (RTI)											
Input Stage (V_{OSI})											
Initial Offset				500			300			200	μV
vs Temperature				5			2			2	μV/°C
vs Input Power Supplies				105			*			*	dB
vs Time			1			*			*		μV/kHr
Output Stage (V_{OSO})											
Initial Offset				500			300			200	μV
vs Temperature				5			2			2	μV/°C
vs Output Power Supplies				105			*			*	dB
vs Time			1			*			*		μV/kHr
Common-Mode Rejection Ratio(2)	60Hz, R_F = 1MΩ		3			*			*		nA/V
	R_{IN} = 10kΩ, Gain = 100		90			*			*		dB
Common-Mode Range		±10			*			*			V
REFERENCE CURRENT SOURCES											
Magnitude											
Nominal		10.5	12	12.5	*	*	*	*	*	*	μA
vs Temperature				300			*			150	ppm/°C
vs Power Supplies			0.3	3		*	*		*	*	nA/V
Matching											
Nominal			50			*			*		nA
vs Temperature			150			*			*		ppm/°C
vs Power Supplies			0.3			*			*		nA/V
Compliance Voltage		–10		+15	*		*	*		*	V
Output Resistance			2 x 10^9			*			*		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	Gain = 1V/μA		60			*			*		kHz
Full Power Bandwidth	Gain = 1V/μA, V_O = ±10V		5			*			*		kHz
Slew Rate		0.22	0.31		*	*		*	*		V/μs
Settling Time	0.1%		100			*			*		μs
TEMPERATURE RANGE											
Specification		–25		+85	*		*	*		*	°C
Operating		–40		+100	*		*	*		*	°C
Storage		–55		+100	*		*	*		*	°C
UNIPOLAR OPERATION											
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		–20		–0.02	*		*	*		*	μA
Without Damage		–1		+1	*		*	*		*	mA
Input Impedance			0.1			*			*		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	–10		0	*		*	*		*	V
Output Impedance	DC, Open-Loop		1200			*			*		Ω
GAIN	$V_O = R_F (I_{IN})$										
Initial Error (adjustable to zero)			2	5		1	2		1	2	% of FS
vs Temperature			0.03	0.07		0.01	0.05		0.005	0.03	%/°C
vs Time			0.05			*			*		%/kHr
Nonlinearity(3)			0.1	0.4		0.03	0.1		0.02	0.07	%
CURRENT NOISE	I_{IN} = 0.2μA										
0.01Hz to 10Hz			20			*			*		pAp-p
10Hz			1			*			*		pA/√Hz
100Hz			0.7			*			*		pA/√Hz
1kHz			0.65			*			*		pA/√Hz

ISO100

5

ISOLATION PRODUCTS

SPECIFICATIONS (CONT)

ELECTRICAL

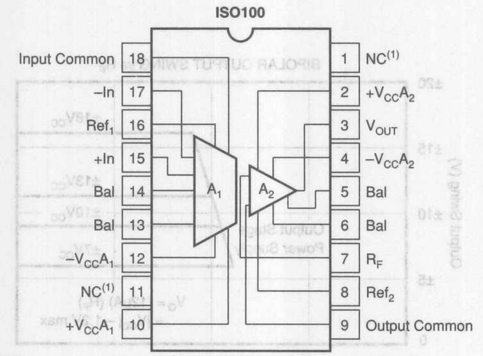
At T_A = +25°C and $\pm V_{CC}$ = 15VDC, unless otherwise specified.

		ISO100AP			ISO100BP			ISO100CP			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT OFFSET CURRENT (I_{OS})											
Initial Offset			1	10		*	*		*	*	nA
vs Temperature			0.05			*			*		nA/°C
vs Power Supplies			0.1			*			*		nA/V
vs Time			100			*			*		pA/kHr
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	I_{IN} = –0.02µA		±1.1	±2		*	*		*	*	mA
	I_{IN} = –20µA		+8, –1.1	+13, –2		*	*		*	*	mA
Output Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	V_O = 0		±1.1	±2		*	*		*	*	mA
Short Circuit Current Limit				±40			*			*	mA
BIPOLAR OPERATION											
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		–10		+10	*		*	*		*	µA
Without Damage		–1		+1	*		*	*		*	mA
Input Impedance			0.1			*			*		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	–10		+10	*		*	*		*	V
Output Impedance			1200			*			*		Ω
GAIN	$V_O = R_F (I_{IN})$										
Initial Error (Adjustable To Zero)			2	5		1	2		1	2	% of FS
vs Temperature			0.03	0.07		0.01	0.05		0.005	0.03	%/°C
vs Time			0.05			*			*		%/kHr
Nonlinearity(3)			0.1	0.4		0.03	0.1		0.02	0.07	%
CURRENT NOISE	I_{IN} = 0.2µA										
0.01Hz to 10Hz			1.5			*			*		nA, p-p
10Hz			17			*			*		pA/√Hz
100Hz			7			*			*		pA/√Hz
1kHz			6			*			*		pA/√Hz
INPUT OFFSET CURRENT (I_{OS}, bipolar(4))											
Initial Offset			40	200		20	70		10	35	nA
vs Temperature				3			2			1	nA/°C
vs Power Supplies				0.7			*			*	nA/V
vs Time			250			*			*		pA/kHr
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	I_{IN} = +10µA		+2, –1.1	+3, –2		*	*		*	*	mA
	I_{IN} = –10µA		+8, –1.1	+13, –2		*	*		*	*	mA
Output Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	V_O = 0		±1.1	±2		*	*		*	*	mA
Short Circuit Current Limit				±40			*			*	mA

* Same as ISO100AP.

NOTES: (1) See Typical Performance Curves for temperature effects. (2) See Theory of Operation section for definitions. For dB see Ex. 2, CM and HV errors. (3) Nonlinearity is the peak deviation from a "best fit" straight line expressed as a percent of full scale output. (4) Bipolar offset current includes effects of reference current mismatch and unipolar offset current.

PIN CONFIGURATION



NOTE: (1) No internal connection.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±18V
Isolation Voltage, AC pk or DC	750V
Input Current	±1mA
Storage Temperature Range	–55°C to +100°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit Duration	Continuous to Ground

PACKAGE INFORMATION

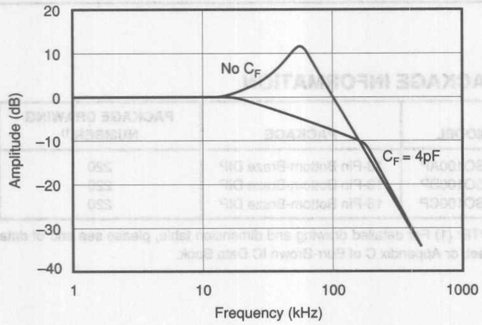
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO100AP	18-Pin Bottom-Braze DIP	220
ISO100BP	18-Pin Bottom-Braze DIP	220
ISO100CP	18-Pin Bottom-Braze DIP	220

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

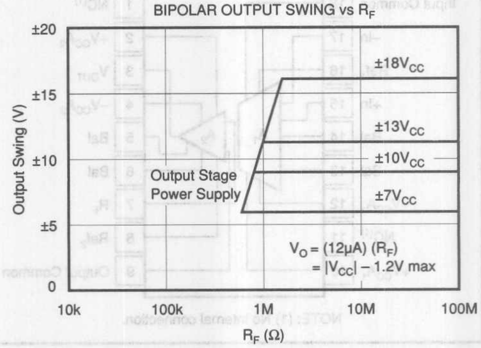
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
ISO100AP	18-Pin Bottom-Braze DIP	–25°C to +85°C
ISO100BP	18-Pin Bottom-Braze DIP	–25°C to +85°C
ISO100CP	18-Pin Bottom-Braze DIP	–25°C to +85°C

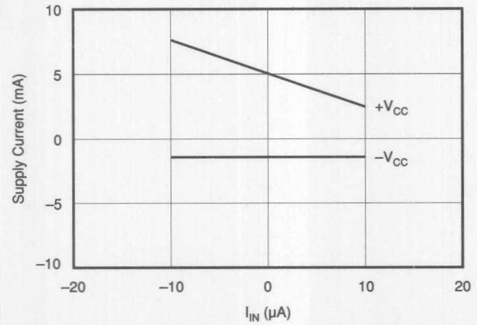
SMALL SIGNAL FREQUENCY RESPONSE



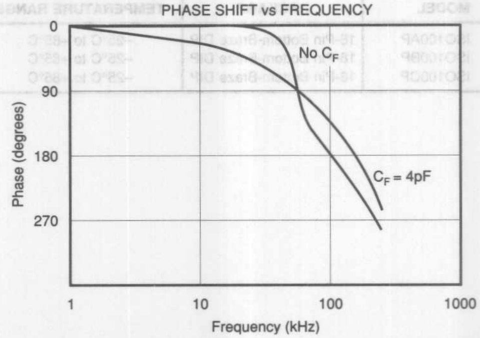
BIPOLAR OUTPUT SWING vs R_F



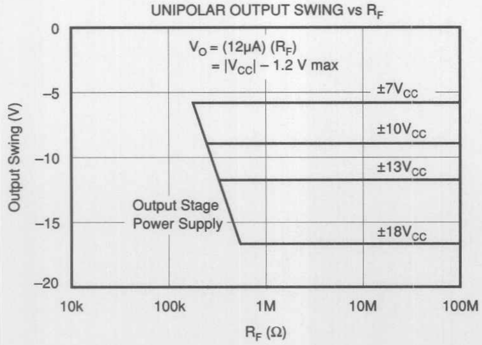
BIPOLAR INPUT STAGE SUPPLY CURRENT vs INPUT CURRENT



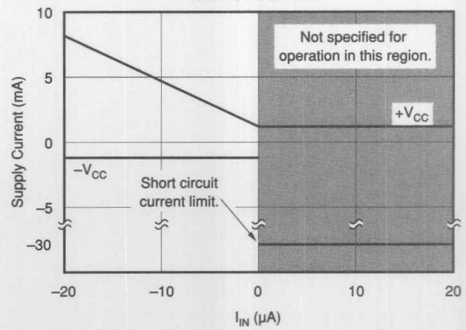
PHASE SHIFT vs FREQUENCY



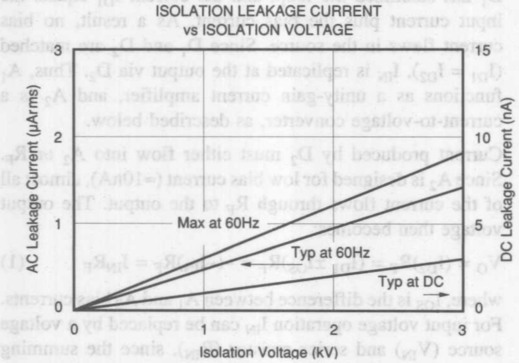
UNIPOLAR OUTPUT SWING vs R_F

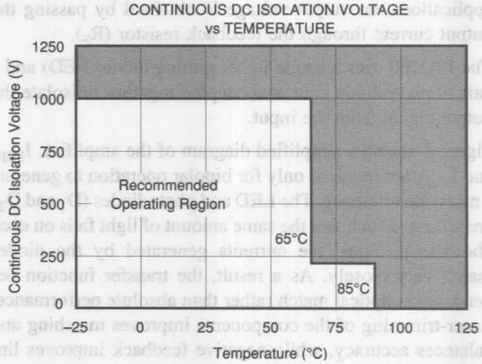


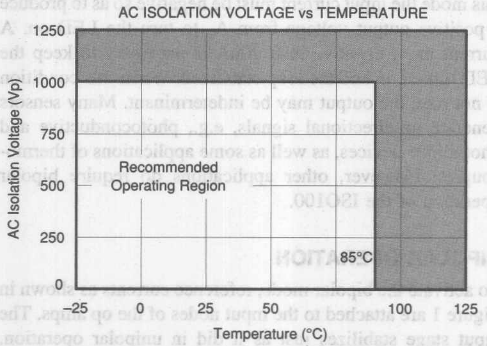
UNIPOLAR INPUT STAGE SUPPLY CURRENT vs INPUT CURRENT

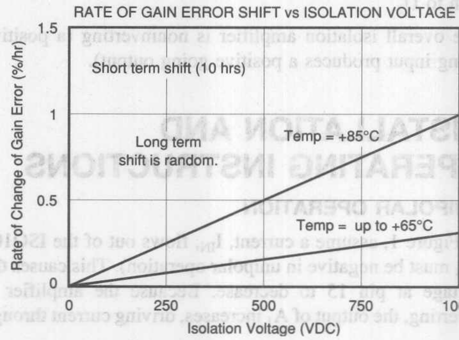


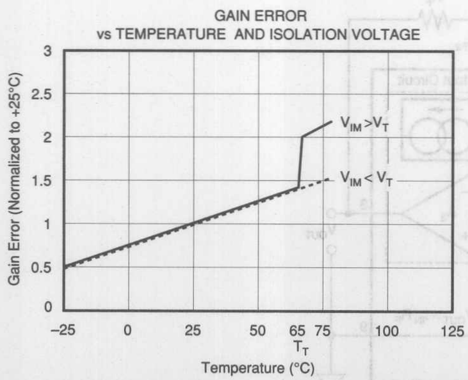
$T_A = +25°C$, $\pm V_{CC} = 15VDC$, unless otherwise specified.











NOTES: V_T and T_T approximate the threshold for the indicated gain shift. This is *caused by the properties of the optical* cavity.
$T_T \approx +65°C$, $V_T \approx 200VDC$. Shift does not occur fo AC voltages.

V_{IM} = Isolation-Mode Voltage
V_T = Threshold Voltage
T_T = Threshold Temperature

ISOLATION PRODUCTS

5

ISO100

THEORY OF OPERATION

The ISO100 is fundamentally a unity gain current amplifier intended to transfer small signals between electrical circuits separated by high voltages or different references. In most applications, an output voltage is obtained by passing the output current through the feedback resistor (R_F).

The ISO100 uses a single light emitting diode (LED) and a pair of photodiode detectors coupled together to isolate the output signal from the input.

Figure 1 shows a simplified diagram of the amplifier. I_{REF1} and I_{REF2} are required only for bipolar operation to generate a midscale reference. The LED and photodiodes (D_1 and D_2) are arranged such that the same amount of light falls on each photodiode. Thus, the currents generated by the diodes match very closely. As a result, the transfer function depends upon optical match rather than absolute performance. Laser-trimming of the components improves matching and enhances accuracy, while negative feedback improves linearity. Negative feedback around A_1 occurs through the optical path formed by the LED and D_1. The signal is transferred across the isolation barrier by the matched light path to D_2.

The overall isolation amplifier is noninverting (a positive going input produces a positive going output).

INSTALLATION AND OPERATING INSTRUCTIONS

UNIPOLAR OPERATION

In Figure 1, assume a current, I_{IN}, flows out of the ISO100 (I_{IN} must be negative in unipolar operation). This causes the voltage at pin 15 to decrease. Because the amplifier is inverting, the output of A_1 increases, driving current through the LED. As the LED light output increases, D_1 responds by generating an increasing current. The current increases until the sum of the currents in and out of the input node (–Input to A_1) is zero. At that point, the negative feedback through D_1 has stabilized the loop, and the current I_{D1} equals the input current plus the bias current. As a result, no bias current flows in the source. Since D_1 and D_2 are matched ($I_{D1} = I_{D2}$), I_{IN} is replicated at the output via D_2. Thus, A_1 functions as a unity-gain current amplifier, and A_2 is a current-to-voltage converter, as described below.

Current produced by D_2 must either flow into A_2 or R_F. Since A_2 is designed for low bias current (≈10nA), almost all of the current flows through R_F to the output. The output voltage then becomes:

$$V_O = (I_{D2})R_F = (I_{D1} \pm I_{OS})R_F \approx -(-I_{IN})R_F = I_{IN}R_F \qquad (1)$$

where, I_{OS} is the difference between A_1 and A_2 bias currents. For input voltage operation I_{IN} can be replaced by a voltage source (V_{IN}) and series resistor (R_{IN}), since the summing node of the op amp is essentially at ground. Thus, $I_{IN} = V_{IN}/R_{IN}$.

Unipolar operation does have some constraints, however. In this mode the input current must be negative so as to produce a positive output voltage from A_1 to turn the LED on. A current more negative than 20nA is necessary to keep the LED turned on and the loop stabilized. When this condition is not met, the output may be indeterminant. Many sensors generate unidirectional signals, e.g., photoconductive and photodiode devices, as well as some applications of thermocouples. However, other applications do require bipolar operation of the ISO100.

BIPOLAR OPERATION

To activate the bipolar mode, reference currents as shown in Figure 1 are attached to the input nodes of the op amps. The input stage stabilizes just as it did in unipolar operation.

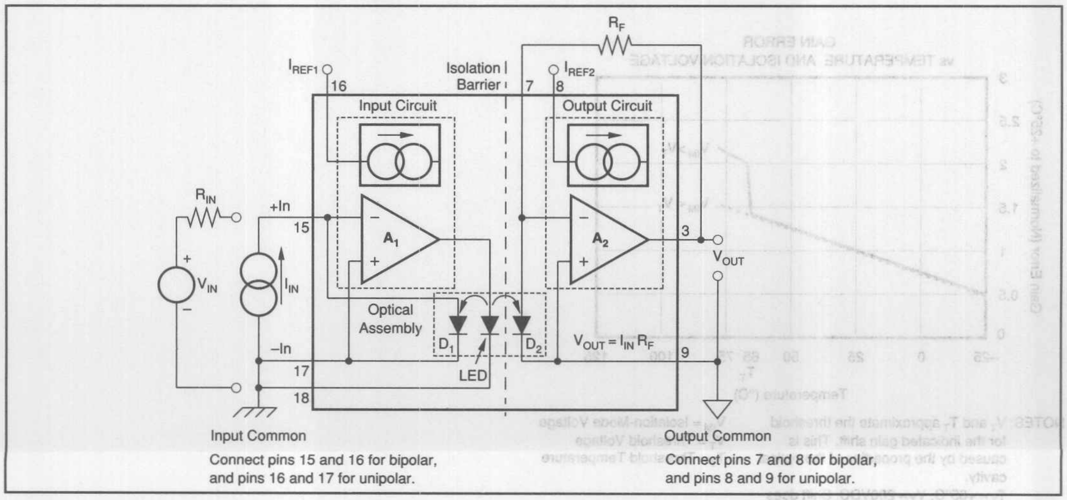


FIGURE 1. Simplified Block Diagram of the ISO100.

Assuming $I_{IN} = 0$, the photodiode has to supply all the I_{REF1} current. Again, due to symmetry, $I_{D1} = I_{D2}$. Since the two references are matched, the current generated by D_2 will equal I_{REF2}. This results in no current flow in R_F, and the output voltage will be zero. When I_{IN} either adds or subtracts current from the input node, the current D_1 will adjust to satisfy $I_{D1} = I_{IN} + I_{REF1}$. Because I_{REF1} equals I_{REF2} and I_{D1} equals I_{D2}, a current equal to I_{IN} will flow in R_F. The output voltage is then $V_O = I_{IN}R_F$. The range of allowable I_{IN} is limited. Positive I_{IN} can be as large as I_{REF1} (10.5μA, min). At this point, D_1 supplies no current and the loop opens. Negative I_{IN} can be as large as that generated by D_1 with maximum LED output (recommended 10μA, max).

DC ERRORS

Errors in the ISO100 take the form of offset currents and voltages plus their drifts with temperature. These are shown in Figure 2.

A_1 and A_2— assumed to be ideal amplifiers.

V_{OSO} and V_{OSI}—the input offset voltages of the output and input stage, respectively. V_{OSO} appears directly at the output but, V_{OSI} appears at the output as

$$V_{OSI}\frac{R_F}{R_{IN}}, \qquad (1)$$

see equation (2).

I_{OS}—the offset current. This is the current at the input necessary to make the output zero. It is equal to the combined effect of the difference between the bias currents of A_1 and A_2 and the matching errors in the optical components in the unipolar mode.

I_{REF1} and I_{REF2}—reference currents that, when connected to the inputs, enable bipolar operation. The two currents are trimmed, in the bipolar mode, to minimize the $I_{OS\ BIPOLAR}$ error.

I_{D1} and I_{D2}—currents generated by each photodiode in response to the light from the LED.

A_e—gain error.

$$A_e = |\text{ Ideal gain/Actual gain }| - 1$$

The output then becomes:

$$V_{OUT} = R_F\left[\left(\frac{V_{IN} \pm V_{OS}}{R_{IN}} - I_{REF1} \pm I_{OS}\right)(1 + A_e) + I_{REF2}\right] \pm V_{OSO} \qquad (2)$$

The total input referred offset voltage of the ISO100 can be simplified in the unipolar case by assuming that $A_e = 0$ and $V_{IN} = 0$:

$$V_{OUT} \approx R_F\left[\frac{\pm V_{OSI}}{R_{IN}} \pm I_{OS\ UNIPOLAR}\right] \pm V_{OSO} \qquad (3)$$

This voltage is then referred back to the input by dividing by R_F/R_{IN}.

$$V_{OS\ (RTI)} = (\pm V_{OSI}) \pm R_{IN}\,(I_{OS\ UNIPOLAR}) + V_{OSO}/(R_F/R_{IN}) \qquad (4)$$

Example 1. Refer to Figure 2 and Electrical Specifications Table.

Given: $I_{OS\ BIPOLAR} = +35\text{nA}$

$R_{IN} = 100\text{k}\Omega$

$R_F = 1\text{M}\Omega$ (gain = 10)

$V_{OSI} = +200\mu\text{V}$

$V_{OSO} = +200\mu\text{V}$

Find: The total offset voltage error referred to the input and output when $V_{IN} = 0\text{V}$.

V_{OS} total RTI

$= \{[\pm V_{OSI} \pm R_{IN}\,(I_{OS\ BIPOLAR}) - R_{IN}\,(I_{REF\ 1})]$
$[1 + A_e] + R_{IN}\,I_{REF\ 2}\} \pm V_{OSO}/(R_F/R_{IN})$

$= \{[+200\mu\text{V} + 100\text{k}\Omega\,(35\text{nA}) - 100\text{k}\Omega\,(12.5\mu\text{A})]$
$[1.02] + 100\text{k}\Omega\,(12.5\mu\text{A})\} +$
$200\mu\text{V}/(1\text{M}\Omega/100\text{k}\Omega)$

$= \{[0.2\text{mV} + 3.5\text{mV} - 1.25\text{V}]$
$[1.02] + 1.25\text{V}\} + 0.02\text{mV}$

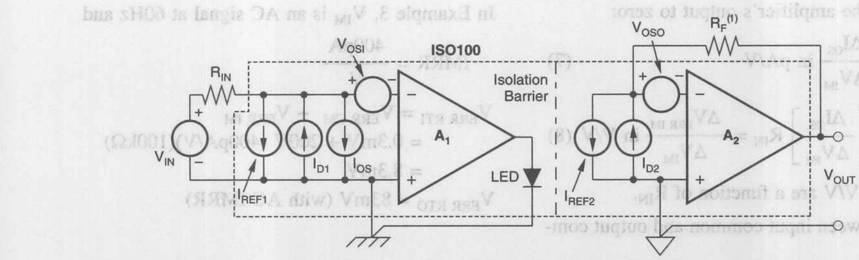
$= -21.2\text{mV}$

V_{OS} total RTO

$= V_{OS}$ total RTI x R_F/R_{IN}

$= -21.2\text{mV} \times 10$

$= -212\text{mV}$



NOTE: (1) Use 1MΩ or greater to achieve a full scale output of 10V.

FIGURE 2. Circuit Model for DC Errors in the ISO100.

reference current times the gain error (which appears as an offset). The error for unipolar operation is much lower. The error due to offset current can be zeroed using circuits shown in Figures 6 and 7. The gain error is adjusted by trimming either R_F or R_{IN}.

COMMON-MODE AND HIGH VOLTAGE ERRORS

Figure 3 shows a model of the ISO100 that can be used to analyze common-mode and high voltage behavior.

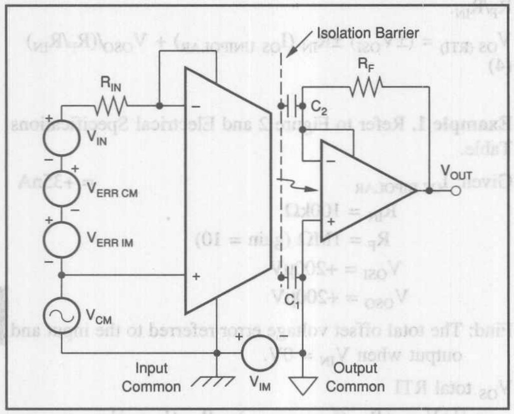


FIGURE 3. High Voltage Error Model.

Definitions of CMR and IMR

I_{OS} is defined as the input current required to make the ISO100's output zero. CMRR and IMRR in the ISO100 are expressed as conductances. CMRR defines the relationship between a change in the applied common-mode voltage (V_{CM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

$$\text{CMRR (I-mode)} = \Delta I_{OS}/\Delta V_{CM} \text{ in nA/V} \quad (5)$$

$$\text{CMRR (V-mode)} = \left[\frac{\Delta I_{OS}}{\Delta V_{CM}}\right] R_{IN} = \frac{\Delta V_{ERR\ CM}}{\Delta V_{CM}} \text{ in V/V} \quad (6)$$

IMRR defines the relationship between a change in the applied isolation mode voltage (V_{IM}) and the change in I_{OS} required to maintain the amplifier's output to zero:

$$\text{IMRR (I-mode)} = \frac{\Delta I_{OS}}{\Delta V_{IM}} \text{ in pA/V} \quad (7)$$

$$\text{IMRR (V-mode)} = \left[\frac{\Delta I_{OS}}{\Delta V_{IM}}\right] R_{IN} = \frac{\Delta V_{ERR\ IM}}{\Delta V_{IM}} \text{ in V/V} \quad (8)$$

CMRR and IMRR in V/V are a function of R_{IN}.

V_{IM} is the voltage between input common and output common.

V_{CM} is the common-mode voltage (noise that is present on both input lines, typically 60Hz).

that produced by application of V_{CM} and V_{IM}.

CMRR and IMRR are the common-mode and isolation-mode rejection ratios, respectively.

Total Capacitance (C_1 and C_2) is distributed along the isolation barrier. Most of the capacitance is coupled to low impedance or noncritical nodes and affects only the leakage current. Only a small capacitance (C_2) couples to the input of the second stage, and contributes to IMRR.

Example 2. Refer to Figure 3 and Electrical Specification Table.

Given: V_{CM} = 1VAC peak at 60Hz, V_{IM} = 200VDC,
CMRR = 3nA/V, IMRR = 5pA/V,
R_{IN} = 100kΩ, R_F = 1MΩ
(Gain = 10)

Find: The error voltage referred to the input and output when V_{IN} = 0V

$V_{ERR\ RTI} = (V_{CM})(\text{CMRR})(R_{IN}) + (V_{IM})(\text{IMRR})(R_{IN})$
= 1V (3nA/V)(100kΩ)
+ 200V (5pA/V)(100kΩ)
= 0.3mV + 0.1mV
= 0.4mV

$V_{ERR\ RTO} = V_{ERR\ RTI}\ (R_F/R_{IN})$
= 0.4mV (10)
=4mV (with DC IMRR)

NOTE: This error is dominated by the CMRR term.

For purposes of comparing CMRR and IMRR directly with **dB specifications**, the following calculations can be performed:

CMRR in V/V = CMRR (I-mode)(R_{IN})
= 3nA/V (100kΩ) = 0.3mV/V

CMR = 20 LOG (0.3mV/V) = –70dB at 60Hz

IMRR in V/V = IMRR (I-mode)(R_{IN}) = 5pA/V(100kΩ)
= 0.5μV/V

IMR = 20 LOG (0.5 x 10^{-6}V/V) = –126dB at DC

Example 3.

In Example 3, V_{IM} is an AC signal at 60Hz and

$$\text{IMRR} = \frac{400\text{pA}}{\text{V}}$$

$V_{ERR\ RTI} = V_{ERR\ CM} + V_{ERR\ IM}$
= 0.3mV + 200V (400pA/V)(100kΩ)
= 8.3mV

$V_{ERR\ RTO}$ = 83mV (with AC IMRR)

worst case.

Find: Percent error of +10V full scale output

$$\% \text{ Error} = \frac{V_{ERR\ TOTAL}}{V_{FS}} \times 100\%$$

$$= \frac{378\text{mV}}{10\text{V}} \times 100\%$$

$$= 3.78\%$$

NOISE ERRORS

Noise errors in the unipolar mode are due primarily to the optical cavity. When the full 60kHz bandwidth is not needed, the output noise of the ISO100 can be limited by either a capacitor, C_F, in the feedback loop or by a low-pass filter following the output. This is shown in Figure 4. Noise in the bipolar mode is due primarily to the reference current sources, and can be reduced by the low-pass filters shown in Figure 5.

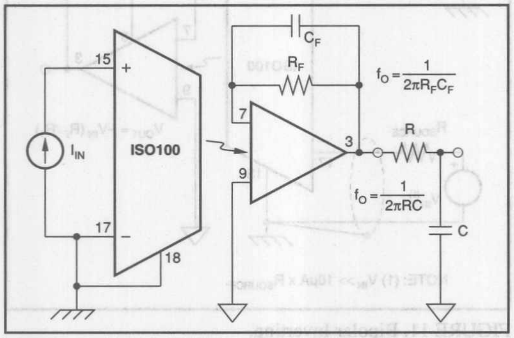


FIGURE 4. Two Circuit Techniques for Reducing Noise in the Unipolar Mode.

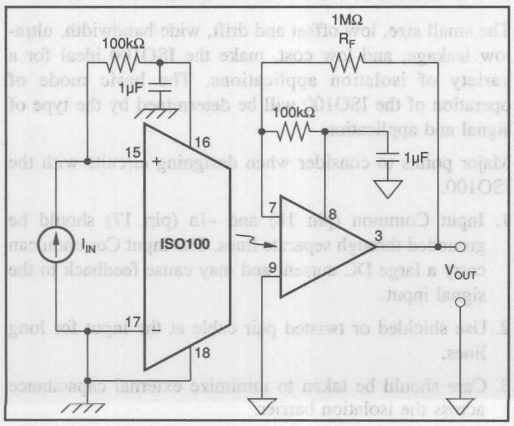


FIGURE 5. Circuit Techniques for Reducing Noise from the Current Sources in the Bipolar Mode.

age and offset current. V_{OSI} and V_{OSO} of the input and output amplifiers can be adjusted independently using external potentiometers. An example is shown in Figure 17. Note that V_{OSO} (500µV, max) appears directly at the output, but V_{OSI} appears at the output multiplied by gain (R_F/R_{IN}). In general, V_{OS} is small compared to the effect of I_{OS} (see Example 1). To adjust for I_{OS} use a circuit which intentionally unbalances the offset in one direction and then allows for adjustment back to zero.

Figure 6 shows how to adjust unipolar errors at zero input. The unipolar amplifier can be used down to zero input if it is made to be "slightly bipolar." By sampling the reference current with R_5 and R_6, the minimum current required to keep the input stage in the linear region of operation can be established. R_7 and R_8 are adjusted to cancel the offset created in the input stage. This brings the output to zero, when the input is zero. Although the amplifier can now operate down to zero input voltage, it has only a small portion of the current drain and noise that the true bipolar configuration would have.

Adjusting the bipolar errors is illustrated in Figure 7. Each of the errors are adjusted in turn. With V_{IN} = "open,", I_{OS} is trimmed by adjusting R_{10} to make the output zero. R_G is then adjusted to trim the gain error. The effects of offset voltage are removed by adjusting R_{14}.

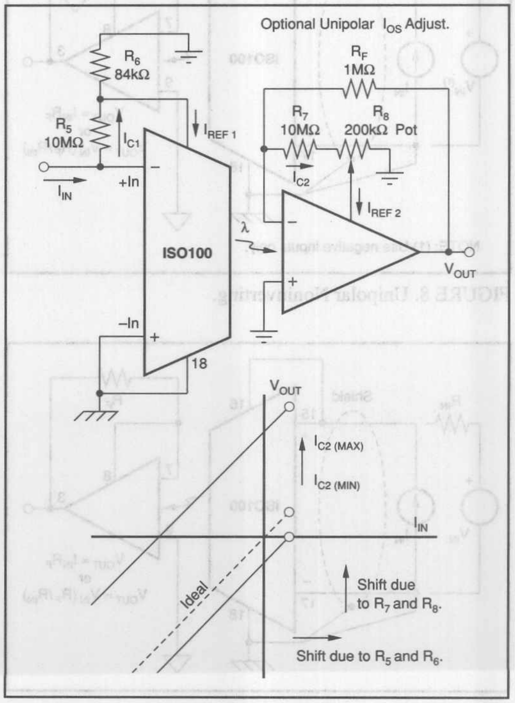


FIGURE 6. Adjusting the Unipolar Amplifier Errors at Zero Input.

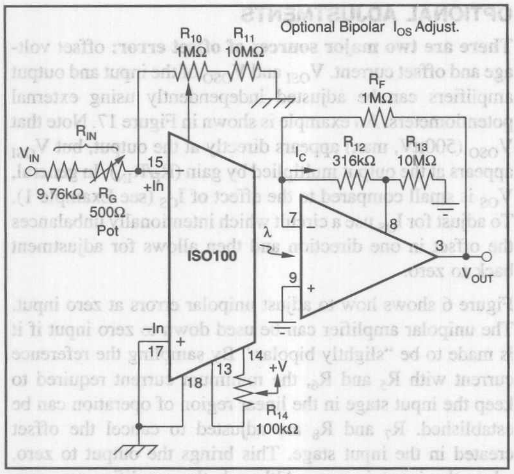


FIGURE 7. Adjusting the Bipolar Errors.

BASIC CIRCUIT CONNECTIONS

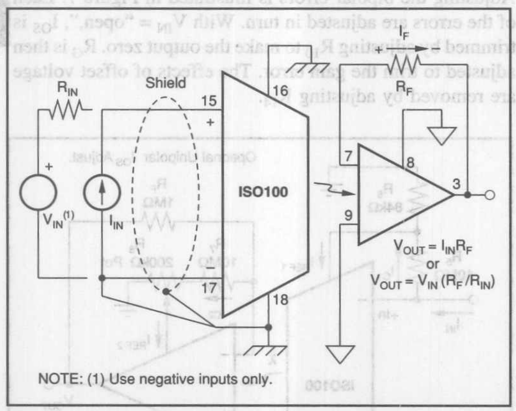


FIGURE 8. Unipolar Noninverting.

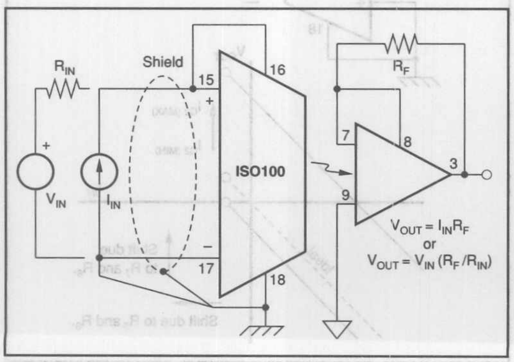


FIGURE 9. Bipolar Noninverting.

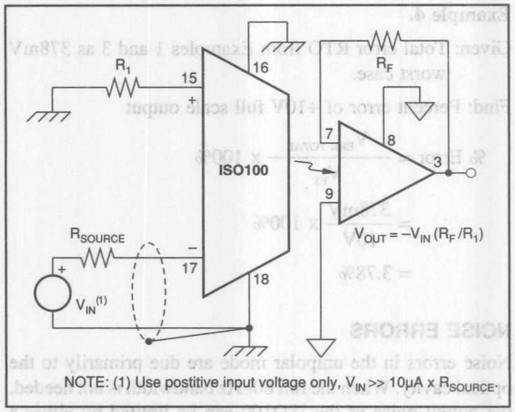


FIGURE 10. Unipolar Inverting.

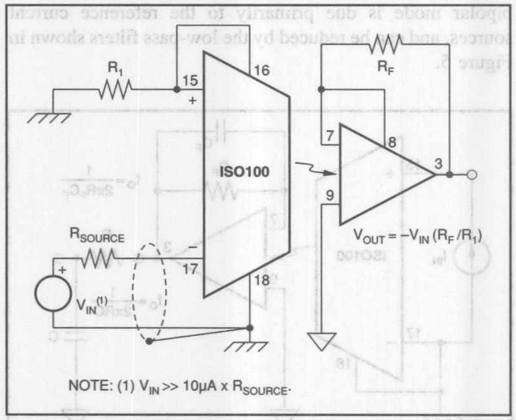


FIGURE 11. Bipolar Inverting.

APPLICATION INFORMATION

The small size, low offset and drift, wide bandwidth, ultra-low leakage, and low cost, make the ISO100 ideal for a variety of isolation applications. The basic mode of operation of the ISO100 will be determined by the type of signal and application.

Major points to consider when designing circuits with the ISO100.

1. Input Common (pin 18) and –In (pin 17) should be grounded through separate lines. The Input Common can carry a large DC current and may cause feedback to the signal input.
2. Use shielded or twisted pair cable at the input for long lines.
3. Care should be taken to minimize external capacitance across the isolation barrier.

4. The distance across the isolation barrier, between external components and conductor patterns, should be maximized to reduce leakage and arcing.
5. Although not an absolute requirement, the use of conformally-coated printed circuit boards is recommended.
6. When in the unipolar mode, the reference currents (pins 8 and 16) must be terminated. I_{IN} should be greater than 20nA to keep internal LED on.
7. The noise contribution of the reference currents will cause the bipolar mode to be noisier than the unipolar mode.
8. The maximum output voltage swing is determined by I_{IN} and R_F.

$$V_{SWING} = I_{IN\ MAX} \times R_F$$

9. A capacitor (about 3pF) can be connected across R_F to compensate for peaking in the frequency response. The peaking is caused by the pole generated by R_F and the capacitance at the input of the output amplifier.

Figure 12 through 18 show applications of the ISO100.

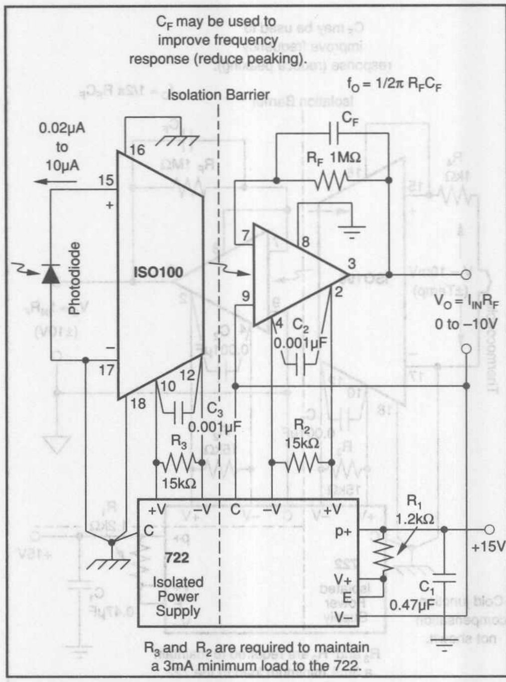


FIGURE 12. Two-Port Isolation Photodiode Amplifier Unipolar.

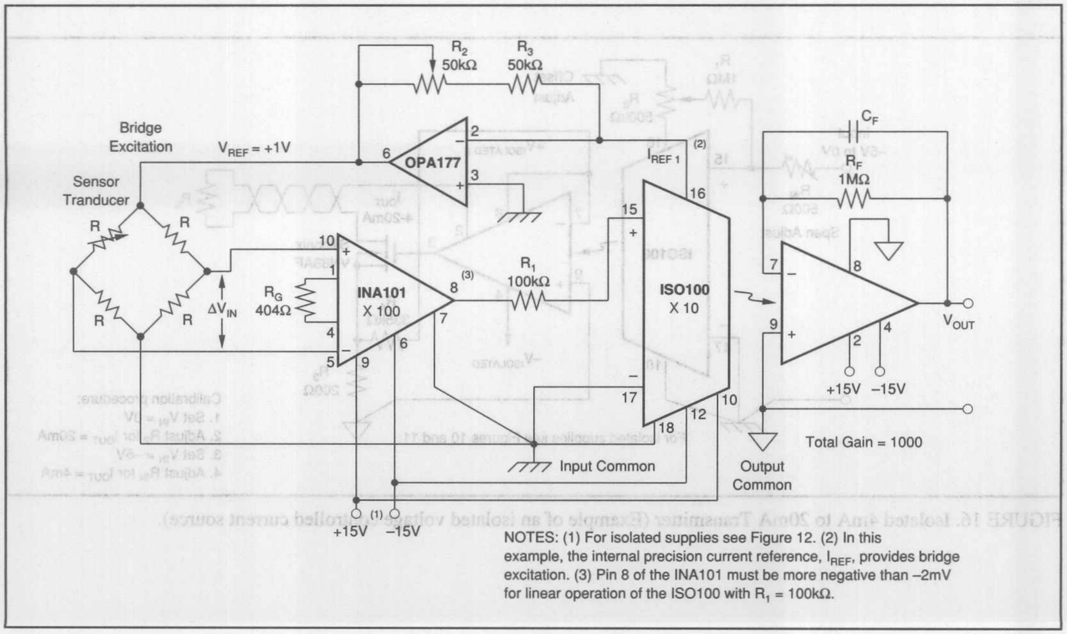


FIGURE 13. Precision Bridge Isolation Amplifier (Unipolar).

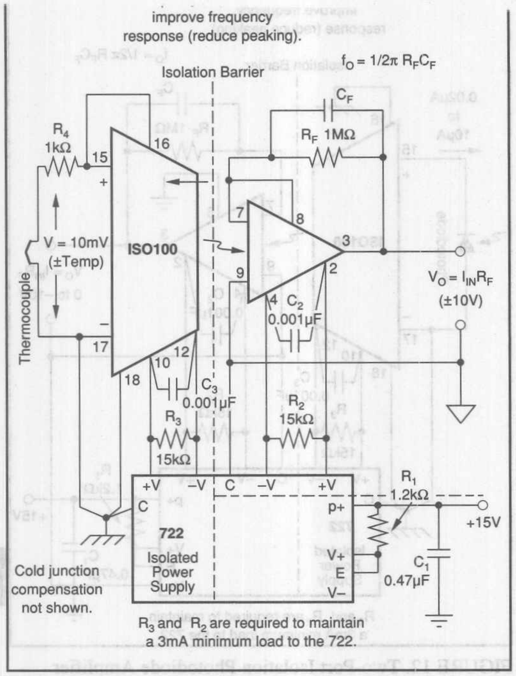


FIGURE 14. Three-Port Isolation Thermocouple Amplifier (Bipolar).

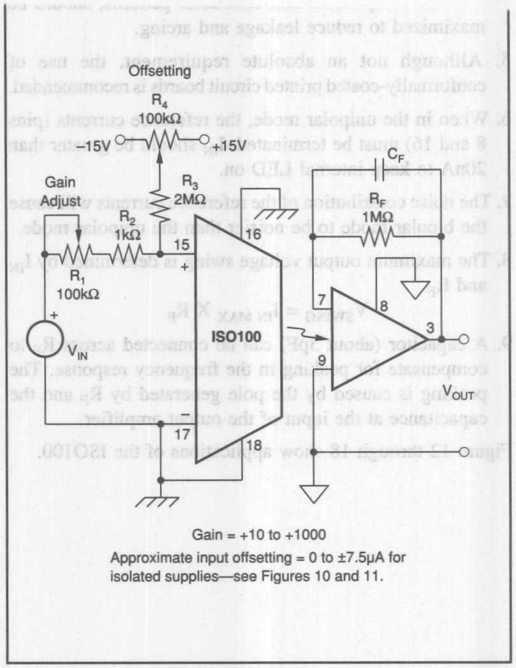


FIGURE 15. Isolated Test Equipment Amplifier (Unipolar with Offsetting).

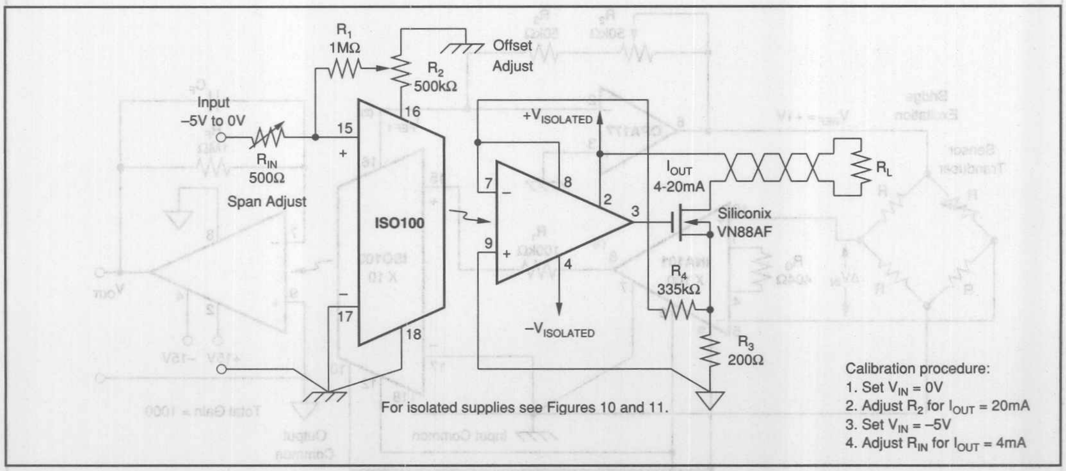


FIGURE 16. Isolated 4mA to 20mA Transmitter (Example of an isolated voltage controlled current source).

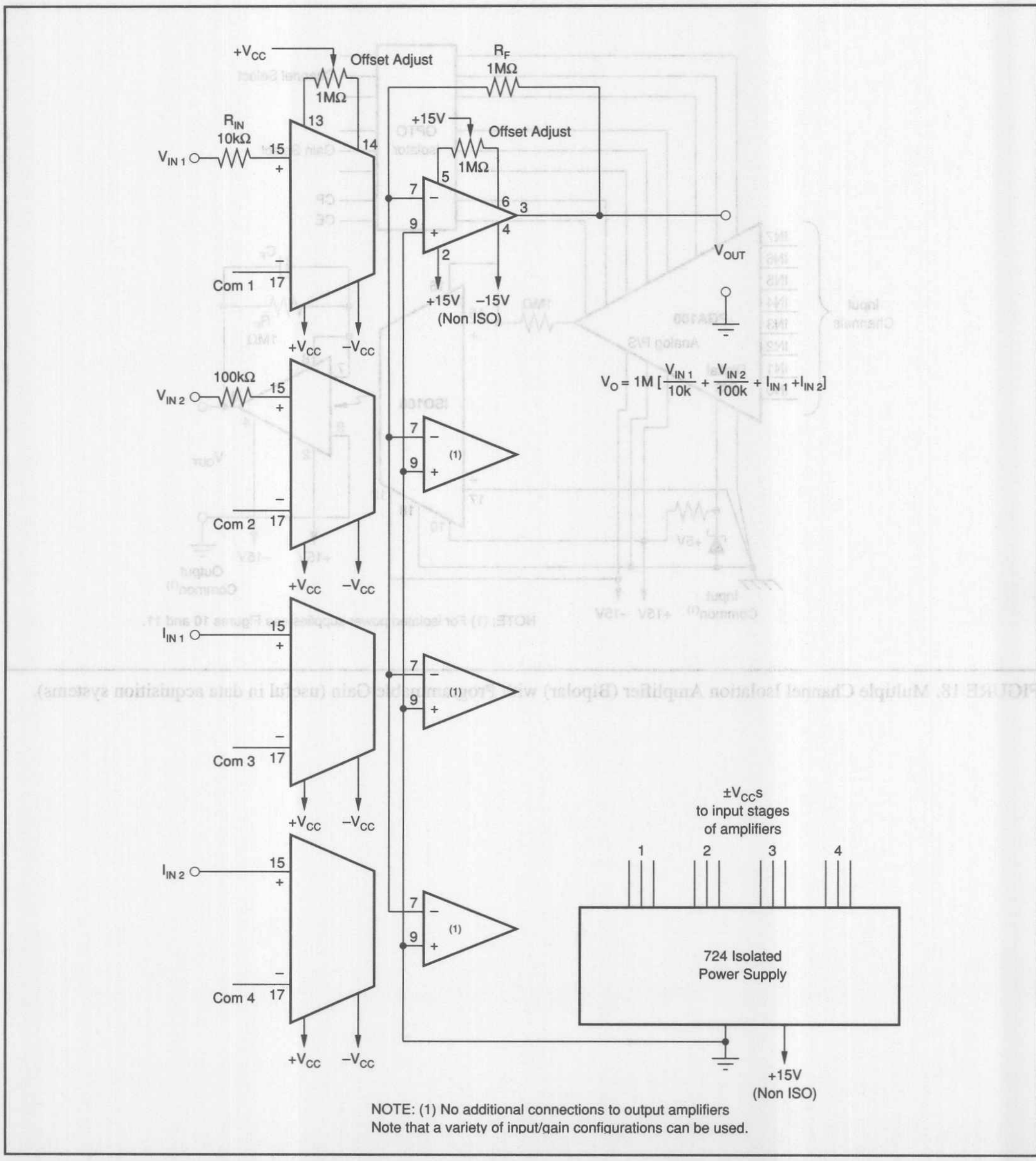


FIGURE 17. Four-Port Isolated Summing Amplifier (Unipolar).

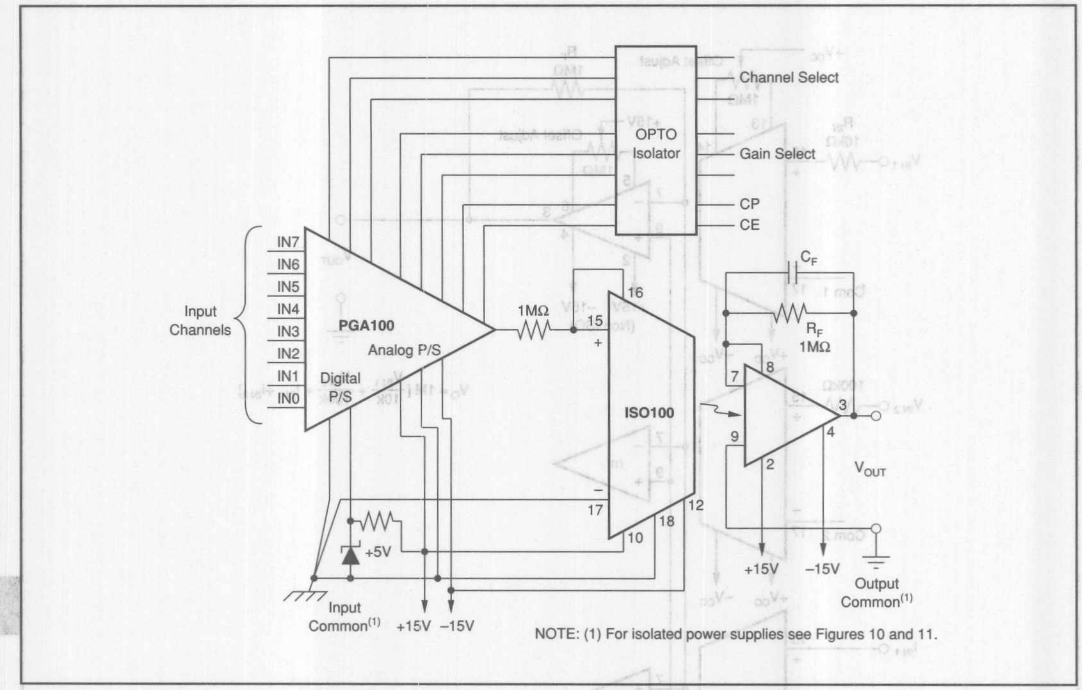
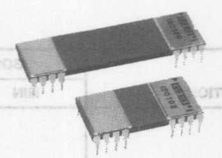


FIGURE 18. Multiple Channel Isolation Amplifier (Bipolar) with Programmable Gain (useful in data acquisition systems).

BURR - BROWN®



ISO102
ISO106

SIGNAL ISOLATION BUFFER AMPLIFIERS

FEATURES

- 14-BIT LINEARITY
- INDUSTRY'S FIRST HERMETIC ISOLATION AMPLIFIERS AT LOW COST
- EASY-TO-USE COMPLETE CIRCUIT
- RUGGED BARRIER, HV CERAMIC CAPACITORS
- 100% TESTED FOR HIGH VOLTAGE BREAKDOWN
  ISO102: 4000Vrms/10s, 1500Vrms/1min
  ISO106: 8000Vpk/10s, 3500Vrms/1min
- ULTRA HIGH IMR: 125dB min at 60Hz, ISO106
- WIDE INPUT RANGE: –10V to +10V
- WIDE BANDWIDTH: 70kHz
- VOLTAGE REFERENCE OUTPUT: 5VDC

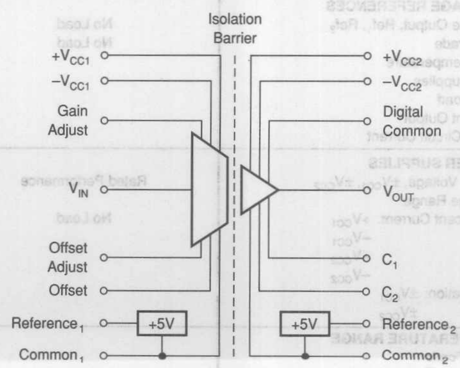
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer channel isolator for thermocouples, RTDs, pressure bridges, flow meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- BIOMEDICAL/ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MILITARY EQUIPMENT

DESCRIPTION

The ISO102 and ISO106 isolation buffer amplifiers are two members of our series of capacitive coupled isolation products from Burr-Brown. They have the same electrical performance and they differ in accuracy. The ISO102 is rated for 1500Vrms in a 24-pin DIP. The ISO106 is rated for 3500Vrms in a 40-pin DIP. Both side-brazed DIPs are 600mil wide and have industry standard package dimensions with the exception of missing pins between input and output stages. This permits utilization of automatic insertion techniques in production. The three-chip hybrid with its generous high voltage spacing is easy to use (no external components are required).

Each buffer accurately isolates ±10V analog signals by digitally encoding the input voltage and uniquely coupling across a differential ceramic capacitive barrier. All elements necessary for operation are contained within the DIP. This provides compact signal isolation in a hermetic package.



Covered by patent number 4,748,419 and others pending.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

At $T_A = +25°C$ and $V_{CC1} = V_{CC2} = ±15V$ unless otherwise noted.

PARAMETER	CONDITIONS	ISO102, ISO106, ISO102B, ISO106B MIN	TYP	MAX	UNITS
ISOLATION					
Voltage					
Rated Continuous[1]					
ISO102: AC, 60Hz	T_{MIN} to T_{MAX}	1500			Vrms
DC	T_{MIN} to T_{MAX}	2121			VDC
ISO106: AC, 60Hz	T_{MIN} to T_{MAX}	3500			Vrms
DC	T_{MIN} to T_{MAX}	4950			VDC
Test Breakdown, AC, 60Hz					
ISO102	10s	4000			Vrms
ISO106	10s	8000			Vpk
Isolation-Mode Rejection[2]	V_{ISO} = Rated Continuous, 60Hz				
AC: ISO102		115	120		dB
			1	2	μVrms/V
ISO106		125	130		dB
			0.3	0.6	μVrms/V
DC		140	160		dB
			0.01	0.10	μVDC/V
Barrier Resistance			10^{14}		Ω
Barrier Capacitance			6		pF
Leakage Current	V_{ISO} = 240Vrms, 60Hz		0.5	1	μArms
INPUT					
Voltage Range	Rated Operation	−10		+10	V
Resistance		75	100		kΩ
Capacitance			5		pF
OUTPUT					
Voltage Range	Rated Operation	−10		+10	V
	Derated Operation	−12		+12	V
Current Drive		±5			mA
Short Circuit Current		9	20	50	mA
Ripple Voltage[6]	f = 0.5MHz to 1.5MHz		3		mVp-p
Resistance			0.3	1	Ω
Capacitive Load Drive Capability		10,000			pF
Overload Recovery Time, 0.1%	$\|V_O\| > 12V$		30		μs
OUTPUT VOLTAGE NOISE					
Voltage: f = 0.1Hz to 10Hz			300		μVp-p
f = 0.1Hz to 70kHz			16		μV/√Hz
Dynamic Range[7]: f = 0.1Hz to 70kHz	12-Bit Resolution, 1LSB, 20V FS		74		dB
f = 0.1Hz to 280Hz	16-Bit Resolution, 1LSB, 20V FS		96		dB
FREQUENCY RESPONSE					
Small Signal Bandwidth			70		kHz
Full Power Bandwidth, 0.1% THD	$V_O = ±10V$		5		kHz
Slew Rate	$V_O = ±10V$		0.5		V/μs
Settling Time, 0.1%	$V_O = -10V$ to $+10V$		100		μs
Overshoot, Small Signal[8]	$C_1 = C_2 = 0$		40		%
VOLTAGE REFERENCES					
Voltage Output, Ref_1, Ref_2	No Load	+4.975	+5	+5.025	VDC
B Grade	No Load	+4.995	+5	+5.005	VDC
vs Temperature			±5	20	ppm/°C
vs Supplies			10		μV/V
vs Load			400	1000	μV/mA
Current Output		−0.1		+5	mA
Short Circuit Current		6	14	30	mA
POWER SUPPLIES					
Rated Voltage, $±V_{CC1}$, $±V_{CC2}$	Rated Performance		±15		V
Voltage Range		±10		±20	V
Quiescent Current: $+V_{CC1}$	No Load		+11	+15	mA
$-V_{CC1}$			−9	−12	mA
$+V_{CC2}$			+25	+33	mA
$-V_{CC2}$			−15	−20	mA
Dissipation: $±V_{CC1}$			300	400	mW
$±V_{CC2}$			600	800	mW
TEMPERATURE RANGE					
Specification		−25		+85	°C
Operating[9]		−25		+85	°C
Storage		−65		+150	°C
Thermal Resistance, θ_{JA}			40		°C/W
θ_{JC}			12		°C/W

PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN								
Nominal Gain			1			*		V/V
Initial Error(3)			±0.1	±0.25		0.07	0.13	% FSR
Gain vs Temperature			±20	±50		±12	±25	ppm FSR/°C
Nonlinearity(4)	$V_O = -10V$ to $+10V$		±0.007	±0.012		±0.002	±0.003	% FSR
INPUT OFFSET VOLTAGE								
Initial Offset	$V_{IN} = 0V$		±25	±70		±15	±25	mV
vs Temperature			±250	±500		±150	±250	μV/°C
vs Power Supplies(5)	Input Stage, V_{CC1} = ±10V to ±20V	0	1.4	4.0	*	*	*	mV/V
	Output Stage, V_{CC2} = ±10V to ±20V	–4	–1.4	0	*	*	*	mV/V

		ISO106			ISO106B			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
GAIN								
Nominal Gain			1			*		V/V
Initial Error(3)			±0.1	±0.25		0.07	*	% FSR
Gain vs Temperature			±20	±50		±12	±25	ppm FSR/°C
Nonlinearity(4)	$V_O = -10V$ to $+10V$		±0.04	±0.075		±0.007	±0.025	% FSR
INPUT OFFSET VOLTAGE								
Initial Offset	$V_{IN} = 0V$		±25	±70		*	*	mV
vs Temperature			±250	±500		±150	±250	μV/°C
vs Power Supplies(5)	Input Stage, V_{CC1} = ±10V to ±20V		3.7			*		mV/V
	Output Stage, V_{CC2} = ±10V to ±20V		–3.7			*		mV/V

* Specification same as model to the left.

NOTES: (1) 100% tested at rated continuous for one minute. (2) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. It is a function of frequency as shown in the Typical Performance Curves. This is specified for barrier voltage slew rates not exceeding 100V/μs. (3) Adjustable to zero. FSR = Full Scale Range = 20V. (4) Nonlinearity is the peak deviation of the output voltage from the best fit straight line. It is expressed as the ratio of deviation to FSR. (5) Power supply rejection = change in V_{OS}/20V supply change. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Dynamic range = FSR/(voltage spectral noise density x square root of user bandwidth). (8) Overshoot can be eliminated by band-limiting. (9) See "Power Dissipation vs Temperature" performance curve for limitations. (10) Band limited to 10Hz, bypass capacitors located less than 0.25" from supply pins.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
ISO102	Ceramic	–25°C to +85°C
ISO102B	Ceramic	–25°C to +85°C
ISO106	Ceramic	–25°C to +85°C
ISO106B	Ceramic	–25°C to +85°C

PACKAGE INFORMATION

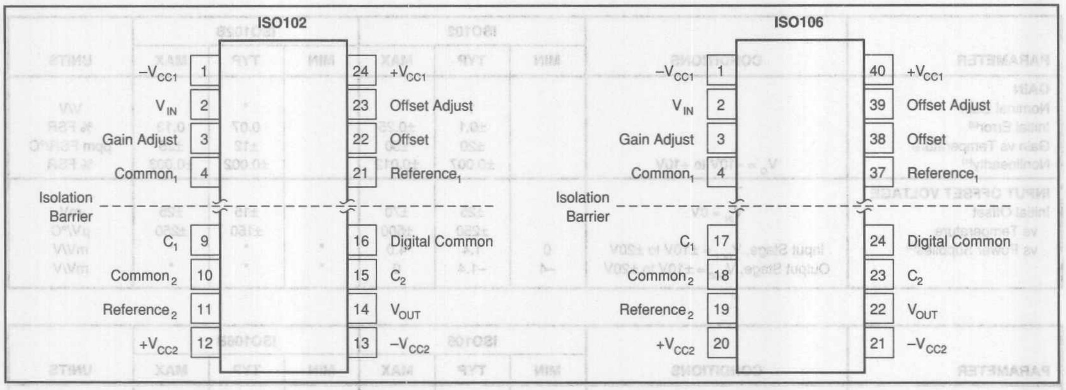
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO102	24-Pin Ceramic	208
ISO102B	24-Pin Ceramic	208
ISO106	40-Pin Ceramic	206
ISO106B	40-Pin Ceramic	206

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage .... ±20V
Input Voltage Range .... ±50V
Transient Immunity, dV/dt 100kV/μs
Continuous Isolation Voltage Across Barrier
ISO102 .... 1500Vrms
ISO106 .... 3500Vrms
Junction Temperature .... +160°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Amplifier and Reference Output
Short Circuit Duration .... Continuous to Common

PIN CONFIGURATION

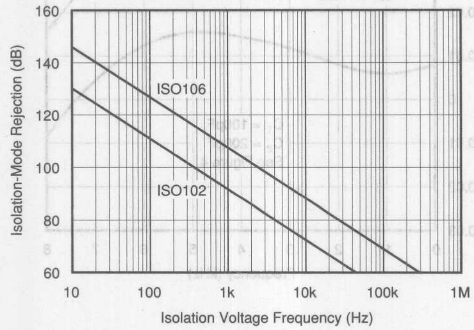


PIN DESCRIPTIONS

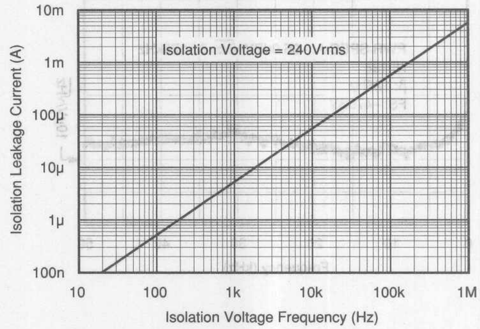
$\pm V_{CC1}$, $Common_1$	Positive and negative power supply voltages and common (or ground) for the input stage. $Common_1$ is the analog reference voltage for input signals. The voltage between $Common_1$ and $Common_2$ is the isolation voltage and appears across the internal high voltage barrier.
$\pm V_{CC2}$, $Common_2$	Positive and negative power supply voltages and common (or ground) for the output stage. $Common_2$ is the analog reference voltage for output signals. The voltage between $Common_1$ and $Common_2$ is the isolation voltage and appears across the internal high voltage barrier.
V_{IN}	Signal input pin. Input impedance is typically 100kΩ. The input range is rated for ±10V. The input level can actually exceed the input stage supplies. Output signal swing is limited only by the output supply voltages.
Gain Adjust	This pin is an optional signal input. A series 5kΩ potentiometer between this pin and the input signal allows a guaranteed ±1.5% gain adjustment range. When gain adjustment is not required, the Gain Adjust should be left open. Figure 4 illustrates the gain adjustment connection.
$Reference_1$	+5V reference output. This low-drift zener voltage reference is necessary for setting the bipolar offset point of the input stage. **This pin must be strapped to either Offset or Offset Adjust to allow the isolation amplifier to function.** The reference is often useful for input signal conditioning circuits. See "Effect of Reference Loading on Offset" performance curve for the effect of offset voltage change with reference loading. $Reference_1$ is identical to, but independent of, $Reference_2$. This output is short circuit protected.
$Reference_2$	+5V reference output. This reference circuit is identical to, but independent of, $Reference_1$. It controls the bipolar offset of the output stage through an internal connection. This output is short-circuit protected.
Offset	Offset input. **This input must be strapped to Reference,** unless user adjustment of bipolar offset is required.
Offset Adjust	This pin is for optional offset control. When connected to the $Reference_1$ pin through a 1kΩ potentiometer, ±150mV of adjustment range is guaranteed. Under this condition, the Offset pin should be connected to the Offset Adjust pin. When offset adjustment is not required, the Offset Adjust pin is left open. See Figure 4.
Digital Common	Digital common or ground. This separate ground carries currents from the digital portions of the output stage circuit. The best grounding practices require that digital common current does not flow in analog common connections. Both pins can be tied directly to a ground plane if available. Difference in potentials between the $Common_2$ and Digital Common pins can be ±1V. See Figure 2.
V_{OUT}	Signal output. Because the isolation amplifier has unity gain, the output signal is ideally identical to the input signal. The output is low impedance and is short-circuit protected. This signal is referenced to $Common_2$; subsequent circuitry should have a separate "sense" connection to $Common_1$ as well as V_{OUT}.
C_1, C_2	Capacitors for small signal bandwidth control. These pins connect to the internal rolloff frequency controlling nodes of the output low-pass filter. Additional capacitance added to these pins will modify the bandwidth of the buffer. C_2 is always twice the value of C_1. See "Bandwidth Control" performance curve for the relationship between bandwidth and C_1 and C_2. When no connections are made to these pins, the full small-signal bandwidth is maintained. Be sure to shield C_1 and C_2 pins from high electric fields on the PC board. This preserves AC isolation-mode rejection by reducing capacitive coupling effects.

TYPICAL PERFORMANCE CURVES

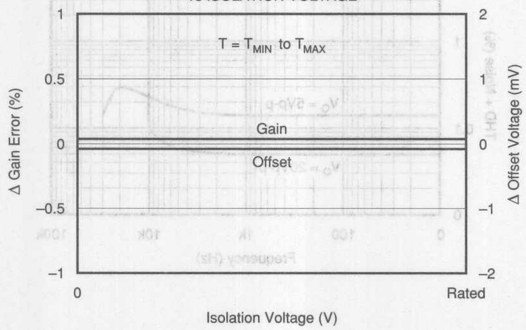
$T_A = +25°C$, $V_{CC} = ±15VDC$ unless otherwise noted.



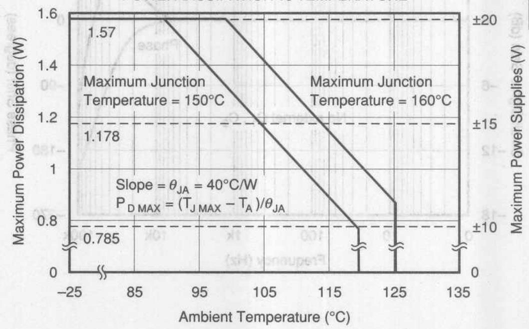
ISOLATION-MODE REJECTION vs ISOLATION VOLTAGE FREQUENCY



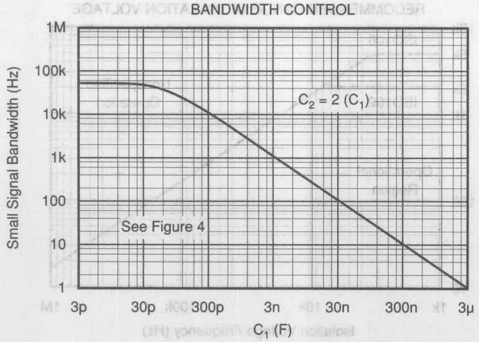
ISOLATION LEAKAGE CURRENT vs ISOLATION VOLTAGE FREQUENCY



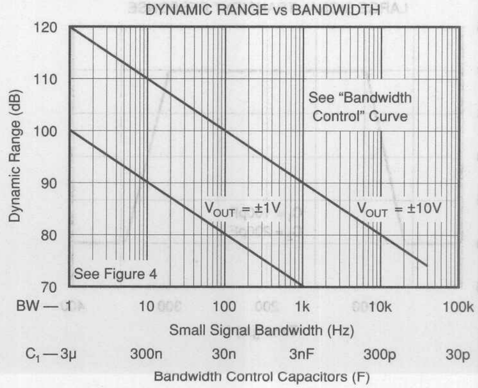
Δ GAIN ERROR AND Δ OFFSET VOLTAGE vs ISOLATION VOLTAGE



POWER DISSIPATION vs TEMPERATURE



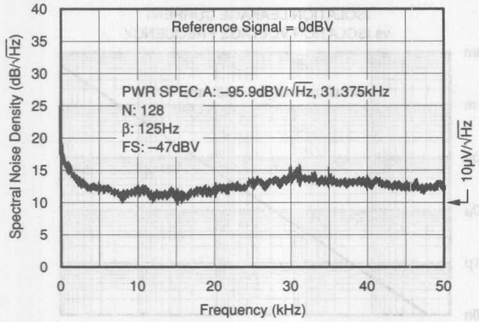
BANDWIDTH CONTROL



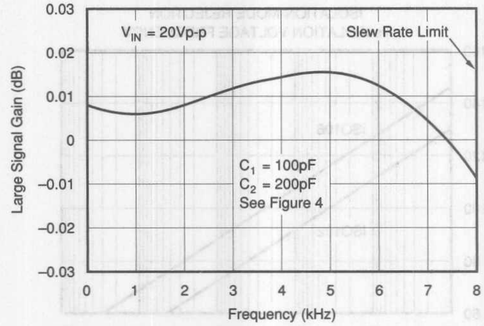
DYNAMIC RANGE vs BANDWIDTH

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

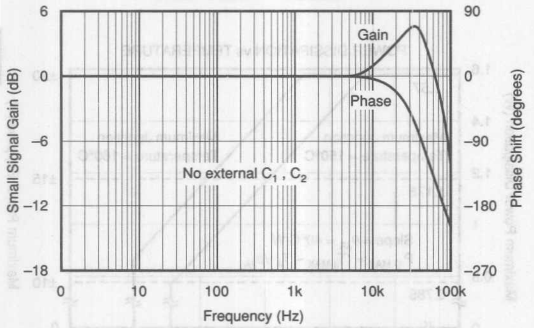
OUTPUT SPECTRAL NOISE DENSITY



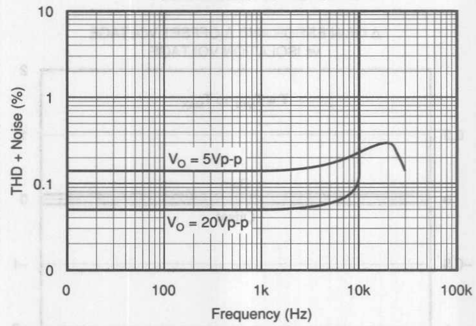
GAIN FLATNESS vs FREQUENCY



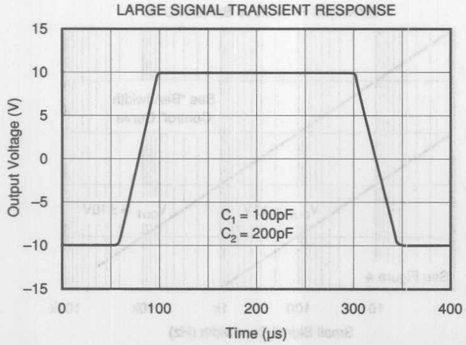
GAIN/PHASE vs FREQUENCY



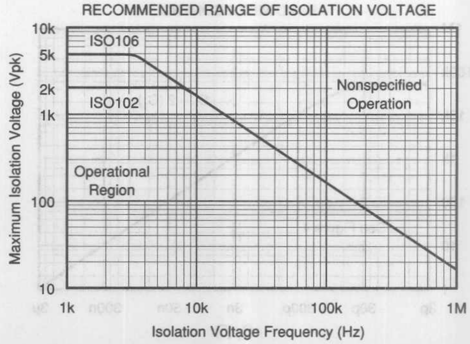
TOTAL HARMONIC DISTORTION



LARGE SIGNAL TRANSIENT RESPONSE

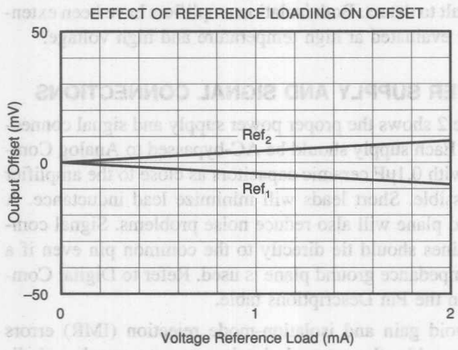


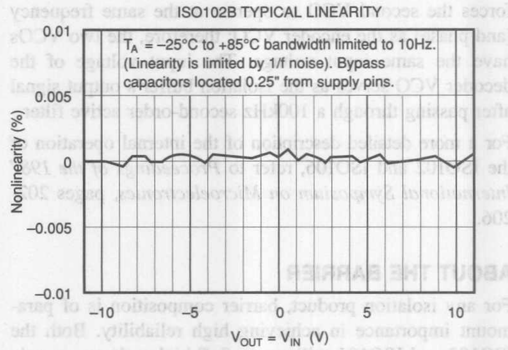
RECOMMENDED RANGE OF ISOLATION VOLTAGE



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.





THEORY OF OPERATION

The ISO102 and ISO106 have no galvanic connection between the input and output. The analog input signal referenced to the input common is accurately duplicated at the output referenced to the output common. Because the barrier information is digital, potentials between the two commons can assume a wide range of voltages and frequencies without influencing the output signal. Signal information remains undisturbed until the slew rate of the barrier voltage exceeds 100V/µs. The isolation amplifier's ability to reject fast dV/dt changes between the two grounds is specified as transient immunity. The amplifier is protected from damage for slew rates up to 100,000V/µs.

A simplified diagram of the ISO102 and ISO106 is shown in Figure 1. The design consists of an input voltage-controlled oscillator (VCO) also known as a voltage-to-frequency converter (VFC), differential capacitors, and output phase lock loop (PLL). The input VCO drives digital levels directly into the two 3pF barrier capacitors. The digital signal is frequency modulated and appears differentially across the barrier, while the externally applied isolation voltage appears common-mode.

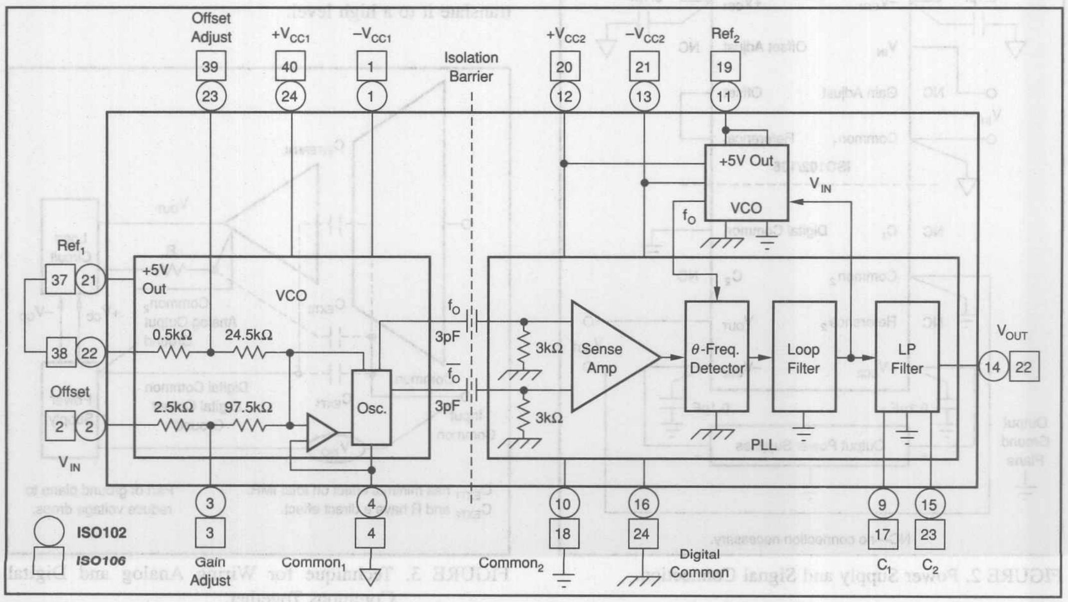


FIGURE 1. Simplified Diagram of ISO102 and ISO106.

A sense amplifier detects only the differential information. The output stage decodes the frequency modulated signal by the means of a PLL. The feedback of the PLL employs a second VCO that is identical to the encoder VCO. The PLL forces the second VCO to operate at the same frequency (and phase) as the encoder VCO; therefore, the two VCOs have the same input voltage. The input voltage of the decoder VCO serves as the isolation buffer's output signal after passing through a 100kHz second-order active filter.

For a more detailed description of the internal operation of the ISO102 and ISO106, refer to *Proceedings of the 1987 International Symposium on Microelectronics,* pages 202-206.

ABOUT THE BARRIER

For any isolation product, barrier composition is of paramount importance in achieving high reliability. Both the ISO102 and ISO106 utilize two 3pF high voltage ceramic coupling capacitors. They are constructed of tungsten thick film deposited in a spiral pattern on a ceramic substrate. Capacitor plates are buried in the package, making the barrier very rugged and hermetically sealed. Capacitance results from the fringing electric fields of adjacent metal runs. Dielectric strength exceeds 10kV and resistance is typically $10^{14}\Omega$. Input and output circuitry are contained in separate solder-sealed cavities, resulting in the industry's first fully hermetic hybrid isolation amplifier.

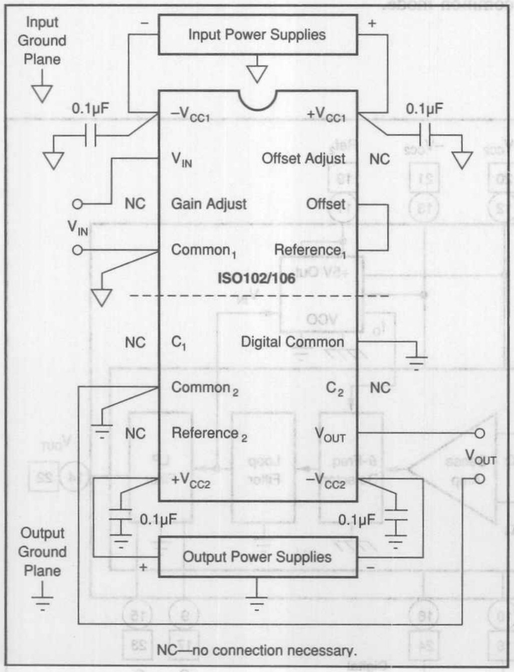


FIGURE 2. Power Supply and Signal Connection.

The ISO102 and ISO106 are designed to be free from partial discharge at rated voltages. Partial discharge is a form of localized breakdown that degrades the barrier over time. Since it does not bridge the space across the barrier, it is difficult to detect. Both isolation amplifiers have been extensively evaluated at high temperature and high voltage.

POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 2 shows the proper power supply and signal connections. Each supply should be AC-bypassed to Analog Common with 0.1µF ceramic capacitors as close to the amplifier as possible. Short leads will minimize lead inductance. A ground plane will also reduce noise problems. Signal common lines should tie directly to the common pin even if a low impedance ground plane is used. Refer to Digital Common in the Pin Descriptions table.

To avoid gain and isolation-mode rejection (IMR) errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Any capacitance across the barrier will increase AC leakage current and may degrade high frequency IMR. The schematic in Figure 3 shows the proper technique for wiring analog and digital commons together.

DISCUSSION OF SPECIFICATIONS

The ISO102 and ISO106 are unity gain buffer isolation amplifiers primarily intended for high level input voltages on the order of 1V to 10V. They may be preceded by operational, differential, or instrumentation amplifiers that precondition a low level signal on the order of millivolts and translate it to a high level.

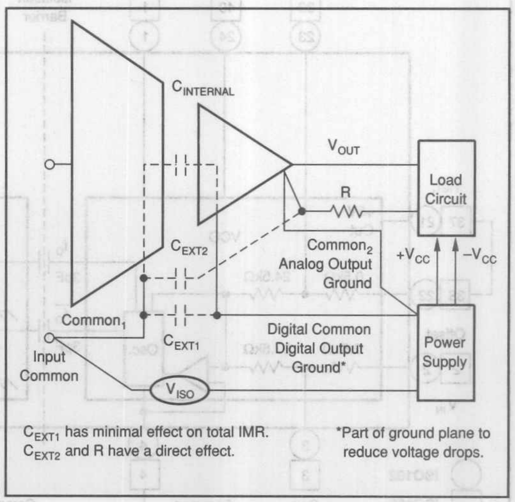


FIGURE 3. Technique for Wiring Analog and Digital Commons Together.

ISOLATION-MODE REJECTION

The IS0102 and IS0106 provide exceptionally high isolation-mode rejection over a wide range of isolation-mode voltages and frequencies. The typical performance curves should be used to insure operation within the recommended range. The maximum barrier voltage allowed decreases as the frequency of the voltage increases. As with all isolation amplifiers, a change of voltage across the barrier will induce leakage current across the barrier. In the case of the IS0102 and IS0106, there exists a threshold of leakage current through the signal capacitors that can cause over-drive of the decoder's sense amplifier. This occurs when the slew rate of the isolation voltage reaches 100V/µs. The output will recover in about 50µs from transients exceeding 100V/µs.

The first two performance curves indicate the expected isolation-mode rejection over a wide range of isolation voltage frequencies. Also plotted is the typical leakage current across the barrier at 240Vrms. The majority of the leakage current is between the input common pin and the output digital ground pin.

The IS0102 and IS0106 are intended to be continuously operated with fully rated isolation voltage and temperature without significant drift of gain and offset. See the "Gain Error/Offset Isolation Voltage" performance curve for changes in gain and offset with isolation voltage.

SUPPLY AND TEMPERATURE RANGE

The IS0102 and IS0106 are rated for +15V supplies; however, they are guaranteed to operate from ±10V to ±20V. Performance is also rated for an ambient temperature range of –25°C to +85°C. For operation outside this temperature range, refer to the "Power Dissipation vs Temperature" performance curve to establish the maximum allowed supply voltage. Supply currents are fairly insensitive to changes in supply voltage or temperature. Therefore, the maximum current limits can be used in computing the maximum junction temperature under nonrated conditions.

OPTIONAL BANDWIDTH CONTROL

The following discussion relates optimum dynamic range performance to bandwidth, noise, and settling time.

The outputs of the IS0102 and IS0106 are the outputs of a second-order low-pass Butterworth filter. Its low impedance output is rated for ±5mA drive and ±12V range with 10,000pF loads. The closed-loop bandwidth of the PLL is 70kHz, while the output filter is internally set at 100kHz. The output filter lowers the residual voltage of the barrier FM signal to below the noise floor of the output signal.

Two pins are available for optional modification of the filter's bandwidth. Only two capacitors are required. The "Bandwidth Control" performance curve gives the value of C_1 (C_2 is equal to twice C_1) for the desired bandwidth. Figure 4 illustrates the optional connection of both capacitors.

A tradeoff can be achieved between the required signal bandwidth and system dynamic range. The noise floor of the output limits the dynamic range of the output signal. The noise power varies with the square root of the bandwidth of the buffer. It is recommended that the bandwidth be reduced to about twice the maximum signal bandwidth for optimum dynamic range as shown in the "Dynamic Range vs Bandwidth" performance curve. The output spectral noise density measurement is displayed in the "Output Spectral Noise Density" performance curve. The noise is flat to within 5dB$\sqrt{\text{Hz}}$ between 0.1Hz to 70kHz.

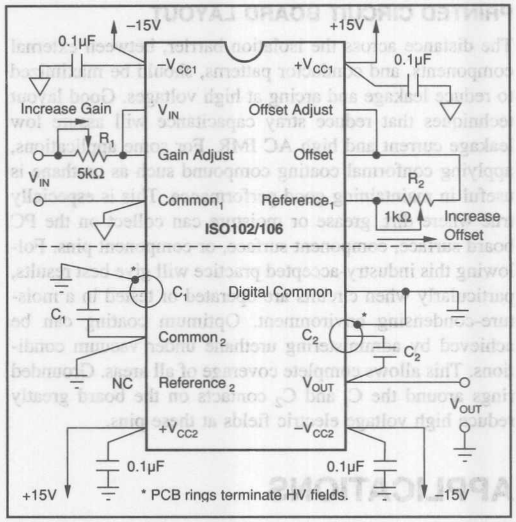


FIGURE 4. Optional Gain Adjust, Offset Adjust, and Bandwidth Control.

The overall AC gain of the buffer amplifiers is shown in two performance curves: "Gain Flatness vs Frequency" and "Gain/Phase vs Frequency." Note that with C_1 = 100pF and C_2 = 200pF, the AC gain remains flat within ±0.01dB up to 7kHz. The total harmonic distortion for large-signal sine wave outputs is plotted in the "Total Harmonic Distortion" performance curve. The phase-lock-loop displays slightly nonuniform rise and fall edges under maximum slew conditions. Reducing the output filter bandwidth to below 70kHz smooths the output signal and eliminates any overshoot. See the "Large Signal Transient Response" performance curve.

OPTIONAL OFFSET AND GAIN ADJUSTMENT

In many applications the factory-trimmed offset is adequate. For situations where reduced or modified gain and offset are required, adjustment of each is easy. The addition of two potentiometers as shown in Figure 4 provides for a two step calibration.

Offset should be adjusted first. Gain adjustment does not interfere with offset. The potentiometer's TCR adds only 2% to overall temperature drift. The offset and gain adjustment procedures are as follows:

1. Set V_{IN} to 0V and adjust R_1 to desired offset at the output.
2. Set V_{IN} to full scale (not zero). Adjust R_2 for desired gain.

The distance across the isolation barrier, between external components, and conductor patterns, should be maximized to reduce leakage and arcing at high voltages. Good layout techniques that reduce stray capacitance will assure low leakage current and high AC IMR. For some applications, applying conformal coating compound such as urethane is useful in maintaining good performance. This is especially true where dirt, grease or moisture can collect on the PC board surface, component surface, or component pins. Following this industry-accepted practice will give best results, particularly when circuits are operated or tested in a moisture-condensing environment. Optimum coating can be achieved by administering urethane under vacuum conditions. This allows complete coverage of all areas. Grounded rings around the C_1 and C_2 contacts on the board greatly reduce high voltage electric fields at these pins.

APPLICATIONS

The ISO102 and ISO106 isolation amplifiers are used in three categories of applications:

1. Accurate isolation of signals from high voltage ground potentials,
2. Accurate isolation of signals from severe ground noise, and
3. Fault protection from high voltages in analog measurement systems.

Figures 5 through 15 show a variety of application circuits. Additional discussion of applications can be found in the December 11, 1986 issue of *Electronic Design,* pages 91-96.

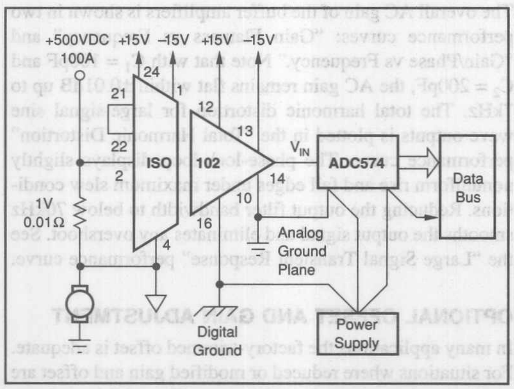


FIGURE 5. Isolated Power Current Monitor for Motor Circuit. (The ISO102 allows reliable, safe measurement at high voltages.)

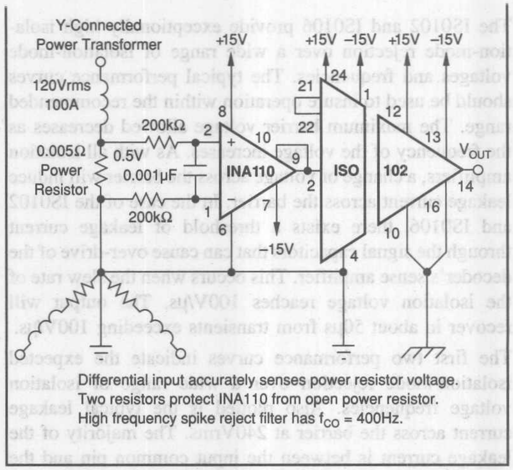


FIGURE 6. Isolated Power Line Monitor (0.5µA leakage current at 120Vrms).

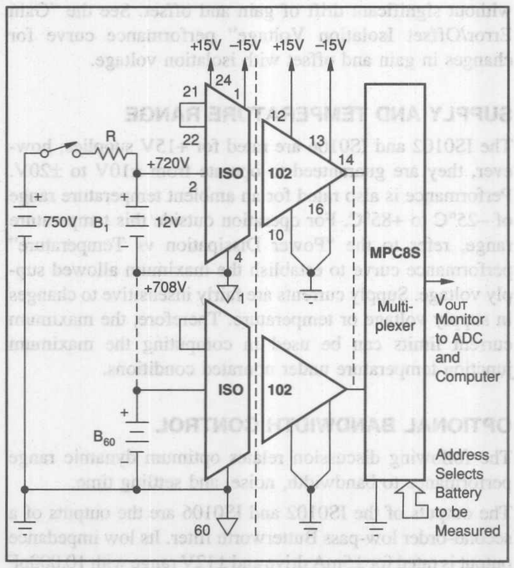


FIGURE 7. Battery Monitor for High Voltage Charging Circuit.

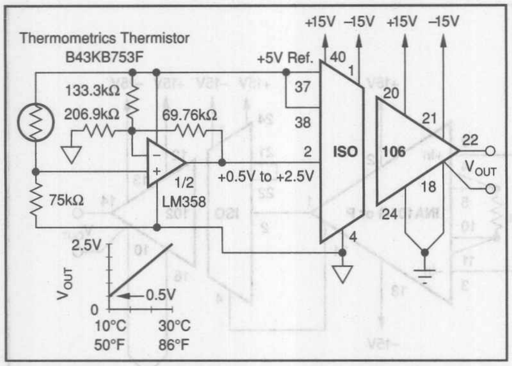


FIGURE 8. Isolated RTD Temperature Amplifier.

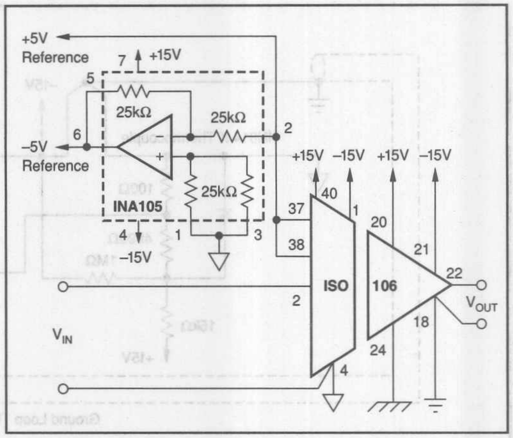


FIGURE 10. Isolation Amplifier with Isolated Bipolar Input Reference.

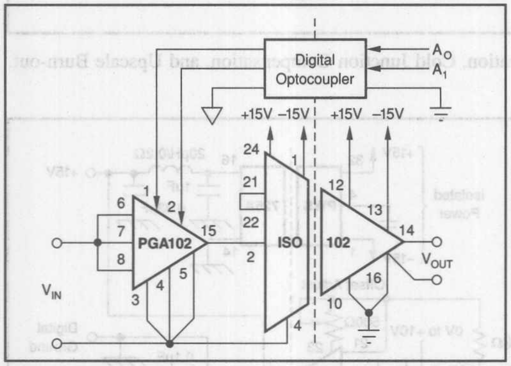


FIGURE 9. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

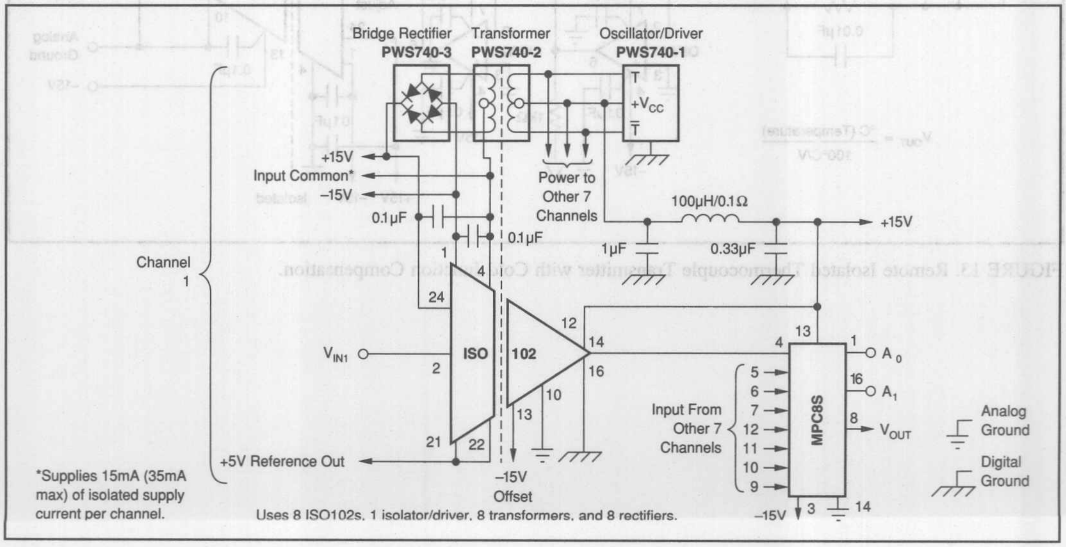


FIGURE 11. Low Cost Eight-Channel Isolation Amplifier Block with Channel-to-Channel Isolation.

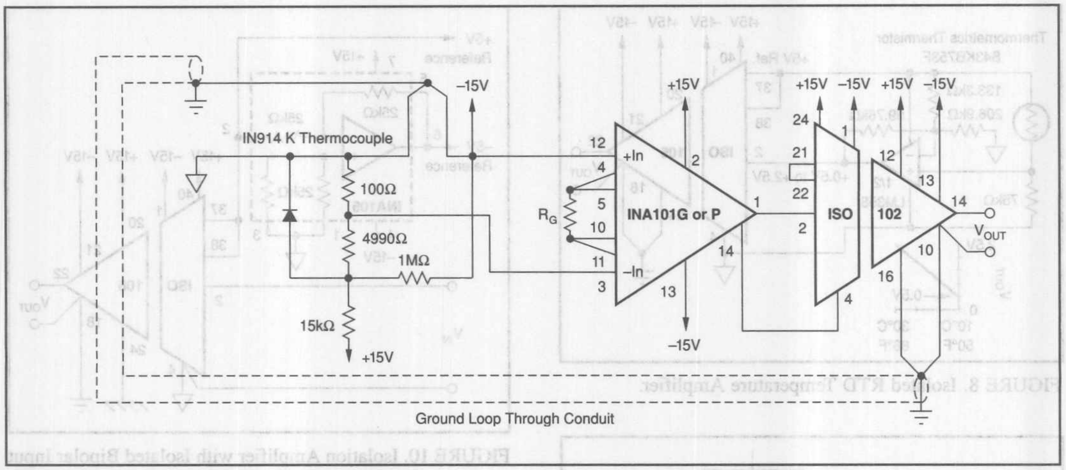


FIGURE 12. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Upscale Burn-out.

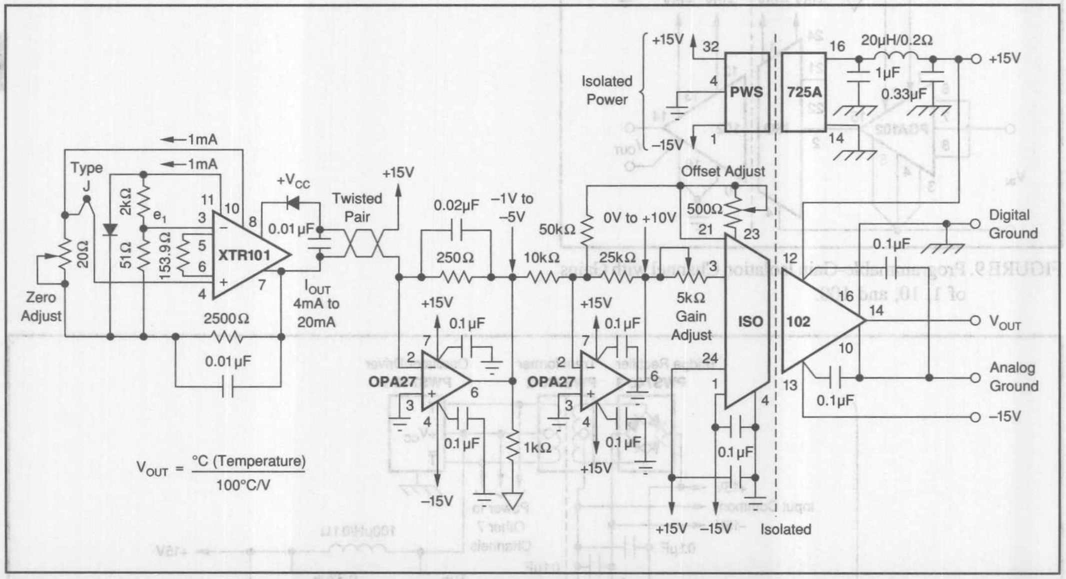


FIGURE 13. Remote Isolated Thermocouple Transmitter with Cold Junction Compensation.

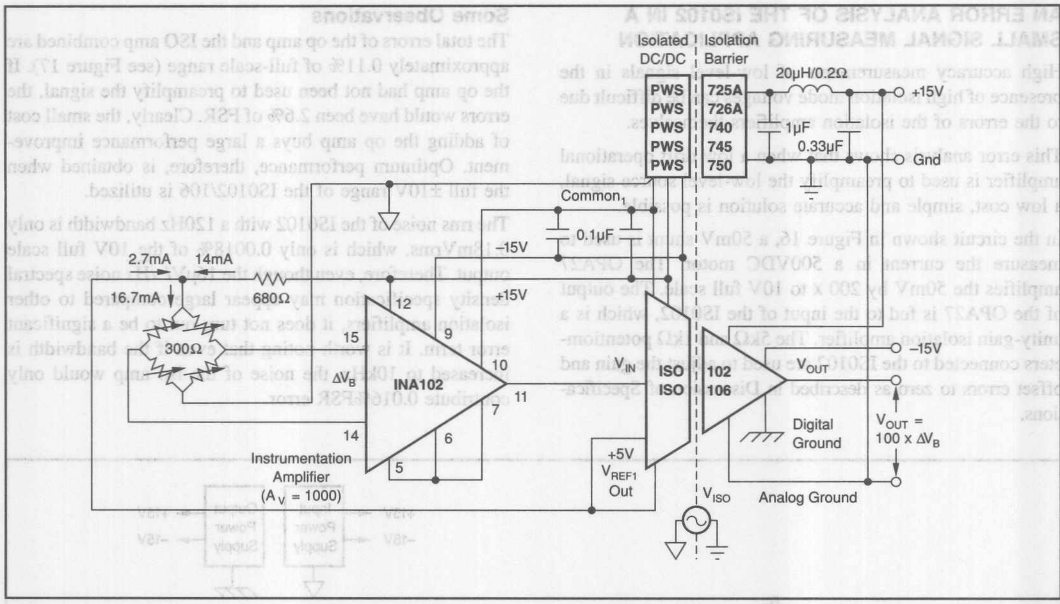


FIGURE 14. Isolated Instrumentation Amplifier for 300Ω Bridge. (Reference voltage from isolation amplifier is used to excite bridge.)

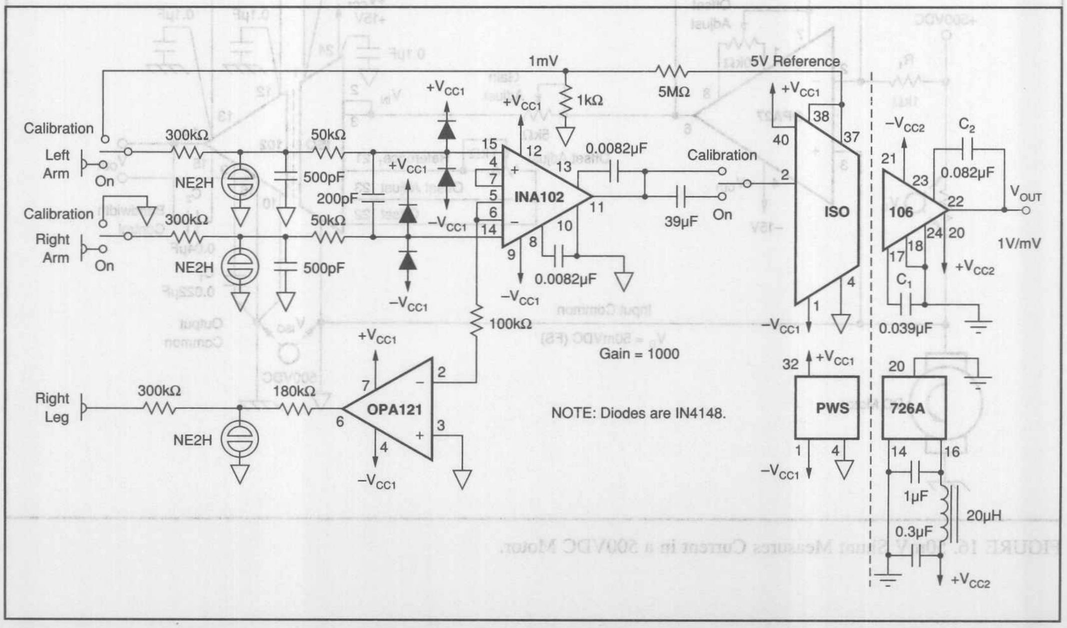


FIGURE 15. Right-Leg-Driven ECG Amplifier (with defibrillator protection and calibrator).

SMALL SIGNAL MEASURING APPLICATION

High accuracy measurements of low-level signals in the presence of high isolation mode voltages can be difficult due to the errors of the isolation amplifiers themselves.

This error analysis shows that when a low drift operational amplifier is used to preamplify the low-level source signal, a low cost, simple and accurate solution is possible.

In the circuit shown in Figure 16, a 50mV shunt is used to measure the current in a 500VDC motor. The OPA27 amplifies the 50mV by 200 x to 10V full scale. The output of the OPA27 is fed to the input of the ISO102, which is a unity-gain isolation amplifier. The 5kΩ and 1kΩ potentiometers connected to the ISO102 are used to adjust the gain and offset errors to zero as described in Discussion of Specifications.

Some Observations

The total errors of the op amp and the ISO amp combined are approximately 0.11% of full-scale range (see Figure 17). If the op amp had not been used to preamplify the signal, the errors would have been 2.6% of FSR. Clearly, the small cost of adding the op amp buys a large performance improvement. Optimum performance, therefore, is obtained when the full ±10V range of the ISO102/106 is utilized.

The rms noise of the ISO102 with a 120Hz bandwidth is only 0.18mVrms, which is only 0.0018% of the 10V full scale output. Therefore, even though the $16\mu V/\sqrt{Hz}$ noise spectral density specification may appear large compared to other isolation amplifiers, it does not turn out to be a significant error term. It is worth noting that even if the bandwidth is increased to 10kHz, the noise of the iso amp would only contribute 0.016%FSR error.

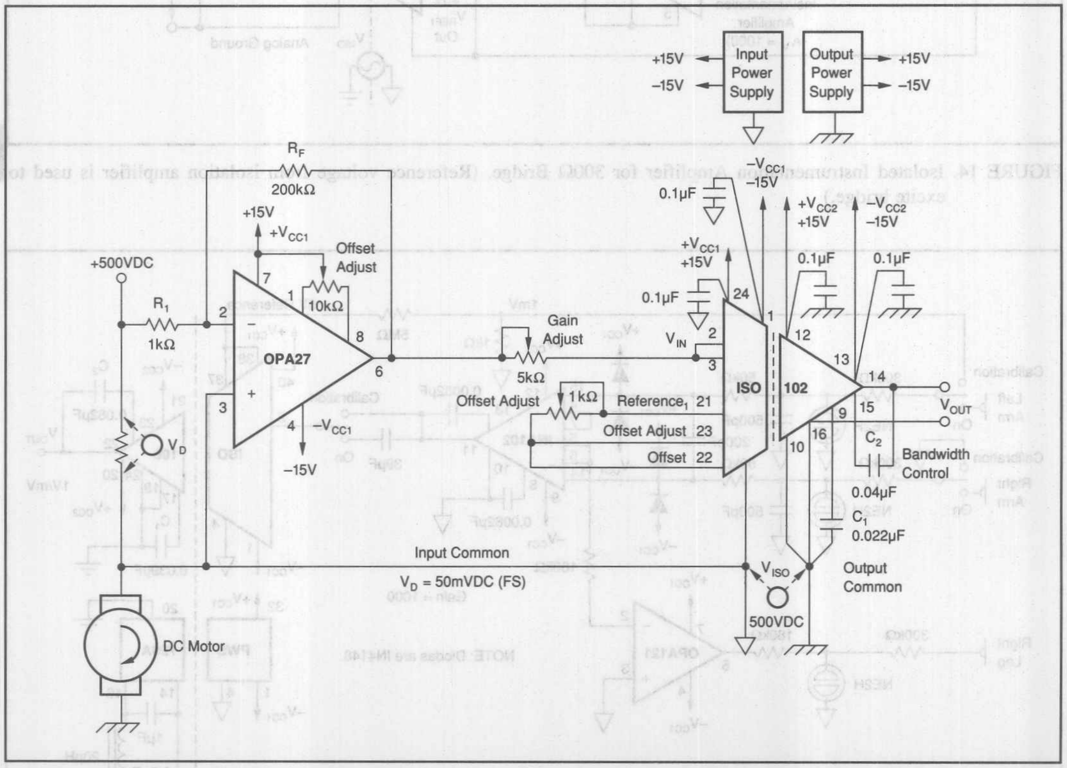


FIGURE 16. 50mV Shunt Measures Current in a 500VDC Motor.

The Errors of the Op Amp at 25°C (Referred to Input, RTI)

$$V_{E\,(OPA)} = V_D\left\{1 - \frac{1}{1 + \frac{1}{\beta A_{VOL}}}\right\} + V_{OS}\,(1 + R_1/R_F) + I_B R_1 + \text{P.S.R.} + \text{Noise}$$

$V_{E\,(OPA)}$ = Total Op Amp Error (RTI)

V_D = Differential Voltage (Full Scale) Across Shunt

$\left\{1 - \frac{1}{1 + \frac{1}{\beta A_{VOL}}}\right\}$ = Gain Error Due to Finite Open Loop Gain

β = Feedback Factor

A_{VOL} = Open Loop Gain at Signal Frequency

V_{OS} = Input Offset Voltage

I_B = Input Bias Current

P.S.R. = Power Supply Rejection (µV/V) [Assuming a 5% change with ±15V supplies. Total error is twice that due to one supply.]

Noise = $5nV/\sqrt{Hz}$ (for 1kΩ source resistance and 1kHz bandwidth)

$ERROR_{(OPA)}$ (RTI)		GAIN ERROR		OFFSET		P.S.R.		NOISE
$V_{E\,(OPA)}$	=	$50mV\left\{1 - \frac{1}{1 + \frac{1}{10^6/200}}\right\}$		$\{0.025mV\,(1 + 1/200) + 40 \times 10^{-9} \times 10^3\}$		($20\mu V/V \times 0.75V \times 2$)		$\{5nV\sqrt{120}$ (nVrms)$\}$
	=	0.01mV		(0.0251mV + 0.04mV)	+	0.03mV	+	0.055×10^{-3}mVrms
Error as % of FSR	=	0.02%	+	(0.05% + 0.08%)	+	0.06%	+	0.00011%
After Nulling								
	=	0.01mV	+	(0mV + 0mV)	+	0.03mV	+	0.055×10^{-3}mVrms
	=	0.10mV						
Error as % of FSR*	=	0.02%	+	(0% + 0%)	+	0.06%	+	0.00011%
	=	0.08% of 50mV						

*FSR = Full-Scale Range. 50mV at input to op amp, or 10V at input (and output) of ISO amp.

The Errors of the Iso Amp at 25°C (RTI)

$$\boxed{V_{E\,(ISO)} = 1/200\,(V_{ISO}/IMR + V_{OS} + \text{G.E.} + \text{Nonlinearity} + \text{P.S.R.} + \text{Noise})}$$

$V_{E\,(ISO)}$ = Total ISO Amp Error

IMR = Isolation Mode Rejection

V_{OS} = Input Offset Voltage

$V_{ISO} = V_{IMV}$ = Isolation Voltage = Isolation Mode Voltage

G.E. = Gain Error (% of FSR)

Nonlinearity = Peak-to-Peak deviation of output voltage from best-fit straight line. It is expressed as ratio based on full-scale range.

P.S.R. = Change in V_{OS}/10V x Supply Change

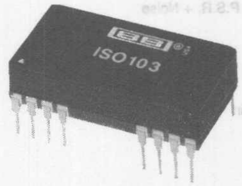
Noise = Spectral noise density x $\sqrt{\text{bandwidth}}$. It is recommended that bandwidth be limited to twice maximum signal bandwidth for optimum dynamic range.

$ERROR_{(ISO)}$ (RTI)		IMR		V_{OS}		G.E.		NONLINEARITY		P.S.R.		NOISE
$V_{E\,(ISO)}$	=	1/200 { 500VDC/140dB	+	70mV	+	20V x 0.25/100	+	0.003/100 x 20V		1.4mV x 0.75V x 2	+	$16\mu V\sqrt{120}$ (rms) }
	=	1/200 { 0.05mV	+	70mV	+	50mV	+	0.6mV	+	2.1mV	+	0.175mVrms }
Error as % of FSR	=	0.0005%	+	0.7%	+	0.5%	+	0.006%	+	0.021%	+	0.00175%
After Nulling												
$V_{E\,(ISO)}$	=	1/200 { 0.05mV	+	0mV	+	0mV	+	0.6mV	+	2.1mV	+	0.175mVrms }
	=	1/200 (3.0mV)										
	=	0.03mV										
Error as % of FSR	=	0.0005%	+	0%	+	0%	+	0.006%	+	0.021%	+	0.00175%
	=	0.03% of 50mV										

Total Error	=	$V_{E\,(OPA)}$	+	$V_{E\,(ISO)}$
	=	0.10mV	+	0.03mV
	=	0.08% of 50mV	+	0.03% of 50mV
	=	0.11% of 50mV		

FIGURE 17. Op Amp and Iso Amp Error Analysis.

BURR - BROWN®



ISO103

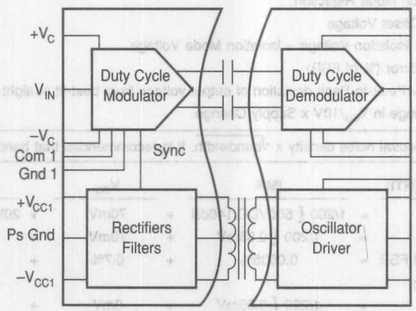
Low-Cost, Internally Powered ISOLATION AMPLIFIER

FEATURES

- SIGNAL AND POWER IN ONE DOUBLE-WIDE (0.6") SIDE-BRAZED PACKAGE
- 5600Vpk TEST VOLTAGE
- 1500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: –10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)
- BOARD AREA ONLY 0.72in.² (4.6cm²)

APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- ISOLATED 4-20mA LOOP RECEIVER AND POWER
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION



*Ground if not used

DESCRIPTION

The ISO103 isolation amplifier provides both signal and power across an isolation barrier. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 1500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO103 easy to use, as well as providing for compact PC board layouts.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At $T_A = +25°C$ and $V_{CC2} = ±15V$, ±15mA output current unless otherwise noted.

		ISO103			ISO103B			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ISOLATION								
Rated Continuous Voltage(1)								
AC, 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
Test Breakdown, 100% AC, 60Hz	10s	5657			*			Vpk
Isolation-Mode Rejection	1500Vrms, 60Hz		130			*		dB
	2121VDC		160			*		dB
Barrier Impedance			10^{12} || 9			*		Ω || pF
Leakage Current	240Vrms, 60Hz		1	2		*	*	µA
GAIN								
Nominal			1			*		V/V
Initial Error			±0.12	±0.3		±0.08	±0.15	% FSR
Gain vs Temperature			±60	±100		±20	±50	ppm/°C
Nonlinearity	V_O = –10V to 10V		±0.026	±0.075		±0.018	±0.050	% FSR
	V_O = –5V to 5V		±0.009			*	±0.025	%FSR
INPUT OFFSET VOLTAGE								
Initial Offset			±20	±60		*	*	mV
vs Temperature			±300	±500		±100	±250	µV/°C
vs Power Supplies	V_{CC2} = ±10V to ±18V		0.9			*		mV/V
vs Output Supply Load	I_O = 0 to ±50mA		±0.3			*		mV/mA
SIGNAL INPUT								
Voltage Range	Output Voltage in Range	±10	±15		*	*		V
Resistance			200			*		kΩ
SIGNAL OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±15		*	*		mA
Ripple Voltage, 800kHz Carrier			25			*		mVp-p
	400Ω/4.7nF (See Figure 4)		5			*		mVp-p
Capacitive Load Drive			1000			*		pF
Voltage Noise			4			*		µV/√Hz
FREQUENCY RESPONSE								
Small Signal Bandwidth			20			*		kHz
Slew Rate			1.5			*		V/µs
Settling Time	0.1%, –10/10V		75			*		µs
POWER SUPPLIES								
Rated Voltage, V_{CC2}			±15			*		V
Voltage Range		±10		±18	*		*	V
Input Current	I_O = ±15mA		+90/–4.5			*		mA
	I_O = 0mA		+60/–4.5			*		mA
Ripple Current	No Filter		60			*		mAp-p
	C_{IN} = 1µF		3			*		mAp-p
Rated Output Voltage	Load = 15mA	±14.25	±15	±15.75	*	*	*	V
Output	50mA Balanced Load	10				*	*	V
	100mA Single-Ended Loads	10				*	*	V
Load Regulation	Balanced Load		0.3			*		%/mA
Line Regulation			1.12			*		V/V
Output Voltage vs Temperature			2.5			*		mV/°C
Voltage Balance Error, $±V_{CC1}$			0.05			*		%
Voltage Ripple (800kHz)	No External Capacitors		50			*		mVp-p
	C_{EXT} = 1µF		5			*		mVp-p
Output Capacitive Load				1			*	µF
Sync Frequency	Sync-Pin Grounded (2)		1.6			*		MHz
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	*		*	°C
Storage		–25		+125	*		*	°C

* Specifications same as ISO103.

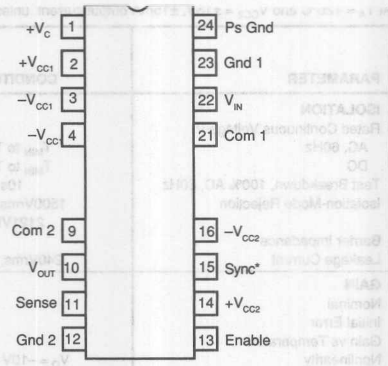
NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute. (2) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

Com 1 to Gnd 1 or Com 2 to Gnd 2 .... ±200mV
Enable, Sync .... 0V to $+V_{CC2}$
Continuous Isolation Voltage 1500Vrms
V_{ISO}, dv/dt 20kV/µs
Junction Temperature .... 150°C
Storage Temperature .... –25°C to +125°C
Lead Temperature,10s .... 300°C
Output Short to Gnd 2 Duration .... Continuous
$\pm V_{CC1}$ to Gnd 1 Duration .... Continuous

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.



*Operation requires this pin be grounded or driven with TTL levels.

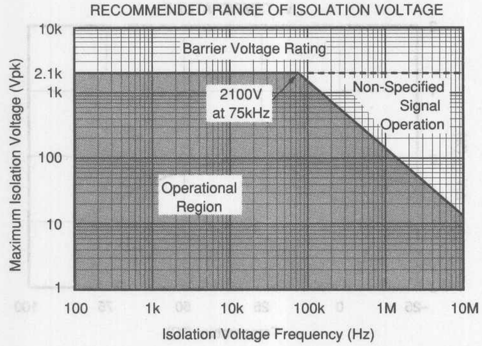
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[(1)]
ISO103	24-Pin DIP	231

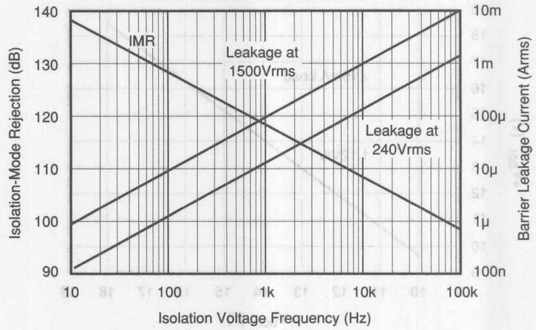
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

$T_A = +25°C$, $V_{CC2} = ±15VDC$, ±15mA output current unless otherwise noted.

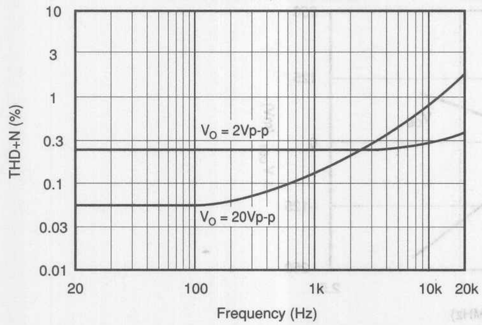
RECOMMENDED RANGE OF ISOLATION VOLTAGE



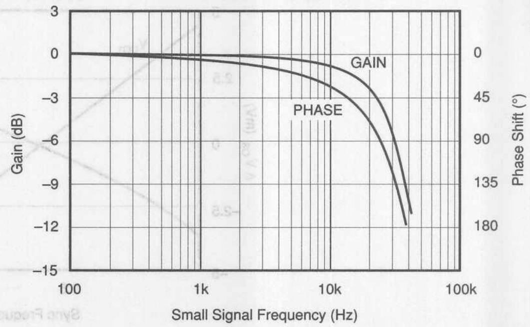
IMR/LEAKAGE vs FREQUENCY



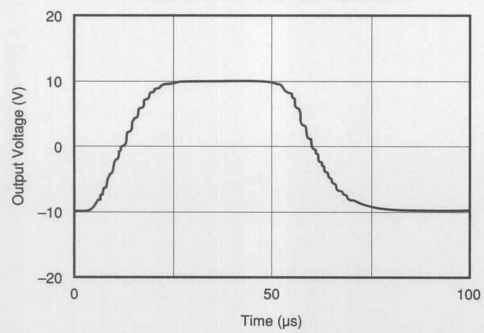
DISTORTION vs FREQUENCY



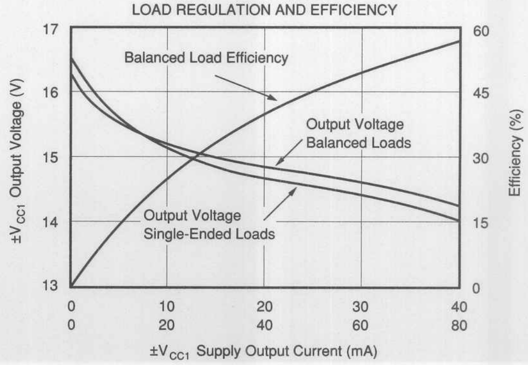
GAIN/PHASE vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE



ISOLATED POWER SUPPLY LOAD REGULATION AND EFFICIENCY



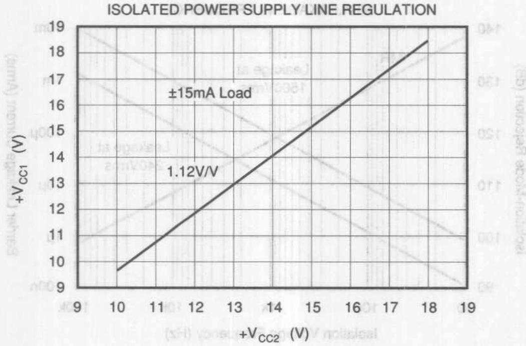
ISO103

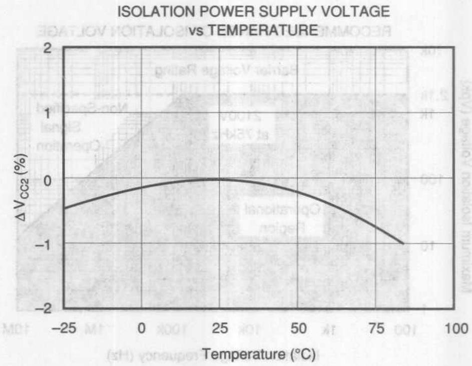
5

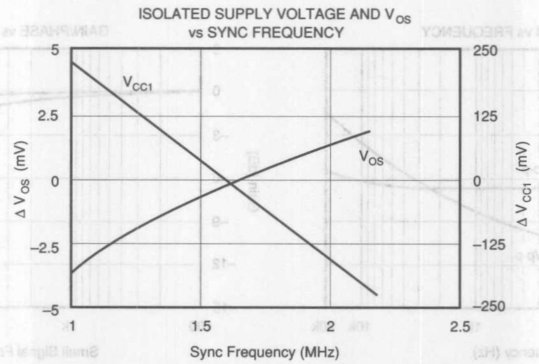
ISOLATION PRODUCTS

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_{CC2} = ±15VDC$, ±15mA output current unless otherwise noted.







THEORY OF OPERATION

The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminate beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the input side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, result in a simple, reliable design.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC2}$, an option recommended if more than ±15mA are drawn from the isolated supply. Separate rectifier output pins ($\pm V_{CC1}$) and amplifier supply input pins ($\pm V_C$) allow additional ripple filtering and/or regulation. The separate input and output common pins and output sense are low current inputs tied to the signal source ground, output ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, Com 2 to Gnd 2, and Sense to V_{OUT} at the ISO103 socket. The enable pin may be left open if the ISO103 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.2MHz to 2MHz TTL clock signal provides synchronization of multiple units.

The ISO103 isolation amplifier contains a transformer-coupled DC/DC converter that is powered from the output side of the isolation amplifier. All power supply pins (1, 2, 3, 4, 14, and 16) of the ISO103 have an internal 0.1µF capacitor to ground. L_1 is used to slow down fast changes in the input current to the DC/DC converter. C_1 is used to help regulate the voltage ripple caused by the current demands of the converter. L_1, C_1, and C_2 are optional, however, recommended for low noise applications.

The DC/DC converter creates an unregulated ±15V output to $\pm V_{CC1}$. If the ISO103 is the only device using the DC/DC converter for power, pins 1 and 2 and pins 3 and 4 can be connected directly without C_O or L_O in the circuit. If an external capacitor is used in this configuration, it should not exceed 1µF. This configuration is possible because the isolation amplifier and the DC/DC converter are synchronized internally.

If additional devices are powered by the DC/DC converter of the ISO103, the application may require that the ripple voltage of the ISO103 converter be attenuated. In which case, L_O and C_O should be added to the circuit. The inductor is used to attenuate the ripple current and a higher value capacitor can be used to reduce the ripple voltage even further.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of ±0.5% for the values shown; greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictate location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R_1 and R_2 may be reversed.

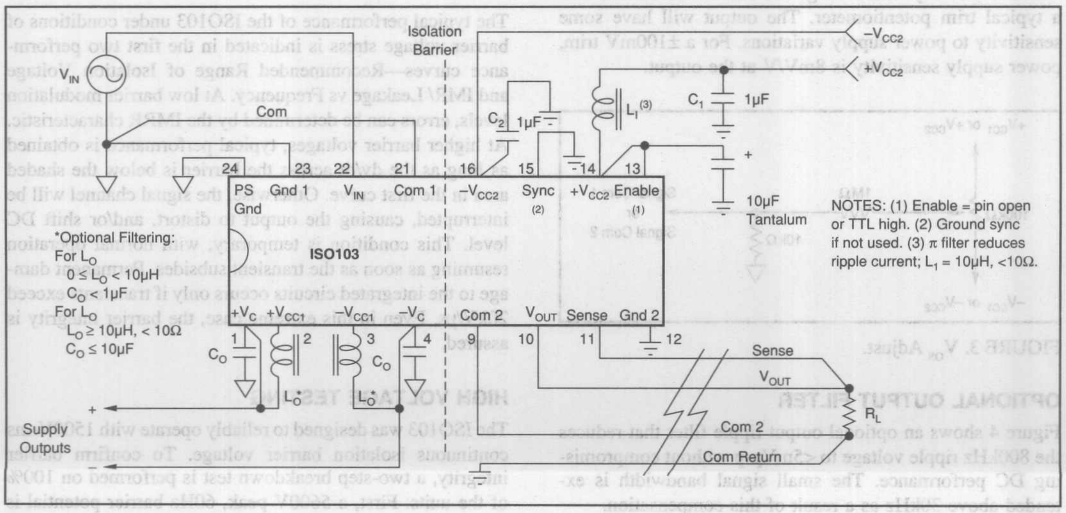


FIGURE 1. Signal and Power Connections.

multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

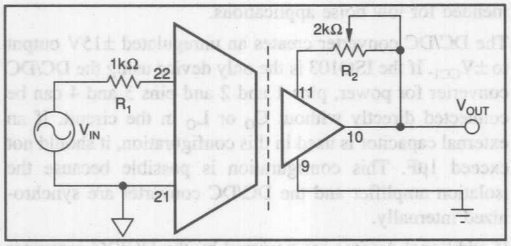


FIGURE 2a. Gain Adjust.

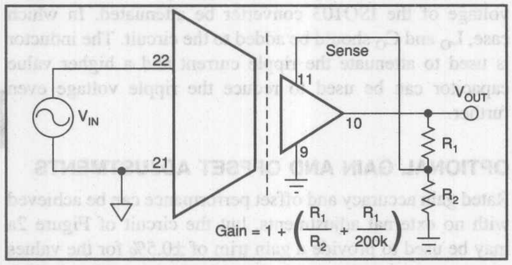


FIGURE 2b. Gain Setting.

Figure 3 shows a method for trimming V_{OS} of the ISO103. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

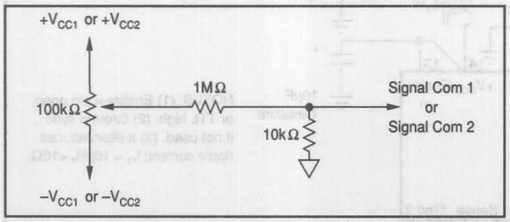


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <5mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

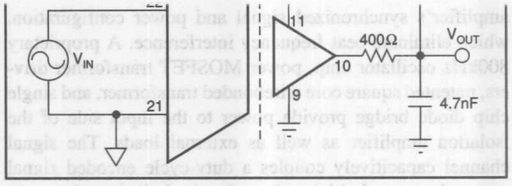


FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO103s can be accomplished by connecting pin 15 of each device to an external TTL level oscillator, as shown in Figure 7. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO103 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull-up resistor can be chosen for different pull-up voltages as shown in Figure 7. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic provided the frequency is between 1.2MHz and 2MHz, and the duty cycle is greater than 25%.

Multichannel synchronization with reduced power dissipation for applications requiring less than ±15mA from V_{CC1} is accomplished by driving both the Sync input pin (15) and Enable pin (13) with the TTL oscillator as shown in Figure 5.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO103 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/ Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO103 was designed to reliably operate with 1500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, a 5600V peak, 60Hz barrier potential is

insulation is above this level. Following this exposure, a 1500Vrms, 60Hz potential is applied for one minute to conform to UL1244. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

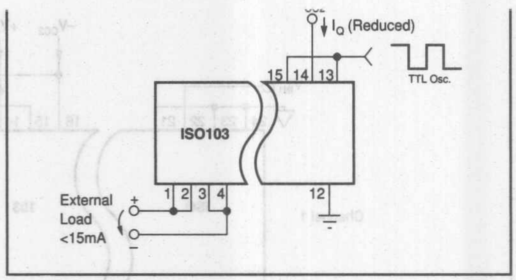


FIGURE 5. Reduced Power Dissipation.

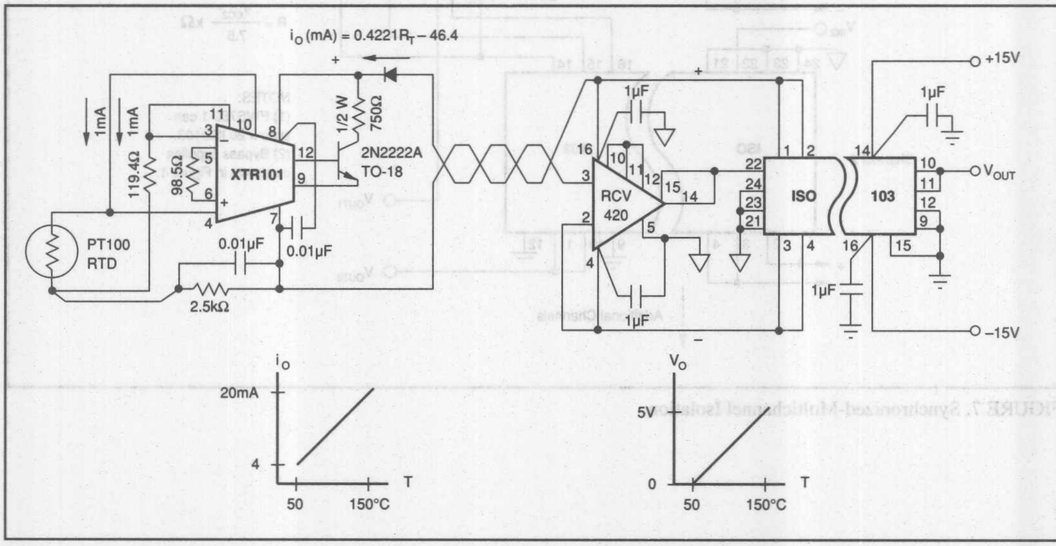


FIGURE 6. Isolated 4-20mA Instrument Loop.

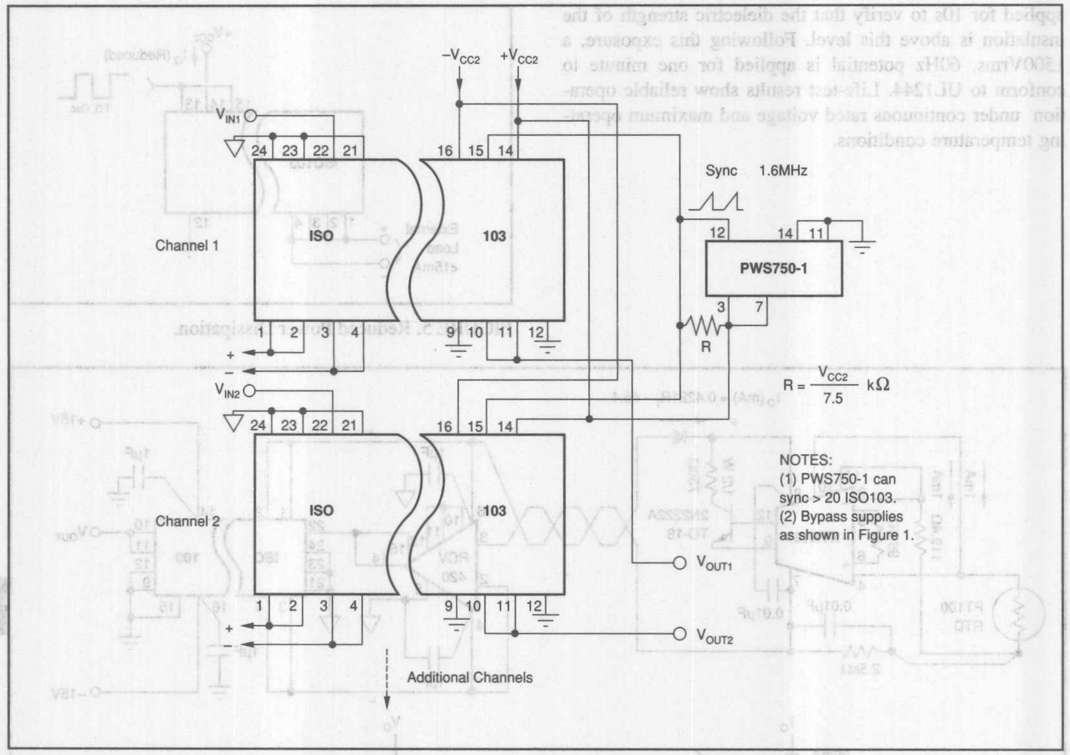
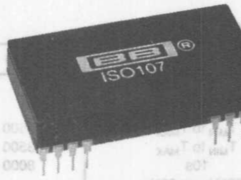


FIGURE 7. Synchronized-Multichannel Isolation.

BURR - BROWN®

ISO107



High-Voltage, Internally Powered ISOLATION AMPLIFIER

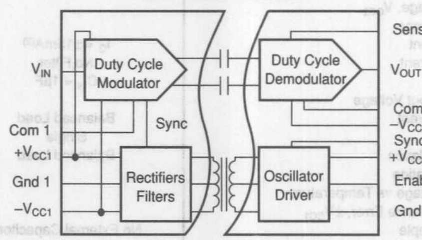
FEATURES

- SIGNAL AND POWER IN ONE TRIPLE-WIDE PACKAGE
- 8000Vpk TEST VOLTAGE
- 2500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: –10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)

APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- BIOMEDICAL INSTRUMENTATION
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION

ISO107 BLOCK DIAGRAM



DESCRIPTION

The ISO107 isolation amplifier provides both signal and power across an isolation barrier. The ceramic side-brazed hybrid package contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 2500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL544 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO107 easy to use, as well as providing for compact PC board layouts.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

T_A = +25°C and V_{CC2} = ±15V, ±15mA output current unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Rated Continuous Voltage (1)					
AC, 60Hz	T_{MIN} to T_{MAX}	2500			Vrms
DC	T_{MIN} to T_{MAX}	3500			VDC
Test Breakdown, AC, 60Hz	10s	8000			Vpk
Isolation-Mode Rejection	2500Vrms, 60Hz		100		dB
	2121VDC		160		dB
Barrier Impedance			10^{12} || 13		Ω || pF
Leakage Current	240Vrms, 60Hz		1.2	2	µA
GAIN					
Nominal			1		V/V
Initial Error			±0.1	±0.25	% FSR
Gain vs Temperature			±50	±120	ppm/°C
Nonlinearity			±0.01	±0.025	% FSR
INPUT OFFSET VOLTAGE					
Initial Offset			±20	±50	mV
vs Temperature			±150	±400	µV/°C
vs Power Supplies	V_{CC2} = ±10V to ±18V		±2		mV/V
INPUT					
Voltage Range	Output Voltage in Range	±10	±15		V
Resistance			200		kΩ
SIGNAL OUTPUT					
Voltage Range		±10	±12.5		V
Current Drive		±5	±15		mA
Ripple Voltage, 800kHz Carrier (See Figure 4)			20		mVp-p
Capacitive Load Drive			1000		pF
Voltage Noise			4		$\mu V/\sqrt{Hz}$
FREQUENCY RESPONSE					
Small Signal Bandwidth			20		kHz
Slew Rate			1.5		V/µs
Settling Time	0.1%, –10/10V		75		µs
POWER SUPPLIES					
Rated Voltage, V_{CC2}			±15		V
Voltage Range		±10		±18	V
Input Current	I_O = ±15mA(2)		+75/–4.5		mA
Ripple Current	No Filter		10		mAp-p
	C_{IN} = 1µF		3		mAp-p
Rated Output Voltage		±14.25	±15	±15.75	V
Output Current	Balanced Load		±15	±50	mA
	Single		30	100	mA
Load Regulation	Balanced Load		0.5		%/mA
Line Regulation			1.18		V/V
Output Voltage vs Temperature			10		mV/°C
Voltage Balance Error, $\pm V_{CC1}$			0.05		%
Voltage Ripple	No External Capacitors		10		mVp-p
Output Capacitive Load (See Figure 1)				1	µF
Sync Frequency	Sync-Pin Grounded(3)		1.6		MHz
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–25		+85	°C
Storage		–25		+125	°C

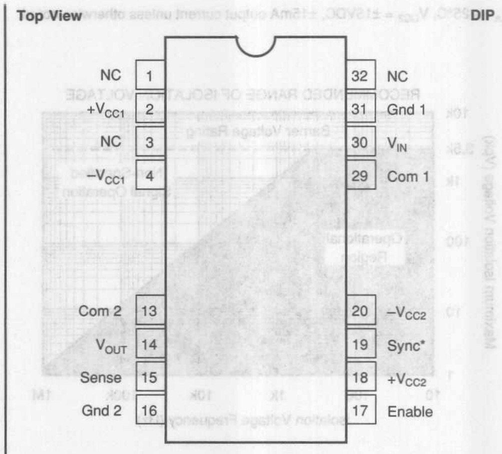
NOTES: (1) Conforms to UL544 test methods. 100% tested at 2500Vrms for 1 minute. (2) For other conditions, see Performance Curve, Input Current ($+V_{CC2}$) vs Output Current. Input Current ($-V_{CC2}$) is constant at –4.5mA (typ) for all output currents. (3) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com 1 to Gnd 1 or Com 2 to Gnd 2	±200mV
Enable, Sync	0V to $+V_{CC2}$
Continuous Isolation Voltage	2500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–25°C to +125°C
Lead Temperature, (soldering, 10s)	300°C
Output Short to Gnd 2 Duration	Continuous
$\pm V_{CC1}$ to Gnd 1 Duration	Continuous

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO107	32-Pin Side-Braze Ceramic	210

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



*Operation requires that this pin be grounded or driven with TTL levels.

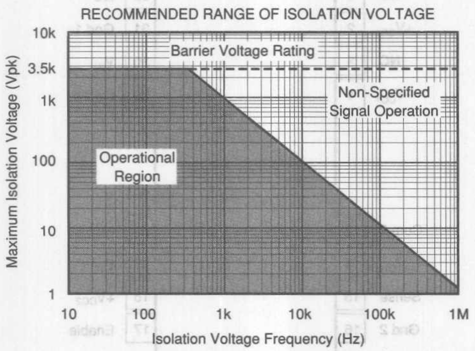
ELECTROSTATIC DISCHARGE SENSITIVITY

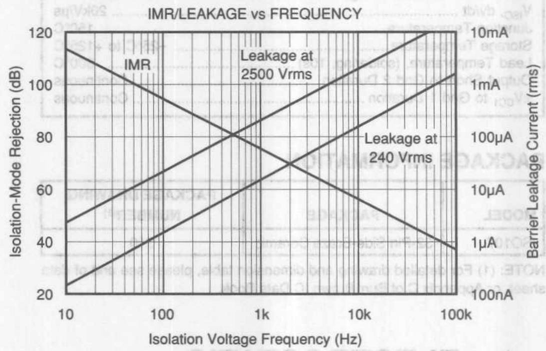
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

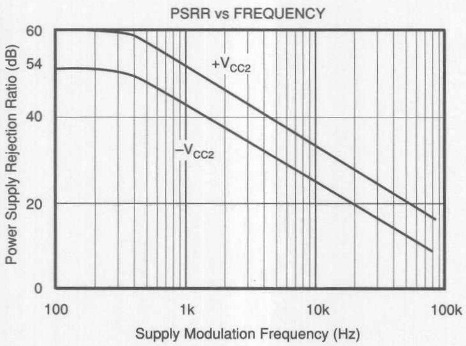
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

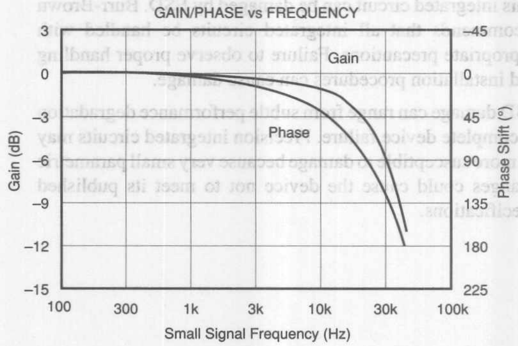
TYPICAL PERFORMANCE CURVES

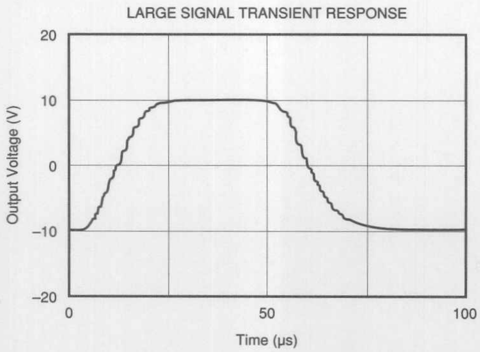
$T_A = +25°C$, $V_{CC2} = ±15VDC$, ±15mA output current unless otherwise noted.

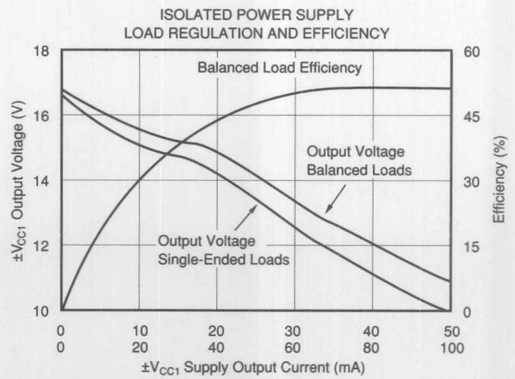








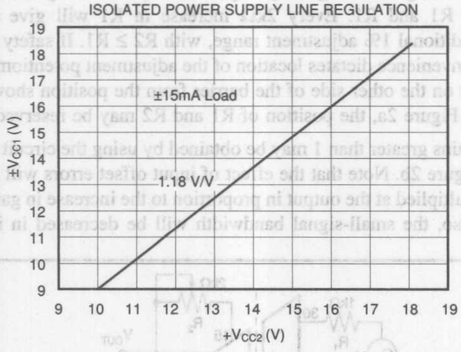




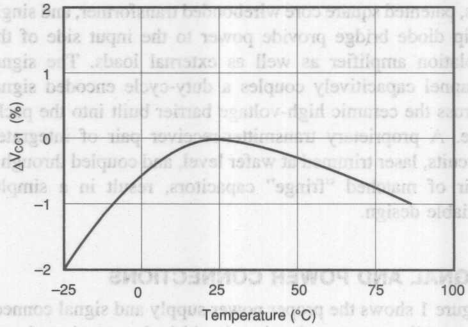
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC2} = ±15VDC, ±15mA output current unless otherwise noted.

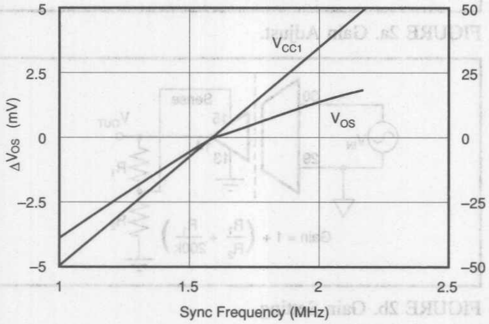
ISOLATED POWER SUPPLY LINE REGULATION



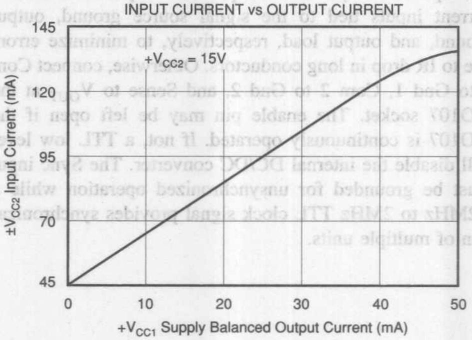
ISOLATED POWER SUPPLY VOLTAGE vs TEMPERATURE



ISOLATED SUPPLY VOLTAGE AND V_{OS} vs SYNC FREQUENCY



ISOLATED POWER SUPPLY INPUT CURRENT vs OUTPUT CURRENT



The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminates beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the input side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, result in a simple, reliable design.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC2}$ an option recommended if more than ±15mA are drawn from the isolated supply. The separate input and output common pins and output sense are low current inputs tied to the signal source ground, output ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, Com 2 to Gnd 2, and Sense to V_{OUT} at the ISO107 socket. The enable pin may be left open if the ISO107 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.2MHz to 2MHz TTL clock signal provides synchronization of multiple units.

with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of ±0.5% for the values shown; greater range may be provided by increasing the size of R1 and R1. Every 2kΩ increase in R1 will give an additional 1% adjustment range, with R2 ≥ R1. If safety or convenience dictates location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R1 and R2 may be reserved.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input offset errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in in-

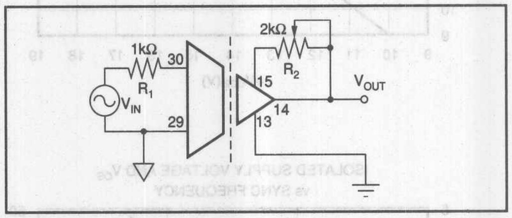


FIGURE 2a. Gain Adjust.

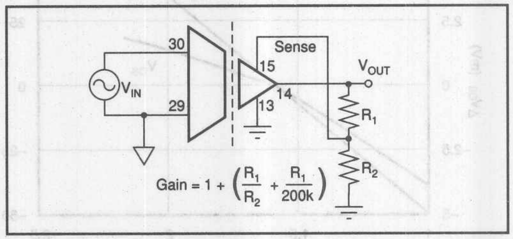


FIGURE 2b. Gain Setting.

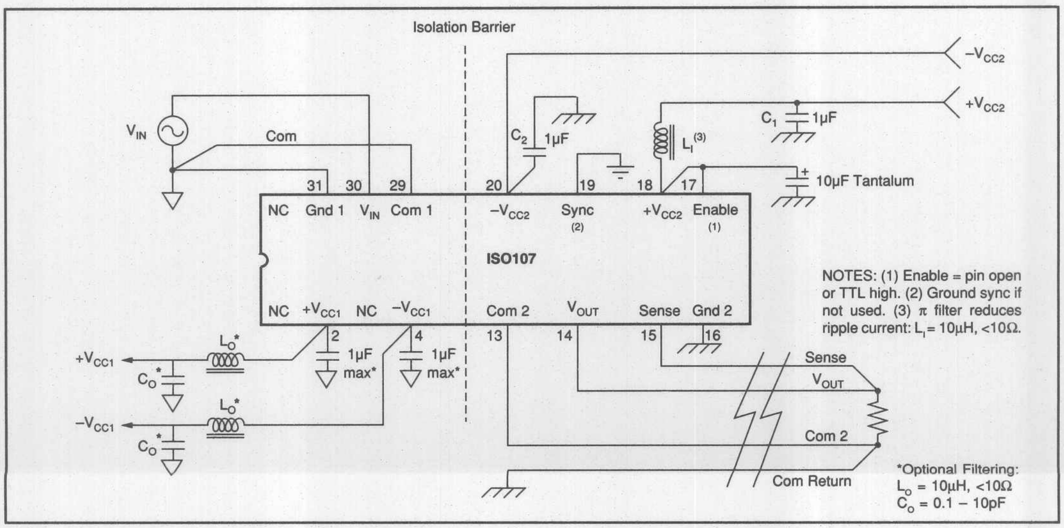


FIGURE 1. Signal and Power Connections.

will provide better overall performance.

Figure 3 shows a method for trimming V_{OS} of the ISO107. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

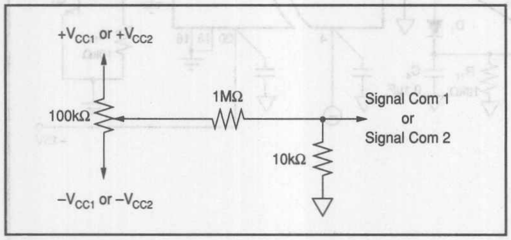


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <3mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

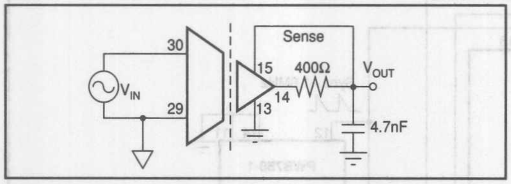


FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO107s can be accomplished by connecting pin 19 of each device to an external TTL level oscillator, as shown in Figure 6. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO107 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull-up resistor can be chosen for different pull-up voltages as shown in Figure 6. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic, provided the frequency is between 1.2MHz and 2MHz, and the duty cycle is greater than 25%.

barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO107 was designed to reliably operate with 2500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, an 8000V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 2500Vrms, 60Hz potential is applied for one minute to conform to UL544. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

APPLICATIONS

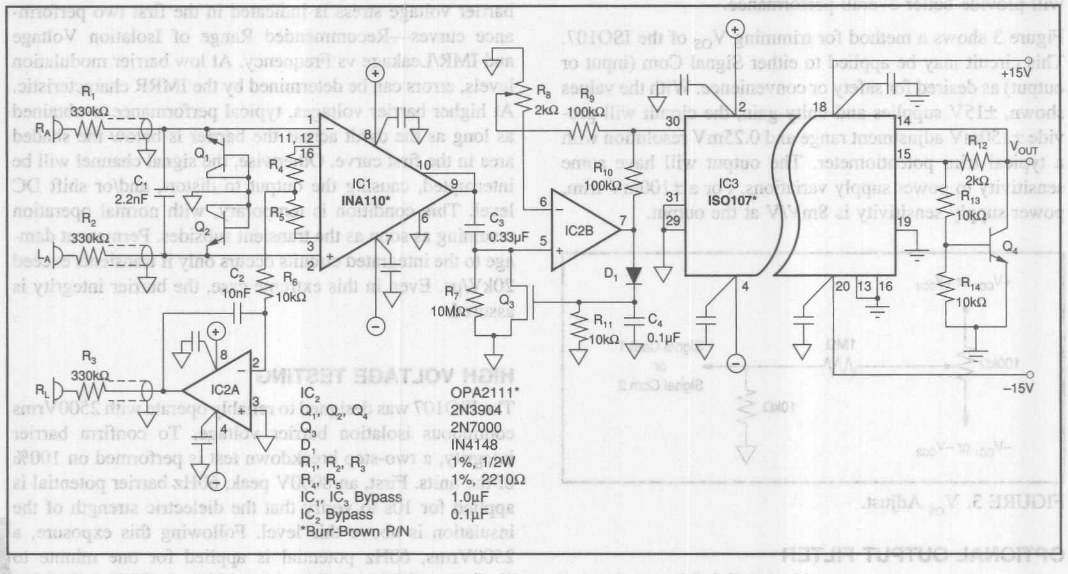


FIGURE 5. ECG Amplifier with Right Leg Drive, Defibrillator Protection, and E.S.U. Blanking.

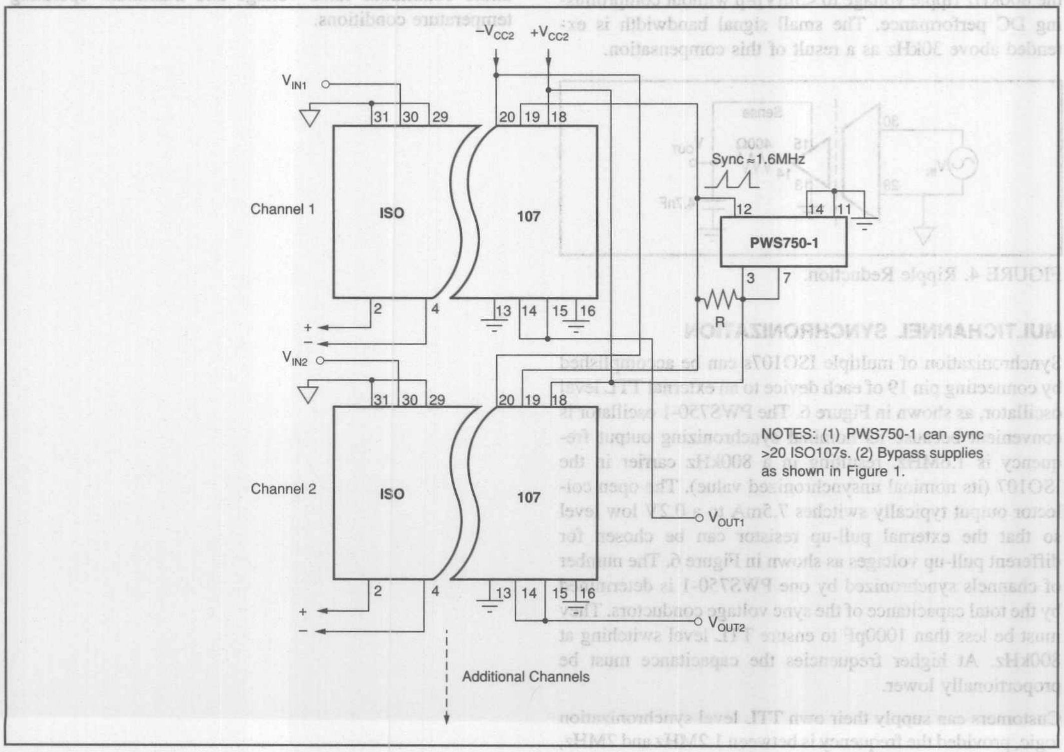
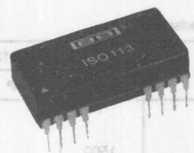


FIGURE 6. Synchronized-Multichannel Isolation.

BURR - BROWN®



ISO113

Low-Cost, High-Voltage, Internally Powered OUTPUT ISOLATION AMPLIFIER

FEATURES

- **SELF-CONTAINED ISOLATED SIGNAL AND OUTPUT POWER**
- **SMALL PACKAGE SIZE: Double-Wide (0.6") Sidebraze DIP**
- **CONTINUOUS AC BARRIER RATING: 1500Vrms**
- **WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power**
- **BUILT-IN ISOLATED OUTPUT POWER: ±10V to ±18V Input, ±50mA Output**
- **MULTICHANNEL SYNCHRONIZATION CAPABILITY**
- **BOARD AREA ONLY 0.72in.^{2} (4.6cm^2)**

APPLICATIONS

- **4mA TO 20mA V/I CONVERTERS**
- **MOTOR AND VALVE CONTROLLERS**
- **ISOLATED RECORDER OUTPUTS**
- **MEDICAL INSTRUMENTATION OUTPUTS**
- **GAS ANALYZERS**

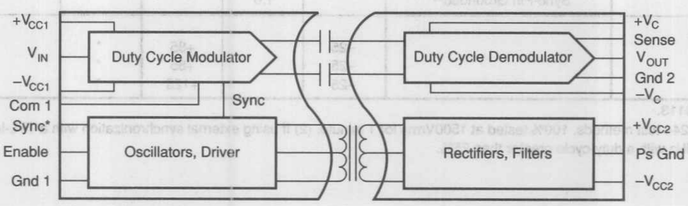
DESCRIPTION

The ISO113 output isolation amplifier provides both signal and output power across an isolation barrier in a small double-wide DIP package. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated output side for driving external loads. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel modulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 1500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO113 easy to use, and provides for compact PC board layout.



*Ground if not used

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

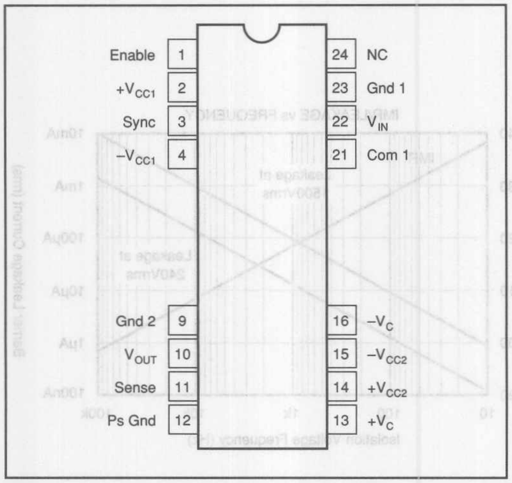
At T_A = +25°C and V_{CC1} = ±15V, ±15mA output current unless otherwise noted.

		ISO113			ISO113B			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ISOLATION								
Rated Continuous Voltage								
AC, 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
Test Breakdown, 100% AC, 60Hz	10s	5657			*			Vpk
Isolation-Mode Rejection	1500Vrms, 60Hz		130			*		dB
	2121VDC		160			*		dB
Barrier Impedance			10^{12} || 9			*		Ω || pF
Leakage Current	240Vrms, 60Hz		1	2		*	*	µA
GAIN								
Nominal			1			*		V/V
Initial Error			±0.3	±0.5		*	*	%FSR
Gain vs Temperature			±60	±100		±20	±50	ppm/°C
Nonlinearity	V_O = –10V to 10V		±0.05	±0.1		±0.03	±0.05	%FSR
	V_O = –5V to 5V		±0.02	±0.04		±0.012	±0.02	%FSR
INPUT OFFSET VOLTAGE								
Initial Offset			±20	±60		*	*	mV
vs Temperature			±300	±500		±100	±250	µV/°C
vs Power Supplies	V_{CC2} = ±10 to ±18V		0.9			*		mV/V
vs Output Supply Load	I_O = 0 to ±50mA		±0.3			*		mV/mA
SIGNAL INPUT								
Voltage Range	Output Voltage in Range	±10	±15		*	*		V
Resistance			200			*		kΩ
SIGNAL OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±15		*	*		mA
Ripple Voltage, 800kHz Carrier			25			*		mVp-p
	400Ω/4.7nF (See Figure 4)		5			*		mVp-p
Capacitive Load Drive			1000			*		pF
Voltage Noise			4			*		µV/√Hz
FREQUENCY RESPONSE								
Small Signal Bandwidth			20			*		kHz
Slew Rate			1.5			*		V/µs
Settling Time	0.1%, –10/10V		75			*		µs
POWER SUPPLIES								
Rated Voltage, V_{CC1}			±15			*		V
Voltage Range		±10		±18	*		*	V
Input Current	I_O = ±15mA		+90/–4.5			*		mA
	I_O = 0mA		+60/–4.5			*		mA
Ripple Current	No Filter		60			*		mAp-p
	C_{IN} = 1µF		3			*		mAp-p
Rated Output Voltage	Load = 15mA	±14.25	±15	±15.75	*	*	*	V
Output	50mA Balanced Load	10				*		V
	100mA Single-Ended Load	10				*		V
Load Regulation	Balanced Load		0.3			*		%/mA
Line Regulation			1.12			*		V/V
Output Voltage vs Temperature			2.5			*		mV/°C
Voltage Balance, ±V_{CC2}			0.05			*		%
Voltage Ripple (800kHz)	No External Capacitors		50			*		mVp-p
	C_{EXT} = 1µF		5			*		mVp-p
Output Capacitive Load				1			*	µF
Sync Frequency	Sync-Pin Grounded(2)		1.6			*		MHz
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	*		*	°C
Storage		–25		+125	*		*	°C

*Specifications same as ISO113.

NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute. (2) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

PIN CONFIGURATION



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO113	24-Pin DIP	231

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com_1 to Gnd_1	±200mV
Enable, Sync	Gnd to $+V_{CC1}$
Continuous Isolation Voltage	1500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	+150°C
Storage Temperature	–25°C to +125°C
Lead Temperature,10s	+300°C
Output Short to Gnd Duration	Continuous
$\pm V_{CC2}$ to Gnd 2 Duration	Continuous

ELECTROSTATIC DISCHARGE SENSITIVITY

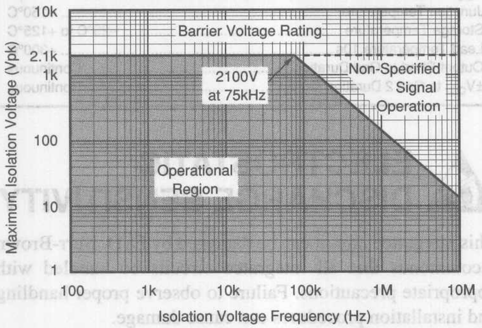
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

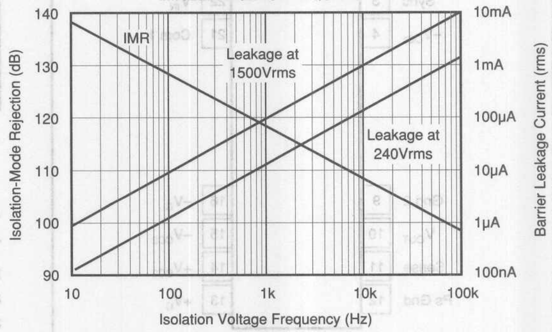
TYPICAL PERFORMANCE CURVES

$T_A = +25°C, V_{CC1} = \pm15VDC$, ±15mA output current unless otherwise noted.

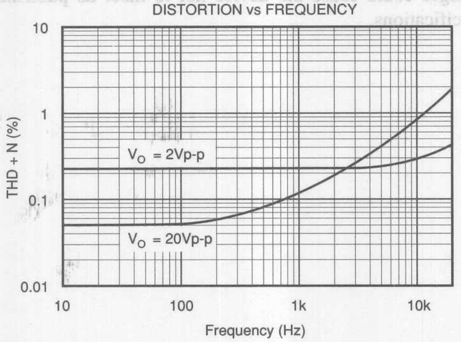
RECOMMENDED RANGE OF ISOLATION VOLTAGE



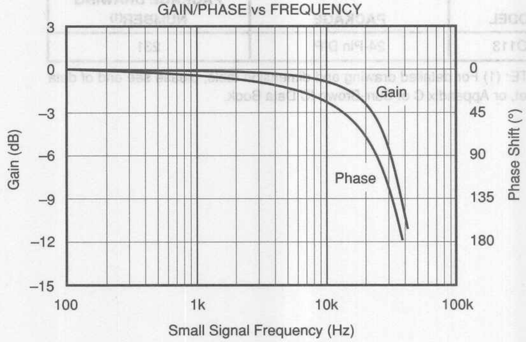
IMR/LEAKAGE vs FREQUENCY



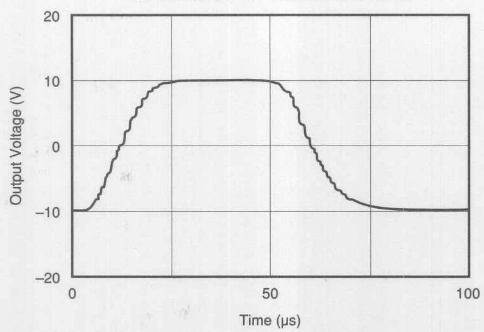
DISTORTION vs FREQUENCY



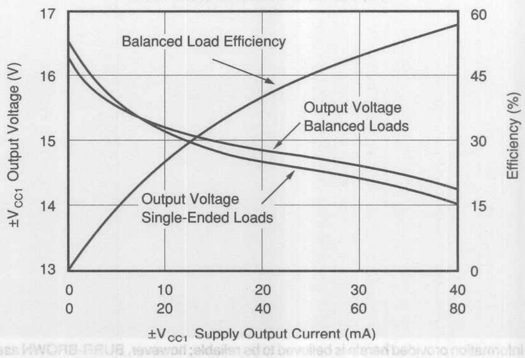
GAIN/PHASE vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE



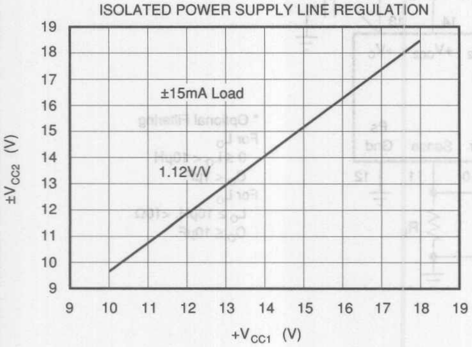
ISOLATED POWER SUPPLY
LOAD REGULATION AND EFFICIENCY



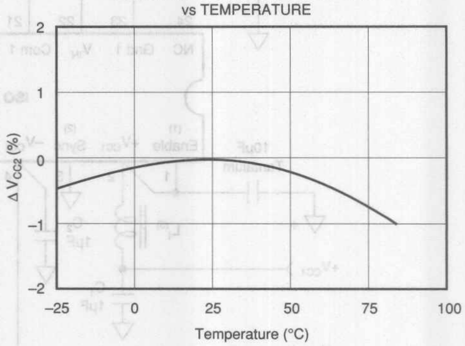
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C, V_{CC1} = ±15VDC$, ±15mA output current unless otherwise noted.

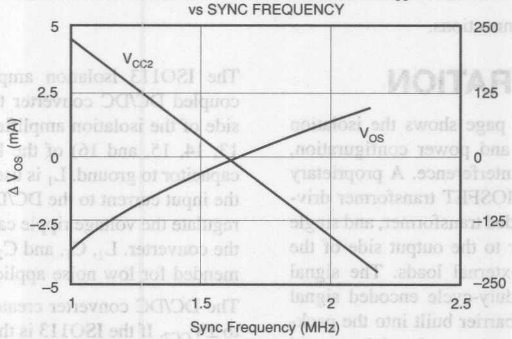
ISOLATED POWER SUPPLY LINE REGULATION



ISOLATION POWER SUPPLY VOLTAGE vs TEMPERATURE



ISOLATED SUPPLY VOLTAGE AND V_{OS} vs SYNC FREQUENCY



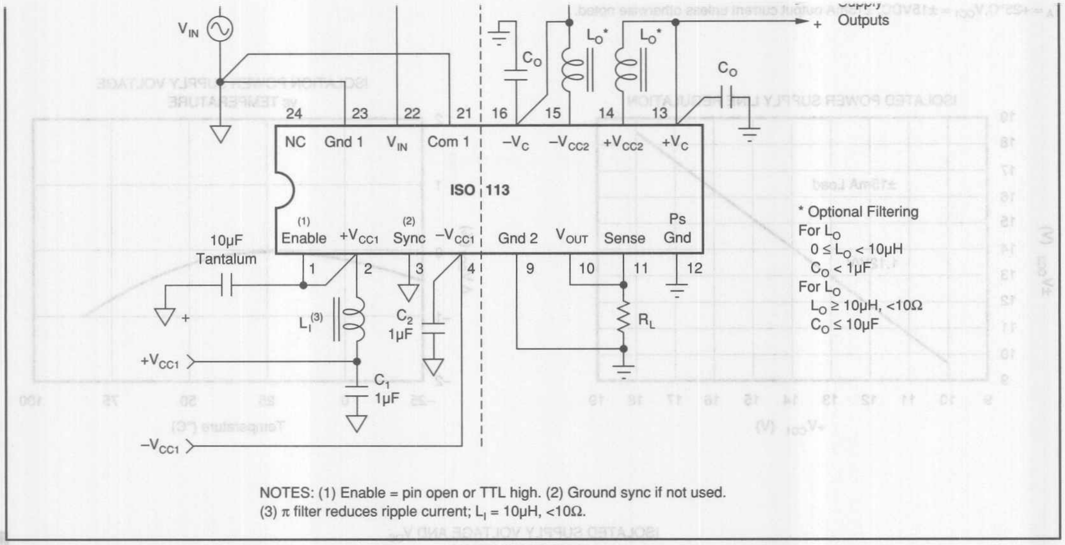


FIGURE 1. Signal and Power Connections.

THEORY OF OPERATION

The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminate beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the output side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, results in a simple, reliable design.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC1}$, an option recommended if more than ±15mA are drawn from the isolated supply. Separate rectifier output pins ($\pm V_{CC2}$) and amplifier supply input pins ($\pm V_C$) allow additional ripple filtering and/or regulation. The separate input common pin and output sense are low current inputs tied to the signal source ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, and Sense to V_{OUT} at the ISO113 socket. The enable pin may be left open if the ISO113 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.2MHz to 2MHz TTL clock signal provides synchronization of multiple units.

The ISO113 isolation amplifier contains a transformer-coupled DC/DC converter that is powered from the input side of the isolation amplifier. All power supply pins (2, 4, 13, 14, 15, and 16) of the ISO113 have an internal 0.1µF capacitor to ground. L_1 is used to slow down fast changes in the input current to the DC/DC converter. C_1 is used to help regulate the voltage ripple caused by the current demands of the converter. L_1, C_1, and C_2 are optional, however, recommended for low noise applications.

The DC/DC converter creates an unregulated ±15V output to $\pm V_{CC2}$. If the ISO113 is the only device using the DC/DC converter for power, pins 13 and 14 and pins 15 and 16 can be connected directly without C_O or L_O in the circuit. If an external capacitor is used in this configuration, it should not exceed 1µF. This configuration is possible because the isolation amplifier and the DC/DC converter are synchronized internally.

If additional devices are powered by the DC/DC converter of the ISO113, the application may require that the ripple voltage of the ISO113 converter be attenuated, in which case, L_O and C_O should be added to the circuit. The inductor is used to attenuate the ripple current and a higher value capacitor can be used to reduce the ripple voltage even further.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of ±0.5% for the values shown. Greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1%

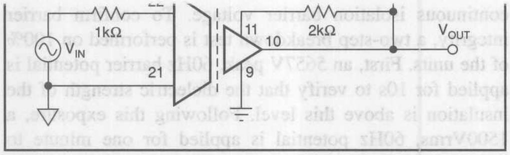


FIGURE 2a. Gain Adjust.

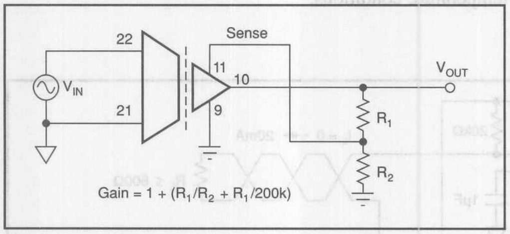


FIGURE 2b. Gain Setting.

adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictate location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R_1 and R_2 may be reversed.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input referred errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 3 shows a method for trimming V_{OS} of the ISO113. This circuit may be applied to Signal Com1. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

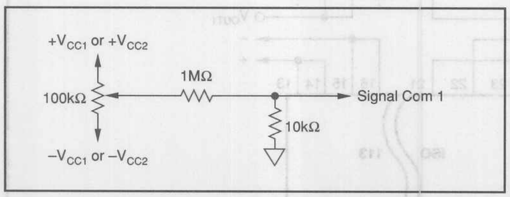


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <5mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

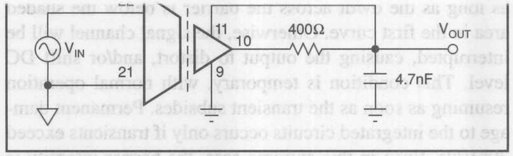


FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO113s can be accomplished by connecting pin 3 of each device to an external TTL level oscillator, as shown in Figure 7. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO113 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull up resistor can be chosen for different pull-up voltages as shown in Figure 7. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic, provided the frequency is between 1.2MHz and 2MHz, and the duty cycle is greater than 25%.

Single or multichannel synchronization with reduced power dissipation for applications requiring less than ±15mA from V_{CC1} is accomplished by driving both the Sync input pin (3) and Enable pin (1) with the TTL oscillator as shown in Figure 5.

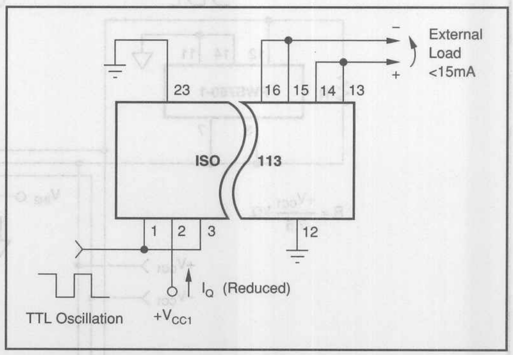


FIGURE 5. Reduced Power Dissipation.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO113 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/ Leakage vs Frequency. At low barrier modulation

levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO113 was designed to reliably operate with 1500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, an 5657V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 1500Vrms, 60Hz potential is applied for one minute to conform to UL1244. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

APPLICATIONS

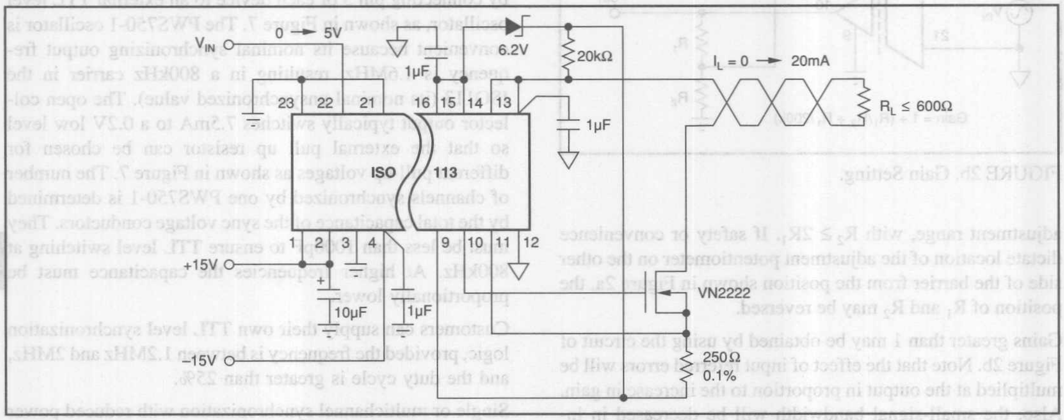


FIGURE 6. Isolated Current Loop Driver.

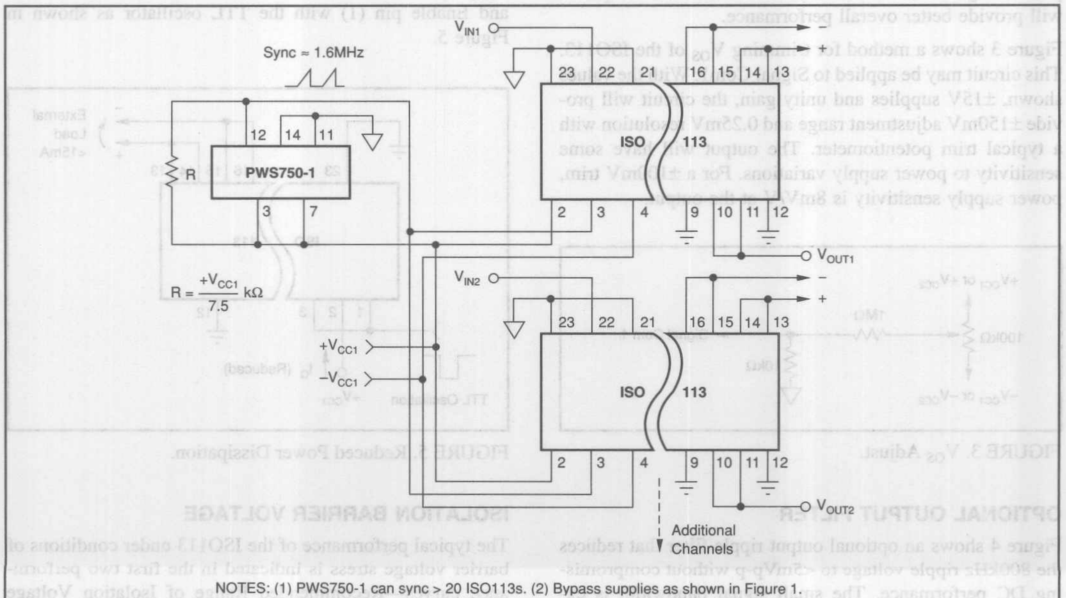
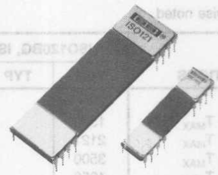


FIGURE 7. Synchronized-Multichannel Isolation.

BURR - BROWN®



ISO120
ISO121

Precision Low Cost ISOLATION AMPLIFIER

FEATURES

- 100% TESTED FOR PARTIAL DISCHARGE
- ISO120: Rated 1500Vrms
- ISO121: Rated 3500Vrms
- HIGH IMR: 115dB at 60Hz
- USER CONTROL OF CARRIER FREQUENCY
- LOW NONLINEARITY: ±0.01% max
- BIPOLAR OPERATION: $V_O = \pm10V$
- 0.3"-WIDE 24-PIN HERMETIC DIP, ISO120
- SYNCHRONIZATION CAPABILITY
- WIDE TEMP RANGE: –55°C to +125°C (ISO120)

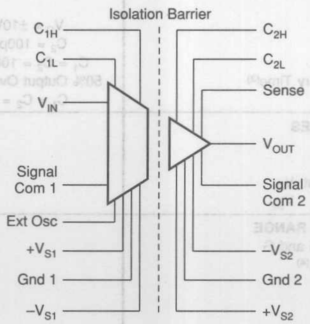
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT

DESCRIPTION

The ISO120 and ISO121 are precision isolation amplifiers incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, which results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a hermetic DIP. The ISO120 and ISO121 differ only in package size and isolation voltage rating.

These amplifiers are easy to use. No external components are required for 60kHz bandwidth. With the addition of two external capacitors, precision specifications of 0.01% max nonlinearity and 150µV/°C max V_{OS} drift are guaranteed with 6kHz bandwidth. A power supply range of ±4.5V to ±18V and low quiescent current make these amplifiers ideal for a wide range of applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

At $T_A = +25°C$: $V_{S1} = V_{S2} = ±15V$: and $R_L = 2kΩ$, unless otherwise noted.

PARAMETER	CONDITIONS	ISO120BG, ISO121BG MIN	ISO120BG, ISO121BG TYP	ISO120BG, ISO121BG MAX	ISO120G, ISO120SG(4), ISO121G MIN	ISO120G, ISO120SG(4), ISO121G TYP	ISO120G, ISO120SG(4), ISO121G MAX	UNITS
ISOLATION								
Voltage Rated Continuous ISO120: AC 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
ISO121: AC 60Hz	T_{MIN} to T_{MAX}	3500			*			Vrms
DC	T_{MIN} to T_{MAX}	4950			*			VDC
100% Test (AC 60Hz): ISO120	1s; Partial Discharge ≤ 5pC	2500			*			Vrms
ISO121	1s; Partial Discharge ≤ 5pC	5600			*			Vrms
Isolation Mode Rejection ISO 120: AC 60Hz	1500Vrms		115			*		dB
DC			160			*		dB
ISO121: AC60Hz	3500Vrms		115			*		dB
DC			160			*		dB
Barrier Impedance			10^{14} || 2			*		Ω || pF
Leakage Current	V_{ISO} = 240Vrms, 60Hz		0.18	0.5		*	*	µArms
GAIN(4)	$V_O = ±10V$							
Nominal Gain	$C_1 = C_2$ = 1000pF		1			1		V/V
Gain Error			±0.04	±0.1		±0.05	±0.25	%FSR
Gain vs Temperature			±5	±20		±10	±40	ppm/°C
Nonlinearity			±0.005	±0.01		±0.01	±0.05	%FSR
Nominal Gain	$C_1 = C_2 = 0$		1			1		V/V
Gain Error			±0.04	±0.25		±0.05	±0.25	%FSR
Gain vs Temperature			±40			±40		ppm/°C
Nonlinearity			±0.02	±0.1		±0.04	±0.1	%FSR
INPUT OFFSET VOLTAGE(4)								
Initial Offset	$C_1 = C_2$ = 1000pF		±5	±25		±10	±50	mV
vs Temperature			±100	±150		±150	±400	µV/°C
Initial Offset	$C_1 = C_2 = 0$		±25	±100		±40	±100	mV
vs Temperature			±250			±500		µV/°C
Initial Offset								
vs Supply	$±V_{S1}$ or $±V_{S2}$ = ±4.5V to ±18V		±2			±2		mV/V
Noise			4			4		$µV/\sqrt{Hz}$
INPUT								
Voltage Range(1)		±10	±15		*	*		V
Resistance			200			*		kΩ
OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±15		*	*		mA
Capacitive Load Drive			0.1			*		µF
Ripple Voltage(2)			10			*		mVp-p
FREQUENCY RESPONSE								
Small Signal Bandwith	$C_1 = C_2 = 0$		60			*		kHz
	$C_1 = C_2$ = 1000pF		6			*		kHz
Slew Rate			2			*		V/µs
Settling Time	$V_O = ±10V$							
0.1%	C_2 = 100pF		50			*		µs
0.01%	$C_1 = C_2$ = 1000pF		350			*		µs
Overload Recovery Time(3)	50% Output Overload, $C_1 = C_2 = 0$		150			*		µs
POWER SUPPLIES								
Rated Voltage			15			*		V
Voltage Range		±4.5		±18	*		*	V
Quiescent Current: V_{S1}			±4.0	±5.5		*	*	mA
V_{S2}			±5.0	±6.5		*	*	mA
TEMPERATURE RANGE								
Specification: BG and G		–25		85	–25		85	°C
SG(4)		–25		85	–55		125	°C
Operating		–55		125	–55		125	°C
Storage		–65		150	–55		150	°C
$θ_{JA}$: ISO120			40			40		°C/W
ISO121			25			25		°C/W

*Specifications same as ISO120BG, ISO121BG.

NOTE: (1) Input voltage range = ±10V for V_{S1}, V_{S2} = ±4.5VDC to ±18VDC. (2) Ripple frequency is at carrier frequency. (3) Overload recovery is approximately three times the settling time for other values of C_2. (4) The SG-grade is specified –55°C to +125°C; performance of the SG in the –25°C to +85°C temperature range is the same as the BG-grade.

External Oscillator Input .... ±25V
Signal Common 1 to Ground 1 .... ±1V
Signal Common 2 to Ground 2 .... ±1V
Continuous Isolation Voltage: ISO120 .... 1500Vrms
ISO121 .... 3500Vrms
V_{ISO}, dv/dt 20kV/μs
Junction Temperature .... 150°C
Storage Temperature .... –65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Output Short Duration .... Continuous to Common

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO120G	24-Pin DIP	225
ISO120BG	24-Pin DIP	225
ISO120SG	24-Pin DIP	225
ISO121G	40-Pin DIP	206
ISO121BG	40-Pin DIP	206

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

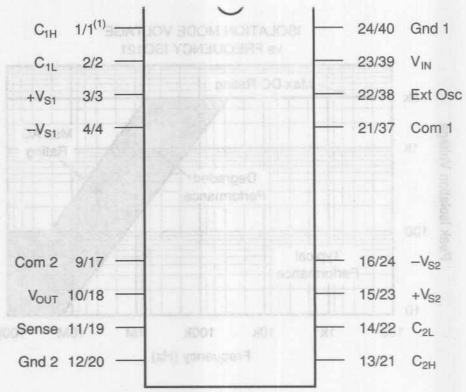
ORDERING INFORMATION

MODEL	TEMPERATURE RANGE
ISO120G	–25°C to 85°C
ISO120BG	–25°C to 85°C
ISO120SG	-55C to 125°C
ISO121G	–25°C to 85°C
ISO121BG	–25°C to 85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



NOTE: (1) First pin number is for ISO120. Second pin number is for ISO121.

ISO120/121

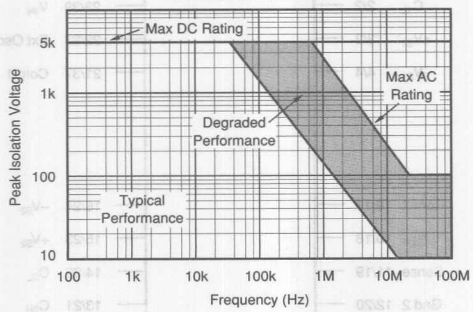
5

ISOLATION PRODUCTS

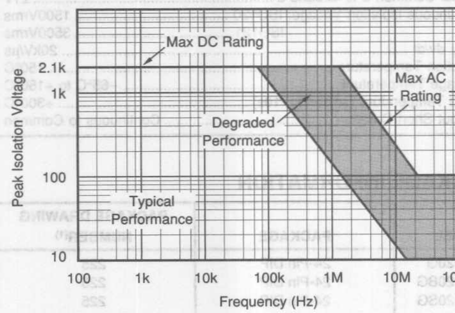
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$; $V_{S1} = V_{S2} = ±15V$; and $R_L = 2kΩ$, unless otherwise noted.

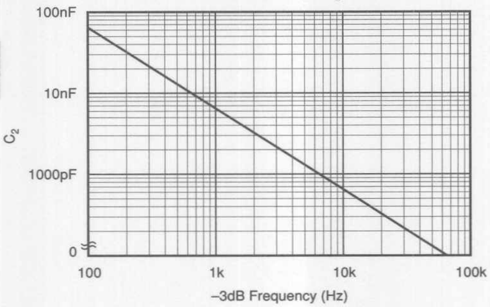
ISOLATION MODE VOLTAGE vs FREQUENCY ISO121



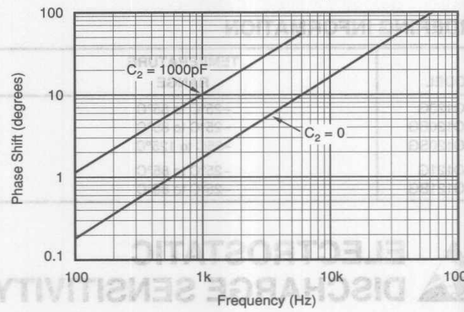
ISOLATION MODE VOLTAGE vs FREQUENCY ISO120



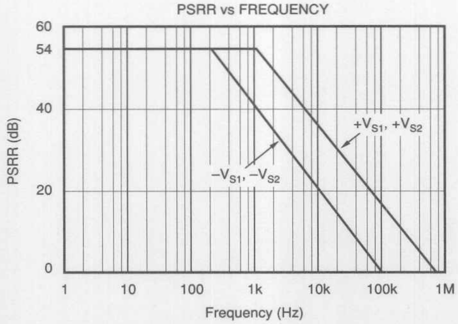
BANDWIDTH vs C_2



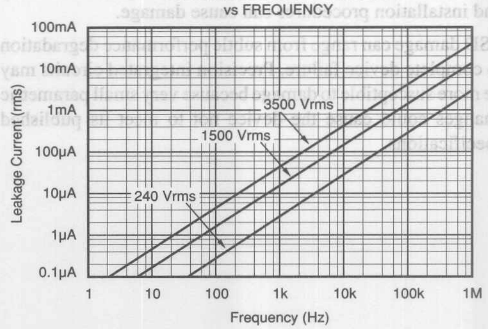
PHASE SHIFT vs C_2



PSRR vs FREQUENCY



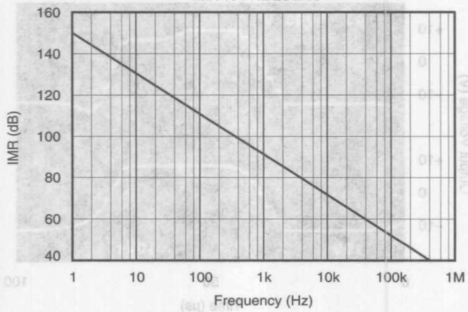
ISOLATION LEAKAGE CURRENT vs FREQUENCY



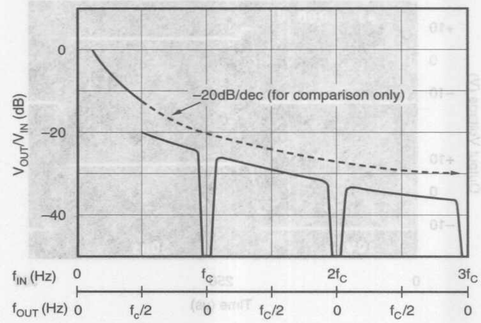
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C; V_{S1} = V_{S2} = ±15V; and R_L = 2kΩ, unless otherwise noted.

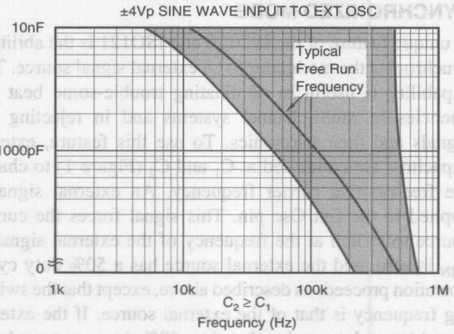
IMR vs FREQUENCY



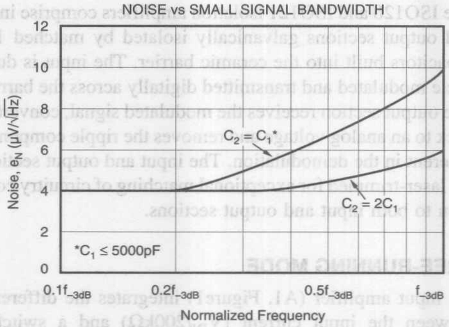
SIGNAL RESPONSE vs CARRIER FREQUENCY



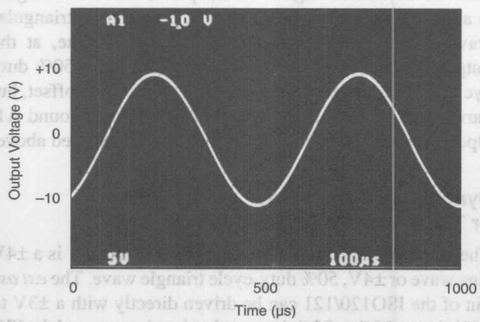
SYNCHRONIZATION RANGE at 25°C
±4Vp SINE WAVE INPUT TO EXT OSC



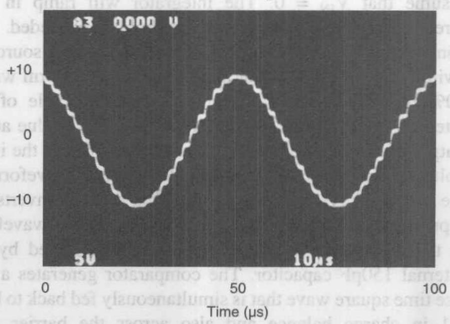
NOISE vs SMALL SIGNAL BANDWIDTH

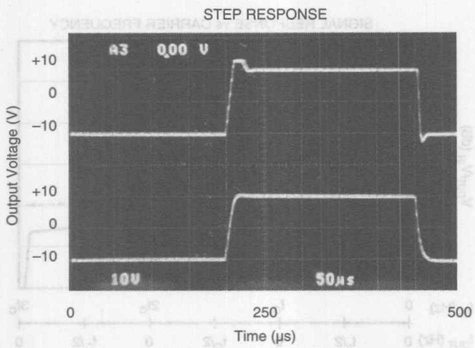


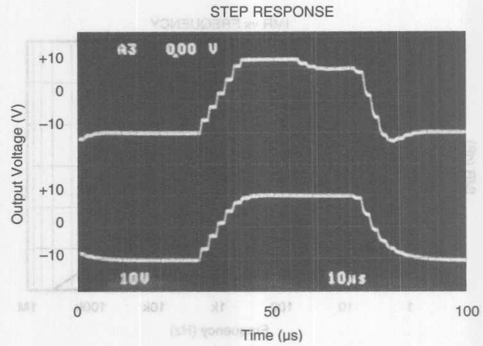
SINE RESPONSE
(f = 2kHz, C_2 = 0)



SINE RESPONSE
(f = 20kHz, C_2 = 0)







THEORY OF OPERATION

The ISO120 and ISO121 isolation amplifiers comprise input and output sections galvanically isolated by matched 1pF capacitors built into the ceramic barrier. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. The input and output sections are laser-trimmed for exceptional matching of circuitry common to both input and output sections.

FREE-RUNNING MODE

An input amplifier (A1, Figure1) integrates the difference between the input current (V_{IN}/200kΩ) and a switched ±100µA current source. This current source is implemented by a switchable 200µA source and a fixed 100µA current sink. To understand the basic operation of the input section, assume that V_{IN} = 0. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. If V_{IN} changes, the duty cycle of the integrator will change to keep the average DC value at the output of A1 near zero volts. This action converts the input voltage to a duty-cycle modulated triangular waveform at the output of A1 near zero volts. This action converts the input voltage to a duty-cycle modulated triangular waveform at the output of A1 with a frequency determined by the internal 150pF capacitor. The comparator generates a fast rise time square wave that is simultaneously fed back to keep A1 in charge balance and also across the barrier to a differential sense amplifier with high common-mode rejection characteristics. The sense amplifier drives a switched current source surrounding A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200kΩ feedback resistor, resulting in an average value at the Sense pin equal to V_{IN}. The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

SYNCHRONIZED MODE

A unique feature of the ISO120 and ISO121 is the ability to synchronize the modulator to an external signal source. This capability is useful in eliminating trouble-some beat frequencies in multi-channel systems and in rejecting AC signals and their harmonics. To use this feature, external capacitors are connected at C_1 and C_2 (Figure 1) to change the free-running carrier frequency. An external signal is applied to the Ext Osc pin. This signal forces the current source to switch at the frequency of the external signal. If V_{IN} is zero, and the external source has a 50% duty cycle, operation proceeds as described above, except that the switching frequency is that of the external source. If the external signal has a duty cycle other than 50%, its average value is not zero. At start-up, the current source does not switch until the integrator establishes an output equal to the average DC value of the external signal. At this point, the external signal is able to trigger the current source, producing a triangular waveform, symmetrical about the new DC value, at the output of A1. For V_{IN} = 0, this waveform has a 50% duty cycle. As V_{IN} varies, the waveform retains its DC offset, but varies in duty cycle to maintain charge balance around A1. Operation of the demodulator is the same as outlined above.

Synchronizing to a Sine or Triangle Wave External Clock

The ideal external clock signal for the ISO120/121 is a ±4V sine wave or ±4V, 50% duty-cycle triangle wave. The *ext osc* pin of the ISO120/121 can be driven directly with a ±3V to ±5V sine or 25% to 75% duty-cycle triangle wave and the ISO amp's internal modulator/demodulator circuitry will synchronize to the signal.

Synchronizing to signals below 400kHz requires the addition of two external capacitors to the ISO120/121. Connect one capacitor in parallel with the internal modulator capacitor and connect the other capacitor in parallel with the internal demodulator capacitor as shown in Figure 1.

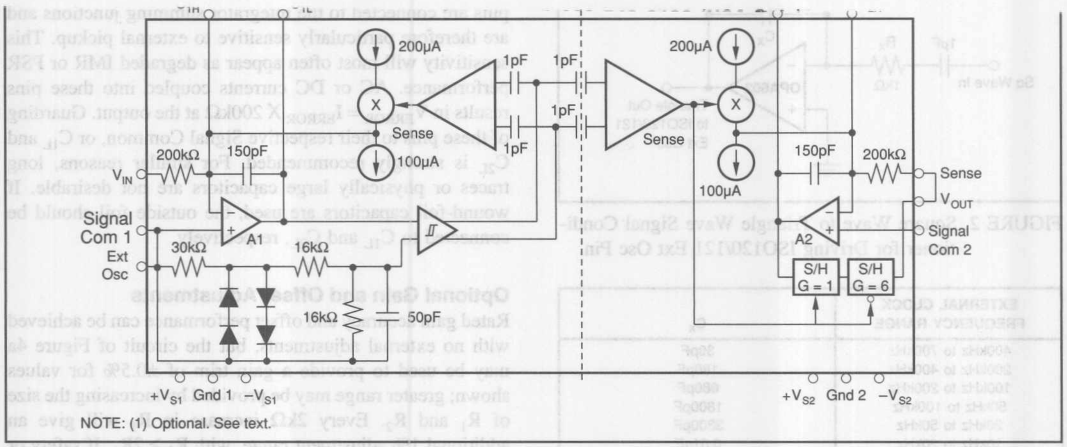


FIGURE 1. Block Diagram.

The value of the external modulator capacitor, C_1, depends on the frequency of the external clock signal. Table I lists recommended values.

EXTERNAL CLOCK FREQUENCY RANGE	C_1, C_2 ISO120/121 MODULATOR, DEMODULATOR EXTERNAL CAPACITOR
400kHz to 700kHz	none
200kHz to 400kHz	500pF
100kHz to 200kHz	1000pF
50kHz to 100kHz	2200pF
20kHz to 50kHz	4700pF
10kHz to 20kHz	0.01µF
5kHz to 10kHz	0.022µF

TABLE I. Recommended ISO120/121 External Modulator/Demodulator Capacitor Values vs External Clock Frequency.

The value of the external demodulator capacitor, C_2, depends on the value of the external modulator capacitor. To assure stability, C_2 must be greater than $0.8 \bullet C_1$. A larger value for C_2 will decrease bandwidth and improve stability:

$$f_{-3\,dB} \approx \frac{1.2}{200k\Omega\,(150\,pF + C_2)}$$

Where:

$f_{-3dB} \approx -3$dB bandwidth of ISO amp with external C_2 (Hz)
C_2 = External demodulator capacitor (f)

For example, with $C_2 = 0.01\mu F$, the f_{-3dB} bandwidth of the ISO120/121 is approximately 600Hz.

Synchronizing to a 400kHz to 700kHz Square-Wave External Clock

At frequencies above 400kHz, an internal clamp and filter provides signal conditioning so that a square-wave signal can be used to directly drive the ISO120/121. A square-wave external clock signal can be used to directly drive the ISO120/121 *ext osc* pin if: the signal is in the 400kHz to 700kHz frequency range with a 25% to 75% duty cycle, and ±3V to ±20V level. Details of the internal clamp and filter circuitry are shown in Figure 1.

Synchronizing to a 10% to 90% Duty-cycle External Clock

With the addition of the signal conditioning circuit shown in Figure 2, any 10% to 90% duty-cycle square-wave signal can be used to drive the ISO120/121 ext osc pin. With the values shown, the circuit can be driven by a 4Vp-p TTL signal. For a higher or lower voltage input, increase or decrease the 1kΩ resistor, R_X, proportionally. e.g. for a ±4V square wave (8Vp-p) R_X should be increased to 2kΩ.

The value of C_X used in the Figure 2 circuit depends on the frequency of the external clock signal. Table II shows recommended capacitor values.

Note: For external clock frequencies below 400kHz, external modulator/demodulator capacitors are required on the ISO120/121 as before.

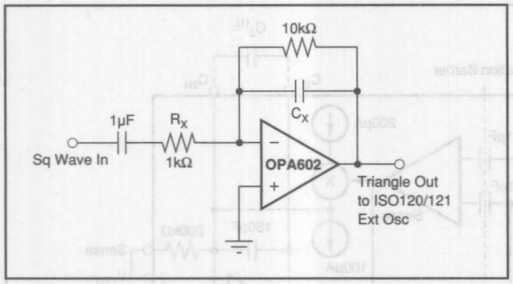


FIGURE 2. Square Wave to Triangle Wave Signal Conditioner for Driving ISO120/121 Ext Osc Pin.

EXTERNAL CLOCK FREQUENCY RANGE	C_X
400kHz to 700kHz	30pF
200kHz to 400kHz	180pF
100kHz to 200kHz	680pF
50kHz to 100kHz	1800pF
20kHz to 50kHz	3300pF
10kHz to 20kHz	0.01μF
5kHz to 10kHz	0.022μF

TABLE II. Recommended C_X Values vs Frequency for Figure 2 Circuit.

BASIC OPERATION

Signal and Power Connections

Figure 3 shows proper power and signal connections. Each power supply pin should be bypassed with 1μF tantalum capacitor located as close to the amplifier as possible. All ground connections should be run independently to a common point if possible. Signal Common on both input and output sections provide a high-impedance point for sensing signal ground in noisy applications. Signal Common must have a path to ground for bias current return and should be maintained within ±1V of Gnd. The output sense pin may be connected directly to V_{OUT} or may be connected to a remote load to eliminate errors due to IR drops. Pins are provided for use of external integrator capacitors. The C_{1H} and C_{2H} pins are connected to the integrator summing junctions and are therefore particularly sensitive to external pickup. This sensitivity will most often appear as degraded IMR or PSR performance. AC or DC currents coupled into these pins results in $V_{ERROR} = I_{ERROR}$ X 200kΩ at the output. Guarding of these pins to their respective Signal Common, or C_{1L} and C_{2L} is strongly recommended. For similar reasons, long traces or physically large capacitors are not desirable. If wound-foil capacitors are used, the outside foil should be connected to C_{1L} and C_{2L}, respectively.

Optional Gain and Offset Adjustments

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 4a may be used to provide a gain trim of ±0.5% for values shown; greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictates location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 4a, the positions of R_1 and R_2 may be reversed. Gains greater than one may be obtained by using the circuit of Figure 4b. Note that the effect of input offset errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 5 shows a method for trimming V_{OS} of the ISO120 and ISO121. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV

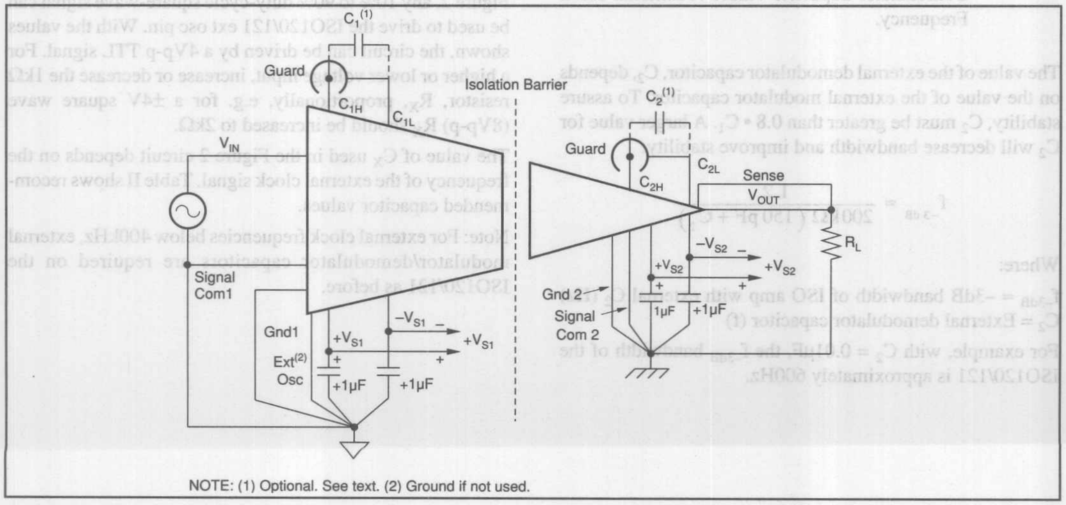


FIGURE 3. Power and Signal Connections.

resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

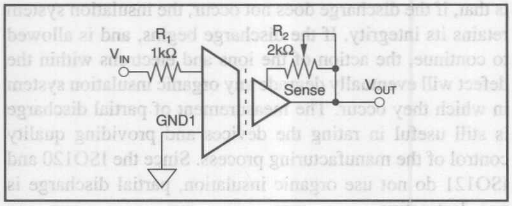


FIGURE 4a. Gain Adjust.

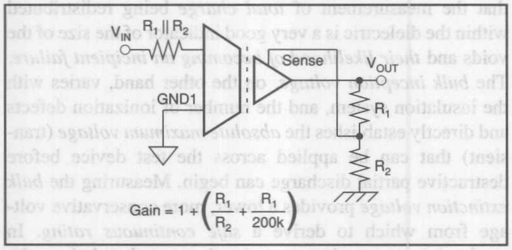


FIGURE 4b. Gain Setting.

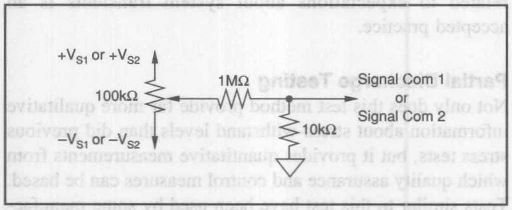


FIGURE 5. V_{OS} Adjust.

CARRIER FREQUENCY CONSIDERATIONS

As previously discussed, the ISO120 and ISO121 amplifiers transmit the signal across the iso-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes more complex. The Signal Response vs Carrier Frequency performance curve describes this behavior graphically. The upper curve illustrates the response for input signals varying from DC to $f_C/2$. At input frequencies at or above $f_C/2$, the device generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go the zero. These characteristics can be exploited in certain applications. It should be noted that when C_1 is zero, the carrier frequency is nominally 500kHz and the –3dB point of the amplifier is 60kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 250kHz.

There are two ways to use these characteristics. One is to move the carrier frequency low enough that the troublesome signal components are attenuated to an acceptable level as shown in Signal Response vs Carrier Frequency. This in effect limits the bandwidth of the amplifier. The Synchronization Range performance curve shows the relationship between carrier frequency and the value of C_1. To maintain stability, C_2 must also be connected and must be equal to or larger in value than C_1. C_2 may be further increased in value for additional attenuation of the undesired signal components and provides the additional benefit of reducing the residual carrier ripple at the output. See the Bandwidth vs C_2 performance curve.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO120 and ISO121 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the Signal Response vs Carrier Frequency performance curve. For proper synchronization, choose C_1 as shown in the Synchronization Range performance curve. Remember that $C_2 \geq C_1$ is a necessary condition for stability of the isolation amplifier. This curve shows the range of lock at the fundamental frequency for a 4V sinusoidal signal source. The applications section shows the ISO120 and ISO121 synchronized to isolation power supplies, while Figure 6 shows circuitry with opto-isolation suitable for driving the Ext Osc input from TTL levels.

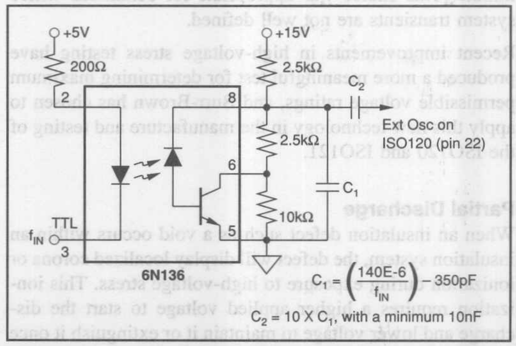


FIGURE 6. Synchronization with Isolated Drive Circuit for Ext Osc Pin.

ISOLATION MODE VOLTAGE

Isolation mode voltage (IMV) is the voltage appearing between isolated grounds Gnd 1 and Gnd 2. IMV can induce error at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs in a manner similar to that described above, and the amplifier response will be identical to that shown in the Signal Response vs Carrier Frequency performance curve. This occurs

by the IMR shown in IMR vs Frequency performance curve and compute the amplifier response to this input-referred error signal from the data given in the Signal Response vs Carrier Frequency performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/µs. For convenience, this is plotted in the typical performance curves for the ISO120 and ISO121 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/µs but falls below 20kV/µs, performance may be degraded. At rates of change above 20kV/µs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltages below ±15V may decrease the dV/dT to 500V/µs for typical performance, but the maximum dV/dT of 20kV/µs remains unchanged.

Leakage current is determined solely by the impedance of the 2pF barrier capacitance and is plotted in the Isolation Leakage Current vs Frequency curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one. Historically, Burr-Brown has chosen a deliberately conservative one: V_{TEST} = (2 X ACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO120 and ISO121.

Partial Discharge

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. Since the ISO120 and ISO121 do not use organic insulation, partial discharge is non-destructive.

The inception voltage for these voids tends to be constant, so that the measurement of *total charge* being redistributed within the dielectric is a very good indicator of the size of the voids and *their likelihood of becoming an incipient failure.* The *bulk inception voltage,* on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the *absolute maximum voltage* (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the *bulk extinction voltage* provides a lower, more conservative voltage from which to derive a *safe continuous rating*. In production, measuring at a level somewhat below the expected inception voltage and then derating by a factor related to expectations about system transients is an accepted practice.

Partial Discharge Testing

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE, the national standards group in Germany and an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display ≤5pC partial discharge level in a 100% production test.

The ISO120 and ISO121 isolation amplifiers are used in three categories of applications:

1. Accurate isolation of signals from high voltage ground potentials,
2. Accurate isolation of signals from severe ground noise and,
3. Fault protection from high voltages in analog measurements.

Figures 7 through 12 show a variety of Application Circuits.

APPLICATION CIRCUITS

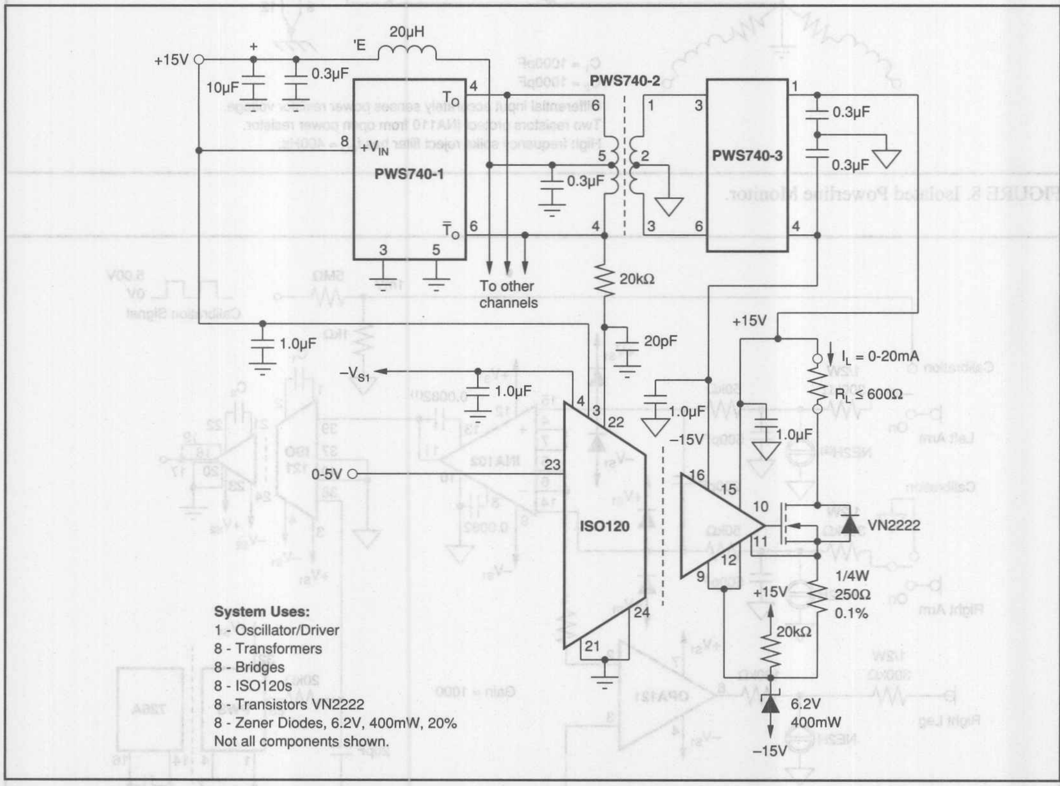


FIGURE 7. Eight-Channel Isolated 0-20mA Loop Driver.

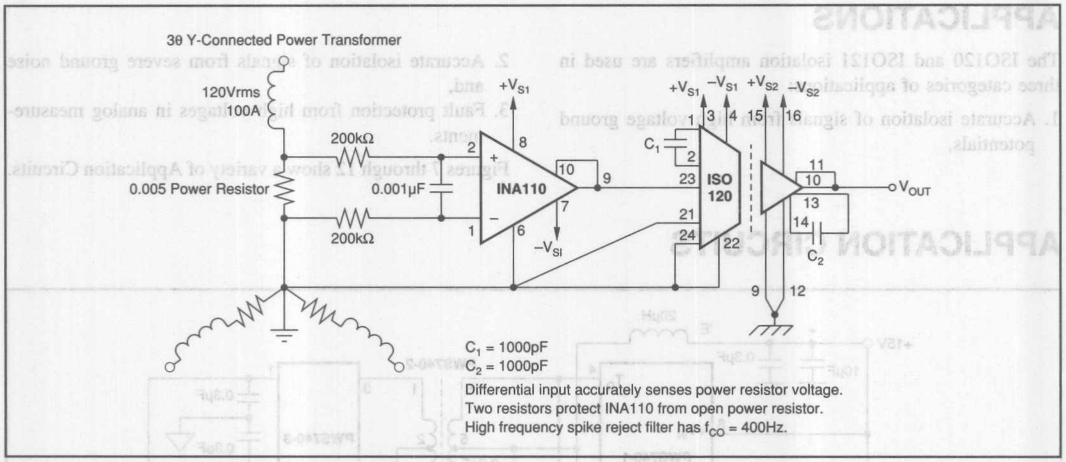


FIGURE 8. Isolated Powerline Monitor.

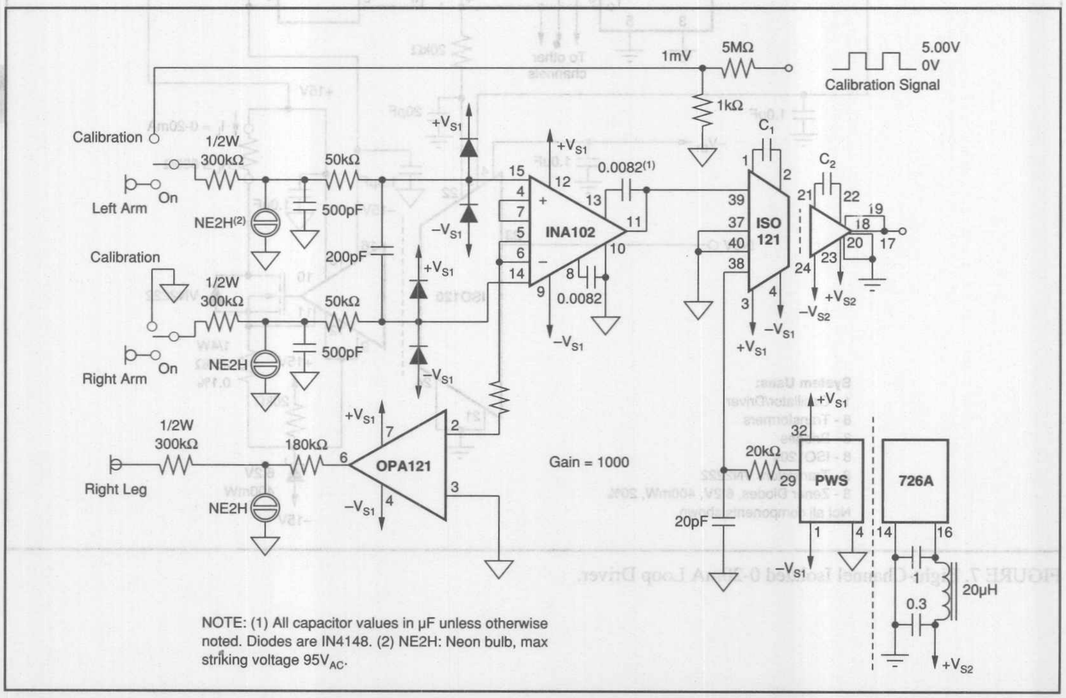


FIGURE 9. Right-Leg Driven ECG Amplifier (with defibrillator protection and calibration).

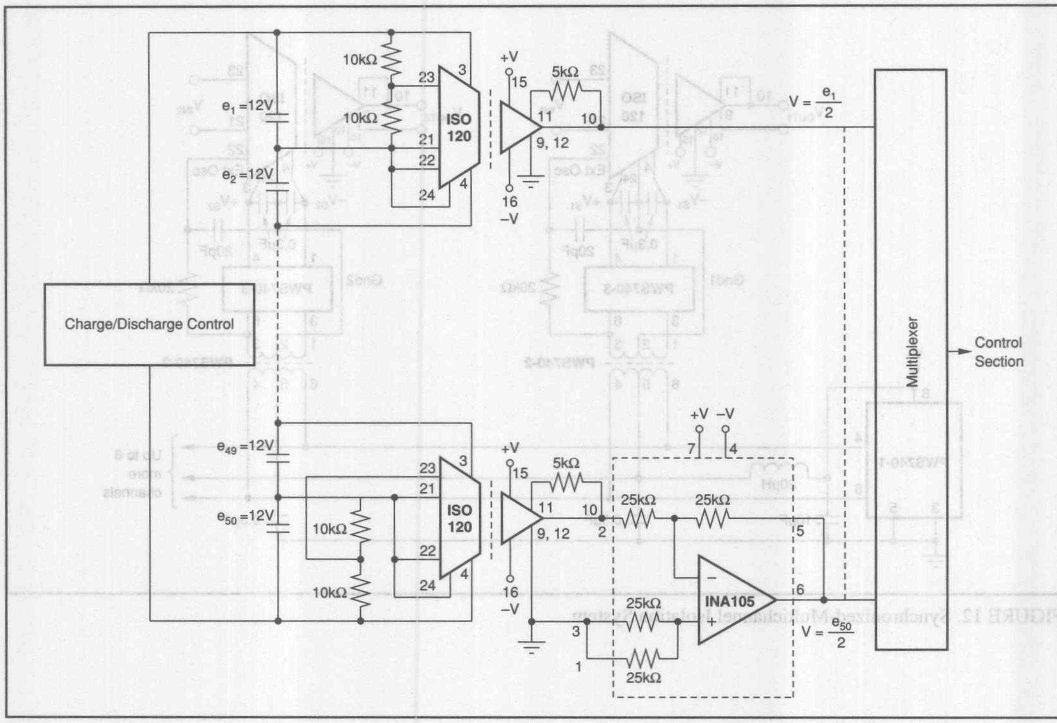


FIGURE 10. Battery Monitor for a 600V Battery Power System.

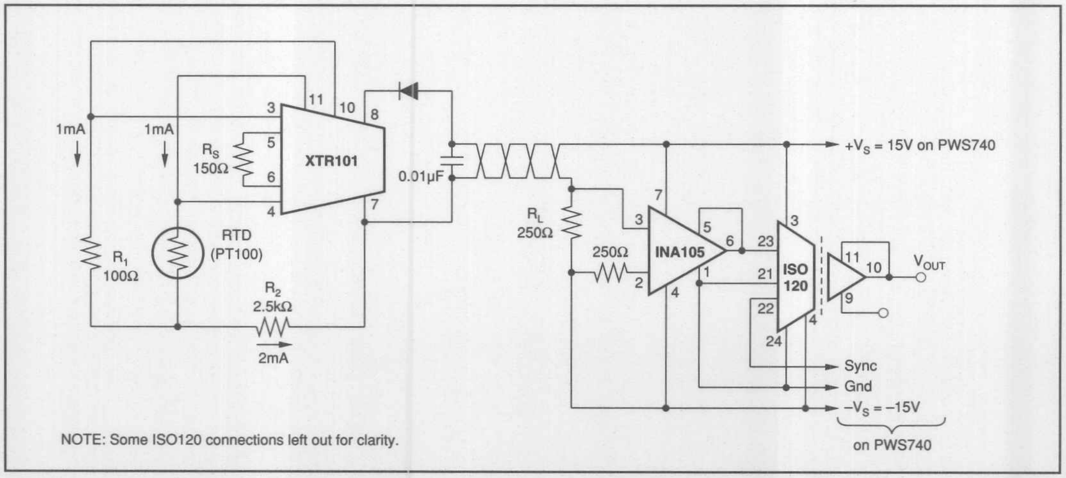


FIGURE 11. Isolated 4-20mA Instrument Loop. (RTD shown).

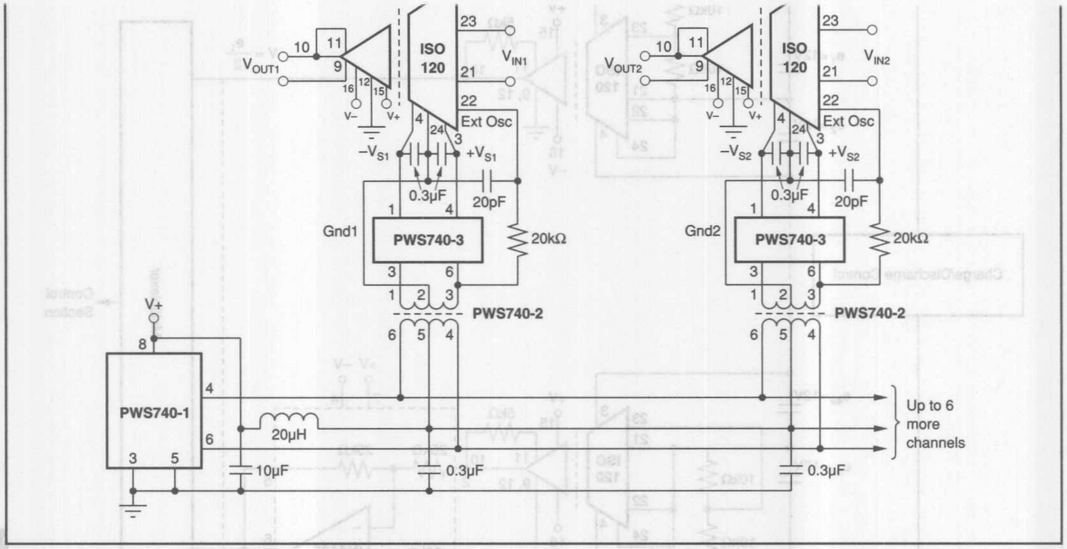
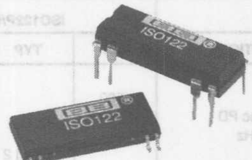


FIGURE 12. Synchronized-Multichannel Isolation System.

BURR - BROWN®

ISO122



Precision Lowest Cost ISOLATION AMPLIFIER

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- HIGH IMR: 140dB at 60Hz
- BIPOLAR OPERATION: $V_O = \pm 10V$
- 16-PIN PLASTIC DIP AND 28-LEAD SOIC
- EASE OF USE: Fixed Unity Gain Configuration
- 0.020% max NONLINEARITY
- ±4.5V to ±18V SUPPLY RANGE

APPLICATIONS

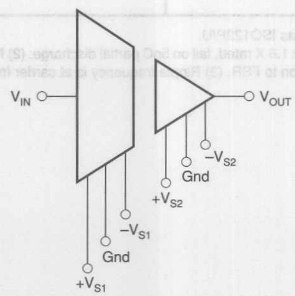
- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- PC-BASED DATA ACQUISITION
- TEST EQUIPMENT

DESCRIPTION

The ISO122 is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, resulting in excellent reliability and good high frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO122 is easy to use. No external components are required for operation. The key specifications are 0.020% max nonlinearity, 50kHz signal bandwidth, and 200μV/°C V_{OS} drift. A power supply range of ±4.5V to ±18V and quiescent currents of ±5.0mA on V_{S1} and ±5.5mA on V_{S2} make these amplifiers ideal for a wide range of applications.

The ISO122 is available in 16-pin plastic DIP and 28-lead plastic surface mount packages.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C , V_{S1} = V_{S2} = ±15V, and R_L = 2kΩ unless otherwise noted.

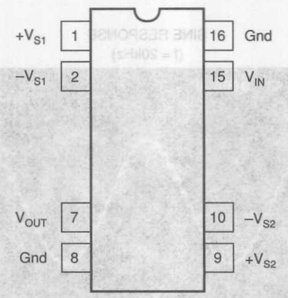
		ISO122P/U			ISO122JP/JU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ISOLATION								
Voltage Rated Continuous AC 60Hz		1500			*			VAC
100% Test (1)	1s, 5pc PD	2400			*			VAC
Isolation Mode Rejection	60Hz		140			*		dB
Barrier Impedance			10^{14} || 2			*		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		0.18	0.5		*	*	µArms
GAIN	V_O = ±10V							
Nominal Gain			1			*		V/V
Gain Error			±0.05	±0.50		*	*	%FSR
Gain vs Temperature			±10			*		ppm/°C
Nonlinearity(2)			±0.016	±0.020		±0.025	±0.050	%FSR
INPUT OFFSET VOLTAGE								
Initial Offset			±20	±50		*	*	mV
vs Temperature			±200			*		µV/°C
vs Supply			±2			*		mV/V
Noise			4			*		µV/√Hz
INPUT								
Voltage Range		±10	±12.5		*			V
Resistance			200			*		kΩ
OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±15		*	*		mA
Capacitive Load Drive			0.1			*		µF
Ripple Voltage(3)			20			*		mVp-p
FREQUENCY RESPONSE								
Small Signal Bandwidth			50			*		kHz
Slew Rate			2			*		V/µs
Settling Time	V_O = ±10V							
0.1%			50			*		µs
0.01%			350			*		µs
Overload Recover Time			150			*		µs
POWER SUPPLIES								
Rated Voltage			±15			*		V
Voltage Range		±4.5		±18	*		*	V
Quiescent Current: V_{S1}			±5.0	±7.0		*	*	mA
V_{S2}			±5.5	±7.0		*	*	mA
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	*		*	°C
Storage		–40		+85	*		*	°C
θ_{JA}			100			*		°C/W
θ_{JC}			65			*		°C/W

* Specification same as ISO122P/U.

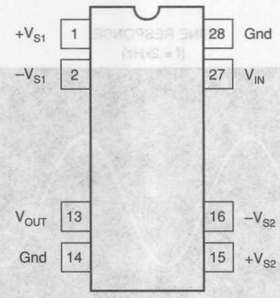
NOTES: (1) Tested at 1.6 X rated, fail on 5pC partial discharge. (2) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (3) Ripple frequency is at carrier frequency (500kHz).

CONNECTION DIAGRAM

Top View —P Package



Top View—U Package



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO122P	16-Pin Plastic DIP	238
ISO122JP	16-Pin Plastic DIP	238
ISO122U	28-Pin Plastic SOIC	217-1
ISO122JU	28-Pin Plastic SOIC	217-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

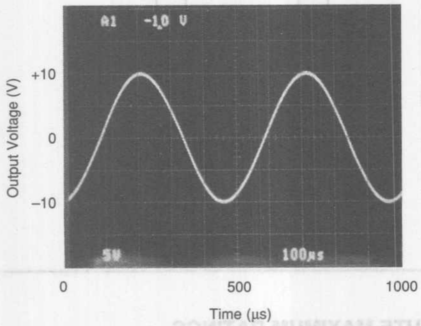
Supply Voltage	±18V
V_{IN}	±100V
Continuous Isolation Voltage	1500Vrms
Junction Temperature	+150°C
Storage Temperature	+85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short to Common	Continuous

ORDERING INFORMATION

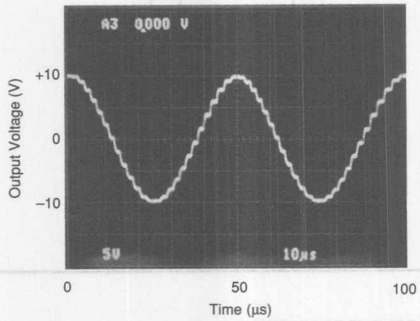
MODEL	PACKAGE	NONLINEARITY MAX %FSR
ISO122P	Plastic DIP	±0.020
ISO122JP	Plastic DIP	±0.050
ISO122U	Plastic SOIC	±0.020
ISO122JU	Plastic SOIC	±0.050

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

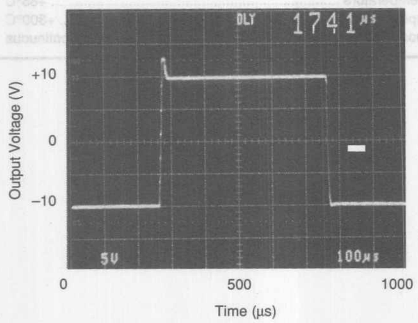
SINE RESPONSE
(f = 2kHz)



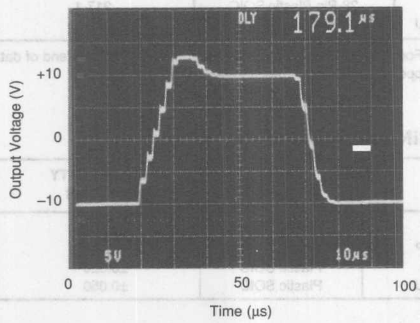
SINE RESPONSE
(f = 20kHz)



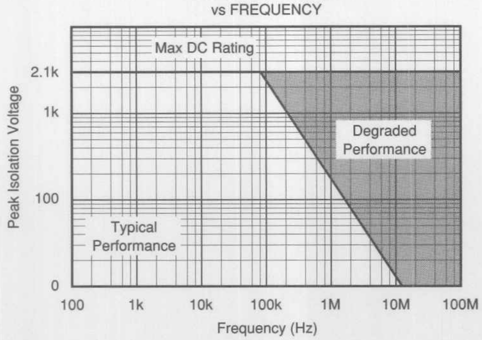
STEP RESPONSE



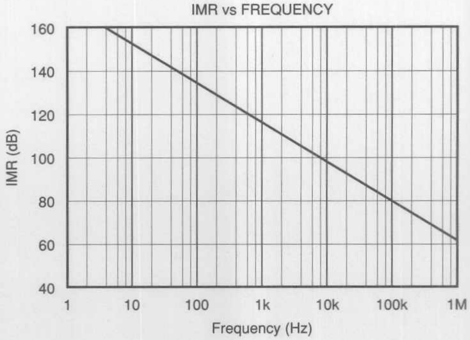
STEP RESPONSE



ISOLATION VOLTAGE
vs FREQUENCY

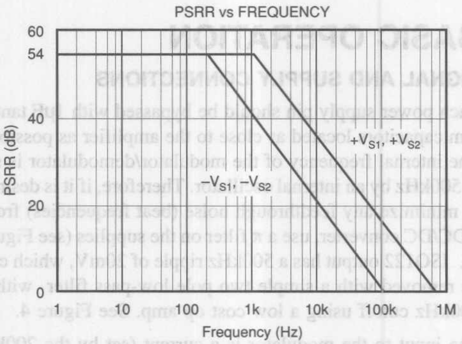


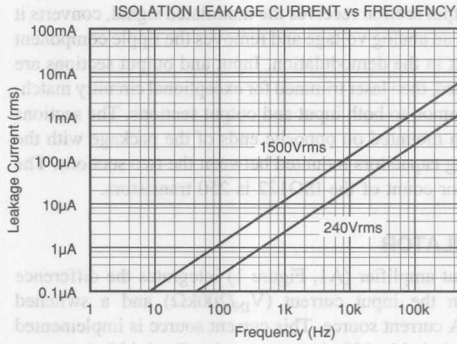
IMR vs FREQUENCY

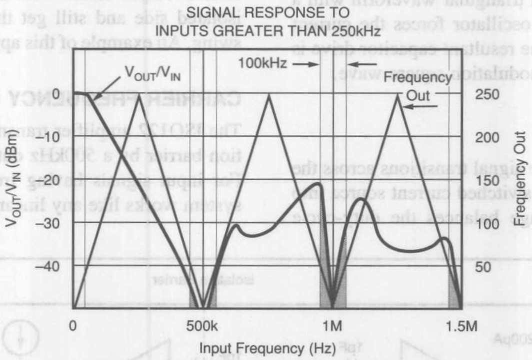


TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, and $V_S = \pm15V$, unless otherwise noted.







(NOTE: Shaded area shows aliasing frequencies that cannot be removed by a low-pass filter at the output.)

ISO122

5

ISOLATION PRODUCTS

THEORY OF OPERATION

The ISO122 isolation amplifier uses an input and an output section galvanically isolated by matched 1pF isolating capacitors built into the plastic package. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. Input and output sections are fabricated, then laser trimmed for exceptional circuitry matching common to both input and output sections. The sections are then mounted on opposite ends of the package with the isolating capacitors mounted between the two sections. The transistor count of the ISO122 is 250 transistors.

MODULATOR

An input amplifier (A1, Figure 1) integrates the difference between the input current (V_{IN}/200kΩ) and a switched ±100µA current source. This current source is implemented by a switchable 200µA source and a fixed 100µA current sink. To understand the basic operation of the modulator, assume that V_{IN} = 0.0V. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. The internal oscillator forces the current source to switch at 500kHz. The resultant capacitor drive is a complementary duty-cycle modulation square wave.

DEMODULATOR

The sense amplifier detects the signal transitions across the capacitive barrier and drives a switched current source into integrator A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200kΩ feedback resistor, resulting in an average value at the V_{OUT} pin equal to V_{IN}. The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

BASIC OPERATION

SIGNAL AND SUPPLY CONNECTIONS

Each power supply pin should be bypassed with 1µF tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500kHz by an internal oscillator. Therefore, if it is desired to minimize any feedthrough noise (beat frequencies) from a DC/DC converter, use a π filter on the supplies (see Figure 4). ISO122 output has a 500kHz ripple of 20mV, which can be removed with a simple two pole low-pass filter with a 100kHz cutoff using a low cost op amp. See Figure 4.

The input to the modulator is a current (set by the 200kΩ integrator input resistor) that makes it possible to have an input voltage greater than the input supplies, as long as the output supply is at least ±15V. It is therefore possible when using an unregulated DC/DC converter to minimize PSR related output errors with ±5V voltage regulators on the isolated side and still get the full ±10V input and output swing. An example of this application is shown in Figure 10.

CARRIER FREQUENCY CONSIDERATIONS

The ISO122 amplifier transmits the signal across the isolation barrier by a 500kHz duty cycle modulation technique. For input signals having frequencies below 250kHz, this system works like any linear amplifier. But for frequencies

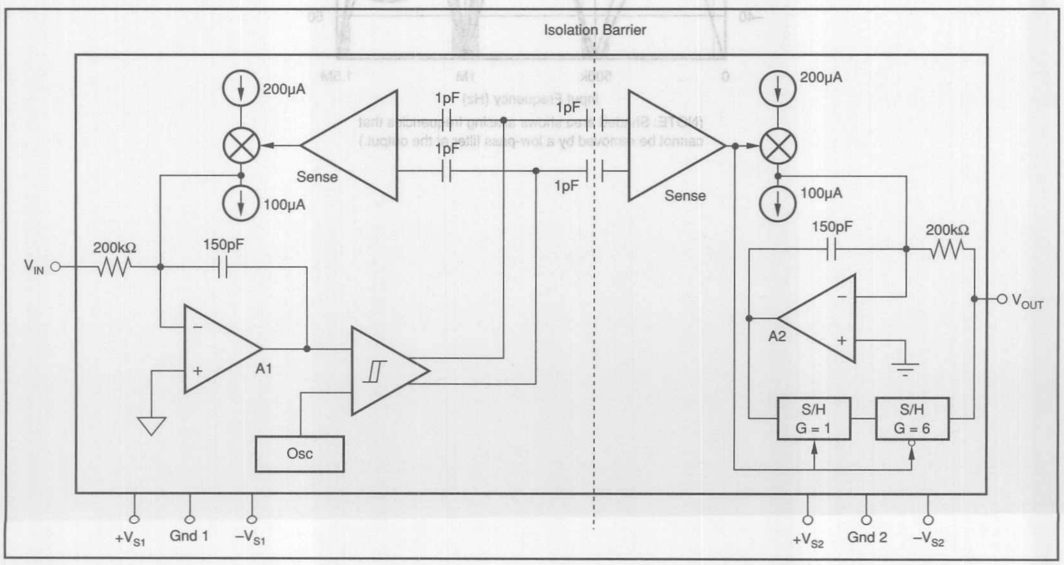


FIGURE 1. Block Diagram.

above 250kHz, the behavior is similar to that of a sampling amplifier. The signal response to inputs greater than 250kHz performance curve shows this behavior graphically; at input frequencies above 250kHz the device generates an output signal component of reduced magnitude at a frequency below 250kHz. This is the aliasing effect of sampling at frequencies less than 2 times the signal frequency (the Nyquist frequency). Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the aliasing go to zero.

ISOLATION MODE VOLTAGE INDUCED ERRORS

IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds 250kHz, the output also will display spurious outputs (aliasing), in a manner similar to that for V_{IN} > 250kHz and the amplifier response will be identical to that shown in the Signal Response to Inputs Greater Than 250kHz performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total error, divide the isolation voltage by the IMR shown in the IMR versus Frequency curve and compute the amplifier response to this input-referred error signal from the data given in the Signal Response to Inputs Greater Than 250kHz performance curve. For example, if a 800kHz 1000Vrms IMR is present, then a total of [(–60dB) + (–30dB)] x (1000V) = 32mV error signal at 200kHz plus a 1V, 800kHz error signal will be present at the output.

HIGH IMV dV/dt ERRORS

As the IMV frequency increases and the dV/dt exceeds 1000V/µs, the sense amp may start to false trigger, and the output will display spurious errors. The common mode current being sent across the barrier by the high slew rate is the cause of the false triggering of the sense amplifier. Lowering the power supply voltages below ±15V may decrease the dV/dt to 500V/µs for typical performance.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (<5pC) while applying 2400Vrms, 60Hz high voltage stress across every ISO122 isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 x 1500Vrms) protection without damage to the ISO122. Lifetest results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state-of-the art" for non-destructive high voltage reliability testing. It is based on the effects of non-uniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01-0.1µs current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage." We have characterized and developed the package insulation processes to yield an inception voltage in excess of 2400Vrms so that transient overvoltages below this level will not damage the ISO122. The extinction voltage is above 1500Vrms so that even overvoltage induced partial discharge will cease once the barrier voltage is reduced to the 1500Vrms (rated) level. Older high voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

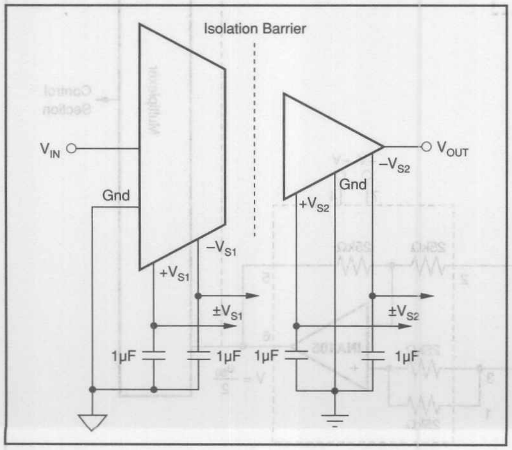


FIGURE 2. Basic Signal and Power Connections.

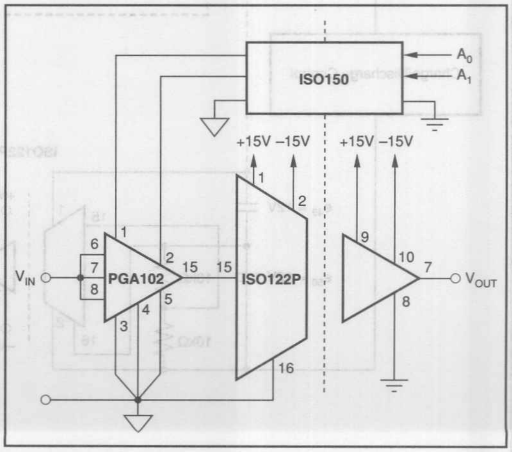


FIGURE 3. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

ISO122

5

ISOLATION PRODUCTS

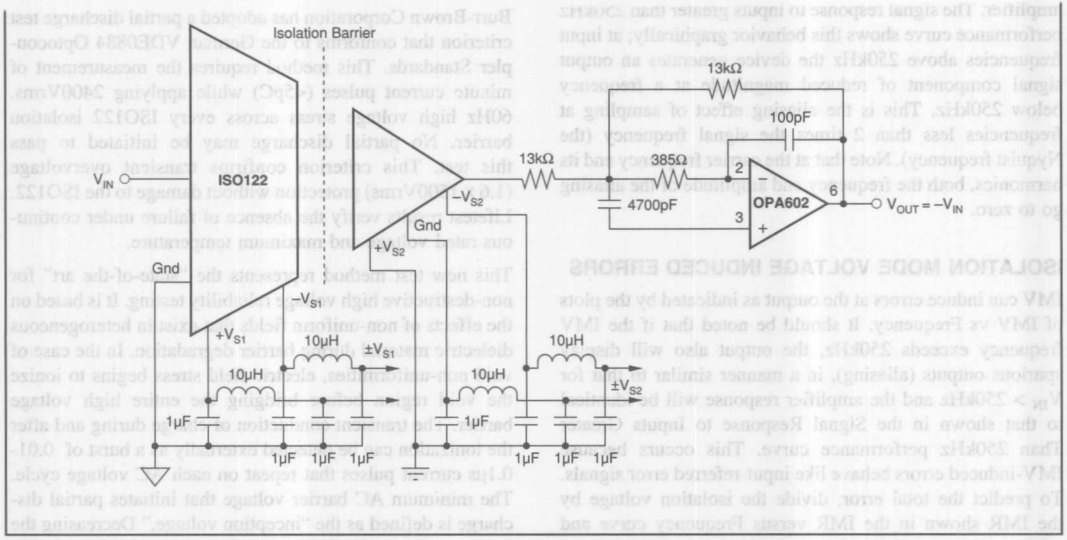


FIGURE 4. Optional π Filter to Minimize Power Supply Feedthrough Noise; Output Filter to Remove 500kHz Carrier Ripple. For more information concerning output filter refer to AB-023.

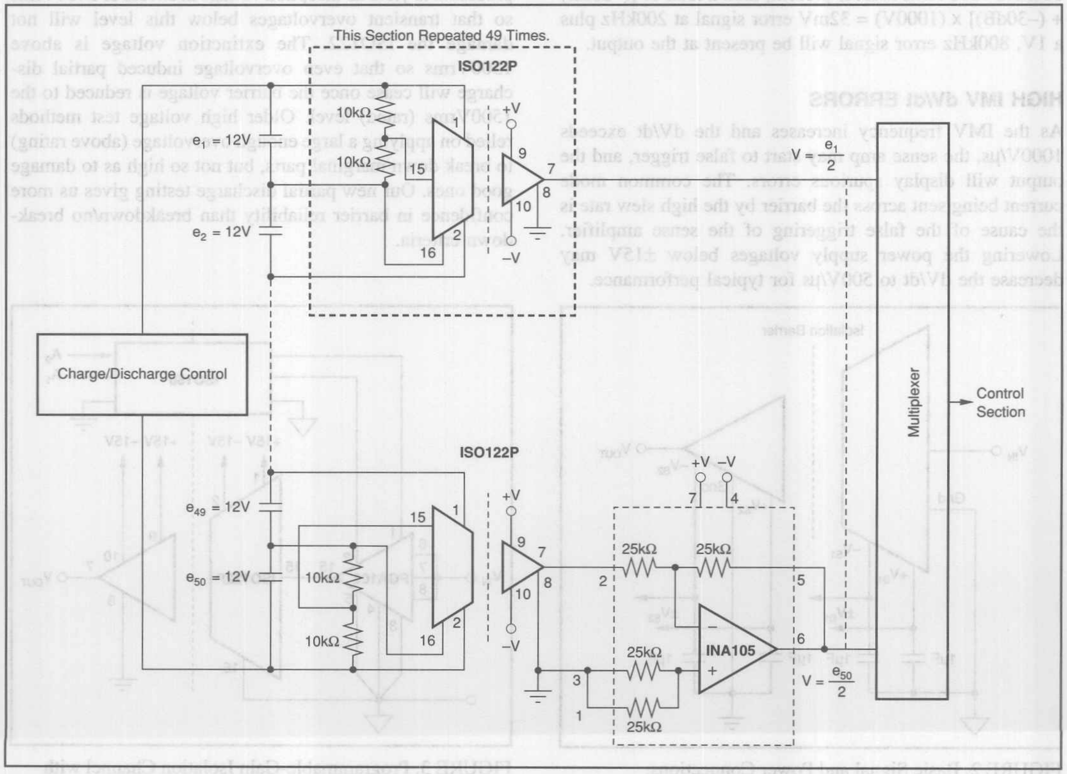
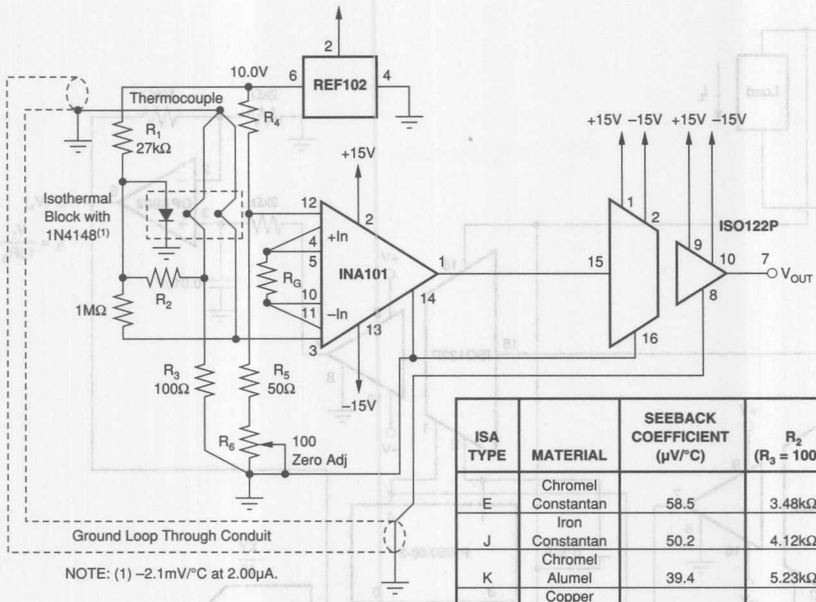


FIGURE 5. Battery Monitor for a 600V Battery Power System. (Derives Input Power from the Battery.)



ISA TYPE	MATERIAL	SEEBACK COEFFICIENT (μV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

FIGURE 6. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out.

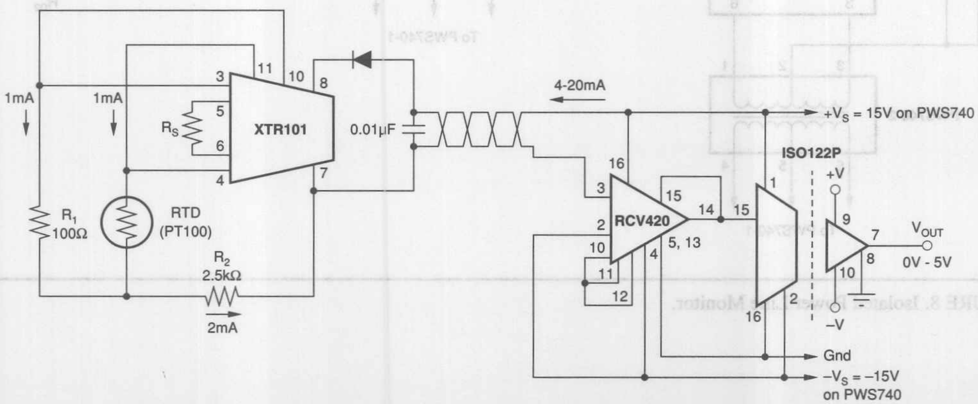


FIGURE 7. Isolated 4-20mA Instrument Loop. (RTD shown.)

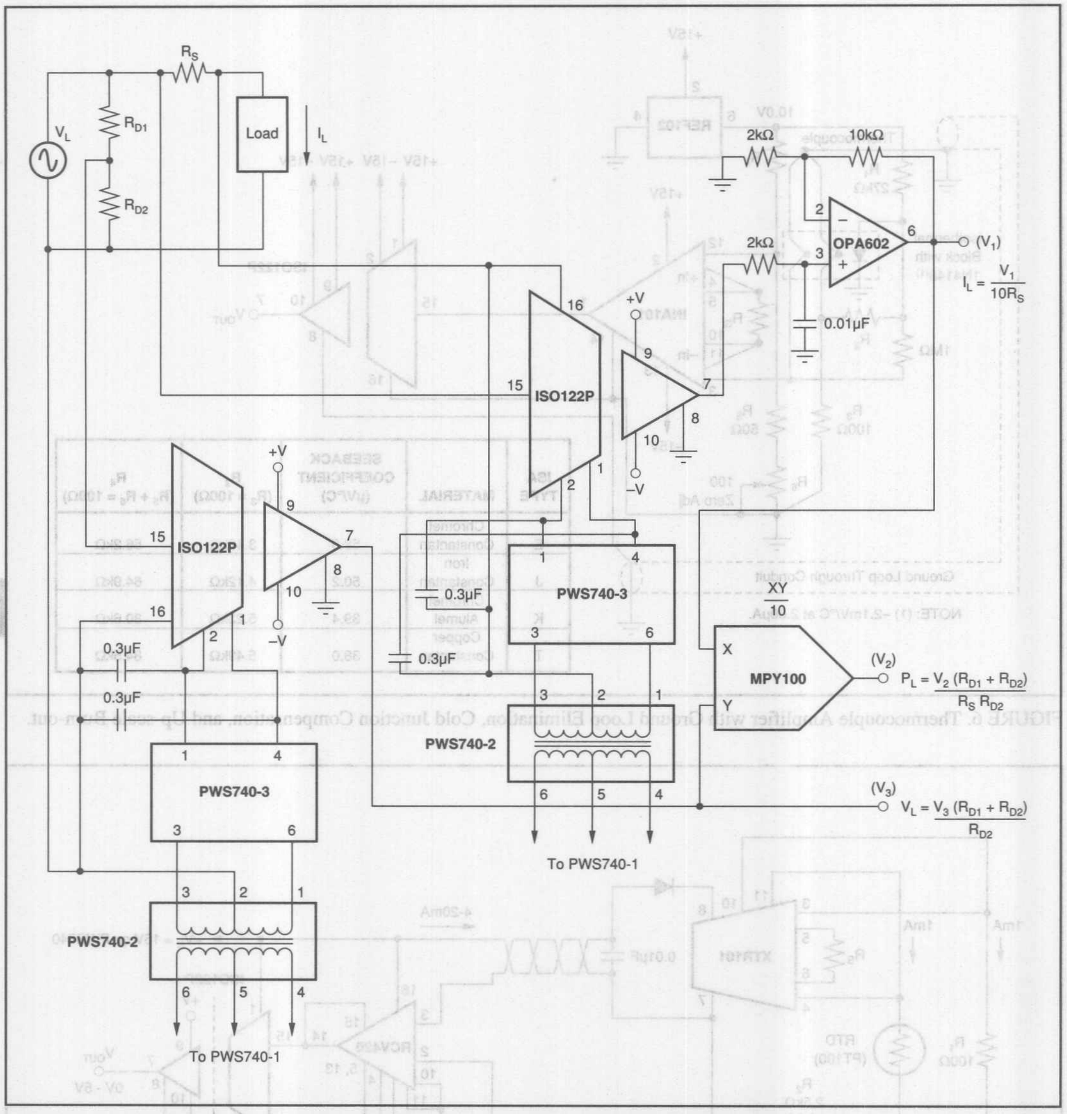


FIGURE 8. Isolated Power Line Monitor.

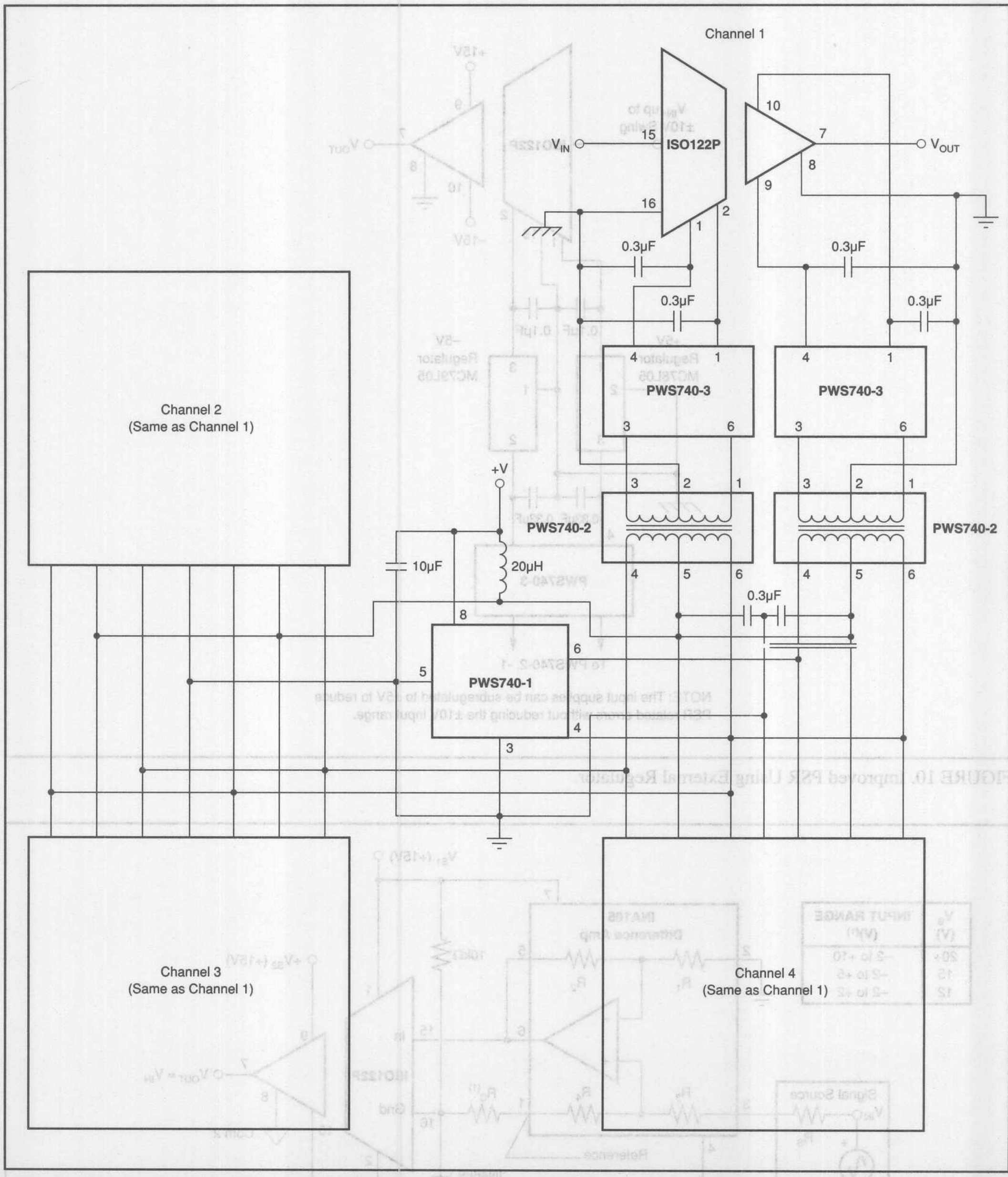


FIGURE 9. Three-Port, Low-Cost, Four-Channel Isolated, Data Acquisition System.

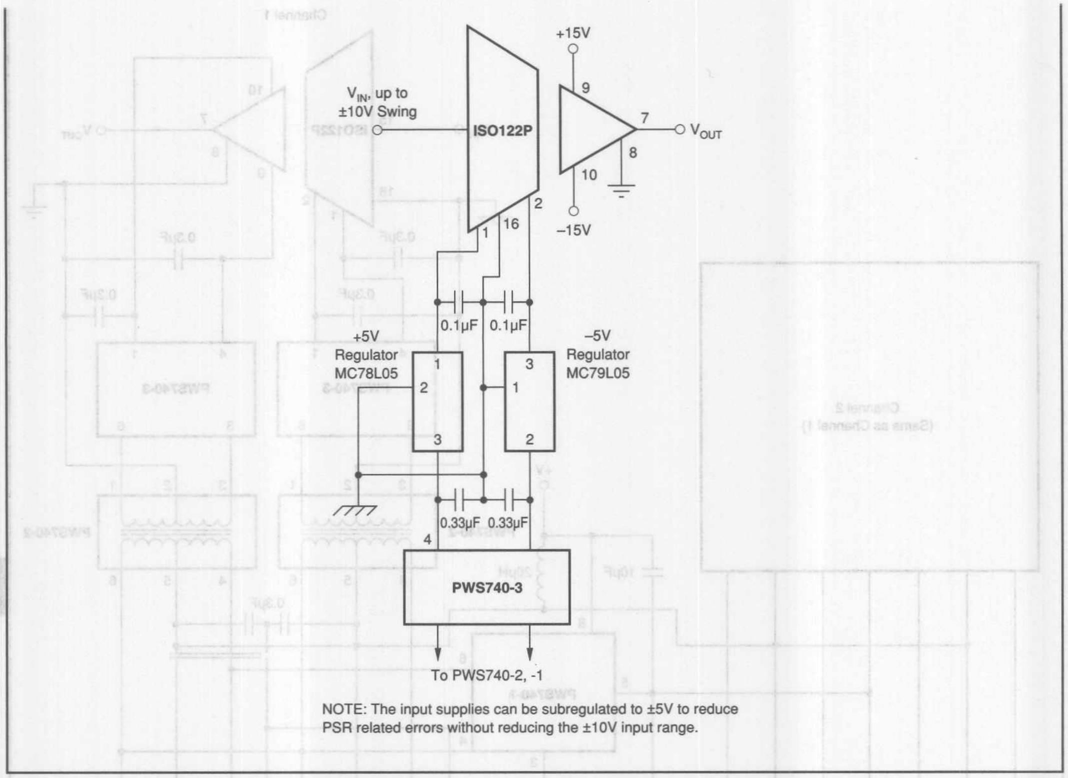
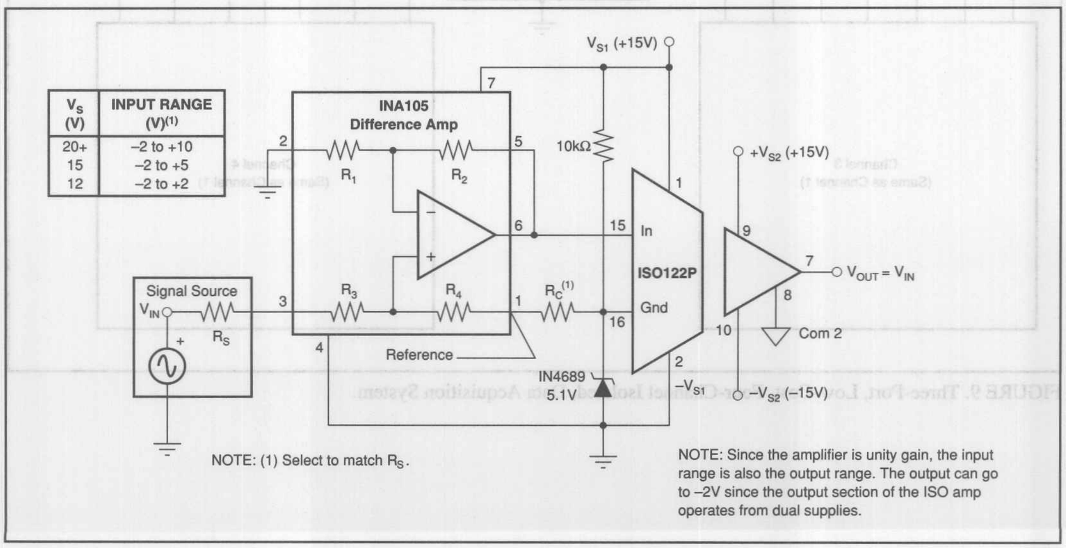


FIGURE 10. Improved PSR Using External Regulator.



V_S (V)	INPUT RANGE (V)(1)
20+	−2 to +10
15	−2 to +5
12	−2 to +2

FIGURE 11. Single Supply Operation of the ISO122P Isolation Amplifier. For additional information refer to AB-009.

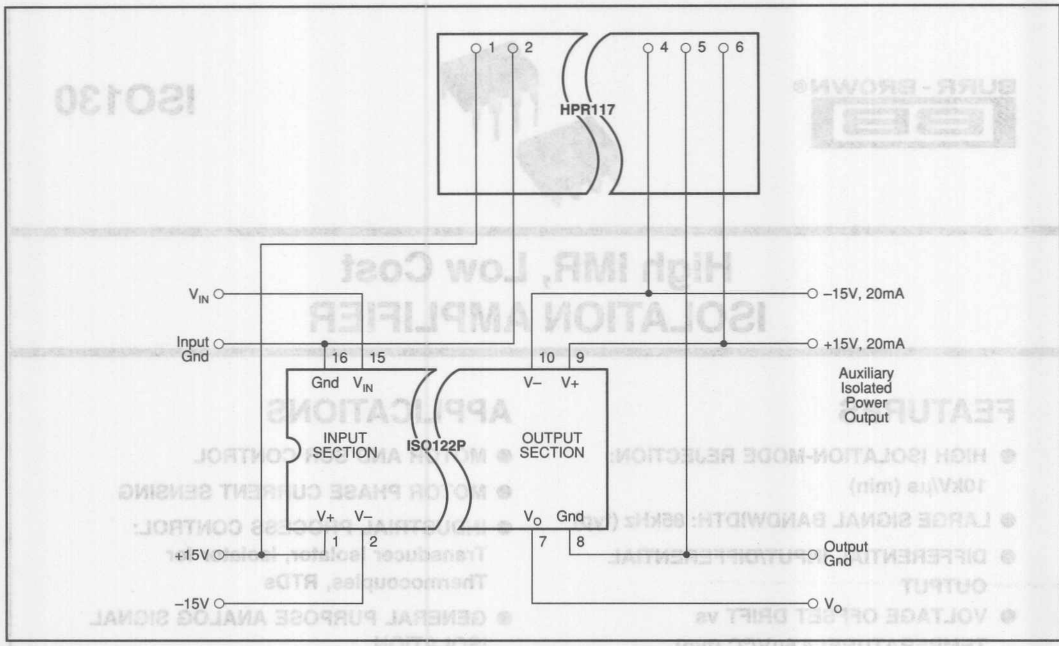


FIGURE 12. Input-Side Powered ISO Amp. For additional information refer to AB-024.

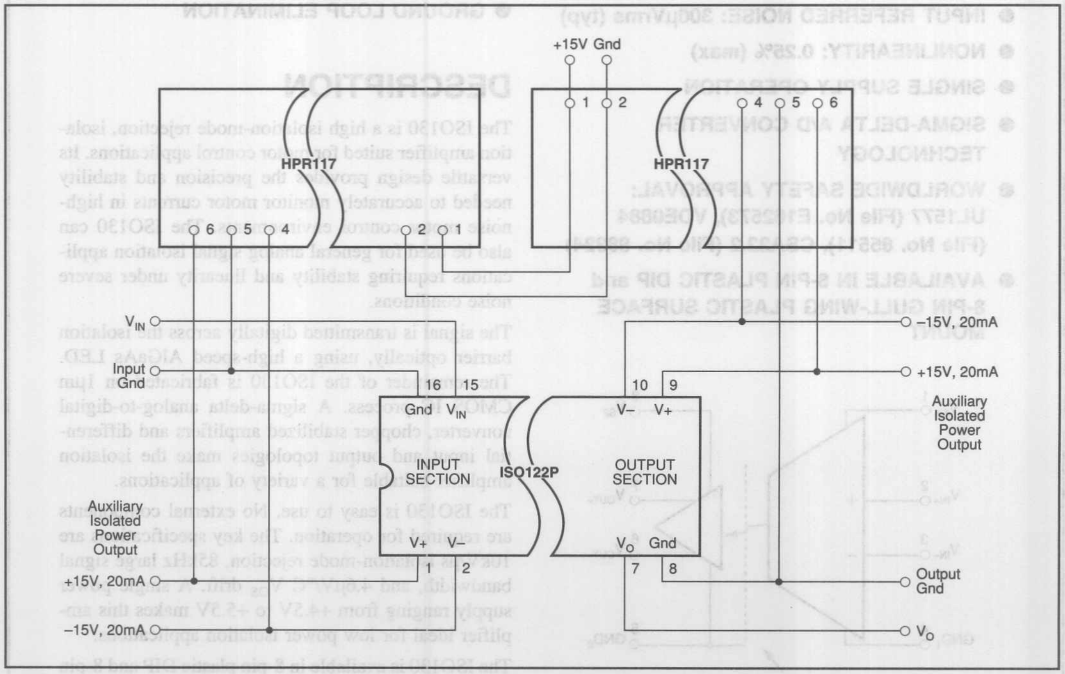
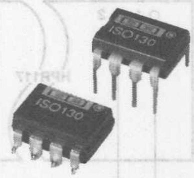


FIGURE 13. Powered ISO Amp with Three-Port Isolation. For additional information refer to AB-024.

BURR - BROWN®

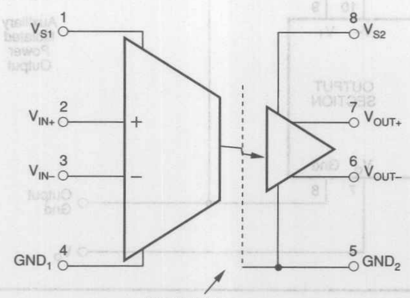


ISO130

High IMR, Low Cost ISOLATION AMPLIFIER

FEATURES

- HIGH ISOLATION-MODE REJECTION: 10kV/μs (min)
- LARGE SIGNAL BANDWIDTH: 85kHz (typ)
- DIFFERENTIAL INPUT/DIFFERENTIAL OUTPUT
- VOLTAGE OFFSET DRIFT vs TEMPERATURE: 4.6μV/°C (typ)
- OFFSET VOLTAGE 1.8mV (max)
- INPUT REFERRED NOISE: 300μVrms (typ)
- NONLINEARITY: 0.25% (max)
- SINGLE SUPPLY OPERATION
- SIGMA-DELTA A/D CONVERTER TECHNOLOGY
- WORLDWIDE SAFETY APPROVAL: UL1577 (File No. E162573), VDE0884 (File No. 85511), CSA22.2 (File No. 88324)
- AVAILABLE IN 8-PIN PLASTIC DIP and 8-PIN GULL-WING PLASTIC SURFACE MOUNT



APPLICATIONS

- MOTOR AND SCR CONTROL
- MOTOR PHASE CURRENT SENSING
- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs
- GENERAL PURPOSE ANALOG SIGNAL ISOLATION
- POWER MONITORING
- GROUND LOOP ELIMINATION

DESCRIPTION

The ISO130 is a high isolation-mode rejection, isolation amplifier suited for motor control applications. Its versatile design provides the precision and stability needed to accurately monitor motor currents in high-noise motor control environments. The ISO130 can also be used for general analog signal isolation applications requiring stability and linearity under severe noise conditions.

The signal is transmitted digitally across the isolation barrier optically, using a high-speed AlGaAs LED. The remainder of the ISO130 is fabricated on 1μm CMOS IC process. A sigma-delta analog-to-digital converter, chopper stabilized amplifiers and differential input and output topologies make the isolation amplifier suitable for a variety of applications.

The ISO130 is easy to use. No external components are required for operation. The key specifications are 10kV/μs isolation-mode rejection, 85kHz large signal bandwidth, and 4.6μV/°C V_{OS} drift. A single power supply ranging from +4.5V to +5.5V makes this amplifier ideal for low power isolation applications.

The ISO130 is available in 8-pin plastic DIP and 8-pin plastic gull-wing surface mount packages.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ISOLATION SPECIFICATIONS – VDE0884 INSULATION CHARACTERISTICS

At V_{IN}–, V_{IN}– = 0V, T_A = 25°C, V_{S1}, V_{S2} = 5.0V unless otherwise noted.

PARAMETER	CONDITIONS	ISO130P/ISO130PB ISO130U/ISO130UB CHARACTERISTIC	UNITS
ISOLATION CHARACTERISTICS			
Installation Classification	As Per VDE0109/12.83		
Table I			
Rated Mains Voltage ≤ 300Vrms		I-IV	
Rated Mains Voltage ≤ 600Vrms		I-III	
Climatic Classification		40/85/21	
Pollution Degree(1)	As Per VDE0109/12.83	2	
Maximum Working Insulation Voltage (V_{IORM})		600	Vrms
Side A to Side B Test Voltage, Method b (V_{PR})(9)			
Partial Discharge < 5pC	V_{PR} = 1.6 x V_{IORM}, t_P = 1s	960	Vrms
Side A to Side B Test Voltage, Method a (V_{PR})(9)	Type and Sample Test		
Partial Discharge < 5pC	V_{PR} = 1.2 x V_{IORM}, t_P = 60s	720	Vrms
Highest Allowable Overvoltage (V_{TR})(9)	Transient Overvoltage, t_{TR} = 10s	6000	V_{PEAK}
Safety-Limiting Values			
Case Temperature (T_{SI})		175	°C
Input Power ($P_{SI\ (INPUT)}$)		80	mW
Output Power ($P_{SI\ (OUTPUT)}$)		250	mW
INSULATION RELATED SPECIFICATIONS			
Min. External Air Gap (clearance)		> 7	mm
Min. External Tracking Path (creepage)		8	mm
Internal Isolation Gap (clearance)		0.5	mm
Tracking Resistance (CTI)		175	V
Isolation Group	per VDE0109	III a	
Insulation Resistance	25°C, V_{ISO} = 500V	≥ 10^{11}	Ω

SPECIFICATIONS

ISOLATION SPECIFICATIONS

At V_{IN}+, V_{IN}– = 0V, T_A = 25°C, V_{S1}, V_{S2} = 5.0V, unless otherwise noted.

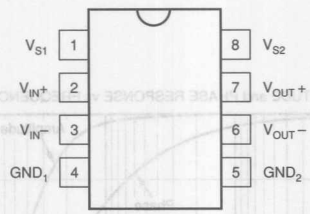
PARAMETER	CONDITIONS	ISO130P, ISO130PB ISO130U, ISO130UP MIN	TYP	MAX	UNITS
ISOLATION					
Input-Output Surge Withstand Voltage(8, 9), (In accordance with UL1577)	t = 1_{MIN}, RH ≤ 50%	3750			Vrms
Barrier Impedance(9)					
Resistance	V_{ISO} = 500VDC		10^{13}		Ω
Capacitance	f = 1MHz		0.7		pF
Isolation Mode Voltage Errors					
Rising Edge Transient Immunity	V_{IM} = 1kV, ∂ V_{OUT} < 50mV	10	25		kV/µs
Falling Edge Transient Immunity	V_{IM} = 1kV, ∂ V_{OUT} < 50mV	10	15		kV/µs
Isolation Mode Rejection Ratio(2)			> 140		dB

At $V_{IN}+$, $V_{IN}-$ = 0V, T_A = 25°C, V_{S1}, V_{S2} = 5.0V unless otherwise noted.

		ISO130P/ISO130PB ISO130U/ISO130UB			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT					
Initial Offset Voltage		–1.8	–0.9	0.0	mV
vs Temperature			4.6		µV/°C
vs V_{S1}			30		µV/V
vs V_{S2}			–40		µV/V
Power Supply Rejection; V_{S1} and V_{S2} Together	1MHz Square Wave, 5ns Rise/Fall Time		5		mV/V
Noise	0.1Hz to 100kHz		300		µVrms
Input Voltage Range		–200		200	mV
Maximum Input Voltage Range before Output Clipping			±300		mV
Initial Input Bias Current[3]			–670		nA
vs Temperature			3		nA/°C
Input Resistance[3]			530		kΩ
vs Temperature			0.38		%/°C
Common-Mode Rejection Ratio[4]			72		dB
GAIN[5]					
Initial Gain					
ISO130P/ISO130U	–200mV < $V_{IN}+$ < 200mV	7.61	8.00	8.40	V/V
ISO130PB/ISO130UB	–200mV < $V_{IN}+$ < 200mV	7.85	7.93	8.01	V/V
Gain vs Temperature			10		ppm/°C
Gain vs V_{S1}			2.1		ppm/mV
Gain vs V_{S2}			–0.6		ppm/mV
Gain Nonlinearity					
for –200mV < $V_{IN}+$ < 200mV			0.2	0.35	%
for –100mV < $V_{IN}+$ < 100mV			0.1	0.25	%
vs Temperature[6]	–200mV < $V_{IN}+$ < 200mV		–0.001		% pts/°C
vs V_{S1}[6]	–200mV < $V_{IN}+$ < 200mV		–0.005		% pts/V
vs V_{S2}[6]	–200mV < $V_{IN}+$ < 200mV		–0.007		% pts/V
OUTPUT					
Voltage Range					
High	$V_{IN}+$ = +500mV		3.61		V
Low	$V_{IN}+$ = –500mV		1.18		V
Common-Mode Voltage	–40°C < T_A < 85°C, 4.5V < V_{S1} < 5.5V	2.2	2.39	2.6	V
Current Drive[7]			1		mA
Short-Circuit Current	V_{OUT} = 0V or V_{OUT} = V_{S2}		9.3		mA
Output Resistance			11		Ω
vs Temperature			0.6		%/°C
FREQUENCY RESPONSE					
Bandwidth					
–3dB	–40°C to 85°C	50	85		kHz
–45°			35		kHz
Rise/Fall Time (10% - 90%)	–40°C to 85°C		4.3	6.6	µs
Propagation Delay					
to 10%	–40°C to 85°C		2.0	3.3	µs
to 50%	–40°C to 85°C		3.4	5.6	µs
to 90%	–40°C to 85°C		6.3	9.9	µs
POWER SUPPLIES					
Rated Voltage			5.0		V
Voltage Range		4.5		5.5	V
Quiescent Current					
V_{S1}	$V_{IN}+$ = 200mV, –40°C < T_A < 85°C, 4.5V < V_{S1} < 5.5V		10.7	15.5	mA
V_{S2}	–40°C < T_A < 85°C, 4.5V < V_{S1} < 5.5V		11.6	15.5	mA
TEMPERATURE RANGE					
Specification		–40		85	°C
Operating		–40		100	°C
Storage		–55		125	°C
θ_{C-A}			86		°C/W

NOTES: (1) This part may also be used in Pollution Degree 3 environments where the rated mains voltage is 300Vrms (per DIN VDE0109/12.83). (2) IMRR = 20 log ($\partial V_{IN}/\partial V_{ISO}$). (3) Time averaged value. (4) $V_{IN}+$ = $V_{IN}-$ = V_{CM}. CMRR = 20 log ($\partial V_{CM}/\partial V_{OS}$). (5) The slope of the best-fit line of ($V_{OUT+} - V_{OUT-}$) vs ($V_{IN+} - V_{IN-}$). (6) Change in nonlinearity vs temperature or supply voltage expressed in number of percentage points per °C or volt. (7) For best offset voltage performance. (8) For devices with minimum V_{ISO} specified at 3750Vrms, each isolation amplifier is proof-tested by applying an insulation test voltage ≥ 4500Vrms for 1 second (leakage current < 5µA). This specification does not guarantee continuous operation. (9) Pins 1-4 are shorted together and pins 5-8 are shorted together for this test.

Top View 8-Pin DIP/SOIC



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Supply Voltages: V_{S1}, V_{S2} .... 0V to 5.5V
Steady-State Input Voltage .... –2V to V_{S1} + 0.5V
2 Second Transient Input Voltage .... –6.0V
Output Voltages: V_{OUT}+, V_{OUT}– .... –0.5V to V_{S2} + 0.5V
Lead Temperature Solder (1.6mm below seating plane, 10s) .... 260°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO130P	8-Pin Plastic DIP	006-3
ISO130PB	8-Pin Plastic DIP	006-3
ISO130U	8-Pin Gull-Wing Plastic Surface Mount	006-2
ISO130UB	8-Pin Gull-Wing Plastic Surface Mount	006-2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

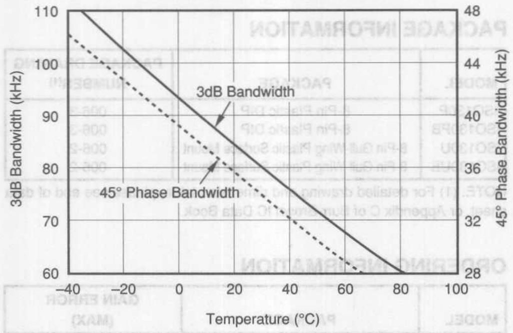
ORDERING INFORMATION

MODEL	PACKAGE	GAIN ERROR (MAX)
ISO130P	8-Pin Plastic DIP	±5% (mean value = 8.00)
ISO130PB	8-Pin Plastic DIP	±1% (mean value = 7.93)
ISO130U	8-Pin Gull-Wing Plastic Surface Mount	±5% (mean value = 8.00)
ISO130UB	8-Pin Gull-Wing Plastic Surface Mount	±1% (mean value = 7.93)

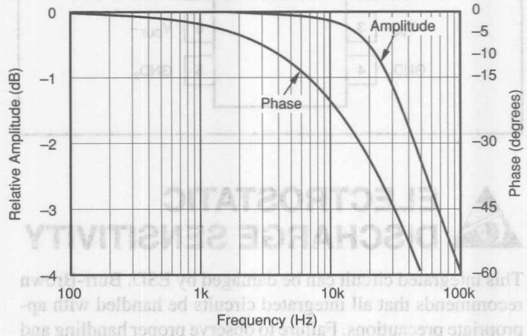
TYPICAL PERFORMANCE CURVES

At $T_A = 25°C$, V_{S1}, $V_{S2} = 5.0V_{DC}$, $V_{IN}+$, $V_{IN}- = 0V$ unless otherwise noted.

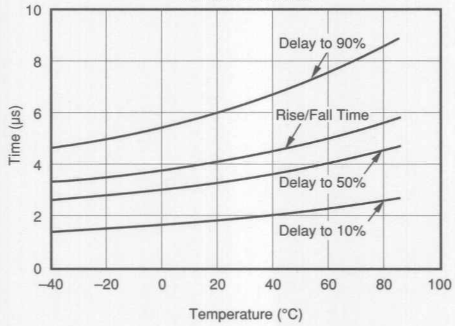
BANDWIDTH vs TEMPERATURE



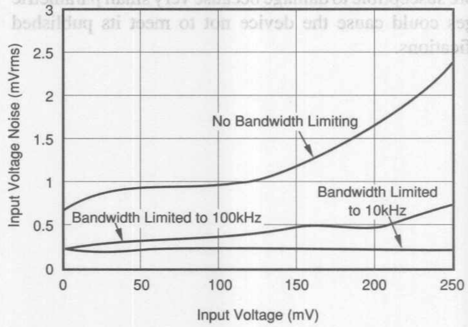
AMPLITUDE and PHASE RESPONSE vs FREQUENCY



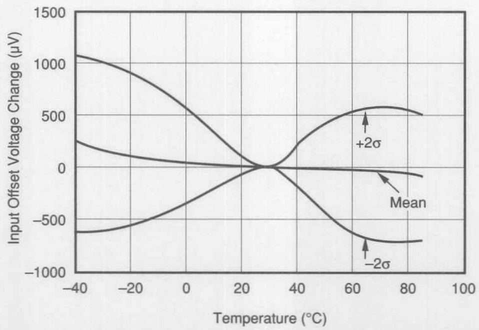
PROPAGATION DELAYS and RISE/FALL TIME vs TEMPERATURE



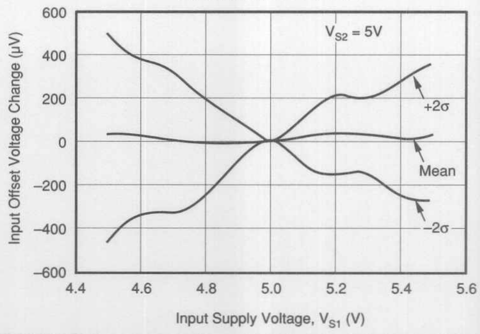
INPUT VOLTAGE NOISE vs INPUT VOLTAGE



INPUT OFFSET VOLTAGE CHANGE vs TEMPERATURE



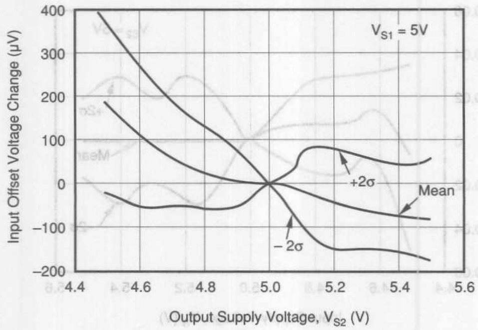
INPUT OFFSET VOLTAGE CHANGE vs INPUT SUPPLY VOLTAGE



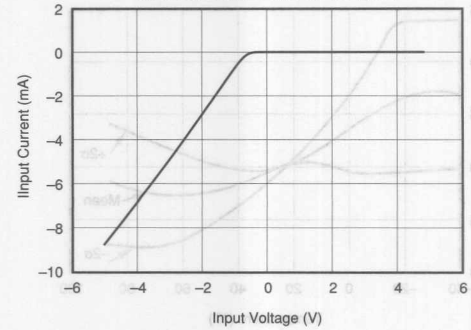
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = 25°C, V_{S1}, V_{S2} = 5.0V_{DC}, V_{IN}+, V_{IN}– = 0V unless otherwise noted.

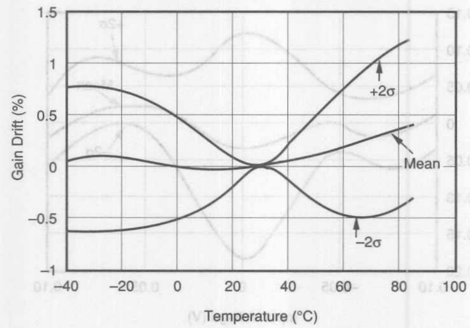
INPUT OFFSET VOLTAGE CHANGE vs OUTPUT SUPPLY VOLTAGE



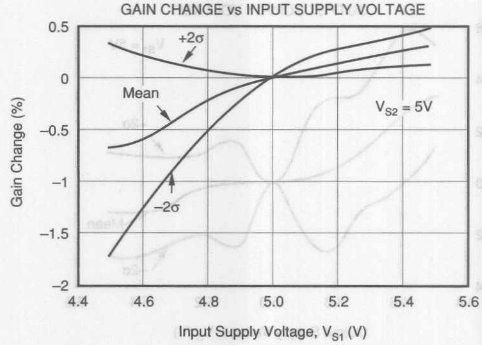
INPUT CURRENT vs INPUT VOLTAGE



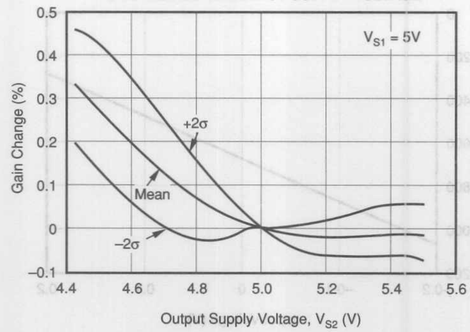
GAIN DRIFT vs TEMPERATURE



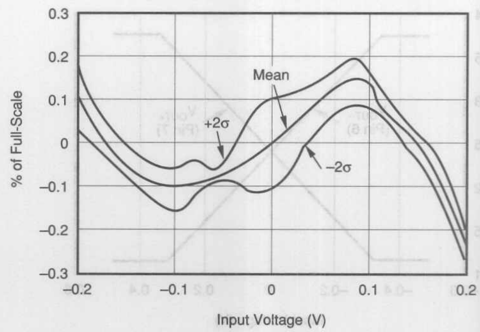
GAIN CHANGE vs INPUT SUPPLY VOLTAGE



GAIN CHANGE vs OUTPUT SUPPLY VOLTAGE

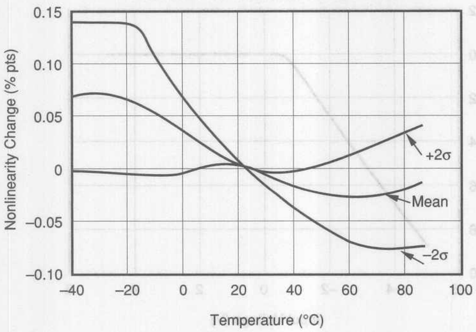


NONLINEARITY ERROR vs INPUT VOLTAGE

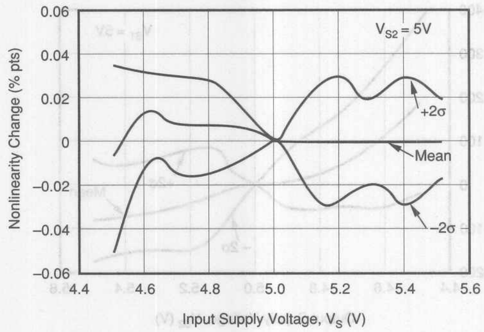


At $T_A = 25°C$, V_{S1}, $V_{S2} = 5.0V_{DC}$, $V_{IN}+$, $V_{IN}- = 0V$ unless otherwise noted.

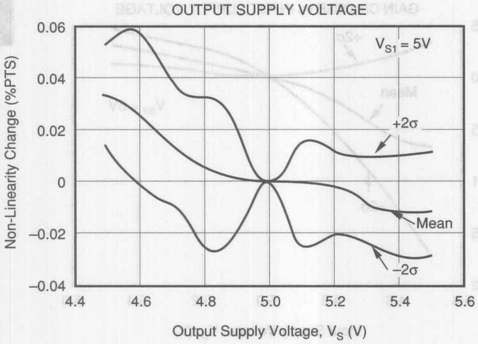
NONLINEARITY CHANGE vs TEMPERATURE



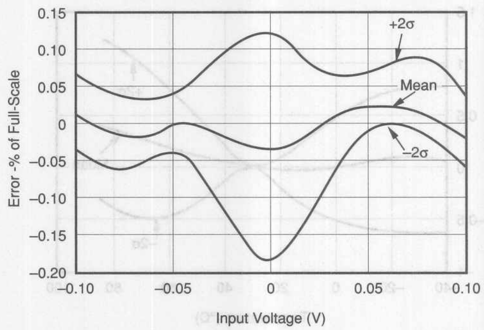
NONLINEARITY CHANGE vs INPUT SUPPLY VOLTAGE



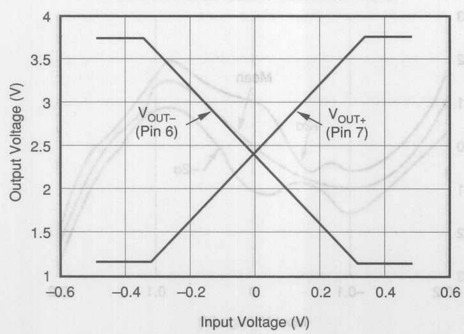
NONLINEARITY CHANGE vs OUTPUT SUPPLY VOLTAGE



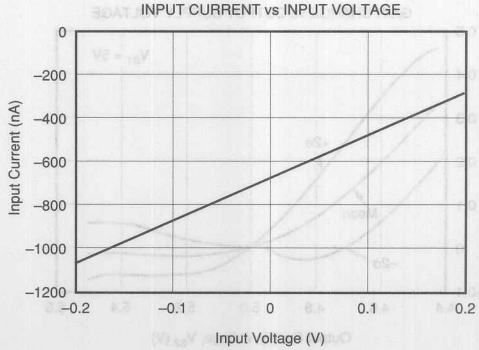
NONLINEARITY ERROR vs INPUT VOLTAGE



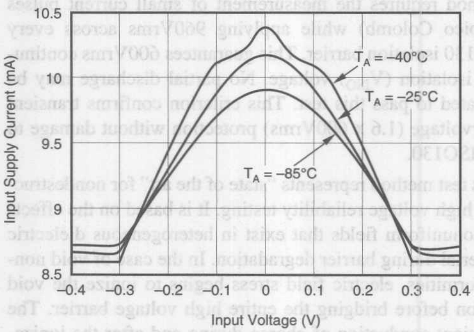
OUTPUT VOLTAGE vs INPUT VOLTAGE



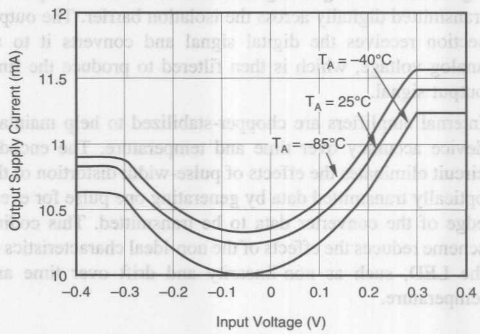
INPUT CURRENT vs INPUT VOLTAGE



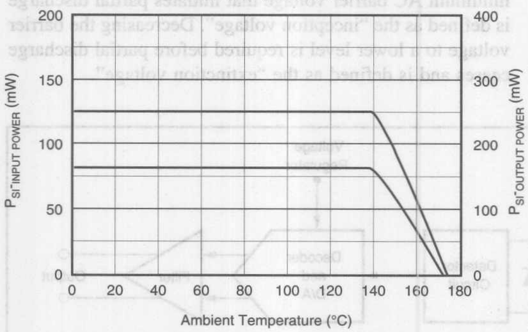
INPUT SUPPLY CURRENT vs INPUT VOLTAGE



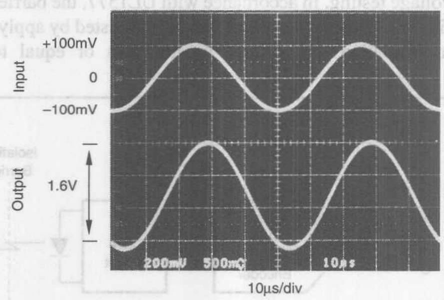
OUTPUT SUPPLY CURRENT vs INPUT VOLTAGE



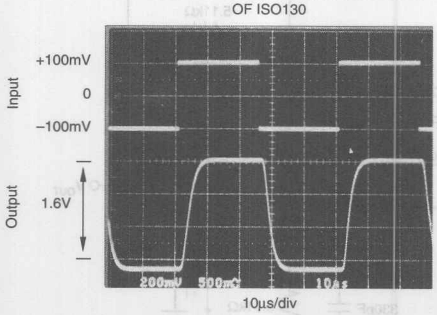
DEPENDENCE OF SAFETY-LIMITING PARAMETERS ON AMBIENT TEMPERATURE



LARGE SIGNAL SINUSOIDAL RESPONSE OF ISO130

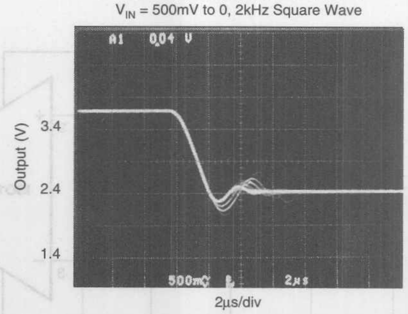


LARGE SIGNAL SQUARE WAVE RESPONSE OF ISO130



OVERLOAD RECOVERY OF ISO130

V_{IN} = 500mV to 0, 2kHz Square Wave



ISOLATION PRODUCTS 5 ISO130

THEORY OF OPERATION

The ISO130 isolation amplifier (Figure 1) uses an input and output section galvanically isolated by a high speed optical barrier built into the plastic package. The input signal is converted to a time averaged serial bit stream by use of a sigma-delta analog-to-digital converter and then optically transmitted digitally across the isolation barrier. The output section receives the digital signal and converts it to an analog voltage, which is then filtered to produce the final output signal.

Internal amplifiers are chopper-stabilized to help maintain device accuracy over time and temperature. The encoder circuit eliminates the effects of pulse-width distortion of the optically transmitted data by generating one pulse for every edge of the converter data to be transmitted. This coding scheme reduces the effects of the non-ideal characteristics of the LED, such as non-linearity and drift over time and temperature.

ISOLATION AND INSULATION SPECIFICATIONS

The performance of the isolation barrier of the ISO130 is specified with three specifications, two of which require high voltage testing. In accordance with UL1577, the barrier integrity of each isolation amplifier is proof-tested by applying an insulation test voltage greater than or equal to 4500Vrms for one second. This is to guarantee the isolation amplifier will survive a 3750V transient voltage. The barrier leakage current test limit is 5µA. Pins 1-4 are shorted together and pins 5-8 are shorted together during the test.

This test is followed by the partial discharge isolation voltage test as specified in the German VDE0884. This method requires the measurement of small current pulses (<5pico Colomb) while applying 960Vrms across every ISO130 isolation barrier. This guarantees 600Vrms continuous isolation (V_{ISO}) voltage. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 x 600Vrms) protection without damage to the ISO130.

This test method represents "state of the art" for nondestructive high voltage reliability testing. It is based on the effects of nonuniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01 to 0.1µs current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the "inception voltage". Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage".

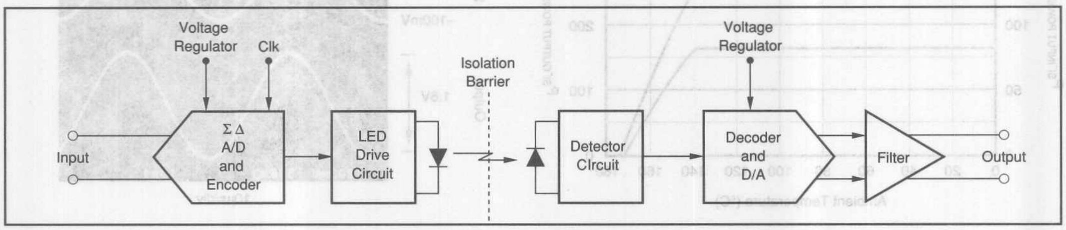


FIGURE 1. Block Diagram of ISO130 Isolation Amplifier.

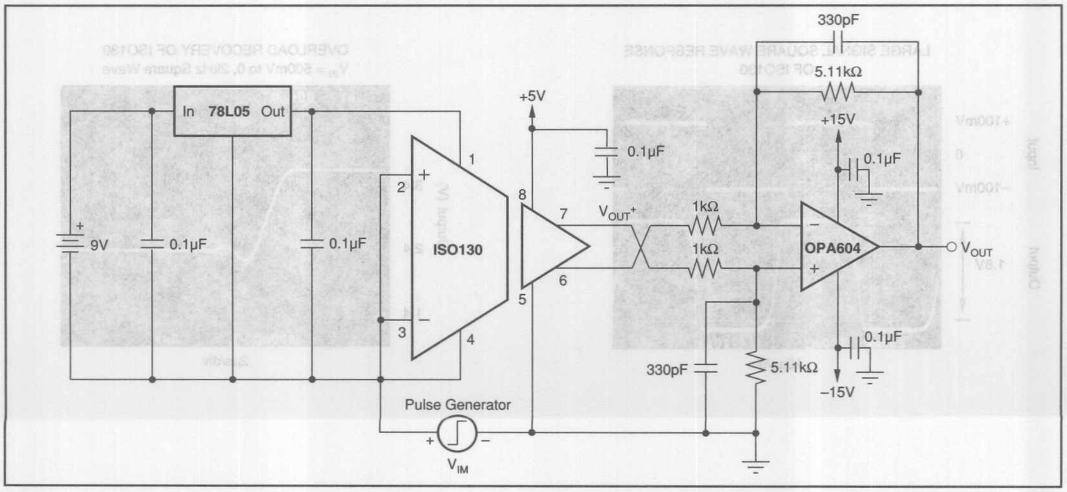


FIGURE 2. Isolation Mode Rejection and Transient Immunity Test Circuit.

Both tests are 100% production tests. The partial discharge testing of the ISO130 is performed after the UL1577 test criterion giving more confidence in the barrier reliability.

The third guaranteed isolation specification for the ISO130 is Transient Immunity (TI), which specifies the minimum rate of rise or fall of an isolation mode noise signal at which small output perturbations begin to occur. An isolation mode signal is defined as a signal appearing between the isolated grounds, GND_1 and GND_2. Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds. Under certain circumstances this voltage across the isolation barrier can induce errors at the output of the isolation amplifier. Figure 2 shows the Transient Immunity Test Circuit for the ISO130. In this test circuit a pulse generator is placed between the isolated grounds (GND_1 and GND_2). The inputs of the ISO130 are both tied to GND_1. A difference amplifier is used to gain the output signal of the ISO130. A Transient Immunity failure is determined when the output of the ISO130 changes by more than 50mV as illustrated in Figure 3.

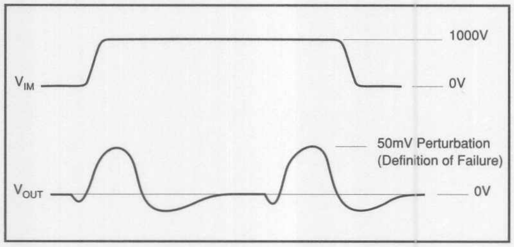


FIGURE 3. Typical Transient Immunity Failure Waveform.

Finally, Isolation Mode Rejection Ratio (typically >140dB for the ISO130) is defined as the ratio of differential signal gain to the isolation mode gain at 60Hz. The magnitude of the 60Hz voltage across the isolation barrier during this test is not so large as to cause Transient Immunity errors. The Isolation Mode Rejection Ratio should not be confused with the Common Mode Rejection Ratio. The Common Mode Rejection Ratio defines the relationship of differential signal gain (signal applied differentially between pins 2 and 3) to the common mode gain (input pins tied together and the signal applied to both inputs at the same time).

APPLICATIONS INFORMATION

APPLICATION CIRCUITS

Figure 4 illustrates a typical application for the ISO130. In this motor control circuit, the current that is sent to the motor is sensed by the resistor, R_{SENSE}. The voltage drop across this resistor is gained up by the ISO130 and then transmitted across the isolation barrier. A difference amplifier, A_2, is used to change the differential output signal of the ISO130 to a single ended signal. This voltage information is then sent to the control circuitry of the motor. The ISO130 is particularly well suited for this application because of its superior Transient Immunity (10kV/µs, max) and its excellent immunity to RF noise.

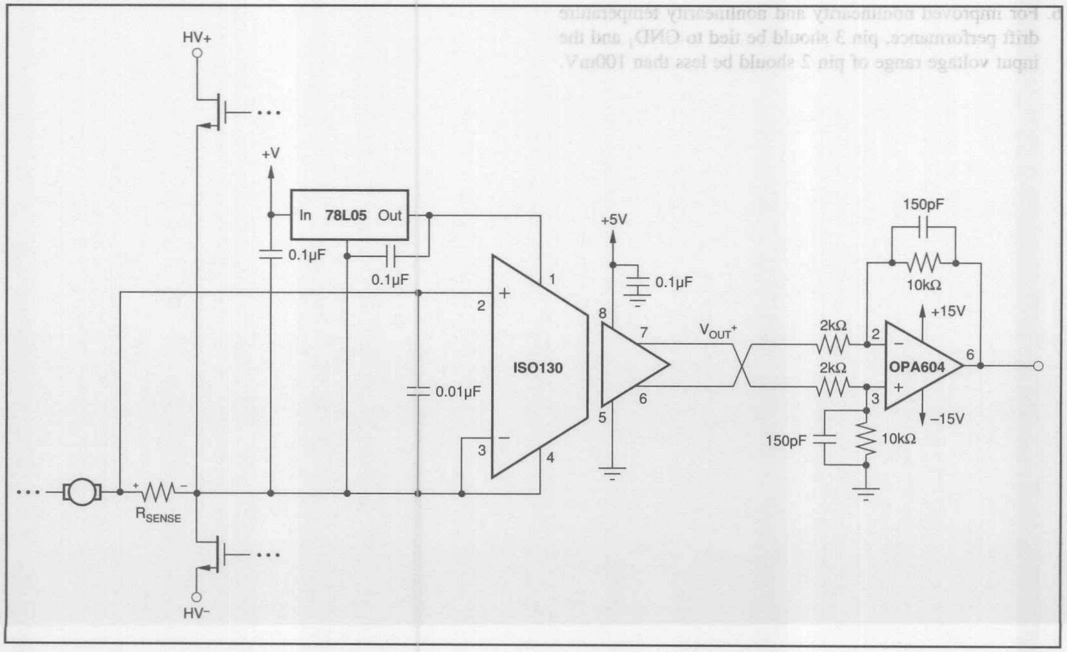


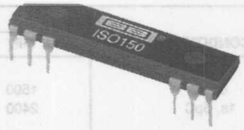
FIGURE 4. ISO130 Used to Monitor Motor Current.

value of resistance (to minimize power dissipation), a fairly low inductance (to accurately reflect high-frequency signal components), and a reasonably tight tolerance (to maintain overall circuit accuracy).

LAYOUT SUGGESTIONS

1. Bypass capacitors should be located as close as possible to the input and output power supply pins.
2. In some applications, offset voltage can be reduced by placing a 0.01µF capacitor from pin 2 and/or pin 3 to GND_1. This noise can be caused by the combination of long input leads and the switched-capacitor nature of the input circuit. This capacitor(s) should be placed as close to the isolation amplifier as possible.
3. The trace lengths at input should be kept short or a twisted wire pair should be used to minimize EMI and inductance effects. For optimum performance, the input signal should be as close to the input pins a possible.
4. A maximum distance between the input and output sides of the isolation amplifier should be maintained in the layout in order to minimize stray capacitance. This practice will help obtain optimal Isolation Mode performance. Ground planes should not pass below the device on the PCB.
5. Care should be taken in selecting isolated power supplies or regulators. The ISO130 can be affected by changes in the power supply voltages. Carefully regulated power supplies are recommended.
6. For improved nonlinearity and nonlinearity temperature drift performance, pin 3 should be tied to GND_1 and the input voltage range of pin 2 should be less than 100mV.

BURR - BROWN®



ISO150

Dual, Isolated, Bi-Directional DIGITAL COUPLER

FEATURES

- REPLACES HIGH-PERFORMANCE OPTOCOUPLERS
- DATA RATE: 80M Baud, typ
- LOW POWER CONSUMPTION: 25mW Per Channel, max
- TWO CHANNELS, EACH BI-DIRECTIONAL, PROGRAMMABLE BY USER
- PARTIAL DISCHARGE TESTED: 2400Vrms
- CREEPAGE DISTANCE OF 16.5mm (DIP)
- LOW COST PER CHANNEL
- PLASTIC DIP AND SOIC PACKAGES

APPLICATIONS

- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- ISOLATED UART INTERFACE
- MULTIPLEXED DATA TRANSMISSION
- ISOLATED PARALLEL TO SERIAL INTERFACE
- TEST EQUIPMENT
- MICROPROCESSOR SYSTEM INTERFACE
- ISOLATED LINE RECEIVER
- GROUND LOOP ELIMINATION

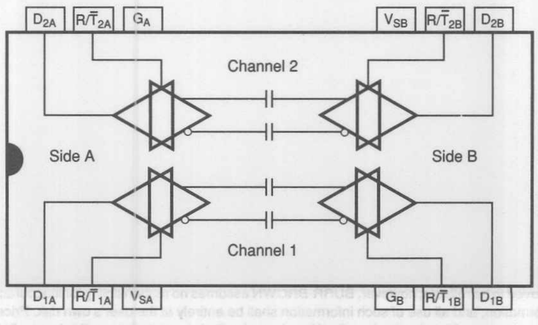
DESCRIPTION

The ISO150 is a two-channel, galvanically isolated data coupler capable of data rates of 80MBaud, typical. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high voltage 0.4pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6kV/µs.

ISO150 avoids the problems commonly associated with optocouplers. Optically isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25mW per channel.

ISO150 is available in a 24-pin DIP package and in a 28-lead SOIC. Both are specified for operation from –40°C to 85°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25°C$ and $V_S = +5V$, unless otherwise noted.

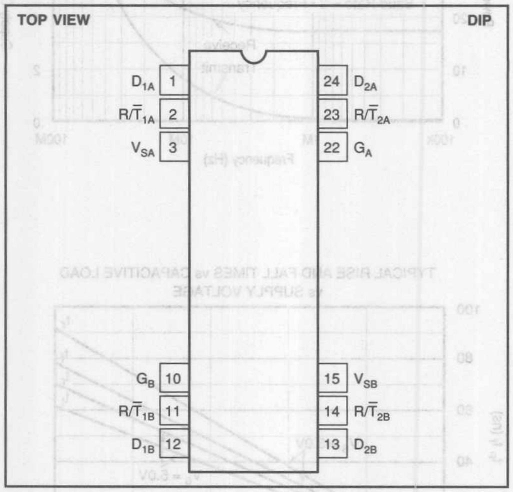
		ISO150AP, AU			
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
ISOLATION PARAMETERS					
Rated Voltage, Continuous	60Hz	1500			Vrms
Partial Discharge, 100% Test(1)	1s, 5pC	2400			Vrms
Creepage Distance (External)					
DIP—"P" Package			16		mm
SOIC—"U" Package			7.2		mm
Internal Isolation Distance			0.10		mm
Isolation Voltage Transient Immunity(2)			1.6		kV/µs
Barrier Impedance			$>10^{14}$ || 7		Ω || pF
Leakage Current	240Vrms, 60Hz		0.6		µArms
DC PARAMETERS					
Logic Output Voltage, High, V_{OH}	I_{OH} = 6mA	V_S–1		V_S	V
Low, V_{OL}	I_{OL} = 6mA	0		0.4	V
Logic Output Short-Circuit Current	Source or Sink		30		mA
Logic Input Voltage, High(3)		2		V_S	V
Low(3)		0		0.8	V
Logic Input Capacitance			5		pF
Logic Input Current			<1		nA
Power Supply Voltage Range(3)		3	5	5.5	V
Power Supply Current(4)					
Transmit Mode	DC		0.001	100	µA
	50MBaud		14		mA
Receive Mode	DC		7.2	10	mA
	50MBaud		16		mA
AC PARAMETERS					
Data Rate, Maximum(5)	C_L = 50pF	50	80		MBaud
Data Rate, Minimum		DC			
Propagation Time(6)	C_L = 50pF	20	27	40	ns
Propagation Delay Skew(7)	C_L = 50pF		0.5	2	ns
Pulse Width Distortion(8)	C_L = 50pF		1.5	6	ns
Output Rise/Fall Time, 10% to 90%	C_L = 50pF		9	14	ns
Mode Switching Time					
Receive-to-Transmit			13		ns
Transmit-to-Receive			75		ns
TEMPERATURE RANGE					
Operating Range		–40		85	°C
Storage		–40		125	°C
Thermal Resistance, θ_{JA}			75		°C/W

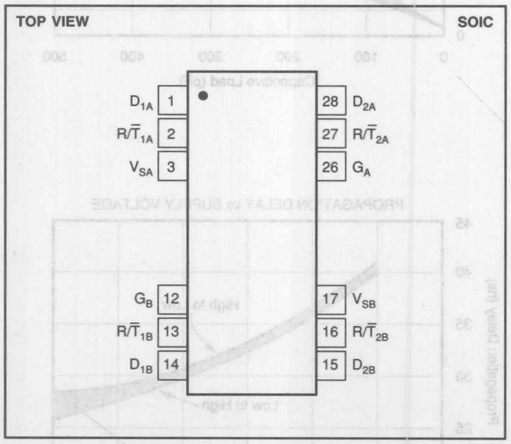
NOTES: (1) All devices receive a 1s test. Failure criterion is ≥5 pulses of ≥5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors. (3) Logic inputs are HCT-type and thresholds are a function of power supply voltage with approximately 0.4V hysteresis—see text. (4) Supply current measured with both tranceivers set for the indicated mode. Supply current varies with data rate—see typical curves. (5) Calculated from the maximum Pulse Width Distortion (PWD), where Data Rate = 0.3/PWD. (6) Propagation time measured from V_{IN} = 1.5V to V_O = 2.5V. (7) The difference in propagation time of channel A and channel B in any combination of transmission directions. (8) The difference between progagation time of a rising edge and a falling edge.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–40°C to +125°C
Supply Voltages, V_S	–0.5 to 6V
Transmitter Input Voltage, V_I	–0.5 to V_S + 0.5V
Receiver Output Voltage, V_O	–0.5 to V_S + 0.5V
$R/\overline{T}_X$ Inputs	–0.5 to V_S + 0.5V
Isolation Voltage dV/dt, V_{ISO}	500kV/µs
D_X Short to Ground	Continuous
Junction Temperature, T_J	175°C
Lead Temperature (soldering, 10s)	260°C
1.6mm below seating plane (DIP package)	300°C

PIN CONFIGURATION





PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ISO150AP	24-Pin Single-Wide DIP	243-1
ISO150AU	28-Lead SOIC	217-2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN DESCRIPTIONS

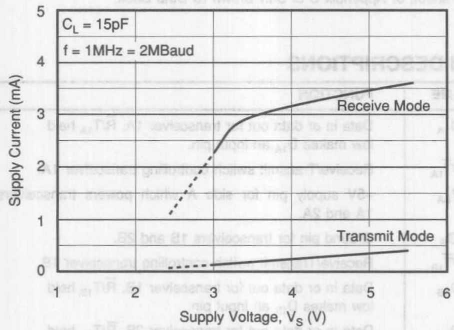
NAME	FUNCTION
D_{1A}	Data in or data out for transceiver 1A. $\overline{R}/T_{1A}$ held low makes D_{1A} an input pin.
$R/\overline{T}_{1A}$	Receive/Transmit switch controlling transceiver 1A.
V_{SA}	+5V supply pin for side A which powers transceivers 1A and 2A.
G_B	Ground pin for transceivers 1B and 2B.
$R/\overline{T}_{1B}$	Receive/Transmit switch controlling transceiver 1B.
D_{1B}	Data in or data out for transceiver 1B. $\overline{R}/T_{1B}$ held low makes D_{1B} an input pin.
D_{2B}	Data in or data out for transceiver 2B. $\overline{R}/T_{2B}$ held low makes D_{2B} an input pin.
$R/\overline{T}_{2B}$	Receive/Transmit switch controlling D_{2B}.
V_{SB}	+5V supply pin for side B which powers transceivers 1B and 2B.
G_A	Ground pin for transceivers 1A and 2A.
$R/\overline{T}_{2A}$	Receive/Transmit switch controlling transceiver 2A.
D_{2A}	Data in or data out for transceiver 2A. $\overline{R}/T_{2A}$ held low makes D_{2A} in input pin.

ELECTROSTATIC DISCHARGE SENSITIVITY

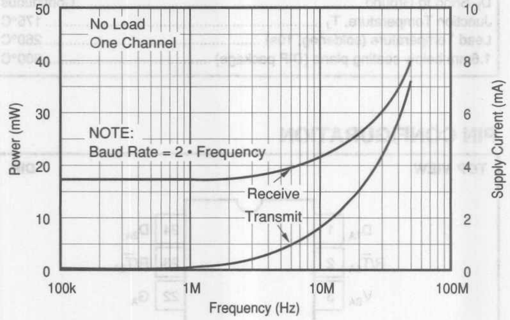
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

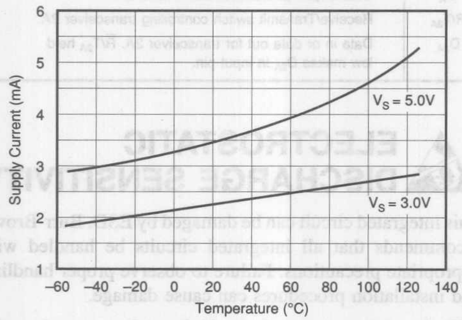
SUPPLY CURRENT PER CHANNEL vs SUPPLY VOLTAGE



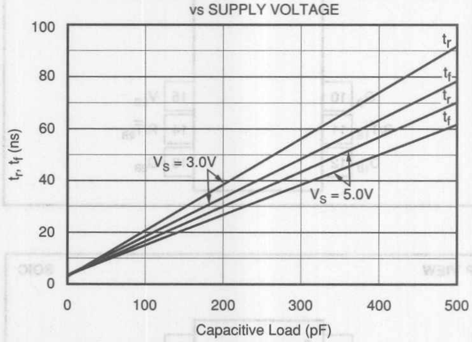
POWER CONSUMPTION PER CHANNEL vs FREQUENCY



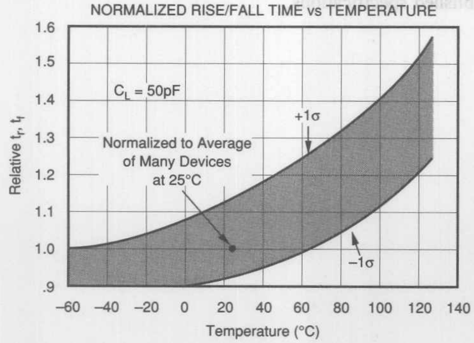
SUPPLY CURRENT PER CHANNEL vs TEMPERATURE



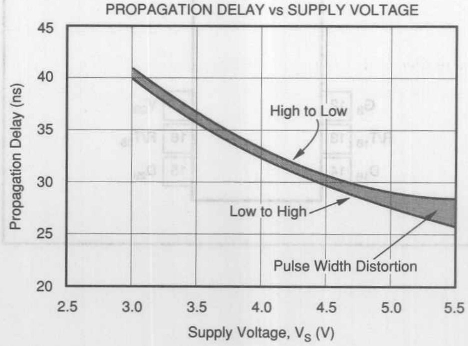
TYPICAL RISE AND FALL TIMES vs CAPACITIVE LOAD vs SUPPLY VOLTAGE

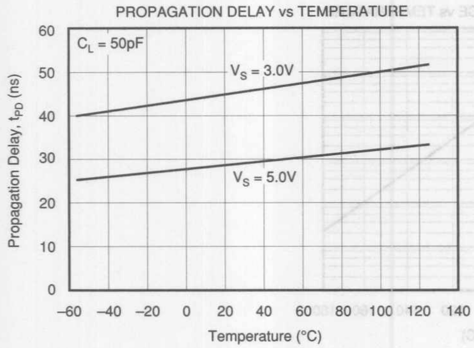


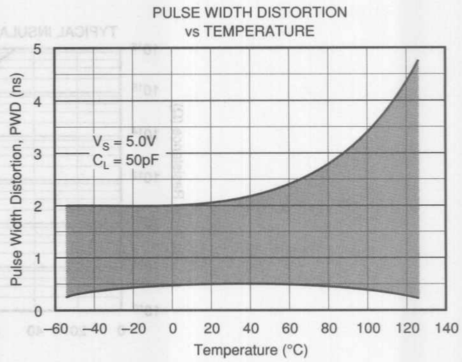
NORMALIZED RISE/FALL TIME vs TEMPERATURE

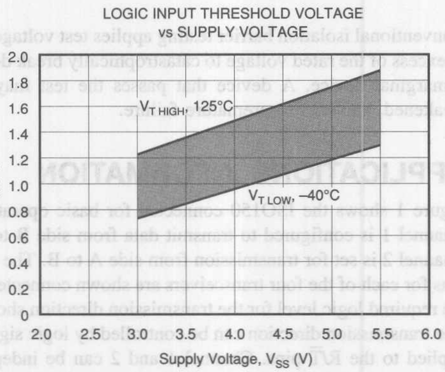


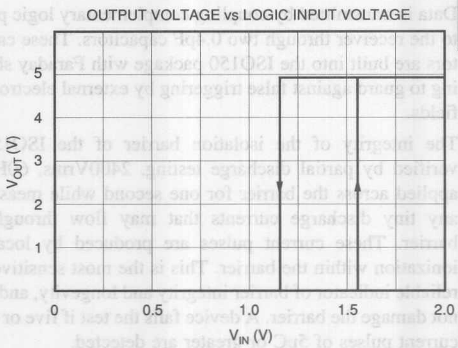
PROPAGATION DELAY vs SUPPLY VOLTAGE

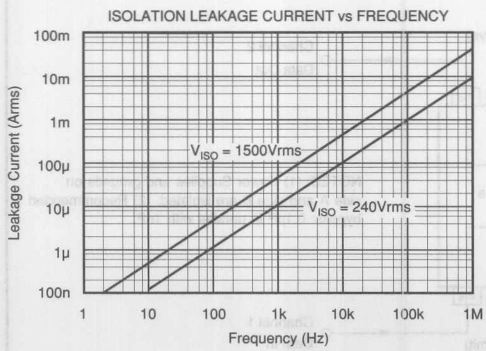


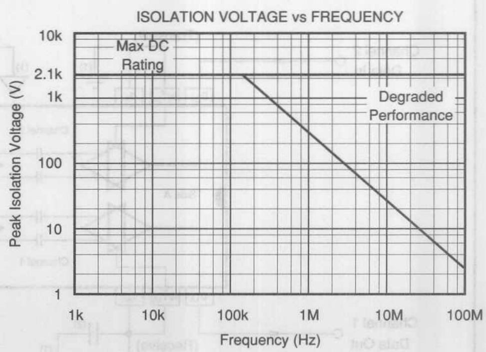

PROPAGATION DELAY vs TEMPERATURE
C_L = 50pF
V_S = 3.0V
V_S = 5.0V
Propagation Delay, t_{PD} (ns)
Temperature (°C)
60
50
40
30
20
10
0
–60 –40 –20 0 20 40 60 80 100 120 140


PULSE WIDTH DISTORTION vs TEMPERATURE
V_S = 5.0V
C_L = 50pF
Pulse Width Distortion, PWD (ns)
Temperature (°C)
5
4
3
2
1
0
–60 –40 –20 0 20 40 60 80 100 120 140


LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE
$V_{T\,HIGH}$, 125°C
$V_{T\,LOW}$, –40°C
V_{IN} (V)
Supply Voltage, V_{SS} (V)
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 6.0

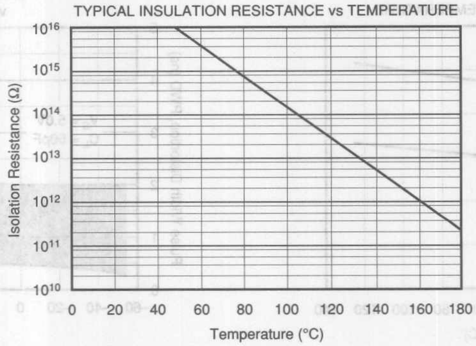

OUTPUT VOLTAGE vs LOGIC INPUT VOLTAGE
V_{OUT} (V)
V_{IN} (V)
5
4
3
2
1
0
0 0.5 1.0 1.5 2.0


ISOLATION LEAKAGE CURRENT vs FREQUENCY
V_{ISO} = 1500Vrms
V_{ISO} = 240Vrms
Leakage Current (Arms)
Frequency (Hz)
100m
10m
1m
100µ
10µ
1µ
100n
1 10 100 1k 10k 100k 1M


ISOLATION VOLTAGE vs FREQUENCY
Max DC Rating
Degraded Performance
Peak Isolation Voltage (V)
Frequency (Hz)
10k
2.1k
1k
100
10
1
1k 10k 100k 1M 10M 100M

TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$ and $V_S = +5V$, unless otherwise noted.



ISOLATION BARRIER

Data is transmitted by coupling complementary logic pulses to the receiver through two 0.4pF capacitors. These capacitors are built into the ISO150 package with Faraday shielding to guard against false triggering by external electrostatic fields.

The integrity of the isolation barrier of the ISO150 is verified by partial discharge testing. 2400Vrms, 60Hz, is applied across the barrier for one second while measuring any tiny discharge currents that may flow through the barrier. These current pulses are produced by localized ionization within the barrier. This is the most sensitive and reliable indicator of barrier integrity and longevity, and does not damage the barrier. A device fails the test if five or more current pulses of 5pC or greater are detected.

Conventional isolation barrier testing applies test voltage far in excess of the rated voltage to catastrophically break down a marginal device. A device that passes the test may be weakened, and lead to premature failure.

APPLICATIONS INFORMATION

Figure 1 shows the ISO150 connected for basic operation. Channel 1 is configured to transmit data from side B to A. Channel 2 is set for transmission from side A to B. The $R/\overline{T}$ pins for each of the four transceivers are shown connected to the required logic level for the transmission direction shown. The transmission direction can be controlled by logic signals applied to the $R/\overline{T}$ pins. Channel 1 and 2 can be independently controlled for the desired transmission direction.

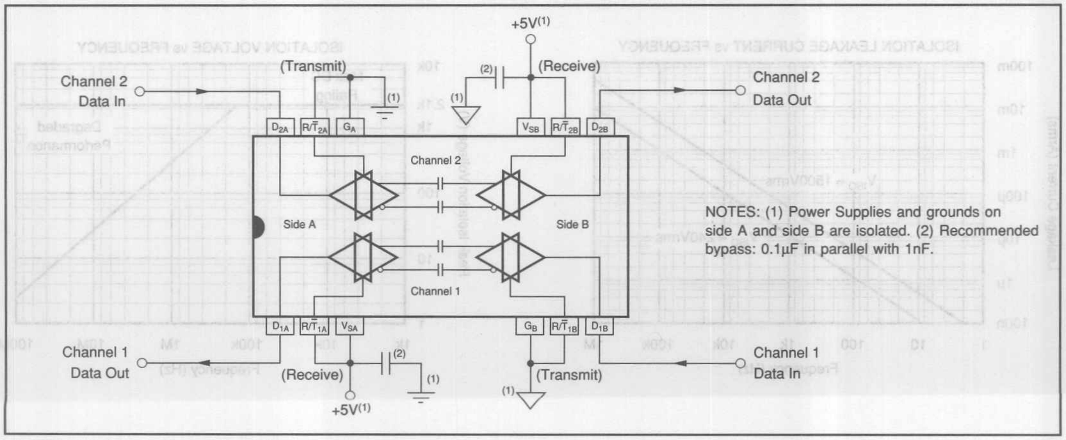


FIGURE 1. Basic Operation Diagram.

LOGIC LEVELS

A single pin serves as a data input or output, depending on the mode selected. Logic inputs are CMOS with thresholds set for TTL compatibility. The logic threshold is approximately 1.3V with 5V supplies and with approximately 400mV of hysteresis. Input logic thresholds vary with the power supply voltage. Drive the logic inputs with signals that swing the full logic voltage swing. The ISO150 will use somewhat greater quiescent current if logic inputs do not swing within 0.5V of the power supply rails.

In receive mode, the data output can drive 15 standard LS-TTL loads. It will also drive CMOS loads. The output drive circuits are CMOS.

POWER SUPPLY

Separate, isolated power supplies must be connected to side A and side B to provide galvanic isolation. Nominal rated supply voltage is 5V. Operation extends from 3V to 5.5V. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier.

The V_S pin for each side powers the transceivers for both channel 1 and 2. The specified supply current is the total of both transceivers on one side, both operating in the indicated mode. Supply current for one transceiver in transmit mode and one in receive mode can be estimated by averaging the specifications for transmit and receive operation. Supply current varies with the data transmission rate—see typical curves.

POWER-UP STATE

The ISO150 transmits information across the barrier only when the input-side data changes logic state. When a transceiver is first programmed for receive mode, or is powered-up in receive mode, its output is initialized "high". Subsequent changes of data applied to the input side will cause the output to properly reflect the input side data.

SIGNAL LOSS

The ISO150's differential-mode signal transmission and careful receiver design make it highly immune to voltage across the isolation barrier (isolation-mode voltage). Rapidly changing isolation-mode voltage can cause data errors. As the rate of change of isolation voltage is increased, there is a very sudden increase in data errors. Approximately 50% of ISO150s will begin to produce data errors with isolation-mode transients of 1.6kV/µs. This may occur as low as 500V/µs in some devices. In comparison, a 1000Vrms, 60Hz isolation-mode voltage has a rate of change of approximately 0.5V/µs.

Still, some applications with large, noisy isolation-mode voltage can produce data errors by causing the receiver output to change states. After a data error, subsequent changes in input data will produce correct output data.

PROPAGATION DELAY AND SKEW

Logic transitions are delayed approximately 27ns through the ISO150. Some applications are sensitive to data skew—the difference in propagation delay between channel 1 and channel 2. Skew is less than 2ns between channel 1 and channel 2. Applications using more than one ISO150 must allow for somewhat greater skew from device to device. Since all devices are tested for delay times of 20ns min to 40ns max, 20ns is the largest device-to-device data skew.

MODE CHANGES

The transmission direction of a channel can be changed "on the fly" by reversing the logic levels at the channel's R/$\overline{T}$ pins on both side A and side B. Approximately 75ns after the transceiver is programmed to receive mode its output is initialized "high", and will respond to subsequent input-side changes in data.

STANDBY MODE

Quiescent current of each transceiver circuit is very low in transmit mode when input data is not changing (1nA typical). To conserve power when data transmission is not required, program both side A and B transceivers for transmit mode. Input data applied to either transceiver is ignored by the other side. High speed data applied to either transceiver will increase quiescent current.

CIRCUIT LAYOUT

The high speed of the ISO150 and its isolation barrier require careful circuit layout. Use good high speed logic layout techniques for the input and output data lines. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier. Use low inductance connections. Ground planes are recommended.

Maintain spacing between side 1 and side 2 circuitry equal or greater than the spacing between the missing pins of the ISO150 (approximately 16mm for the DIP version). Sockets are not recommended.

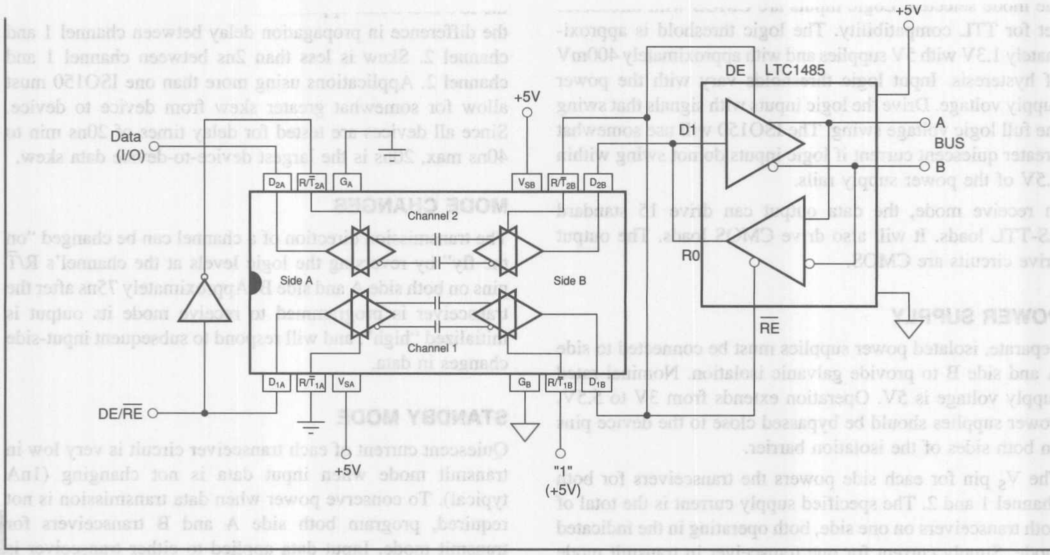


FIGURE 2. Isolated RS-485 Interface.

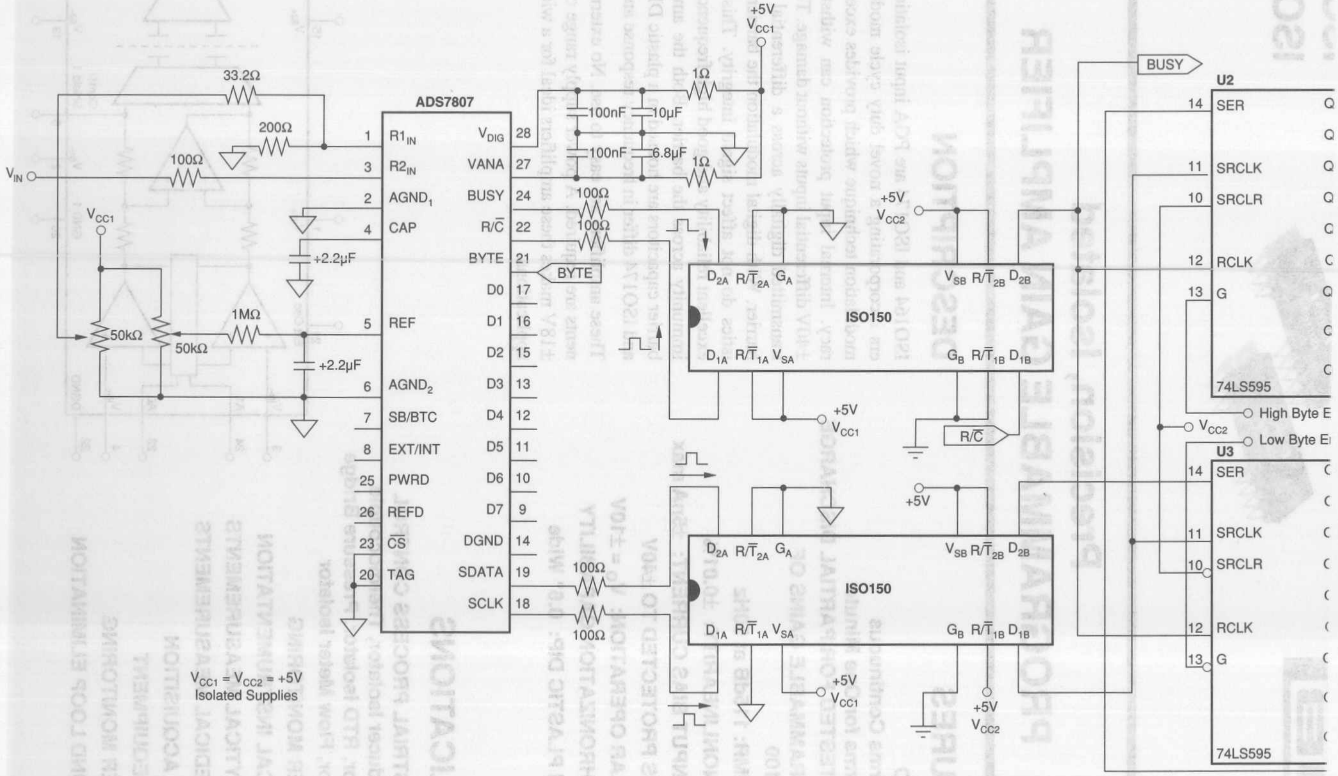
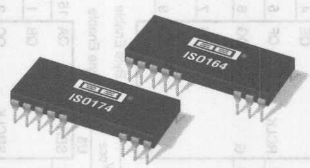


FIGURE 3. ISO150 and ADS7807 is Used to Reduce Circuit Noise in a Mixed Signal Application.

BURR - BROWN®



ISO164
ISO174

Precision, Isolated
PROGRAMMABLE GAIN AMPLIFIER

FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
  100% TESTED FOR PARTIAL DISCHARGE
- PROGRAMMABLE GAINS OF 1, 10, 100
- HIGH IMR: 115dB at 50Hz
- LOW NONLINEARITY: ±0.01%
- LOW INPUT BIAS CURRENT: ±5nA max
- INPUTS PROTECTED TO ±40V
- BIPOLAR OPERATION: $V_O = \pm 10V$
- SYNCHRONIZATION CAPABILITY
- 24-PIN PLASTIC DIP: 0.6" Wide

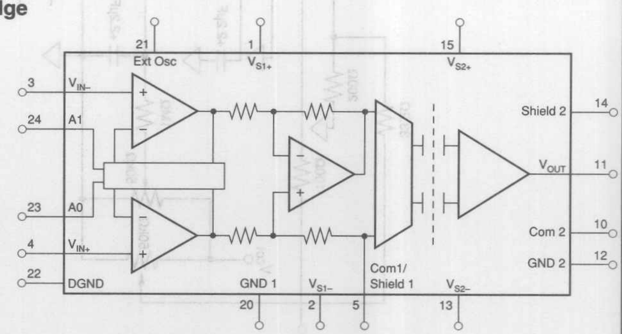
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- POWER MONITORING
- GROUND LOOP ELIMINATION

DESCRIPTION

ISO164 and ISO174 are PGA input isolation amplifiers incorporating a novel duty cycle modulation-demodulation technique which provides excellent accuracy. Internal input protection can withstand up to ±40V differential inputs without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a plastic DIP. ISO164 and ISO174 differ in frequency response and linearity.

These amplifiers are easy to use. No external components are required. A power supply range of ±4.5V to ±18V makes these amplifiers ideal for a wide range of applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25°C$, $V_{S1} = V_{S2} = ±15V$, and $R_L = 2kΩ$, unless otherwise noted.

		ISO164P			ISO174P			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ISOLATION[1]								
Voltage Rated Continuous:								
AC	T_{MIN} to T_{MAX}	1500			1500			Vrms
100% Test (AC 50Hz)	1s; Partial Discharge ≤ 5pC	2500			2500			Vrms
Isolation-Mode Rejection								
AC 50Hz	1500Vrms		115			115		dB
Barrier Impedance			$10^{14} \| 10$			$10^{14} \| 10$		Ω || pF
Leakage Current	VISO = 240Vrms, 50Hz		0.8	1		0.8	1	μArms
GAIN								
Gain Error	G = 1			±0.3			±0.3	%
	G = 10		±0.06			±0.06		
	G = 100			±0.3			±0.3	%
Gain vs Temperature	G = 1		±12.5			±42.5		ppm/°C
	G = 10		±12.5			±42.5		ppm/°C
	G = 100		±12.5			±42.5		ppm/°C
Nonlinearity	G = 1		±0.01	±0.052		±0.04	±0.102	%
	G = 10		±0.01			±0.04		%
	G = 100		±0.01	±0.054		±0.04	±0.104	%
INPUT OFFSET VOLTAGE								
Initial Offset			$±\left(0.125 + \frac{51}{G}\right)$			$±\left(0.125 + \frac{101}{G}\right)$		mV
vs Temperature	G = 1		±155			±505		μV/°C
vs Supply	DC, G = 1		2			2		mV/V
CMRR	DC, G = 1		90			90		dB
INPUT								
Voltage Range		±10.0			±10.0			V
Bias Current				±5			±5	nA
vs Temperature			±8			±8		pA/°C
Offset Current				±5			±5	nA
vs Temperature			±8			±8		pA/°C
OUTPUT								
Voltage Range		±10			±10			V
Current Drive		±5			±5			mA
Capacitive Load Drive			0.1			0.1		μF
Ripple Voltage			10			10		mVp-p
FREQUENCY RESPONSE								
Small Signal Bandwidth	100mVrms, G = 1		6			60		kHz
	100mVrms, G = 10		6			60		kHz
	100mVrms, G = 100		6			10		kHz
Slew Rate	$V_O = ±10V$, G = 10		0.7			0.7		V/μs
POWER SUPPLIES								
Rated Voltage			15			15		V
Voltage Range		±4.5		±18	±4.5		±18	V
Quiescent Current								
V_{S1}				±15			±15	mA
V_{S2}				±7.5			±7.5	mA
TEMPERATURE RANGE								
Operating		–40		85	–40		85	°C
Storage		–40		125	–40		125	°C

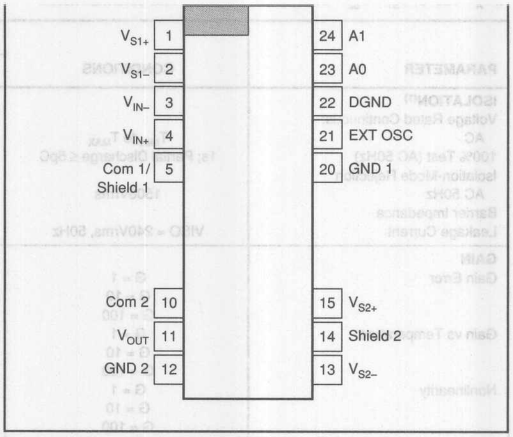
NOTE: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC.

V_{IN}, Analog Input Voltage Range	±40V
External Oscillator Input	±25V
Signal Common 1 to Ground 1	±1V
Signal Common 2 to Ground 2	±1V
Continuous Isolation Voltage	1500Vrms
IMV, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–40°C to 125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Duration	Continuous to Common

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ISO164P	24-Pin Plastic DIP	167-1
ISO174P	24-Pin Plastic DIP	167-1

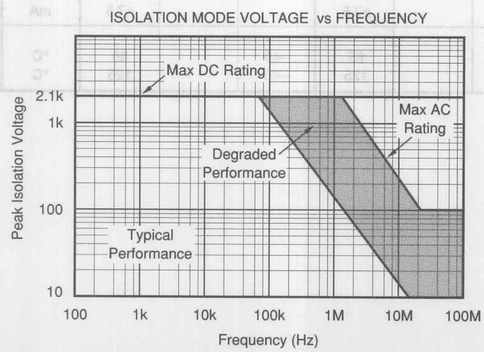
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

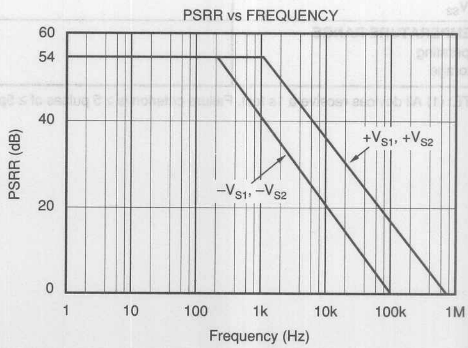
ORDERING INFORMATION

MODEL	PACKAGE	BANDWIDTH
ISO164P	24-Pin Plastic DIP	6kHz
ISO174P	24-Pin Plastic DIP	60kHz

TYPICAL PERFORMANCE CURVES

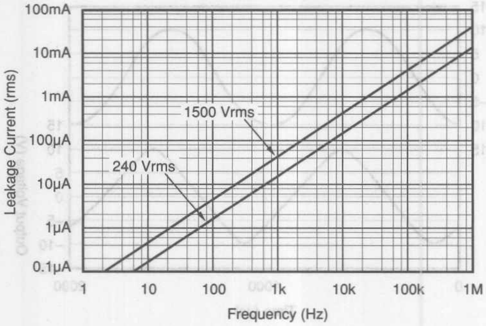
At T_A = +25°C, V_{S1} = V_{S2} = ±15V, and R_L = 2kΩ, unless otherwise noted.



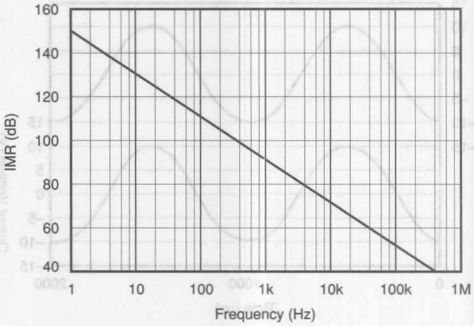


At $T_A = +25°C$, $V_{S1} = V_{S2} = \pm15V$, and $R_L = 2k\Omega$, unless otherwise noted.

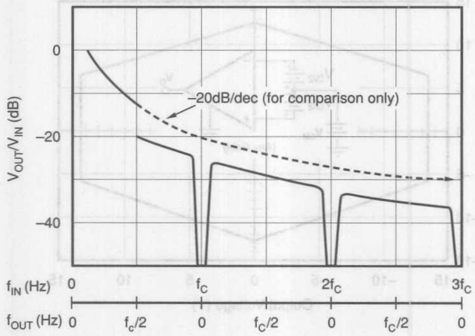
ISOLATION LEAKAGE CURRENT vs FREQUENCY



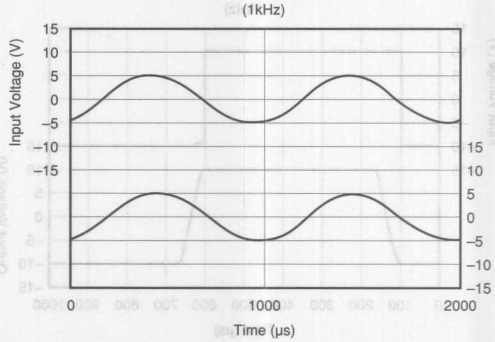
IMR vs FREQUENCY



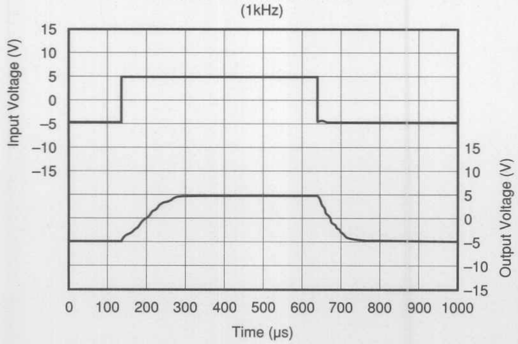
SIGNAL RESPONSE vs CARRIER FREQUENCY



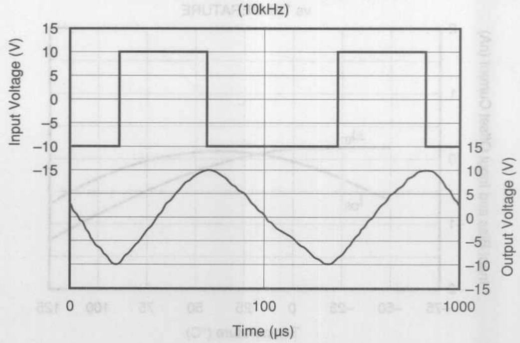
SINE RESPONSE ISO164 (1kHz)



STEP RESPONSE ISO164 (1kHz)



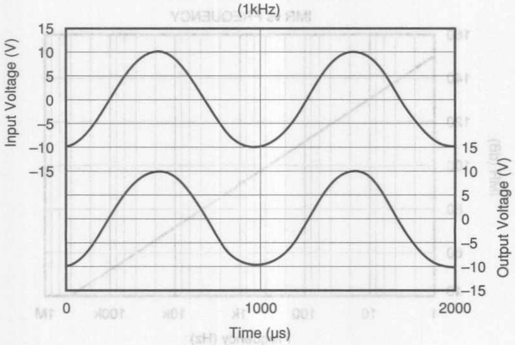
PULSE RESPONSE ISO174 (10kHz)



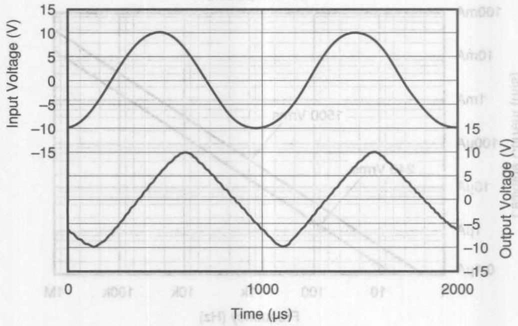
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_{S1} = V_{S2} = ±15V$, and $R_L = 2kΩ$, unless otherwise noted.

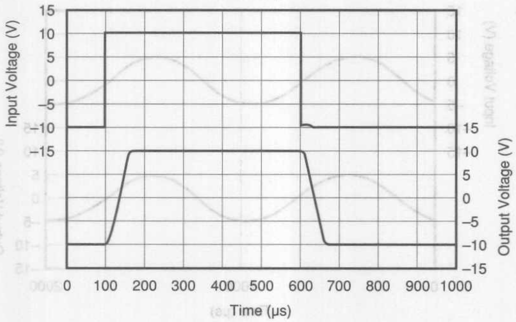
SINE RESPONSE ISO174
(1kHz)



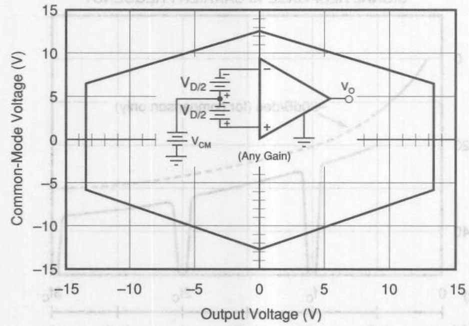
SINE RESPONSE ISO174
(10kHz)



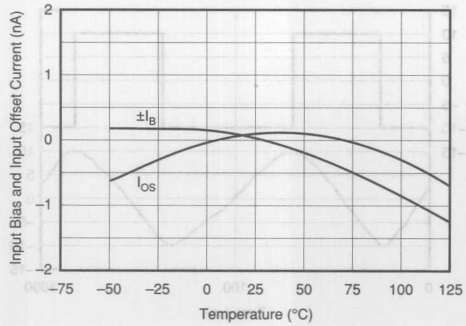
STEP RESPONSE ISO174
(1kHz)



INPUT COMMON-MODE VOLTAGE RANGE
vs OUTPUT VOLTAGE



INPUT BIAS AND INPUT OFFSET CURRENT
vs TEMPERATURE



BASIC OPERATION

ISO164 and ISO174 are comprised of a precision programmable gain amplifier followed by an isolation amplifier. The input and output isolation sections are galvanically isolated by matched and EMI shielded capacitors.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows power and signal connections. Each power supply pin should be bypassed with a 1µF tantalum capacitor located as close to the amplifier as possible. All ground connections should be run independently to a common point. Signal Common on both input and output sections provide a high-impedance point for sensing signal ground in noisy applications. Com 1 and Com 2 must have a path to ground for bias current return and should be maintained within ±1V of GND 1 and GND 2 respectively.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input circuitry of the ISO164/174 is approximately ±12.7V (or 2.3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the internal amplifiers. Thus, the linear common-mode range is related to the output voltage of the complete input amplifier—see performance curves "Input Common-Mode Range vs Output Voltage."

A combination of common-mode and differential input voltage can cause the output voltage of the internal amplifiers to saturate. For applications where input common-mode range must be maximized, limit the output voltage swing by selecting a lower gain of the programmable-gain input. Input-overload can produce an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the programmable-gain amplifier will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the programmable-gain amplifiers are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The inputs are protected even if no power supply is present.

SYNCHRONIZED OPERATION

ISO164 and ISO174 can be synchronized to an external signal source. This capability is useful in eliminating troublesome beat frequencies in multichannel systems and in rejecting AC signals and their harmonics. To use this feature, an external signal must be applied to the Ext Osc pin. ISO164 can be synchronized over the 100kHz to 200kHz range and ISO174 can be synchronized over the 400kHz to 700kHz range.

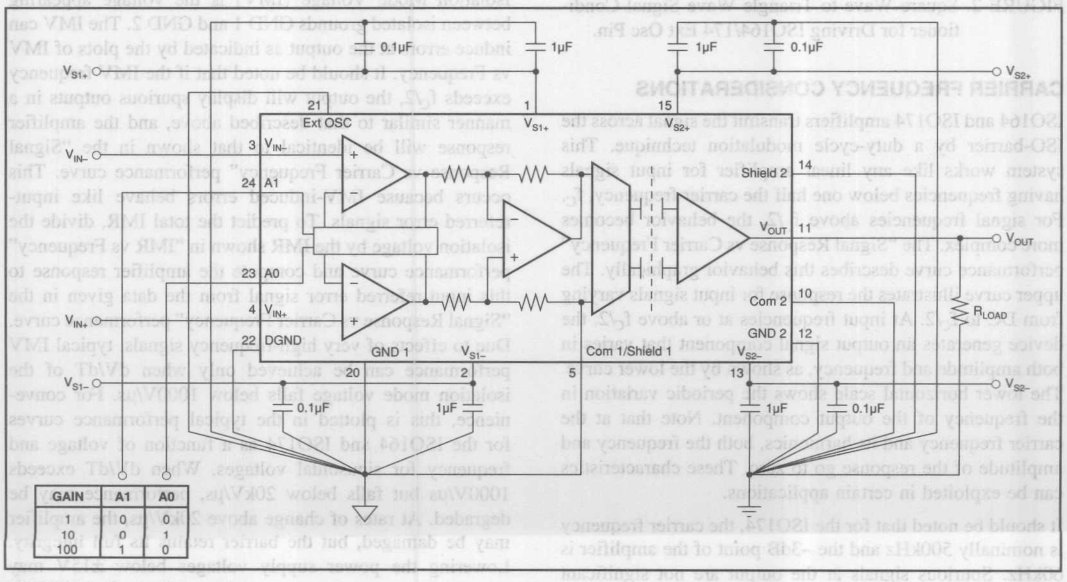


FIGURE 1. Basic Connections.

The Ext Osc pin of the ISO164 and ISO174 can be driven directly with a ±3V to ±5V sine or 25% to 75% duty-cycle triangle wave and the ISO amp's internal modulator/demodulator circuitry will synchronize to the signal.

ISO174 can also be synchronized to a 400kHz to 700kHz Square-Wave External Clock since an internal clamp and filter provide signal conditioning. A square-wave signal of 25% to 75% duty cycle, and ±3V to ±20V level can be used to directly drive the ISO174.

With the addition of the signal conditioning circuit shown in Figure 2, any 10% to 90% duty-cycle square-wave signal can be used to drive the ISO164 and ISO174 Ext Osc pin. With the values shown, the circuit can be driven by a 4Vp-p TTL signal. For a higher or lower voltage input, increase or decrease the 1kΩ resistor, R_X, proportionally, e.g., for a ±4V square-wave (8Vp-p) R_X should be increased to 2kΩ. The value of C_X used in the Figure 2 circuit depends on the frequency of the external clock signal. C_X should be 30pF for ISO174 and 680pF for ISO164.

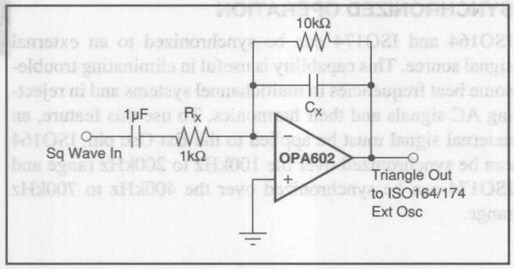


FIGURE 2. Square-Wave to Triangle Wave Signal Conditioner for Driving ISO164/174 Ext Osc Pin.

CARRIER FREQUENCY CONSIDERATIONS

ISO164 and ISO174 amplifiers transmit the signal across the ISO-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes more complex. The "Signal Response vs Carrier Frequency" performance curve describes this behavior graphically. The upper curve illustrates the response for input signals varying from DC to $f_C/2$. At input frequencies at or above $f_C/2$, the device generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go to zero. These characteristics can be exploited in certain applications.

It should be noted that for the ISO174, the carrier frequency is nominally 500kHz and the –3dB point of the amplifier is 60kHz. Spurious signals at the output are not significant For the ISO164, the carrier frequency is nominally 110kHz and the –3dB point of the amplifier is 6kHz.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO164 and ISO174 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the "Signal Response vs Carrier Frequency" performance curve. Figure 3 shows circuitry with opto-isolation suitable for driving the Ext Osc input from TTL levels.

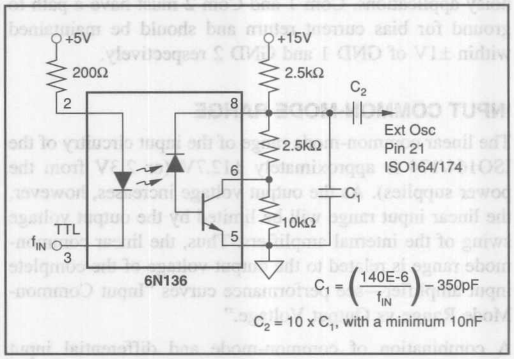


FIGURE 3. Synchronization with Isolated Drive Circuit for Ext Osc Pin.

ISOLATION MODE VOLTAGE

Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds GND 1 and GND 2. The IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs in a manner similar to that described above, and the amplifier response will be identical to that shown in the "Signal Response vs Carrier Frequency" performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in "IMR vs Frequency" performance curve and compute the amplifier response to this input-referred error signal from the data given in the "Signal Response vs Carrier Frequency" performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/μs. For convenience, this is plotted in the typical performance curves for the ISO164 and ISO174 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/μs but falls below 20kV/μs, performance may be degraded. At rates of change above 20kV/μs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltages below ±15V may

the maximum dV/dT of 20kV/µs remains unchanged.

Leakage current is determined solely by the impedance of the barrier capacitance and is plotted in the "Isolation Leakage Current vs Frequency" curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one.

Historically, Burr-Brown has chosen a deliberately conservative one: VTEST = (2 x ACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO164 and ISO174.

Partial Discharge

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process.

that the measurement of total charge being redistributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure. The bulk inception voltage, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the bulk extinction voltage provides a lower, more conservative voltage from which to derive a safe continuous rating. In production, measuring at a level somewhat below the expected inception voltage and then derating by a factor related to expectations about system transients is an accepted practice.

Partial Discharge Testing

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE in Germany, an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

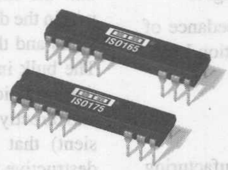
To accommodate poorly-defined transients, the part under test is exposed to a voltage that is 1.6 times the continuous-rated voltage and must display less than or equal to 5pC partial discharge level in a 100% production test.

APPLICATIONS

The ISO164 and ISO174 isolation amplifiers are used in three categories of applications:

- Accurate isolation of signals from high voltage ground potentials
- Accurate isolation of signals from severe ground noise and
- Fault protection from high voltages in analog measurements

BURR - BROWN®



ISO165
ISO175

Precision, Isolated INSTRUMENTATION AMPLIFIER

FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
  100% TESTED FOR PARTIAL DISCHARGE
- HIGH IMR: 115dB at 50Hz
- LOW NONLINEARITY: ±0.01%
- LOW INPUT BIAS CURRENT: 10nA max
- LOW INPUT OFFSET VOLTAGE: 101mV max
- INPUTS PROTECTED TO ±40V
- BIPOLAR OPERATION: $V_O = \pm 10V$
- SYNCHRONIZATION CAPABILITY
- 24-PIN PLASTIC DIP: 0.3" Wide

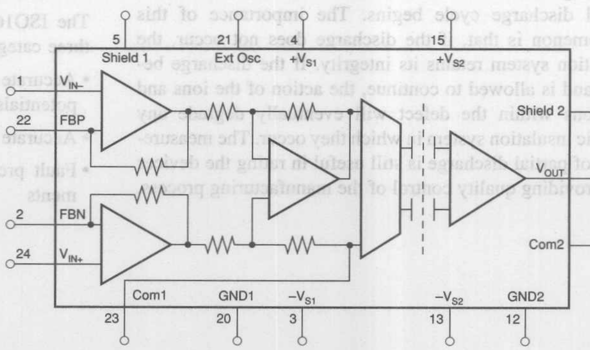
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- POWER MONITORING
- GROUND LOOP ELIMINATION

DESCRIPTION

ISO165 and ISO175 are precision isolated instrumentation amplifiers incorporating a novel duty cycle modulation-demodulation technique and excellent accuracy. A single external resistor sets the gain. Internal input protection can withstand up to ±40V without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a plastic DIP. ISO165 and ISO175 differ in frequency response and linearity.

These amplifiers are easy to use. A power supply range of ±4.5V to ±18V makes these amplifiers ideal for a wide range of applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25°C$, $V_{S1} = V_{S2} = ±15V$, and $R_L = 2kΩ$ unless otherwise noted.

PARAMETER	CONDITIONS	ISO165P MIN	ISO165P TYP	ISO165P MAX	ISO175P MIN	ISO175P TYP	ISO175P MAX	UNITS
ISOLATION[1]								
Voltage Rated Continuous:								
AC	T_{MIN} to T_{MAX}	1500			1500			Vrms
DC	T_{MIN} to T_{MAX}	2121			2121			VDC
100% Test (AC, 50Hz)	1s; Partial Discharge ≤ 5pC	2500			2500			Vrms
Isolation-Mode Rejection								
AC 50Hz	1500Vrms		115			115		dB
DC			160			160		dB
Barrier Impedance			$10^{14} \parallel 6$			$10^{14} \parallel 6$		Ω ‖ pF
Leakage Current	VISO = 240Vrms, 50Hz		0.8	1		0.8	1	µArms
GAIN			$1+\left(\frac{50k}{R_G}\right)$			$1+\left(\frac{50k}{R_G}\right)$		V/V
Gain Error	G = 1			±0.35			±0.35	%
	G = 10		±0.07			±0.07		%
	G = 100			±0.95			±0.95	%
Gain vs Temperature	G = 1		±11			±11		ppm/°C
Nonlinearity	G = 1			±0.052			±0.102	%
	G = 10		±0.01			±0.04		%
	G = 100			±0.054			±0.104	%
INPUT OFFSET VOLTAGE								
Initial Offset	G = 1, 100		$\pm\left(0.125+\frac{51}{G}\right)$			$\pm\left(0.125+\frac{101}{G}\right)$		mV
vs Temperature			$\pm\left(1+\frac{170}{G}\right)$			$\pm\left(1+\frac{520}{G}\right)$		µV/°C
vs Supply	G = 1		±2			±2		mV/V
INPUT								
Voltage Range		±10			±10			V
Bias Current				±10			±10	nA
vs Temperature			±40			±40		pA/°C
Offset Current				±10			±10	nA
vs Temperature			±40			±40		pA/°C
OUTPUT								
Voltage Range		±10			±10			V
Current Drive		±5			±5			mA
Capacitive Load Drive			0.1			0.1		µF
Ripple Voltage			10			10		mVp-p
FREQUENCY RESPONSE								
Small Signal Bandwidth	G = 1		6			60		kHz
	G = 10		6			60		kHz
	G = 100		6			50		kHz
Slew Rate	$V_O = ±10V$, G = 10		0.9			0.9		V/µs
POWER SUPPLIES								
Rated Voltage			15			15		V
Voltage Range		±4.5		±18	±4.5		±18	V
Quiescent Current								
V_{S1}				±7.4			±7.4	mA
V_{S2}				±7.5			±7.5	mA
TEMPERATURE RANGE								
Operating		–40		85	–40		85	°C
Storage		–40		125	–40		125	°C

NOTE: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pc.

ABSOLUTE MAXIMUM RATINGS

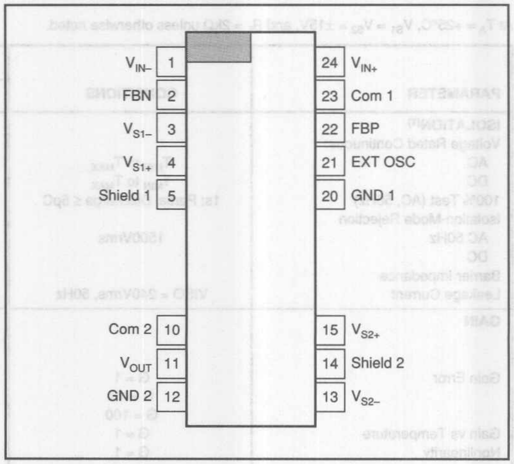
Supply Voltage	±18V
Analog Input Voltage Range	±40V
External Oscillator Input	±25V
Com 1 to GND1	±1V
Com 2 to GND2	±1V
Continuous Isolation Voltage:	1500Vrms
IMV, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Duration	Continuous to Common

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[(1)]
ISO165P	24-Pin Plastic DIP	243-2
ISO175P	24-Pin Plastic DIP	243-2

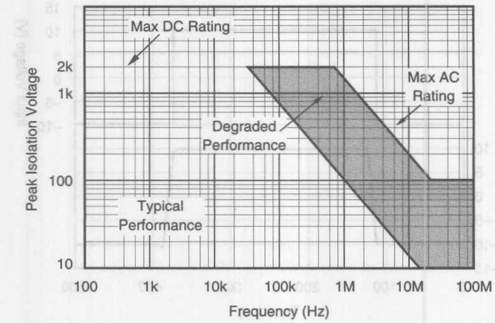
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

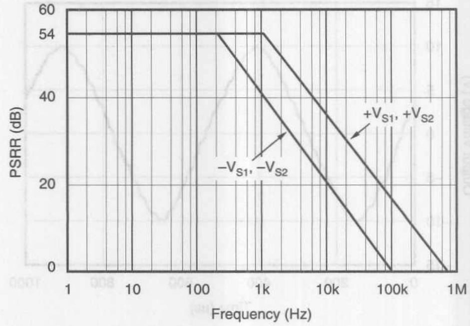
MODEL	PACKAGE	BANDWIDTH
ISO165P	24-Pin Plastic DIP	6kHz
ISO175P	24-Pin Plastic DIP	60kHz

At $T_A = +25°C$, $V_{S1} = V_{S2} = \pm15V$, and $R_L = 2k\Omega$ unless otherwise noted.

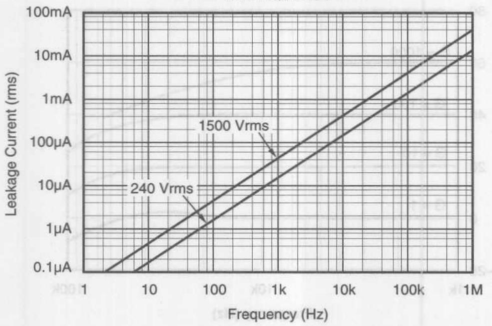
ISOLATION MODE VOLTAGE vs FREQUENCY



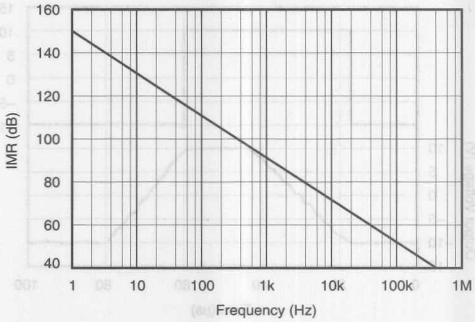
PSRR vs FREQUENCY



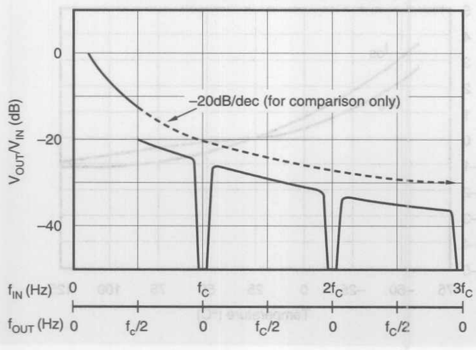
ISOLATION LEAKAGE CURRENT vs FREQUENCY



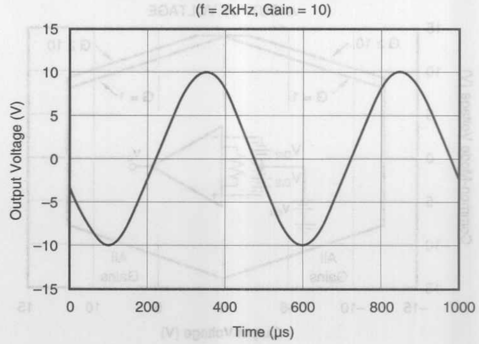
IMR vs FREQUENCY



SIGNAL RESPONSE vs CARRIER FREQUENCY



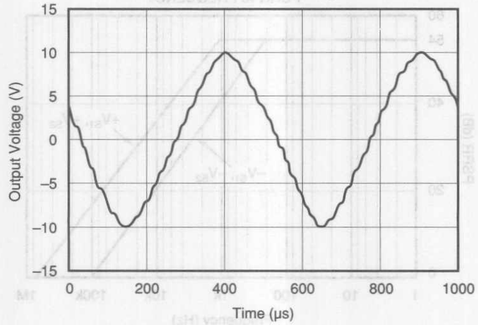
SINE RESPONSE ISO175
(f = 2kHz, Gain = 10)



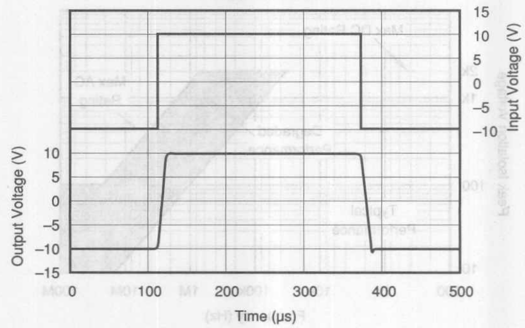
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_{S1} = V_{S2} = \pm 15V$, and $R_L = 2k\Omega$ unless otherwise noted.

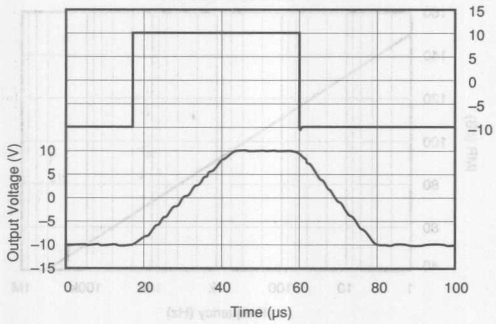
SINE RESPONSE ISO175
(f = 20kHz, Gain = 10)



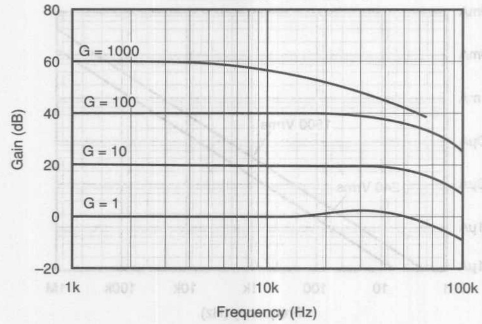
STEP RESPONSE ISO175



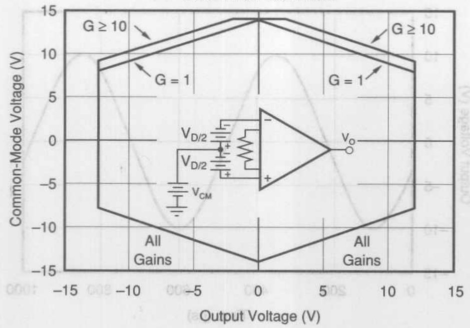
STEP RESPONSE ISO175



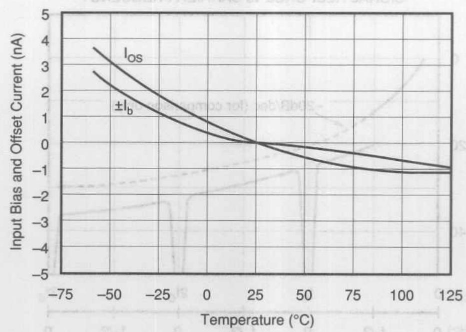
GAIN vs FREQUENCY ISO175



INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE



INPUT BIAS AND OFFSET CURRENT
vs TEMPERATURE



BASIC OPERATION

ISO165 and ISO175 instrumentation input isolation amplifiers are comprised of a precision instrumentation amplifier followed by an isolation amplifier. The input and output isolation sections are galvanically isolated and EMI shielded by matched capacitors.

Signal and Power Connections

Figure 1 shows power and signal connections. Each power supply pin should be bypassed with a 1µF tantalum capacitor located as close to the amplifier as possible. All ground connections should be run independently to a common point if possible. Signal Common on both input and output sections provide a high-impedance point for sensing signal ground in noisy applications. Com 1 and Com 2 must have a path to ground for bias current return and should be maintained within ±1V of GND1 and GND2, respectively.

SETTING THE GAIN

Gain of the ISO165 and ISO175 is set by connecting a single external resistor R_G, connected between pins 2 and 22.

$$G = 1 + \frac{50k\Omega}{R_G} \qquad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in equation (1) comes from the sum of the two internal feedback resistors. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the ISO165 and ISO175.

The stability and temperature drift of the external gain setting resistor R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

INPUT COMMON-MODE RANGE

The linear voltage range of the input circuitry of the ISO165 and ISO175 are from approximately 2.5V below the positive supply voltage to 2.5V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range will be limited by the output voltage swing of the internal amplifiers. Thus, the linear common-mode input range is related to the output voltage of the complete input amplifier.

This behavior also depends on the supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage."

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the ISO165 and ISO175 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the ISO165 and ISO175 are individually protected for voltages up to ±40V referenced to GND1. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC(1)	NC(1)
2	50.00k	49.9k
8	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.2	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
6000	10.00	10
10000	5.001	4.99

NOTE: (1) No Connection.

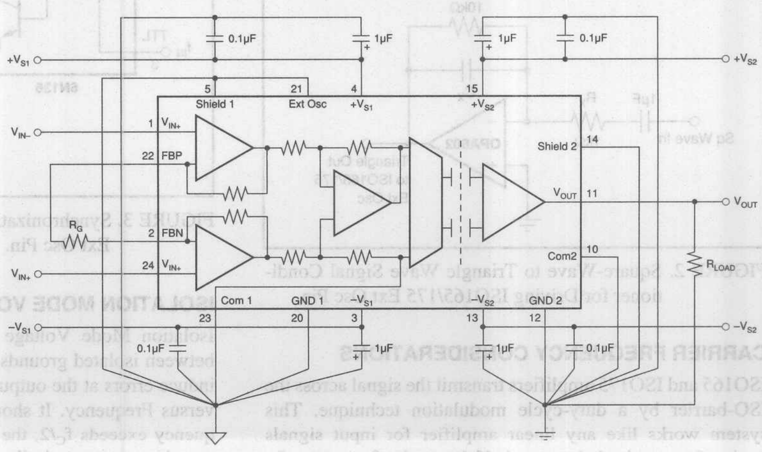


FIGURE 1. Basic Connections.

protected even if the power supplies are disconnected or turned off.

SYNCHRONIZED OPERATION

ISO165 and ISO175 can be synchronized to an external signal source. This capability is useful in eliminating troublesome beat frequencies in multichannel systems and in rejecting AC signals and their harmonics. To use this feature, an external signal must be applied to the Ext Osc pin. ISO165 can be synchronized over the 100kHz to 200kHz range and ISO175 can be synchronized over the 400kHz to 700kHz range.

The ideal external clock signal for the ISO165 and ISO175 is a ±4V sine wave or ±4V, 50% duty-cycle triangle wave. The Ext Osc pin of the ISO165 and ISO175 can be driven directly with a ±3V to ±5V sine or 25% to 75% duty-cycle triangle wave and the ISO amp's internal modulator/demodulator circuitry will synchronize to the signal.

ISO175 can also be synchronized to a 400kHz to 700kHz Square-Wave External Clock since an internal clamp and filter provide signal conditioning. A square-wave signal of 25% to 75% duty cycle, and ±3V to ±20V level can be used to directly drive the ISO175.

With the addition of the signal conditioning circuit shown in Figure 2, any 10% to 90% duty-cycle square-wave signal can be used to drive the ISO165 and ISO175 Ext Osc pin. With the values shown, the circuit can be driven by a 4Vp-p TTL signal. For a higher or lower voltage input, increase or decrease the 1kΩ resistor, R_X, proportionally, e.g. for a ±4V square-wave (8Vp-p) R_X should be increased to 2kΩ. The value of C_X used in the Figure 2 circuit depends on the frequency of the external clock signal. C_X should be 30pF for ISO175 and 680pF for ISO165.

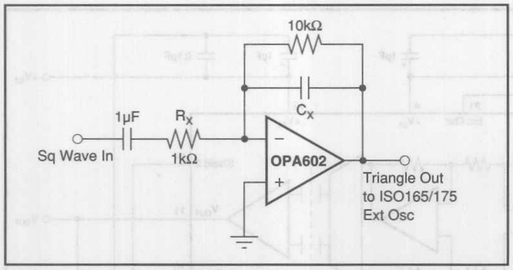


FIGURE 2. Square-Wave to Triangle Wave Signal Conditioner for Driving ISO165/175 Ext Osc Pin.

CARRIER FREQUENCY CONSIDERATIONS

ISO165 and ISO175 amplifiers transmit the signal across the ISO-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes upper curve illustrates the response for input signals varying from DC to $f_C/2$. At input frequencies at or above $f_C/2$, the device generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go to zero. These characteristics can be exploited in certain applications.

It should be noted that for the ISO175, the carrier frequency is nominally 500kHz and the –3dB point of the amplifier is 60kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 250kHz.

For the ISO165, the carrier frequency is nominally 110kHz and the –3dB point of the amplifier is 6kHz.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO165 and ISO175 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the "Signal Response vs Carrier Frequency" performance curve. Figure 3 shows circuitry with opto-isolation suitable for driving the Ext Osc input from TTL levels.

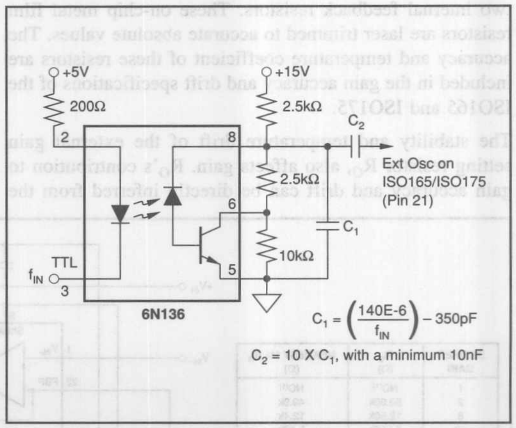


FIGURE 3. Synchronization with Isolated Drive Circuit for Ext Osc Pin.

ISOLATION MODE VOLTAGE

Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds GND1 and GND2. The IMV can induce errors at the output as indicated by the plots of IMV versus Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs in a manner similar to that described above, and the amplifier response will be identical to that shown in the

referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in "IMR vs Frequency" performance curve and compute the amplifier response to this input-referred error signal from the data given in the "Signal Response vs Carrier Frequency" performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/µs. For convenience, this is plotted in the typical performance curves for the ISO165 and ISO175 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/µs but falls below 20kV/µs, performance may be degraded. At rates of change above 20kV/µs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltages below ±15V may decrease the dV/dT to 500V/µs for typical performance, but the maximum dV/dT of 20kV/µs remains unchanged.

Leakage current is determined solely by the impedance of the barrier capacitance and is plotted in the "Isolation Leakage Current vs Frequency" curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one.

Historically, Burr-Brown has chosen a deliberately conservative one: VTEST = (2 x ACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO165 and ISO175.

PARTIAL DISCHARGE

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this gins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. The inception voltage for these voids tends to be constant, so that the measurement of total charge being redistributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure. The bulk inception voltage, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the bulk extinction voltage provides a lower, more conservative voltage from which to derive a safe continuous rating. In production, measuring at a level somewhat below the expected inception voltage and then derating by a factor related to expectations about system transients is an accepted practice.

PARTIAL DISCHARGE TESTING

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE in Germany, an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

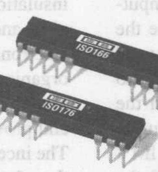
To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display less than or equal to 5pC partial discharge level in a 100% production test.

APPLICATIONS

The ISO165 and ISO175 isolation amplifiers are used in three categories of applications:

- Accurate isolation of signals from high voltage ground potentials,
- Accurate isolation of signals from severe ground noise and,
- Fault protection from high voltages in analog measurements.

BURR - BROWN®



ISO166
ISO176

Precision, Isolated OPERATIONAL AMPLIFIER

FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
  100% TESTED FOR PARTIAL DISCHARGE
- HIGH IMR: 115dB at 50Hz
- LOW NONLINEARITY: ±0.05%
- LOW INPUT BIAS CURRENT: ±5nA max
- LOW INPUT OFFSET VOLTAGE: ±20μV
- OP AMP INPUTS PROTECTED TO ±30V
- MOD INPUT PROTECTED TO ±100V
- BIPOLAR OPERATION: $V_O = \pm10V$
- SYNCHRONIZATION CAPABILITY
- 24-PIN PLASTIC DIP: 0.3" Wide

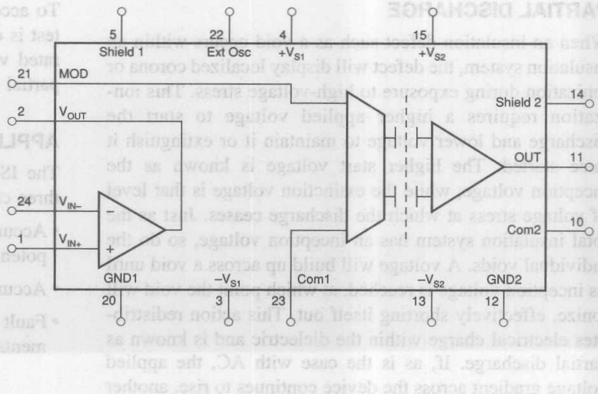
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- POWER MONITORING
- GROUND LOOP ELIMINATION

DESCRIPTION

ISO166 and ISO176 are precision isolation amplifiers incorporating an uncommitted operational amplifier for input conditioning, a novel duty cycle modulation-demodulation technique and excellent accuracy. Internal input protection can withstand up to ±30V differential without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a plastic DIP. ISO166 and ISO176 differ in frequency response and linearity.

These amplifiers are easy to use. No external components are required. A power supply range of ±4.5V to ±18V makes these amplifiers ideal for a wide range of applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

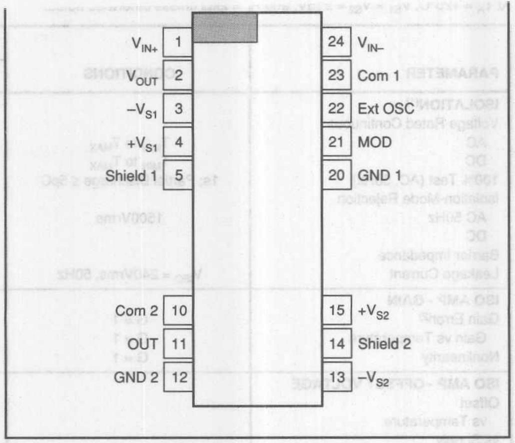
SPECIFICATIONS

At $T_A = +25°C$, $V_{S1} = V_{S2} = ±15V$, and $R_L = 2kΩ$ unless otherwise noted.

		ISO166P			ISO176P			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ISOLATION[1]								
Voltage Rated Continuous:								
AC	T_{MIN} to T_{MAX}	1500			1500			Vrms
DC	T_{MIN} to T_{MAX}	2121			2121			VDC
100% Test (AC, 50Hz)	1s; Partial Discharge ≤ 5pC	2500			2500			Vrms
Isolation-Mode Rejection								
AC 50Hz	1500Vrms		115			115		dB
DC			160			160		dB
Barrier Impedance			$10^{14} \parallel 6$			$10^{14} \parallel 6$		Ω || pF
Leakage Current	V_{ISO} = 240Vrms, 50Hz		0.8	1		0.8	1	μArms
ISO AMP - GAIN								
Gain Error[2]	G = 1		±0.05			±0.05		%FSR
Gain vs Temperature	G = 1		±10			±10		ppm/°C
Nonlinearity	G = 1			±0.052			±0.102	%
ISO AMP - OFFSET VOLTAGE								
Offset				50			100	mV
vs Temperature			±150			±500		μV/°C
vs Supply			±2			±2		μV/V
ISO AMP - INPUT								
Input Resistance			200			200		kΩ
ISO AMP - OUTPUT								
Voltage Range		±10			±10			V
Current Drive		±5			±5			mA
Capacitive Load Drive			0.1			0.1		μF
Ripple Voltage			10			10		mVp-p
OP AMP - INPUT								
Voltage Range			±13			±13		V
Bias Current				±5			±5	nA
vs Temperature			±15			±15		pA/°C
Offset Voltage			±20			±20		μV
Offset Current				±5			±5	nA
vs Temperature			±1.5			±1.5		pA/°C
FREQUENCY RESPONSE								
Small Signal Bandwidth	100mV, G = 1		6			60		kHz
	100mV, G = 10		6			60		kHz
	100mV, G = 100		6			60		kHz
Slew Rate	$V_O = ±10V$, G = 10		0.3			0.3		V/μs
POWER SUPPLIES								
Rated Voltage			15			15		V
Voltage Range		±4.5		±18	±4.5		±18	V
Quiescent Current								
V_{CC1}			9			9		mA
V_{CC2}			7.5			7.5		mA
TEMPERATURE RANGE								
Operating		–40		85	–40		85	°C
Storage		–40		125	–40		125	°C

NOTE: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pX. (2) Tested as a OPA and ISO, max ±0.35% FSR.

Op Amp Analog Input Voltage Range	$\pm V_{S1}$
External Oscillator Input	±25V
Signal Common 1 to Ground 1	±1V
Signal Common 2 to Ground 2	±1V
Continuous Isolation Voltage:	1500Vrms
IMV, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Duration	Continuous to Common
MOD Input Voltage Range	±100V



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO166P	24-Pin Plastic DIP	243-2
ISO176P	24-Pin Plastic DIP	243-2

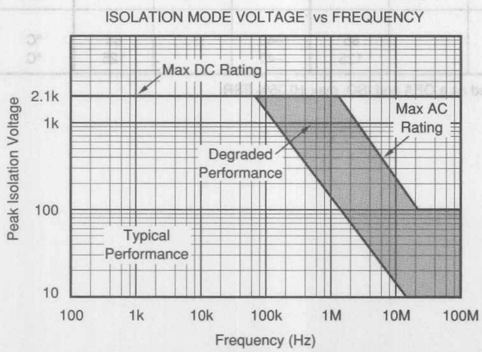
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

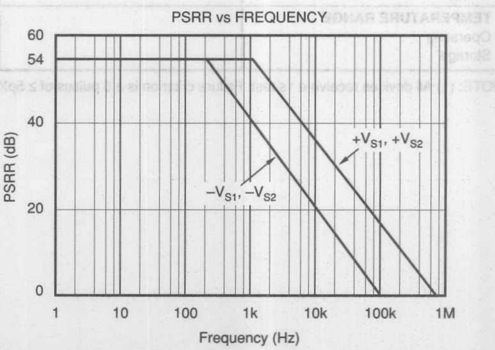
ORDERING INFORMATION

MODEL	PACKAGE	BANDWIDTH
ISO166P	24-Pin Plastic DIP	6kHz
ISO176P	24-Pin Plastic DIP	60kHz

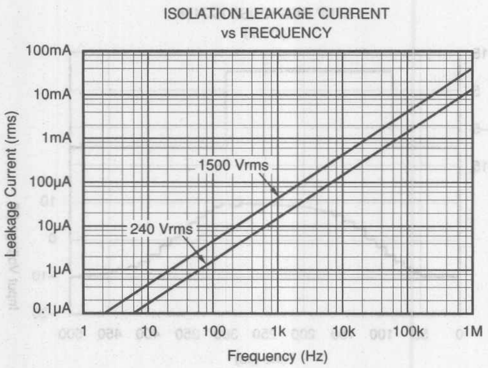
TYPICAL PERFORMANCE CURVES

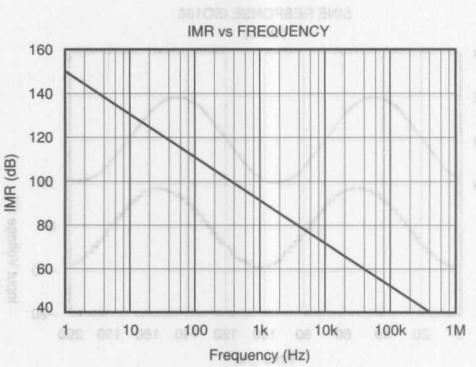
At $T_A = +25°C$, $V_{S1} = V_{S2} = \pm15V$, and $R_L = 2k\Omega$ unless otherwise noted.

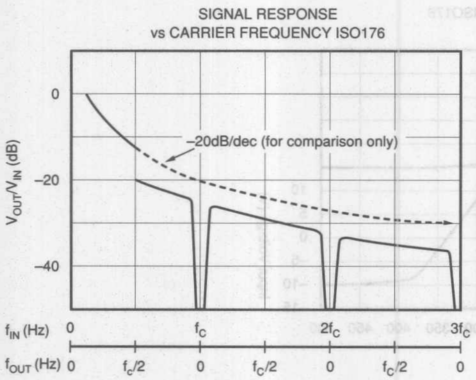


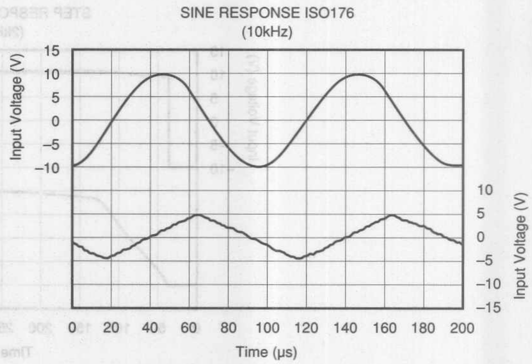


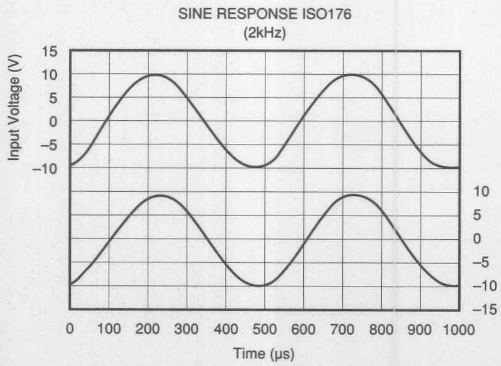
At $T_A = +25°C$, $V_{S1} = V_{S2} = ±15V$, and $R_L = 2kΩ$ unless otherwise noted.

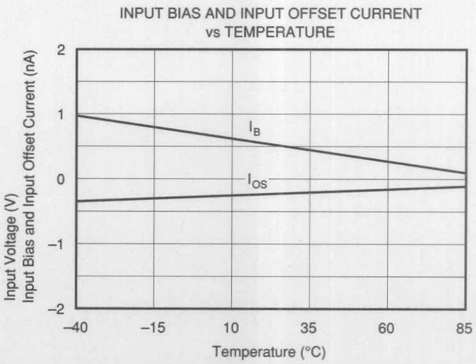












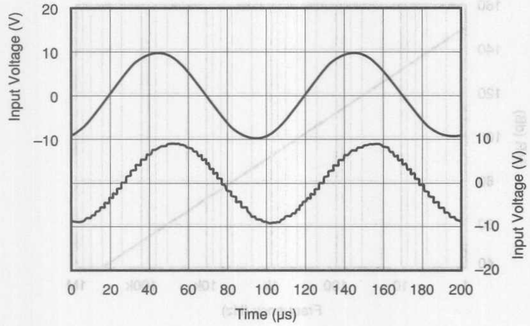
ISO166/ISO176

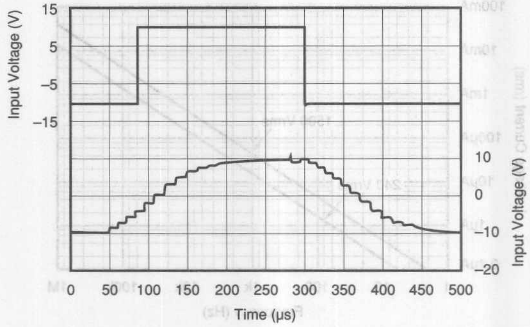
5

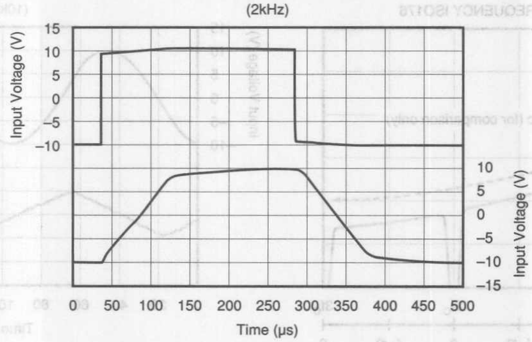
ISOLATION PRODUCTS

TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_{S1} = V_{S2} = \pm15V$, and $R_L = 2k\Omega$ unless otherwise noted.







BASIC OPERATION

ISO166 and ISO176 isolation amplifiers are comprised of a precision uncommitted operational amplifier followed by an isolation amplifier. The input and output isolation sections are galvanically isolated by matched and EMI shielded capacitors.

Signal and Power Connections

Figure 1 shows power and signal connections. Each power supply pin should be bypassed with a 1µF tantalum capacitor located as close to the amplifier as possible. All ground connections should be run independently to a common point. Signal Common on both input and output sections provide a high-impedance point for sensing signal ground in noisy applications. Com 1 and Com 2 must have a path to ground for bias current return and should be maintained within ±1V of GND1 and GND2, respectively.

INPUT PROTECTION

The amplifier inputs of ISO166 and ISO176 are protected with 500Ω series input resistors and diode clamps. The inputs can withstand ±30V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are over-driven. This may disturb the slewing behavior of unity-gain follower applications, but it will not damage the op amp. The MOD input is a 200kΩ resistor and can withstand ±100V without damage.

INPUT BIAS CURRENT CANCELLATION

The input stage base current of the uncommitted op amp is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to balance the DC resistance seen at the two input terminals. **A resistor added to balance the input resistances may actually increase offset and noise.**

SYNCHRONIZED OPERATION

ISO166 and ISO176 can be synchronized to an external signal source. This capability is useful in eliminating troublesome beat frequencies in multichannel systems and in rejecting AC signals and their harmonics. To use this feature, an external signal must be applied to the Ext Osc pin. ISO166 can be synchronized over the 100kHz to 200kHz range and ISO176 can be synchronized over the 400kHz to 700kHz range.

The ideal external clock signal for ISO166 and ISO176 is a ±4V sine wave or ±4V, 50% duty-cycle triangle wave. The Ext Osc pin of the ISO166 and ISO176 can be driven directly with a ±3V to ±5V sine or 25% to 75% duty-cycle triangle wave and the ISO amp's internal modulator/demodulator circuitry will synchronize to the signal.

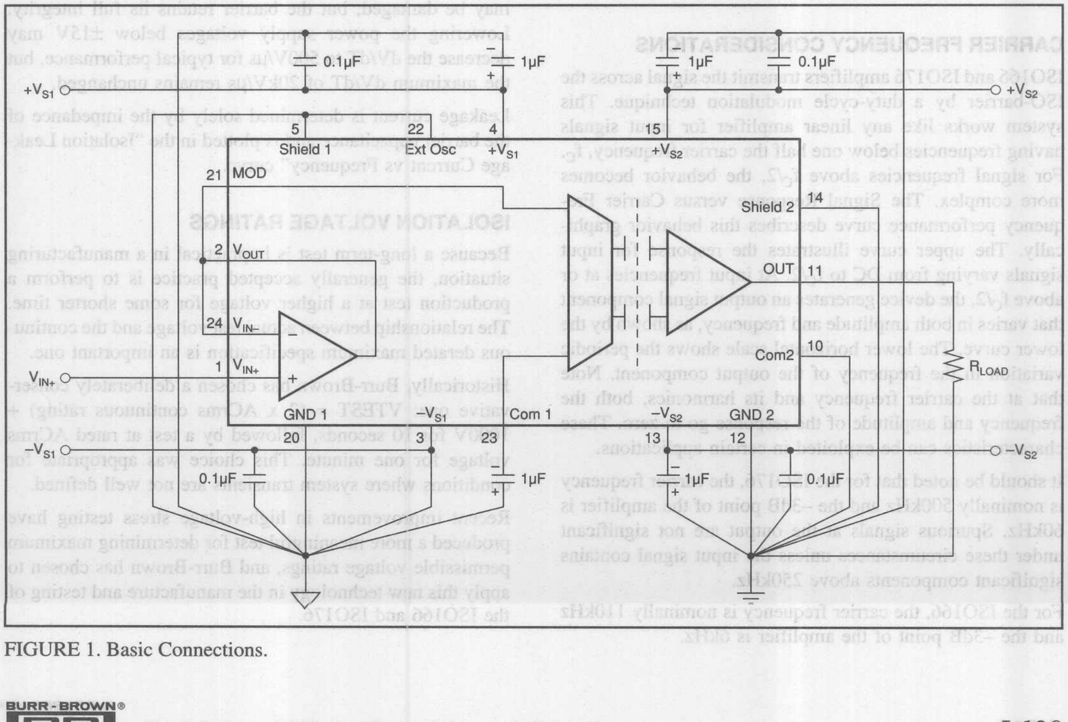


FIGURE 1. Basic Connections.

filter provide signal conditioning. A square-wave signal of 25% to 75% duty cycle, and ±3V to ±20V level can be used to directly drive the ISO176.

With the addition of the signal conditioning circuit shown in Figure 2, any 10% to 90% duty-cycle square-wave signal can be used to drive the ISO166 and ISO176 Ext Osc pin. With the values shown, the circuit can be driven by a 4Vp-p TTL signal. For a higher or lower voltage input, increase or decrease the 1kΩ resistor, R_X, proportionally, e.g. for a ±4V square-wave (8Vp-p) R_X should be increased to 2kΩ. The value of C_X used in the Figure 2 circuit depends on the frequency of the external clock signal. C_X should be 30pF for ISO176 and 680pF for ISO166.

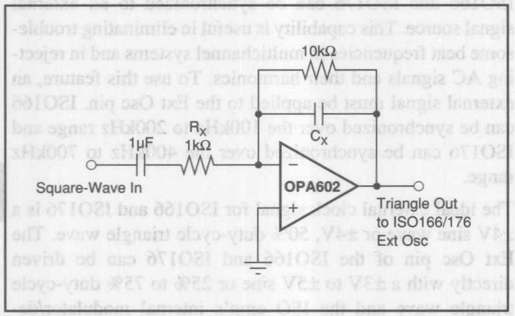


FIGURE 2. Square-Wave to Triangle Wave Signal Conditioner for Driving ISO166/176 Ext Osc Pin.

CARRIER FREQUENCY CONSIDERATIONS

ISO166 and ISO176 amplifiers transmit the signal across the ISO-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes more complex. The Signal Response versus Carrier Frequency performance curve describes this behavior graphically. The upper curve illustrates the response for input signals varying from DC to $f_C/2$. At input frequencies at or above $f_C/2$, the device generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go to zero. These characteristics can be exploited in certain applications.

It should be noted that for the ISO176, the carrier frequency is nominally 500kHz and the –3dB point of the amplifier is 60kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 250kHz.

For the ISO166, the carrier frequency is nominally 110kHz and the –3dB point of the amplifier is 6kHz. In this case, spurious signals at the output are possible, and ISO166 and ISO176 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the "Signal Response vs Carrier Frequency" performance curve.

ISOLATION MODE VOLTAGE

Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds GND1 and GND2. The IMV can induce error at the output as indicated by the plots of IMV versus Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs in a manner similar to that described above, and the amplifier response will be identical to that shown in the "Signal Response vs Carrier Frequency" performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in "IMR vs Frequency" performance curve and compute the amplifier response to this input-referred error signal from the data given in the "Signal Response vs Carrier Frequency" performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/μs. For convenience, this is plotted in the typical performance curves for the ISO166 and ISO176 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/μs but falls below 20kV/μs, performance may be degraded. At rates of change above 20kV/μs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltages below ±15V may decrease the dV/dT to 500V/μs for typical performance, but the maximum dV/dT of 20kV/μs remains unchanged.

Leakage current is determined solely by the impedance of the barrier capacitance and is plotted in the "Isolation Leakage Current vs Frequency" curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one.

Historically, Burr-Brown has chosen a deliberately conservative one: VTEST = (2 x ACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO166 and ISO176.

insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. The inception voltage for these voids tends to be constant, so that the measurement of total charge being redistributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure. The bulk inception voltage, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the bulk extinction voltage provides a lower, more conservative voltage from which to derive a safe continuous rating.

information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE in Germany, an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display less than or equal to 5pC partial discharge level in a 100% production test.

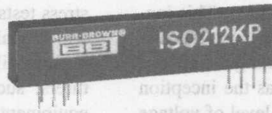
APPLICATIONS

The ISO166 and ISO176 isolation amplifiers are used in three categories of applications:

- Accurate isolation of signals from high voltage ground potentials.
- Accurate isolation of signals from severe ground noise and,
- Fault protection from high voltages in analog measurements.

BURR - BROWN®

ISO212P



Low Cost, Two-Port Isolated, 1500Vrms ISOLATION AMPLIFIER

FEATURES

- 12-BIT ACCURACY
- 2.5mA (typ) QUIESCENT CURRENT
- LOW PROFILE (LESS THAN 0.5" HIGH)
- SMALL FOOTPRINT
- EXTERNAL POWER CAPABILITY (±8V at 5mA)
- "MASTER/SLAVES" SYNCHRONIZATION CAPABILITY
- INPUT OFFSET ADJUSTMENT
- LOW POWER (75mW)
- SINGLE 10V TO 15V SUPPLY OPERATION

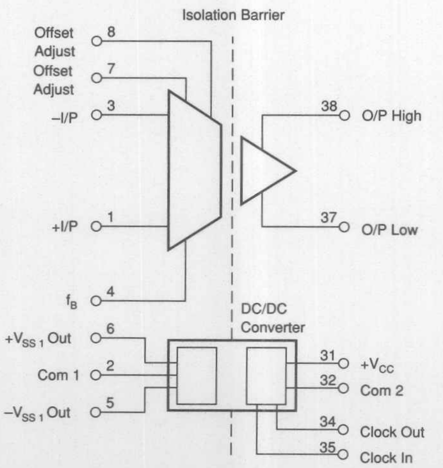
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Channel Isolator for Thermocouples, RTDs, Pressure Bridges, Flow Meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MULTIPLEXED SYSTEMS WITH CHANNEL TO CHANNEL ISOLATION

DESCRIPTION

The ISO212P signal isolation amplifier is a member of a series of low-cost isolation products from Burr-Brown. The low-profile SIL plastic package allows PCB spacings of 0.5" to be achieved, and the small footprint results in efficient use of board space.

To provide isolation, the design uses high-efficiency, miniature toroidal transformers in both the signal and power paths. An uncommitted input amplifier and an isolated external bipolar supply ensure the majority of input interfacing or conditioning needs can be met. The ISO212P accepts an input voltage range of ±5V for single 15V supply operation or ±3.0V for single 10V supply operation.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC} = +15V, unless otherwise noted.

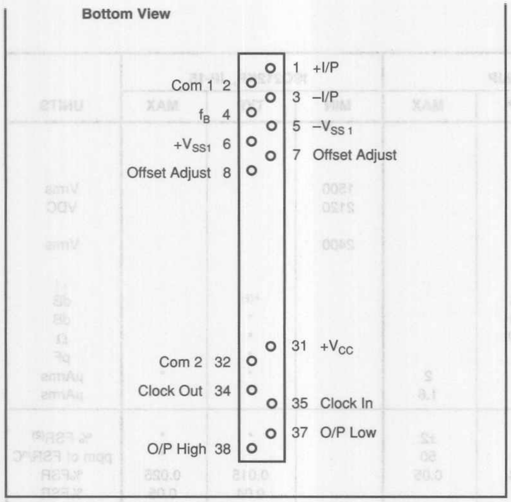
		ISO212JP			ISO212KP, JP-15			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ISOLATION								
Voltage								
Rated Continuous								
AC, 50Hz		750			1500			Vrms
DC		1060			2120			VDC
100% Test (AC, 50Hz)	Partial Discharge 1s : <5pC	1200			2400			Vrms
Isolation-Mode Rejection(1)	V_{ISO} = Rated Continuous 60Hz							
AC			115			*(9)		dB
DC			160			*		dB
Barrier Resistance			10^{10}			*		Ω
Barrier Capacitance			12			*		pF
Leakage Current(8)	V_{ISO} = 240Vrms, 60Hz		1	2		*	*	µArms
	V_{ISO} = 240Vrms, 50Hz			1.6			*	µArms
GAIN								
Initial Error			±1	±2		*	*	% FSR(2)
Gain vs Temperature			20	50		*	*	ppm of FSR/°C
Nonlinearity(3): KP	V_O = –5V to +5V		0.04	0.05		0.015	0.025	%FSR
JP-15						0.04	0.05	%FSR
INPUT OFFSET VOLTAGE								
Offset Voltage RTI: KP				±10 ±10/G			±7.5 ±7.5/G	mV
JP-15							±10 ±10/G	mV
vs Temperature			30 ±30/G			*		µV/°C
vs Power Supply(4)	V_{CC} = 14V to 16V		±1.5			*		mV/V
Adjustment Range		±20			*			mV
INPUT CURRENT								
Bias				50			*	nA
Offset				4			*	nA
INPUT								
Voltage Range(5)	G = 1	±5			*			V
Resistance			10^{12}			*		Ω
OUTPUT								
Output Impedance			3			*		kΩ
Voltage Range	Out Hi to Out Lo Min Load = 1MΩ	±5			*			V
Ripple Voltage(6)	f = 0 to 100kHz		8			*		mVp-p
	f = 0 to 5kHz		0.4			*		mVrms
Ouput Compliance	Out Hi or Out Lo		7.5					V
FREQUENCY RESPONSE								
Small Signal Bandwidth	I/P = 1Vp-p, –3dB G = 1		1			*		kHz
Full Signal Bandwidth	I/P = 10Vp-p, G = 1		200			*		Hz
	G = 10 (–3dB)		1.8					kHz
ISOLATED POWER OUTPUTS								
Voltage Outputs ($\pm V_{SS\ 1}$)(7)	No Load	±7.5	±8		*	*		VDC
vs Temperature			–8			*		mV/°C
vs Load			90			*		mV/mA
Current Output (7)								
(Both Loaded)				5			*	mA
(One Loaded)				8			*	mA
POWER SUPPLIES								
Rated Voltage	Rated Performance		15			*		V
Voltage Range(5)			11.4 to 16		*		*	V
Quiescent Current	No Load		2.5	3.5		*	*	mA
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Operating		–25		+85	*		*	°C

NOTES: (1) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. It is a function of frequency. (2) FSR = Full Scale Range = 10V. (3) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (4) Power Supply Rejection is the change in V_{OS}/Supply Change. (5) At V_{CC} = +10.0V, input voltage range = ±3.0V min. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Derated at V_{CC} < +15V. (8) Tested at 2400Vrms, 50Hz limit 16µA. (9) Asterisk (*) same as ISO212JP.

ISO212P

5

ISOLATION PRODUCTS



Supply Voltage Without Damage 18V
Continuous Isolation Voltage Across Barrier: JP 750Vrms
KP, JP-15 .... 1500Vrms
Storage Temperature Range .... –25°C to 100°C
Lead Temperature (soldering, 10s) .... +300°C
Amplifier Output Short-Circuit Duration .... Continuous to Common
Output Voltage Hi or Lo to Com 2 .... $\pm V_{CC}/2$

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ISO212JP	38-Pin Plastic SIP	326
ISO212JP-15	38-Pin Plastic SIP	326
ISO212KP	38-Pin Plastic SIP	326

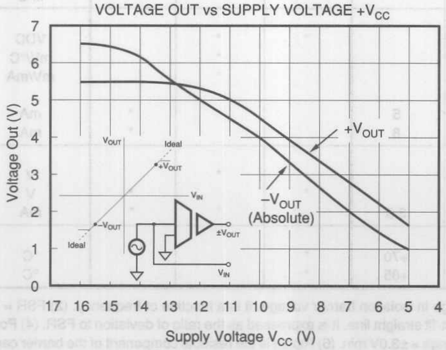
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

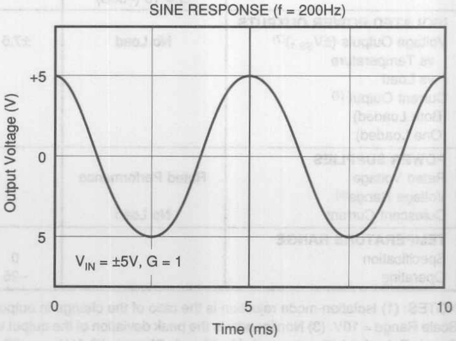
ORDERING INFORMATION

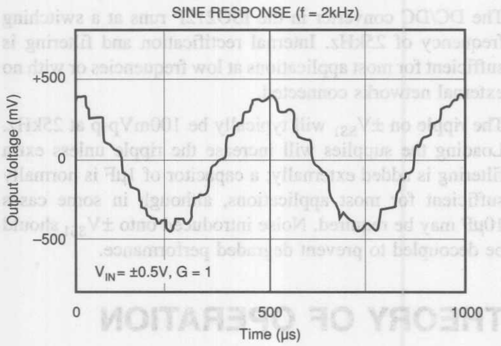
MODEL	PACKAGE	OPERATING TEMPERATURE RANGE
ISO212JP	38-Pin Plastic SIP	–25°C to +85°C
ISO212JP-15	38-Pin Plastic SIP	–25°C to +85°C
ISO212KP	38-Pin Plastic SIP	–25°C to +85°C

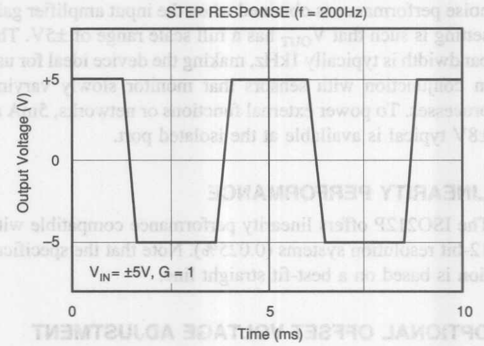
TYPICAL PERFORMANCE CURVES

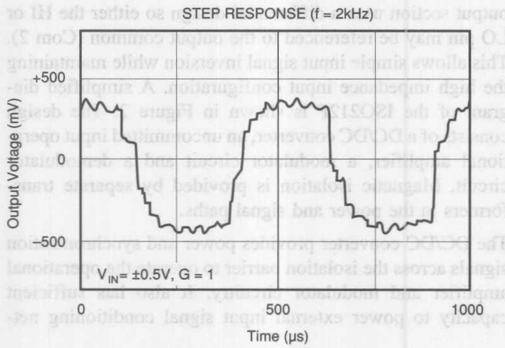
At $T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.

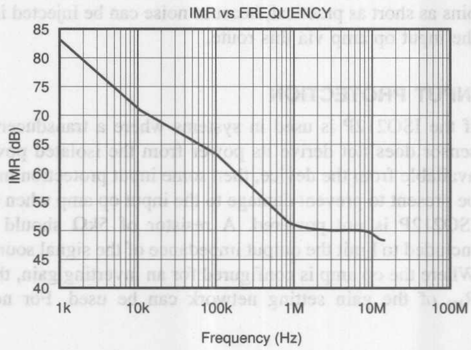


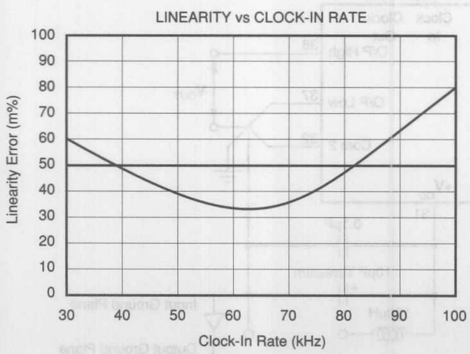



SINE RESPONSE (f = 2kHz)
Output Voltage (mV)
+500
0
–500
V_{IN} = ±0.5V, G = 1
0
500
1000
Time (µs)


STEP RESPONSE (f = 200Hz)
Output Voltage (V)
+5
0
–5
V_{IN} = ±5V, G = 1
0
5
10
Time (ms)


STEP RESPONSE (f = 2kHz)
Output Voltage (mV)
+500
0
–500
V_{IN} = ±0.5V, G = 1
0
500
1000
Time (µs)


IMR vs FREQUENCY
IMR (dB)
85
80
75
70
65
60
55
50
45
40
1k
10k
100k
1M
10M
100M
Frequency (Hz)


LINEARITY vs CLOCK-IN RATE
Linearity Error (m%)
100
90
80
70
60
50
40
30
20
10
0
30
40
50
60
70
80
90
100
Clock-In Rate (kHz)


GAIN ERROR vs CLOCK-IN RATE
Gain Error (% FSR)
0
–0.5
–1
–1.5
–2
–2.5
30
40
50
60
70
80
90
100
Clock-In Rate (kHz)

DISCUSSION OF SPECIFICATIONS

The ISO212P is intended for applications where isolation and input signal conditioning are required. Best signal-to-noise performance is obtained when the input amplifier gain setting is such that V_{OUT} has a full scale range of ±5V. The bandwidth is typically 1kHz, making the device ideal for use in conjunction with sensors that monitor slowly varying processes. To power external functions or networks, 5mA at ±8V typical is available at the isolated port.

LINEARITY PERFORMANCE

The ISO212P offers linearity performance compatible with 12-bit resolution systems (0.025%). Note that the specification is based on a best-fit straight line.

OPTIONAL OFFSET VOLTAGE ADJUSTMENT

In many applications, the untrimmed input offset voltage will be adequate. For situations where it is necessary to trim the offset, a potentiometer can be used. See Figure 1 for details. It is important to keep the traces to the offset adjust pins as short as practical, because noise can be injected into the input op amp via this route.

INPUT PROTECTION

If the ISO212P is used in systems where a transducer or sensor does not derive its power from the isolated power available from the device, then some input protection must be present to prevent damage to the input op amp when the ISO212P is not powered. A resistor of 5kΩ should be included to limit the output impedance of the signal source. Where the op amp is configured for an inverting gain, then R_{IN} of the gain setting network can be used. For non-inverting configurations, a separate resistor is required. Neglecting this point may also lead to problems when powering on the ISO212P.

USING $\pm V_{SS1}$ TO POWER EXTERNAL CIRCUITRY

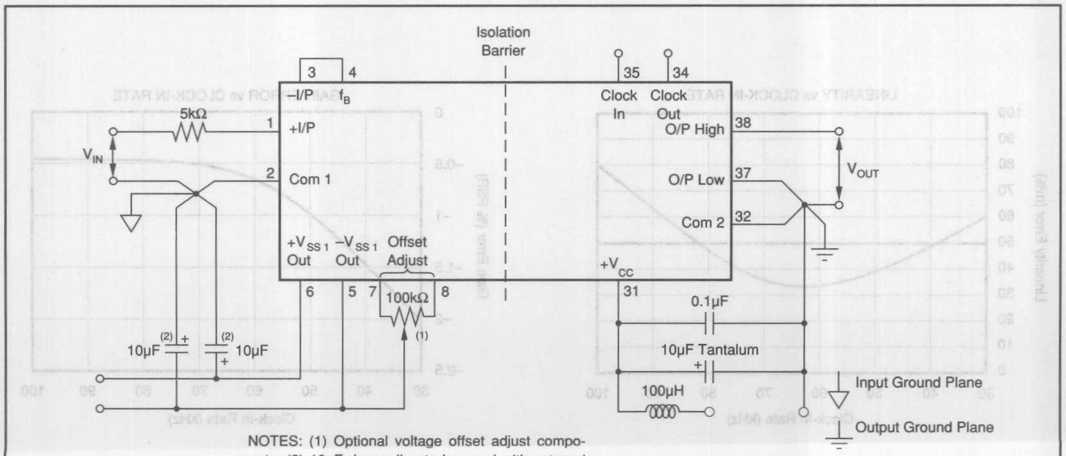
The DC/DC converter in the ISO212P runs at a switching frequency of 25kHz. Internal rectification and filtering is sufficient for most applications at low frequencies or with no external networks connected.

The ripple on $\pm V_{SS1}$ will typically be 100mVp-p at 25kHz. Loading the supplies will increase the ripple unless extra filtering is added externally; a capacitor of 1µF is normally sufficient for most applications, although in some cases 10µF may be required. Noise introduced onto $\pm V_{SS1}$ should be decoupled to prevent degraded performance.

THEORY OF OPERATION

The ISO212P has no galvanic connection between the input and output. The analog input signal referenced to the input common (Com 1) is multiplied by the gain of the input amplifier and accurately reproduced at the output. The output section uses a differential design so either the HI or LO pin may be referenced to the output common (Com 2). This allows simple input signal inversion while maintaining the high impedance input configuration. A simplified diagram of the ISO212P is shown in Figure 2. The design consists of a DC/DC converter, an uncommitted input operational amplifier, a modulator circuit and a demodulator circuit. Magnetic isolation is provided by separate transformers in the power and signal paths.

The DC/DC converter provides power and synchronization signals across the isolation barrier to operate the operational amplifier and modulator circuitry. It also has sufficient capacity to power external input signal conditioning net-



NOTES: (1) Optional voltage offset adjust components. (2) 10µF decoupling to be used with external loads connected.

FIGURE 1. Power Supply and Signal Connections Shown for Non-Inverting, Unity Gain Configuration.

works. The uncommitted operational amplifier may be configured for signal buffering or amplification, depending on the application.

The modulator converts the input signal to an amplitude-modulated AC signal that is magnetically coupled to the demodulator by a miniature transformer providing the signal-path isolation. The demodulator recovers the input signal from the modulated signal using a synchronous technique to minimize noise and interference.

ABOUT THE BARRIER

For any isolation product, barrier integrity is of paramount importance in achieving high reliability. The ISO212P uses miniature toroidal transformers designed to give maximum isolation performance when encapsulated with a high-dielectric-strength material. The internal component layout is designed so that circuitry associated with each side of the barrier is positioned at opposite ends of the package. Areas where high electric fields can exist are positioned in the center of the package. The result is that the dielectric strength of the barrier typically exceeds 3kVrms.

ISOLATION VOLTAGE RATINGS

Because a long term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a high voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one. Historically, Burr-Brown has chosen a deliberately conservative one: V_{TEST} = (2 x ACrms continuous rating) + 1000V for ten seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients were not well defined.

Recent improvements in high voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO212P.

PARTIAL DISCHARGE

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high voltage stress. This ionization requires a higher applied voltage to start the discharge and a lower voltage to extinguish it once started. The higher start voltage is known as the inception voltage and the lower voltage is called the extinction voltage. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached. At this point, the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that if the discharge does not occur, the insulation system retains its integrity. If the discharge begins and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is both useful in rating the devices and in providing quality control of the manufacturing process. The inception voltage of these voids tends to be constant, so that the measurement of total charge being re-distributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure.

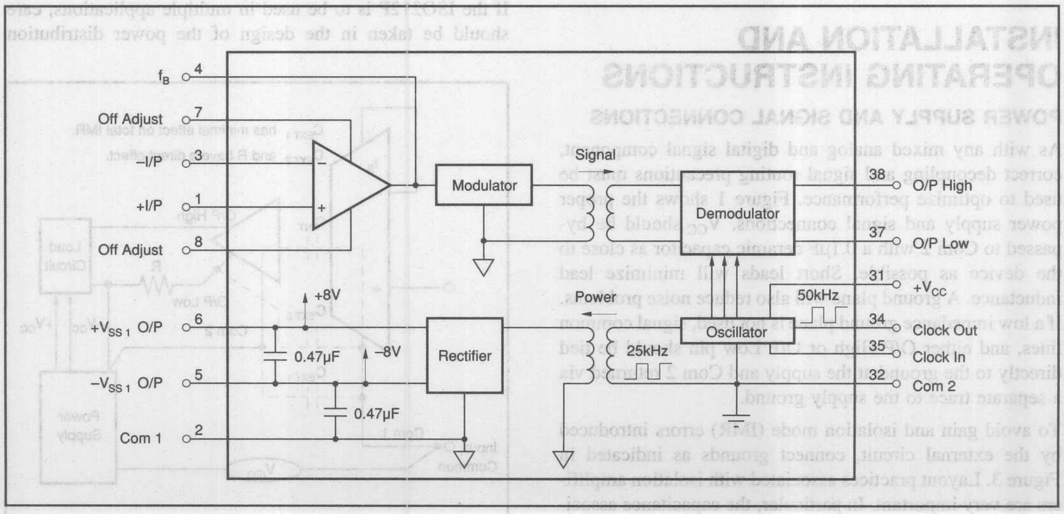


FIGURE 2. Simplified Diagram of Isolation Amplifier.

This directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin.

Measuring the bulk extinction voltage provides a lower, more conservative, voltage from which to derive a safe continuous rating. In production, it's acceptable to measure at a level somewhat below the expected inception voltage and then de-rate by a factor related to expectations about the system transients. The isolation amplifier has been extensively evaluated under a combination of high temperatures and high voltage to confirm its performance in this respect. The ISO212P is free of partial discharges at rated voltages.

PARTIAL DISCHARGE TESTING IN PRODUCTION

Not only does this test method provide far more qualitative information about stress withstand levels than did previous stress tests, but it also provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers such as those of high voltage power distribution equipment for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to measure partial discharge, and VDE, the German standards group, has adopted use of this method for the testing of opto-couplers. To accommodate poorly defined transients, the part under test is exposed to a voltage that is 1.6 times the continuous rated voltage and must display < 5pC partial discharge level in a 100% production test.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

As with any mixed analog and digital signal component, correct decoupling and signal routing precautions must be used to optimize performance. Figure 1 shows the proper power supply and signal connections. V_{CC} should be bypassed to Com 2 with a 0.1µF ceramic capacitor as close to the device as possible. Short leads will minimize lead inductance. A ground plane will also reduce noise problems. If a low impedance ground plane is not used, signal common lines, and either O/P High or O/P Low pin should be tied directly to the ground at the supply and Com 2 returned via a separate trace to the supply ground.

To avoid gain and isolation mode (IMR) errors introduced by the external circuit, connect grounds as indicated in Figure 3. Layout practices associated with isolation amplifiers are very important. In particular, the capacitance associated with the barrier, and series resistance in the signal and reference leads, must be minimized. Any capacitance across ... capacitance, may degrade high frequency IMR.

VOLTAGE GAIN MODIFICATIONS

The uncommitted operational amplifier at the input can be used to provide gain, signal inversion, active filtering or current to voltage conversion. The standard design approach for any op-amp stage can be used, provided that the full scale voltage appearing on f_B does not exceed ±5V.

If the input op-amp is overdriven, ripple at the output will result. To prevent this, the feedback resistor should have a minimum value of 10kΩ.

Also, it should be noted that the current required to drive the equivalent impedance of the feedback network is supplied by the internal DC/DC converter and must be taken into account when calculating the loading added to $\pm V_{SS1}$.

Since gain inversion can be incorporated in either the input or output stage of the ISO212P, it is possible to use the input amplifier in a non-inverting configuration and preserve the high impedance this configuration offers. Signal inversion at the output is easily accomplished by connecting O/P High to Com 2 instead of O/P Low.

ISOLATED POWER OUTPUT DRIVE CAPABILITY

On the input side of the ISO212P, there are two power supplies capable of delivering 5mA at ±8V to power external circuitry. When using these supplies with external loads, it is recommended that additional decoupling in the form of 10µF tantalum bead capacitors be added to improve the voltage regulation. Loss of linearity will result if additional filtering is not used with an output load. Again, power dissipated in the feedback loop around the input op amp must be subtracted from the available power output at $\pm V_{SS1}$.

If the ISO212P is to be used in multiple applications, care should be taken in the design of the power distribution

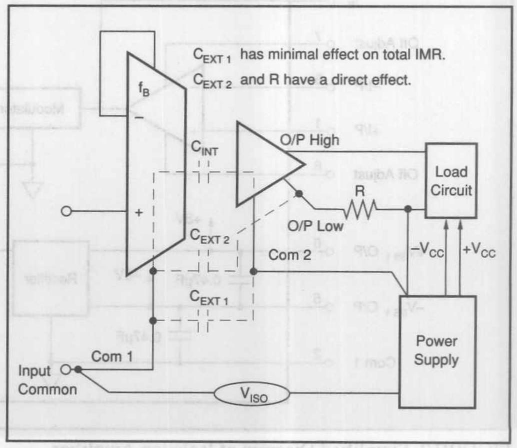


FIGURE 3. Technique for Connecting Com 1 and Com 2.

arrangement as shown in Figure 4.

NOISE

Output noise is generated by residual components of the 25kHz carrier that have not been removed from the signal. This noise may be reduced by adding an output low pass filter (see Figure 8). The filter time constants should be set below the carrier frequency. The output from the ISO212P is a switched capacitor and requires a high impedance load to prevent degradation of linearity. Loads of less than 1MΩ will cause an increase in noise at the carrier frequency and will appear as ripple in the output waveform. Since the output signal power is generated from the input side of the barrier, decoupling of the $\pm V_{SS\,1}$ outputs will improve the signal to noise ratio.

SYNCHRONIZATION OF THE INTERNAL OSCILLATOR

The ISO212P has an internal oscillator and associated timing components, which can be synchronized, incorporated into the design. This alleviates the requirement for an external high-power clock driver. The typical frequency of oscillation is 50kHz. The internal clock will start when power is applied to the ISO212P and Clk In is not connected.

Because the frequencies of several ISO212Ps can be marginally different, "beat" frequencies ranging from a few Hz to a few kHz can exist in multiple amplifier applications. The design of the ISO212P accommodates "internal synchronous" noise, but a synchronous beat frequency noise will not be strongly attenuated, especially at very low frequencies if it is introduced via the power, signal, or potential grounding paths. To overcome this problem in systems where several ISO212Ps are used, the design allows synchronization of each oscillator in a system to one frequency. Do this by forcing the timing node on the internal oscillator with an used as the master clock for the system. See Figure 6 and 7 for connections in multiple ISO212P installations.

CHARGE ISOLATION

When more than one ISO212P is used in synchronous mode, the charge which is returned from the timing capacitor (220pF in Figure 5) on each transition of the clock becomes significant. Figure 7 illustrates a method of isolating the "Clk Out" clamp diodes (Figure 5) from this charge.

A 22kΩ resistor (recommended maximum to use) together with the 39kΩ internal oscillator timing resistor (Figure 5) forms a potential divider. The ratio of these resistors should be greater than 0.6 which ensures that the input voltage triggers the inverter connected to "Clk In". If using a single resistor, then account must be taken of the paralleled timing resistors. This means that the 22kΩ resistor must be halved to drive two ISO212Ps, or divided by 8 if driving 8 ISO212Ps to insure that the ratio of greater than 0.6 is maintained. The series resistors shown in Figure 7 reduce the high frequency content of the power supply current.

APPLICATIONS

The ISO212P isolation amplifier, together with a few low cost components, can isolate and accurately convert a 4-to-20mA input to a ±10V output with no external adjustment. Its low height (0.43" (11mm)) and small footprint (2.5" x 0.33" (57mm x 8mm)) make it the solution of choice in 0.5" board spacing systems and in all applications where board area savings are critical.

The ISO212P operates from a single +15V supply and offers low power consumption and 12-bit accuracy. On the input side, two isolated power supplies capable of supplying 5mA at ±8V are available to power external circuitry.

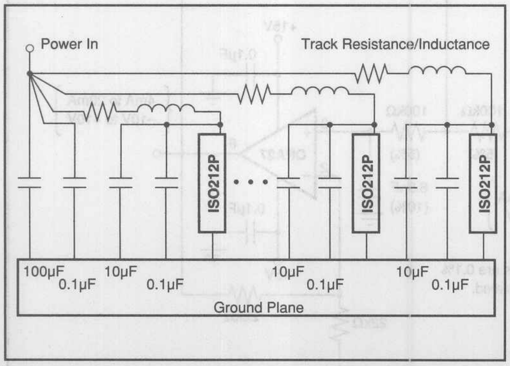


FIGURE 4. Recommended Decoupling and Power Distribution.

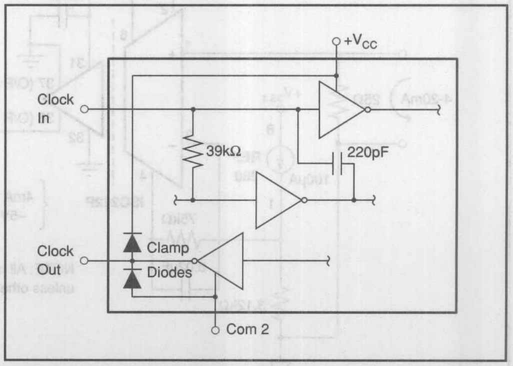


FIGURE 5. Equivalent Circuit, Clock Input/Output. Inverters are CMOS.

ISOLATION PRODUCTS 5 ISO212P

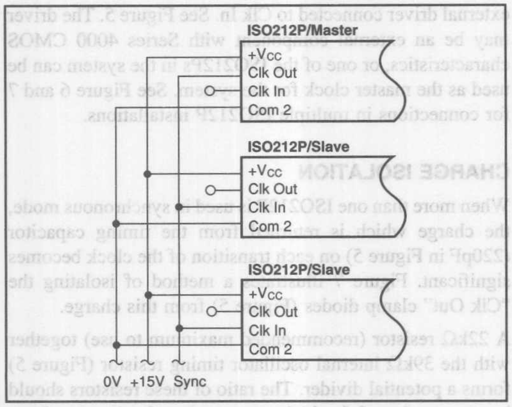


FIGURE 6. Oscillator Connections for Synchronous Operation in Multiple ISO212P Installations.

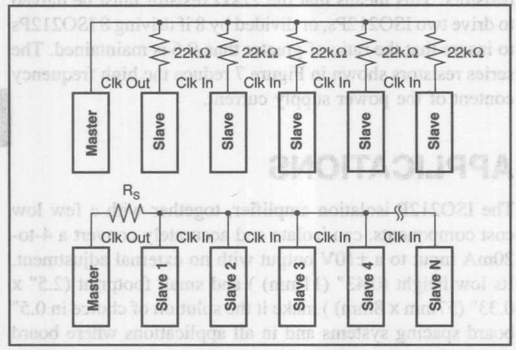


FIGURE 7. Isolating the Clk Out Node.

APPLICATIONS FLEXIBILITY

In Figure 8, the ISO212P's $+V_{ss\ 1}$ isolated supply powers a REF200 to provide an accurate 100μA current source. This current is opposed by an equal but opposite current through the 75kΩ feedback resistor to establish an offset of –7.5V at I_{in} = 0mA. With I_{in} = 4-to-20mA, the output is –5 to +5V. The ratio of the 75kΩ and 3.12kΩ resistors assures the correct gain.

The polarity of the output can be reversed by simply reversing the O/P HI and O/P LO pins. This could be used in the Figure 8 circuit to change the –5V to +5V output to a +5V to –5V output range.

The primary function of the output circuitry is to add gain to produce a ±10V output and to reduce output impedance. The addition of a few resistors and capacitors provides a low pass filter with a cut-off frequency equal to the full signal bandwidth of the ISO212P, typically 200Hz. The filter response is flat to 1dB and rolls off from cut off at –12dB per octave.

The accuracy of the REF200 and external resistors eliminates the need for expensive trim pots and adjustments. The errors introduced by the external circuitry only add about 10% of the ISO212P's specified gain and offset voltage error.

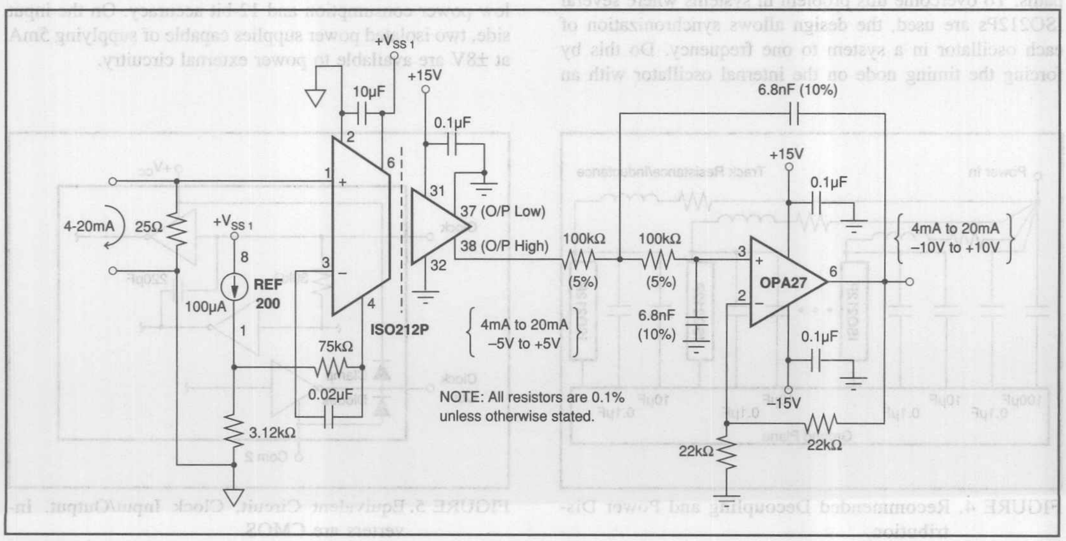


FIGURE 8. Isolated 4-20mA Current Receiver with Output Filter.

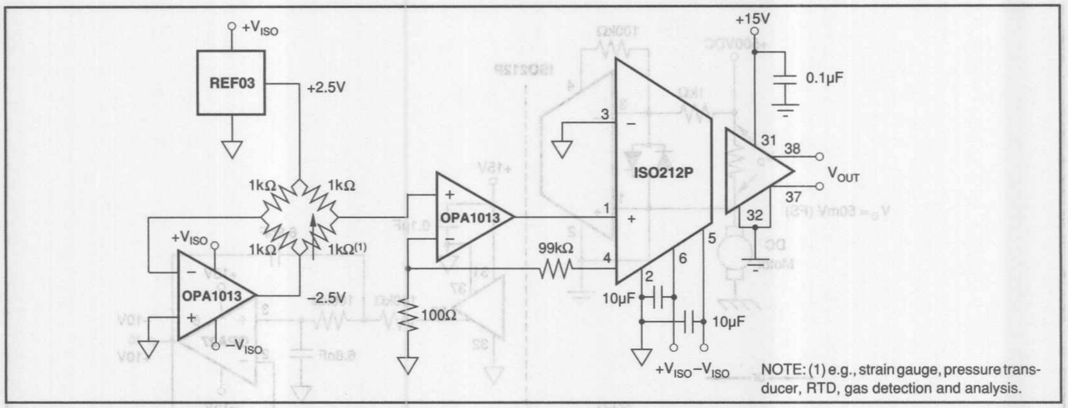


FIGURE 9. Instrument Bridge Isolation Amplifier.

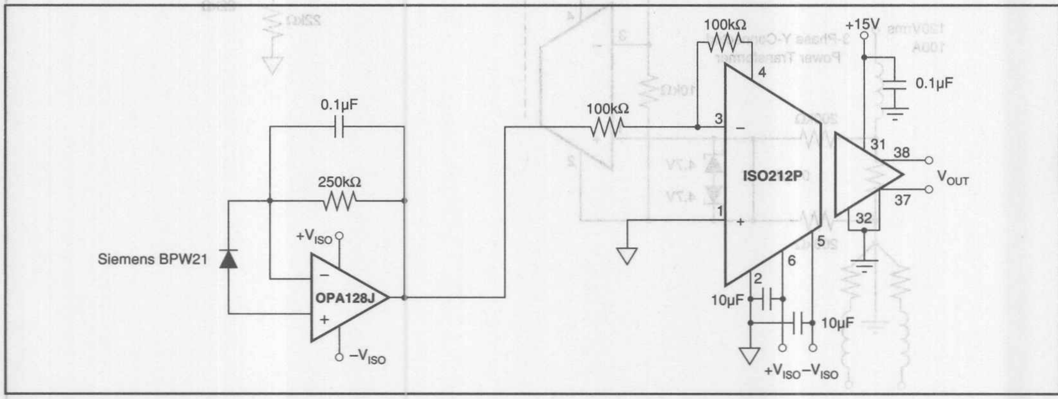


FIGURE 10. Photodiode Isolation Amplifier.

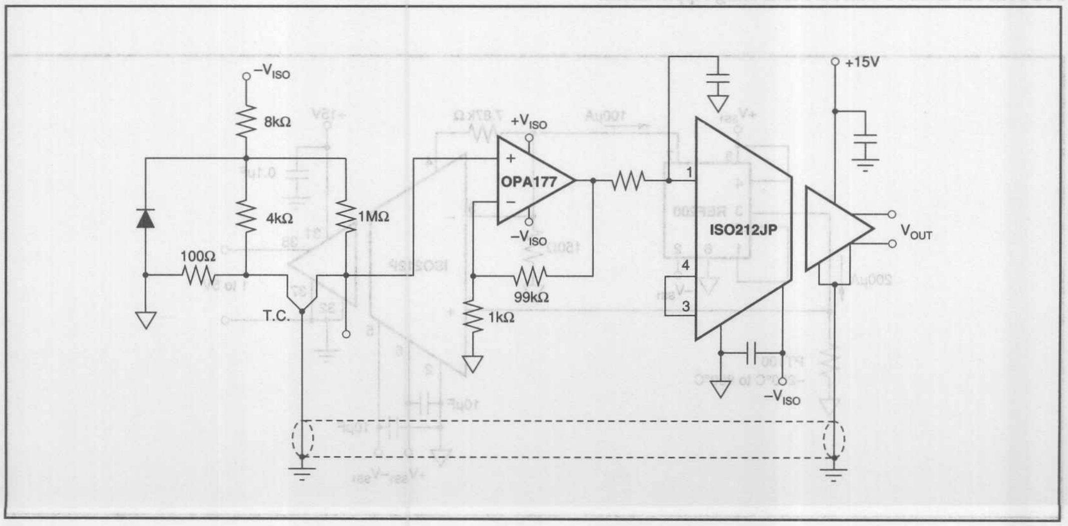


FIGURE 11. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation and Down-Scale Burn-Out.

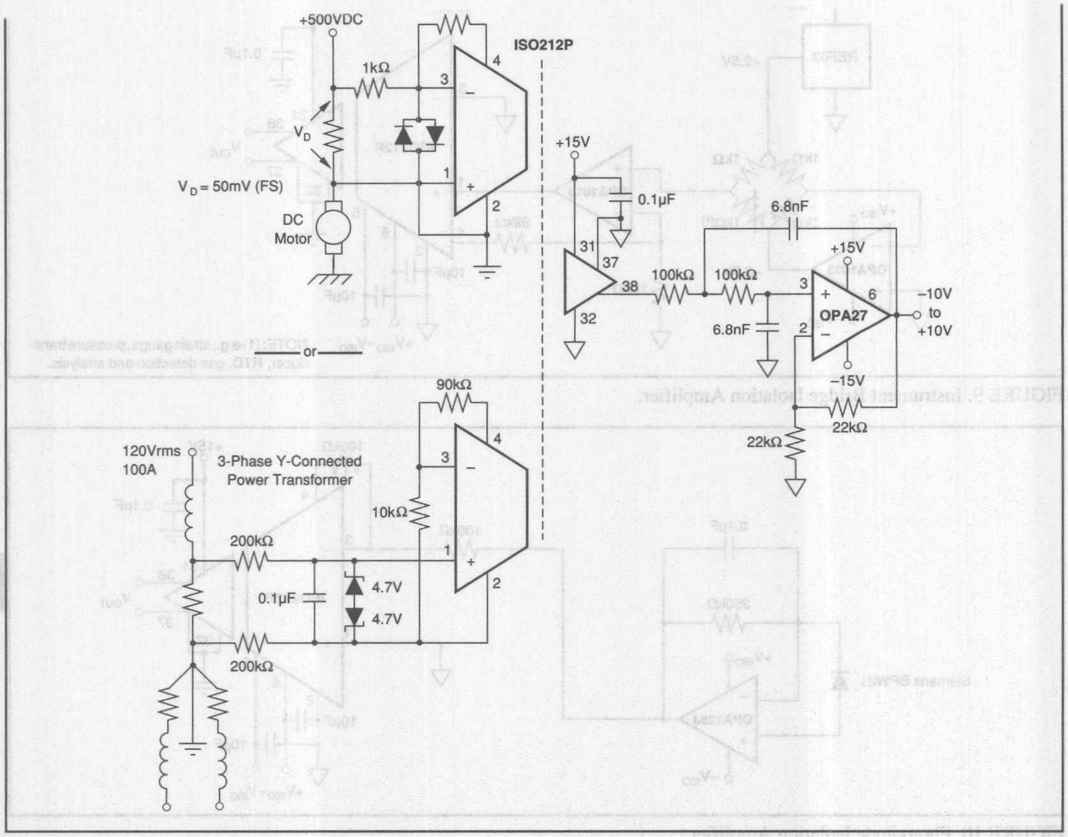


FIGURE 12. Isolated Current Monitoring Applications.

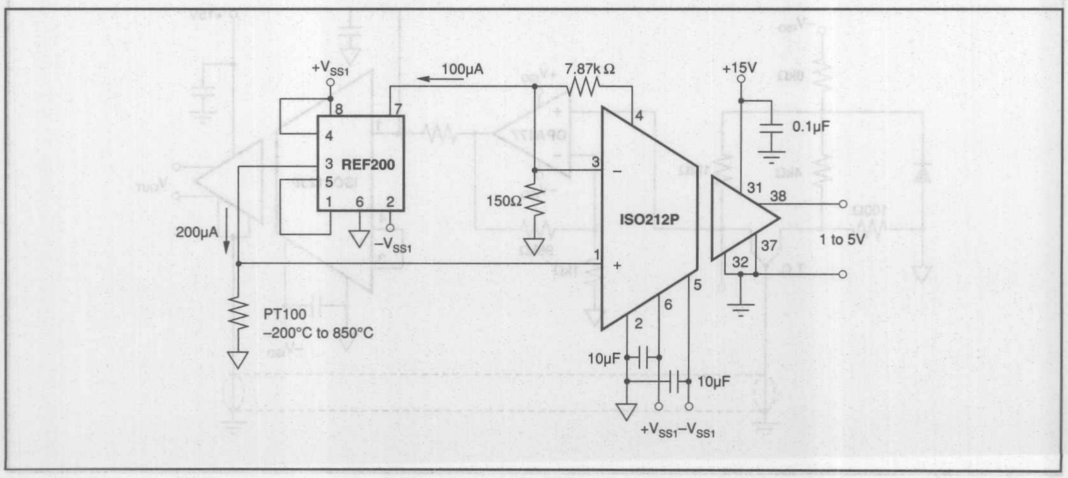
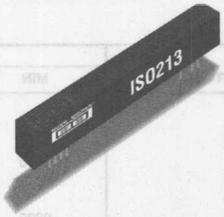


FIGURE 13. Isolated Temperature Sensing and Amplification.

BURR - BROWN®



ISO213

Two-Port Isolated, Low Profile ISOLATED INSTRUMENTATION AMPLIFIER

FEATURES

- GAIN RANGE: 0.5 - 5000
- ±10V INPUT SIGNAL RANGE
- INSTRUMENTATION AMPLIFIER INPUTS
- ±40V INPUT OVER VOLTAGE PROTECTION
- 12-BIT ACCURACY
- LOW PROFILE (Less Than 0.5" High)
- SMALL FOOTPRINT
- EXTERNAL POWER CAPABILITY (±14V at 3mA)
- SYNCHRONIZATION CAPABILITY
- SINGLE 12V TO 15V SUPPLY OPERATION
- LOW POWER (45mW)

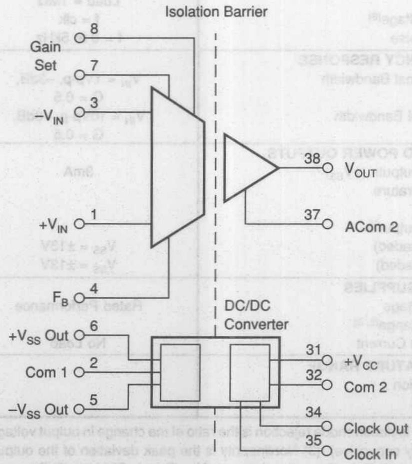
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Channel Isolator for Thermocouples, RTDs, Pressure Bridges, Flow Meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MULTIPLEXED SYSTEMS WITH CHANNEL TO CHANNEL ISOLATION

DESCRIPTION

ISO213 signal isolation amplifier is a member of a series of low-cost isolation products from Burr-Brown. The low-profile ZIP plastic package allows PCB spacings of 0.5" to be achieved, and the small footprint results in efficient use of board space.

To provide isolation, the design uses high-efficiency, miniature toroidal transformers in both the signal and power paths. An uncommitted instrumentation amplifier on the input and an isolated external bipolar supply ensure the majority of input interfacing or conditioning needs can be met.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

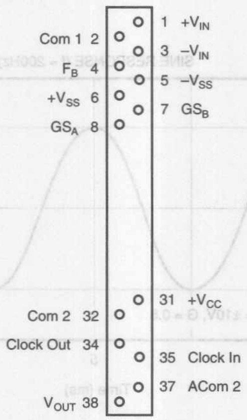
At T_A = +25°C, V_{CC} = +15V, unless otherwise noted.

PARAMETER	CONDITIONS	ISO213P MIN	TYP	MAX	UNITS
ISOLATION					
Voltage					
Rated Continuous					
AC, 50/60Hz		1500			Vrms
DC		2120			VDC
Rated 1 min					
AC, 50/60Hz		2500			Vrms
100% Test (AC, 50Hz)	Partial Discharge 1s <5pC	2500			Vrms
Isolation-Mode Rejection(1)	V_{ISO} = Rated Continuous 50/60Hz				
AC			115		dB
DC			160		dB
Barrier Resistance			10^{10}		Ω
Barrier Capacitance			15		pF
Leakage Current(2)	V_{ISO} = 240Vrms, 60Hz			3	μArms
	V_{ISO} = 240Vrms, 50Hz			2.4	μArms
GAIN					
Equation			$G = (1 + 50k/R_G)/2$		
Initial Error	G = 0.5		±0.2	±3	% FSR(8)
Gain vs Temperature	G = 0.5		10	50	ppm of FSR/°C
Non-Linearity(3)	V_O = –5V to +5V, G = 0.5		0.01	0.025	%FSR
INPUT OFFSET VOLTAGE					
Offset Voltage RTI				±0.5 ±25/G	mV
vs Temperature			±5 ±35/G		μV/°C
vs Power Supply(4)	G = 0.5, V_{CC} = 14V to 16V		±3		mV/V
INPUT CURRENT					
Bias			±1	±10	nA
Offset			±1	±10	nA
INPUT					
Linear Input Range(5)	G = 0.5	±10	±12		V
Common-Mode Rejection	V_{CM} = ±10V, ΔR_S = 1kΩ				
	G = 0.5	73	90		dB
	G = 5	89	110		dB
	G = 50	98	120		dB
	G = 500	100	125		dB
Impedance					
Differential			10^{10} ‖ 3		Ω ‖ pF
Common-Mode			10^{10} ‖ 6		Ω ‖ pF
OUTPUT					
Output Impedance			3		kΩ
Voltage	Load = 1MΩ	±5			V
Ripple Voltage(6)	f = clk		1		mVp-p
Output Noise	f = 0 to 5kHz		20		$\mu V/\sqrt{Hz}$
FREQUENCY RESPONSE					
Small Signal Bandwidth	V_{IN} = 1Vp-p, –3dB, G = 0.5		1		kHz
Full Signal Bandwidth	V_{IN} = 10Vp-p, –3dB, G = 0.5		200		Hz
ISOLATED POWER OUTPUTS					
Voltage Outputs (±V_{SS})(7)	3mA	±13	±14		VDC
vs Temperature			7		mV/°C
vs Load			180		mV/mA
Current Output(7)					
(Both Loaded)	V_{SS} = ±13V	3	6		mA
(One Loaded)	V_{SS} = ±13V	4	6		mA
POWER SUPPLIES					
Rated Voltage	Rated Performance		15		V
Voltage Range(5, 9)			11.4 to 16		V
Quiescent Current	No Load		3	6	mA
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–25		+85	°C

NOTES: (1) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. (2) Tested at 2500Vrms 50Hz limit 25μA (barrier is essentially capacitive). (3) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (4) Power Supply Rejection is the change in V_{OS}/Supply Change. (5) See max V_{OUT} and V_{IN} vs Supply Voltage in typical performance curves. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Derated at V_{CC} < 15V. (8) FSR = Full Scale Output Range = 10V. (9) Minimum supply voltage is given as 11.4V. This is the minimum supply to ensure a ±5V output swing can be achieved. The ISO213 actually works down to a minimum supply of 4V as shown in the typical performance curve "Max V_{OUT} and V_{IN} vs Supply Voltage."

PIN CONFIGURATION

Bottom View



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Without Damage	18V
Continuous Isolation Voltage Across Barrier:	2500Vrms
Storage Temperature Range	–25°C to 100°C
Lead Temperature (soldering, 10s)	+300°C
Amplifier Output Short-Circuit Duration	Continuous to Common
Output Voltage to Com 2	$\pm V_{CC}/2$

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO213P	38-Pin Plastic ZIP	326

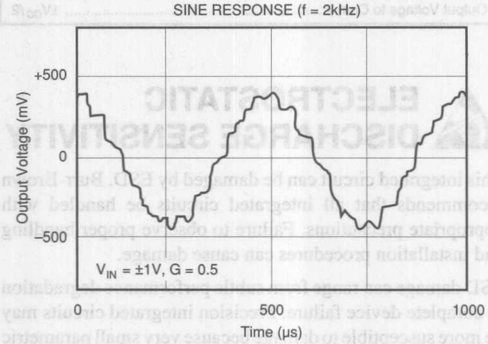
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

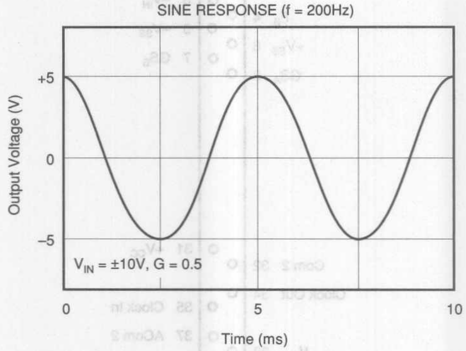
ORDERING INFORMATION

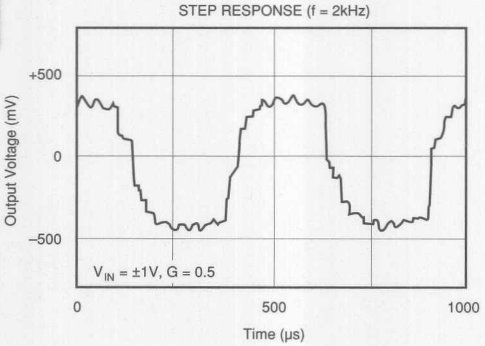
MODEL	PACKAGE	OPERATING TEMPERATURE RANGE	ISOLATION RATING 1 MIN
ISO213P	38-Pin Plastic ZIP	–25°C to +85°C	2500Vrms

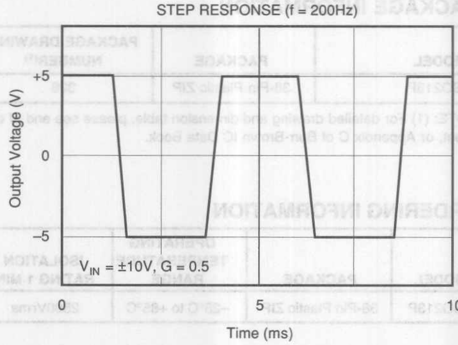
TYPICAL PERFORMANCE CURVES

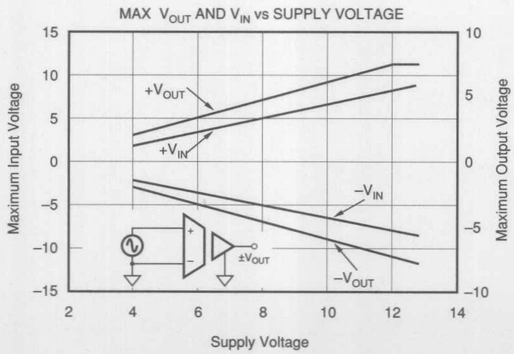
At T_A = +25°C, V_{CC} = +15V, unless otherwise noted.

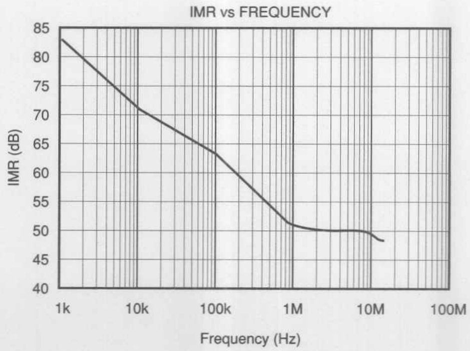








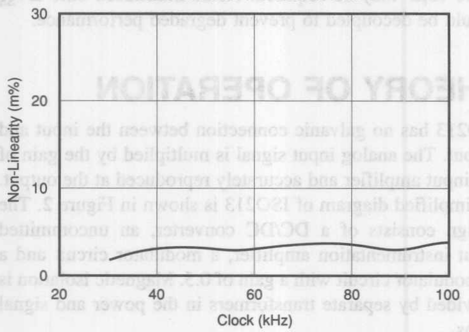




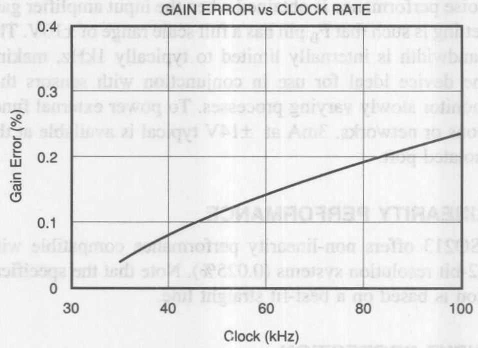
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = +15V, unless otherwise noted.

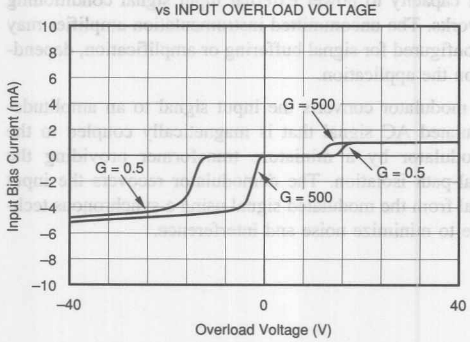
NON-LINEARITY vs CLOCK RATE



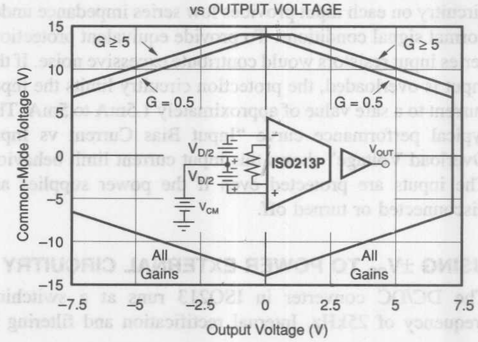
GAIN ERROR vs CLOCK RATE



INPUT BIAS CURRENT
vs INPUT OVERLOAD VOLTAGE



INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE



DISCUSSION OF SPECIFICATIONS

ISO213 is intended for applications where isolation and input signal conditioning are required. The best signal-to-noise performance is obtained when the input amplifier gain setting is such that F_B pin has a full scale range of ±10V. The bandwidth is internally limited to typically 1kHz, making the device ideal for use in conjunction with sensors that monitor slowly varying processes. To power external functions or networks, 3mA at ±14V typical is available at the isolated port.

LINEARITY PERFORMANCE

ISO213 offers non-linearity performance compatible with 12-bit resolution systems (0.025%). Note that the specification is based on a best-fit straight line.

INPUT PROTECTION

The inputs of ISO213 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5mA to 5mA. The typical performance curve "Input Bias Current vs Input Overload Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

USING $\pm V_{SS}$ TO POWER EXTERNAL CIRCUITRY

The DC/DC converter in ISO213 runs at a switching frequency of 25kHz. Internal rectification and filtering is sufficient for most applications at low frequencies with no external networks connected.

The unloaded ripple on $\pm V_{SS}$ is typically 100mVp-p at 25kHz, which increases with loading. A capacitor of 1µF is normally sufficient for most applications, although in some cases 10µF may be required. Noise introduced onto $\pm V_{SS}$ should be decoupled to prevent degraded performance.

THEORY OF OPERATION

ISO213 has no galvanic connection between the input and output. The analog input signal is multiplied by the gain of the input amplifier and accurately reproduced at the output. A simplified diagram of ISO213 is shown in Figure 2. The design consists of a DC/DC converter, an uncommitted input instrumentation amplifier, a modulator circuit and a demodulator circuit with a gain of 0.5. Magnetic isolation is provided by separate transformers in the power and signal paths.

The DC/DC converter provides power and synchronization signals across the isolation barrier to operate the instrumentation amplifier and modulator circuitry. It also has sufficient capacity to power external input signal conditioning networks. The uncommitted instrumentation amplifier may be configured for signal buffering or amplification, depending on the application.

The modulator converts the input signal to an amplitude-modulated AC signal that is magnetically coupled to the demodulator by a miniature transformer providing the signal-path isolation. The demodulator recovers the input signal from the modulated signal using a synchronous technique to minimize noise and interference.

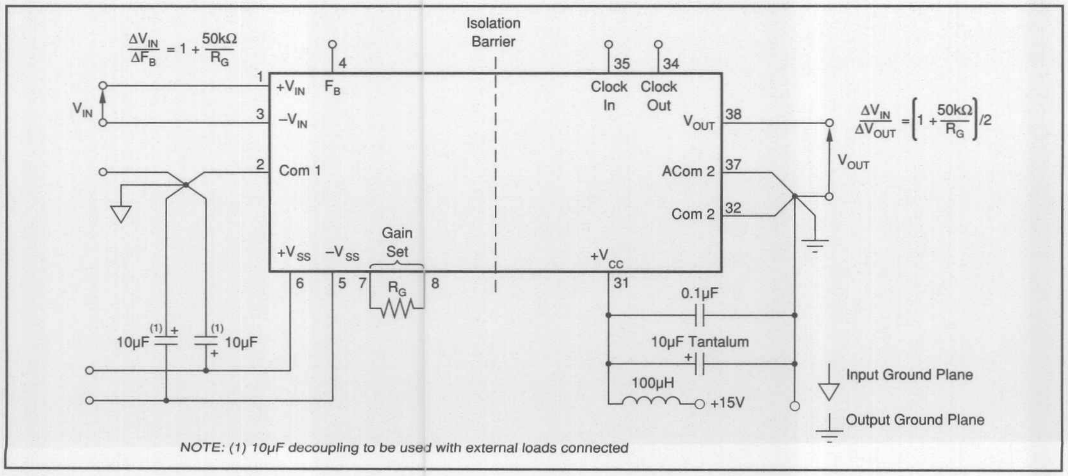


FIGURE 1. Power Supply and Signal Connections Shown for Non-Inverting, Unity Gain Configuration.

ABOUT THE BARRIER

For any isolation product, barrier integrity is of paramount importance in achieving high reliability. ISO213 uses miniature toroidal transformers designed to give maximum isolation performance when encapsulated with a high dielectric-strength material. The internal component layout is designed so that circuitry associated with each side of the barrier is positioned at opposite ends of the package. Areas where high electric fields can exist are positioned in the center of the package. The result is that the dielectric strength of the barrier typically exceeds 3kVrms.

ISOLATION VOLTAGE RATINGS

Because a long term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a high voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one. Historically, Burr-Brown has chosen a deliberately conservative one: V_{TEST} = (2 x ACrms continuous rating) + 1000V for ten seconds, followed by a test at rated ACrms voltage for one minute.

Recent improvements in high voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology to the manufacture and testing of ISO213.

PARTIAL DISCHARGE

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high voltage stress. This ionization requires a higher applied voltage to start the discharge and a lower voltage to extinguish it once started. The higher start voltage is known as the inception voltage and the lower voltage is called the extinction voltage. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached. At this point, the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that if the discharge does not occur, the insulation system retains its integrity. If the discharge begins and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is both useful in rating the devices and in providing quality control of the manufacturing process. The inception voltage of these voids tend to be constant, so that the measurement of total charge being redistributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure.

The bulk inception voltage, on the other hand, varies with the insulation system and the number of ionization defects. This directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin.

Measuring the bulk extinction voltage provides a lower, more conservative, voltage from which to derive a safe continuous rating. In production, it's acceptable to measure at a level somewhat below the expected inception voltage and then de-rate by a factor related to expectations about the

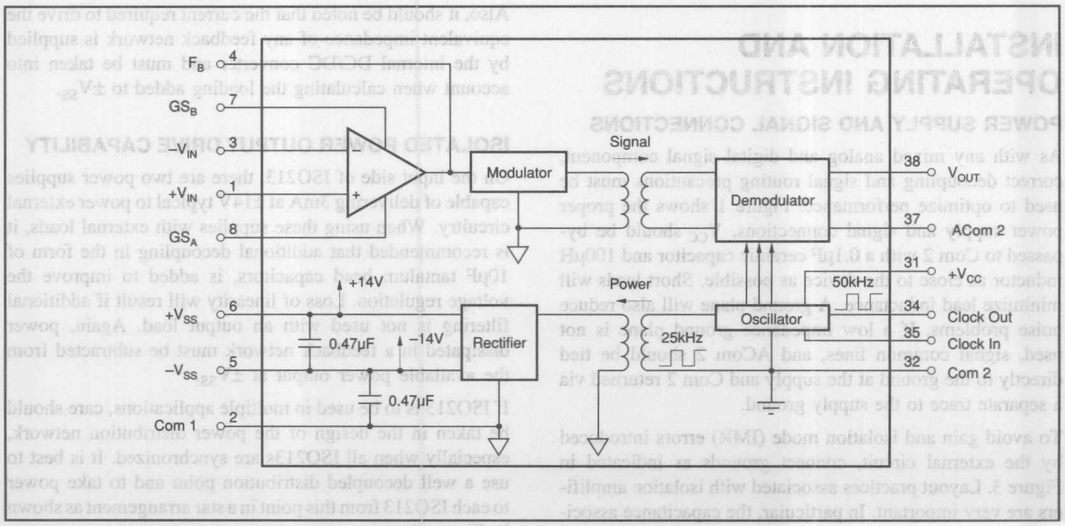


FIGURE 2. Simplified Diagram of Isolation Amplifier.

ISO213

5

ISOLATION PRODUCTS

system transients. The isolation barrier has been extensively evaluated under a combination of high temperatures and high voltage to confirm its performance in this respect. ISO213 is free from partial discharges at rated voltages.

PARTIAL DISCHARGE TESTING IN PRODUCTION

This test method provides far more qualitative information about stress withstand levels than did previous stress tests. It also provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers such as those of high voltage power distribution equipment for some time. They employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to measure partial discharge, and VDE, the German standards group, has adopted use of this method for the testing of opto-couplers. To accommodate poorly defined transients, the part under test is exposed to a voltage that is 1.6 times the continuous rated voltage and must display <5pC partial discharge level in a 100% production test. Where transients are not present on an applied voltage and the bulk inception voltage is not exceeded, degradation will not take place. This is the case where OEM production testing is performed to satisfy regulatory requirements. The normal test is to apply a relatively slow ramp to a defined test voltage. Maintain that voltage for 1 minute and then ramp to zero. Where this test voltage is less than or equal to the partial discharge test voltage it can be seen that degradation will not occur. Hence ISO213 is guaranteed to withstand a continuous test voltage for 1 minute at the partial discharge test voltage.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

As with any mixed analog and digital signal component, correct decoupling and signal routing precautions must be used to optimize performance. Figure 1 shows the proper power supply and signal connections. V_{CC} should be bypassed to Com 2 with a 0.1µF ceramic capacitor and 100µH inductor as close to the device as possible. Short leads will minimize lead inductance. A ground plane will also reduce noise problems. If a low impedance ground plane is not used, signal common lines, and ACom 2 should be tied directly to the ground at the supply and Com 2 returned via a separate trace to the supply ground.

To avoid gain and isolation mode (IMR) errors introduced by the external circuit, connect grounds as indicated in Figure 3. Layout practices associated with isolation amplifiers are very important. In particular, the capacitance associated with the barrier, and series resistance in the signal and reference leads, must be minimized. Any capacitance across the barrier will increase AC leakage and, in conjunction with ground line resistance, may degrade high frequency IMR.

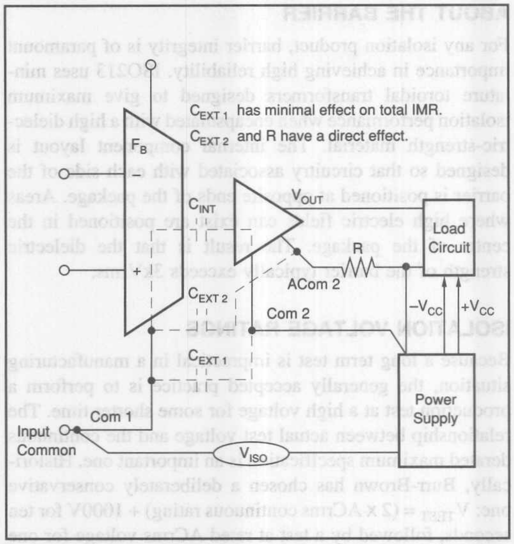


FIGURE 3. Technique for Connecting Com 1 and Com 2.

VOLTAGE GAIN MODIFICATIONS

The uncommitted instrumentation amplifier at the input can be used to provide gain, signal inversion, or current to voltage conversion. The standard design approach for any instrumentation amplifier stage can be used, provided that the full scale voltage appearing on F_B does not exceed ±10V.

Also, it should be noted that the current required to drive the equivalent impedance of any feedback network is supplied by the internal DC/DC converter and must be taken into account when calculating the loading added to $\pm V_{SS}$.

ISOLATED POWER OUTPUT DRIVE CAPABILITY

On the input side of ISO213, there are two power supplies capable of delivering 3mA at ±14V typical to power external circuitry. When using these supplies with external loads, it is recommended that additional decoupling in the form of 10µF tantalum bead capacitors, is added to improve the voltage regulation. Loss of linearity will result if additional filtering is not used with an output load. Again, power dissipated in a feedback network must be subtracted from the available power output at $\pm V_{SS}$.

If ISO213 is to be used in multiple applications, care should be taken in the design of the power distribution network, especially when all ISO213s are synchronized. It is best to use a well decoupled distribution point and to take power to each ISO213 from this point in a star arrangement as shown in Figure 4.

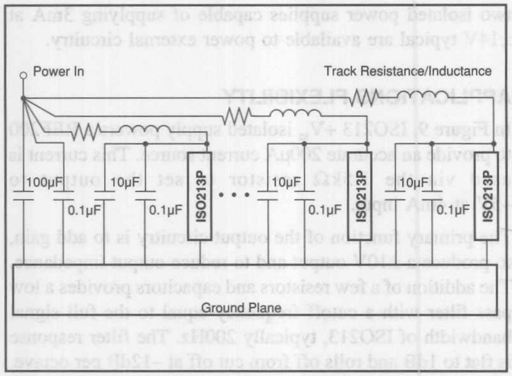


FIGURE 4. Recommended Decoupling and Power Distribution.

NOISE

Output noise is generated by residual components of the 25kHz carrier that have not been removed from the signal. This noise may be reduced by adding an output low-pass filter (see Figure 9). The filter time constant should be set below the carrier frequency. The output from ISO213 is a switched capacitor and requires a high impedance load to prevent degradation of linearity. Loads of less than 1MΩ will cause an increase in noise at the carrier frequency and will appear as ripple in the output waveform. Since the output signal power is generated from the input side of the barrier, decoupling of the $\pm V_{SS}$ outputs will improve the signal to noise ratio.

SYNCHRONIZATION OF THE INTERNAL OSCILLATOR

ISO213 has an internal oscillator and associated timing components, which can be synchronized. This alleviates the requirement for an external high-power clock driver. The typical frequency of oscillation is 50kHz. The internal clock will start when power is applied to ISO213 and Clk In is not connected.

Because the oscillator frequency of each ISO213 can be marginally different, "beat" frequencies ranging from a few Hz to a few kHz can exist in multiple amplifier applications. The design of ISO213 accommodates "internal synchronous" noise, but a synchronous beat frequency noise will not be strongly attenuated, especially at very low frequencies if it is introduced via the power, signal, or potential grounding paths. To overcome this problem in systems where several ISO213s are used, the design allows synchronization of each oscillator in a system to one frequency. Do this by forcing the timing node on the internal oscillator with an external driver connected to Clk In (Figure 5). The driver may be an external component with Series 4000 CMOS characteristics, or one ISO213 in the system can be used as the master clock for the system. An alternative where a specific frequency is not required is to lock all ISO213s together by joining all Clk Ins. This method can be used to lock an unlimited number of ISO213s. See Figure 6, 7, and 8 for connections in multiple ISO213 installations.

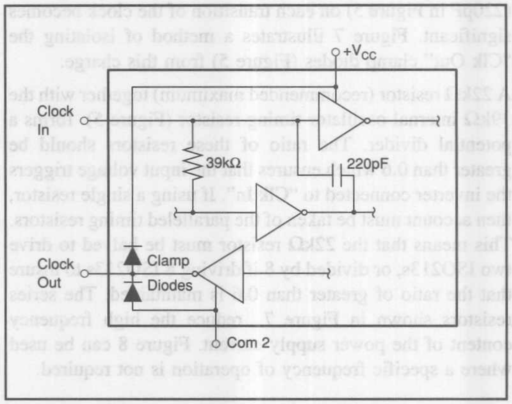


FIGURE 5. Equivalent Circuit, Clock Input/Output. Inverters are CMOS.

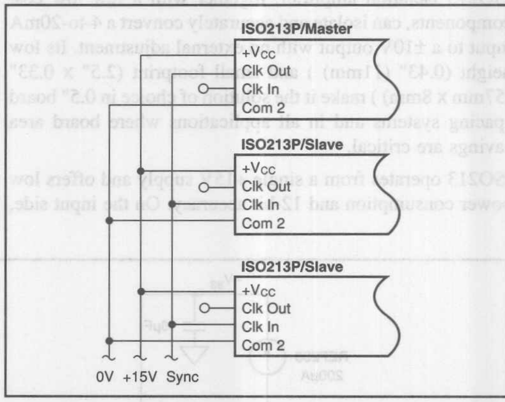


FIGURE 6. Oscillator Connections for Synchronous Operation in Multiple ISO213P Installations.

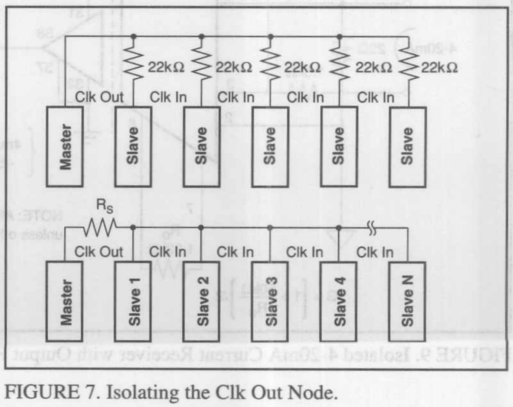


FIGURE 7. Isolating the Clk Out Node.

CHARGE ISOLATION

When more than one ISO213 is used in synchronous mode, the charge which is returned from the timing capacitor (220pF in Figure 5) on each transition of the clock becomes significant. Figure 7 illustrates a method of isolating the "Clk Out" clamp diodes (Figure 5) from this charge.

A 22kΩ resistor (recommended maximum) together with the 39kΩ internal oscillator timing resistor (Figure 5) forms a potential divider. The ratio of these resistors should be greater than 0.6 which ensures that the input voltage triggers the inverter connected to "Clk In". If using a single resistor, then account must be taken of the paralleled timing resistors. This means that the 22kΩ resistor must be halved to drive two ISO213s, or divided by 8 if driving 8 ISO213s to insure that the ratio of greater than 0.6 is maintained. The series resistors shown in Figure 7 reduce the high frequency content of the power supply current. Figure 8 can be used where a specific frequency of operation is not required.

APPLICATIONS

ISO213 isolation amplifier, together with a few low cost components, can isolate and accurately convert a 4-to-20mA input to a ±10V output with no external adjustment. Its low height (0.43" (11mm)) and small footprint (2.5" x 0.33" (57mm x 8mm)) make it the solution of choice in 0.5" board spacing systems and in all applications where board area savings are critical.

ISO213 operates from a single +15V supply and offers low power consumption and 12-bit accuracy. On the input side, two isolated power supplies capable of supplying 3mA at ±14V typical are available to power external circuitry.

APPLICATIONS FLEXIBILITY

In Figure 9, ISO213 $+V_{SS}$ isolated supply powers a REF200 to provide an accurate 200µA current source. This current is used via the 1.5kΩ resistor to set the output to –5V at 4mA input.

The primary function of the output circuitry is to add gain, to produce a ±10V output and to reduce output impedance. The addition of a few resistors and capacitors provides a low pass filter with a cutoff frequency equal to the full signal bandwidth of ISO213, typically 200Hz. The filter response is flat to 1dB and rolls off from cut off at –12dB per octave.

The accuracy of REF200 and external resistors eliminates the need for expensive trim pots and adjustments. The errors introduced by the external circuitry only add about 10% of ISO213 specified gain and offset voltage error.

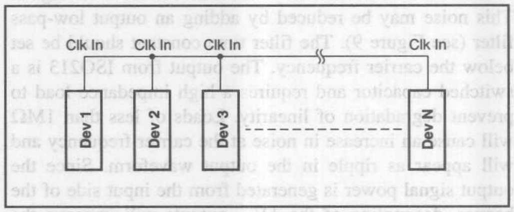


FIGURE 8. Recommended Synchronizing Scheme.

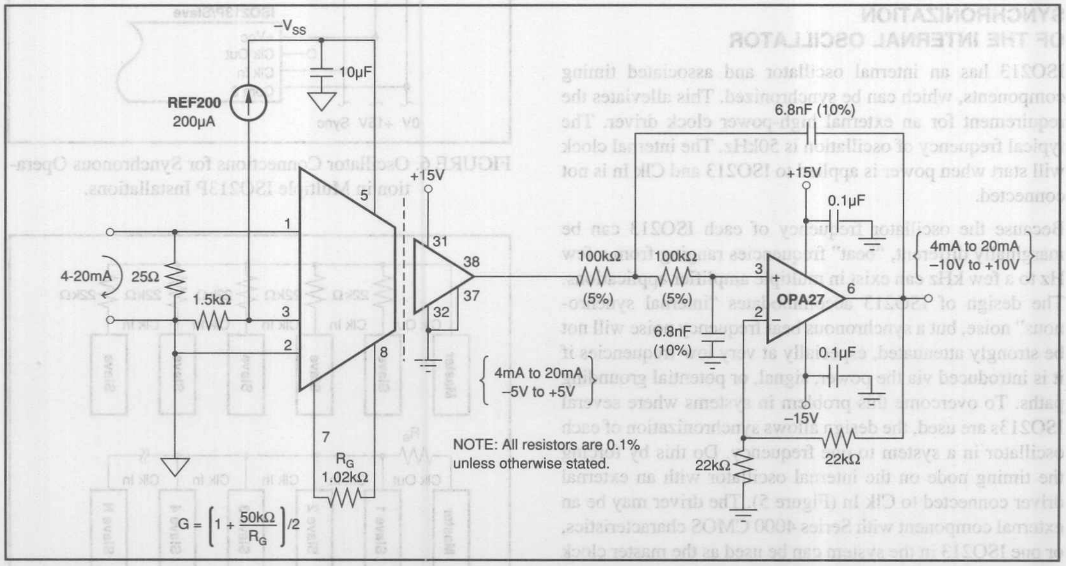


FIGURE 9. Isolated 4-20mA Current Receiver with Output Filter.

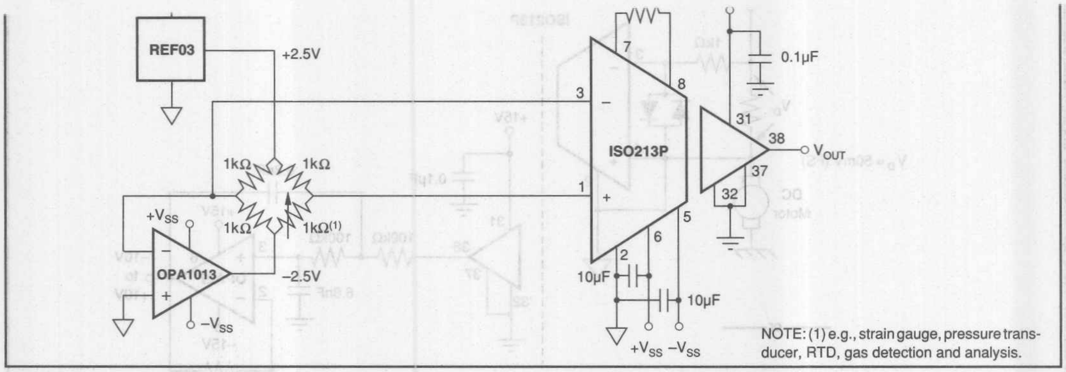


FIGURE 10. Instrument Bridge Isolation Amplifier.

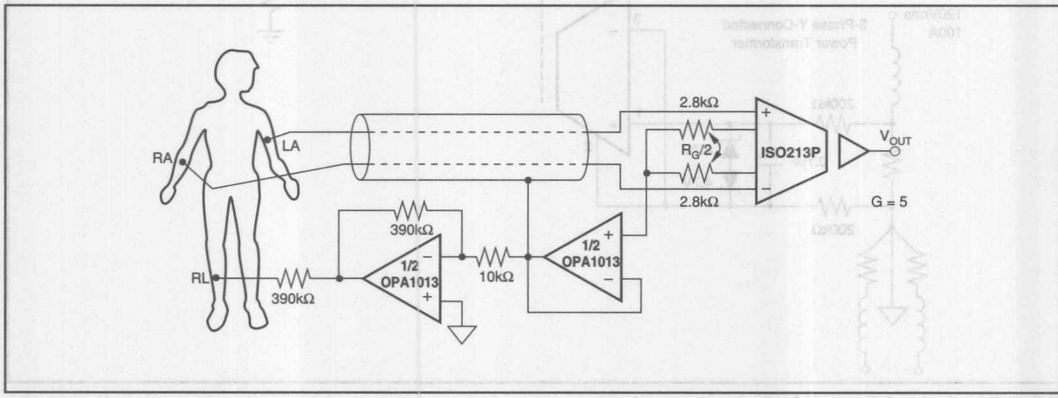
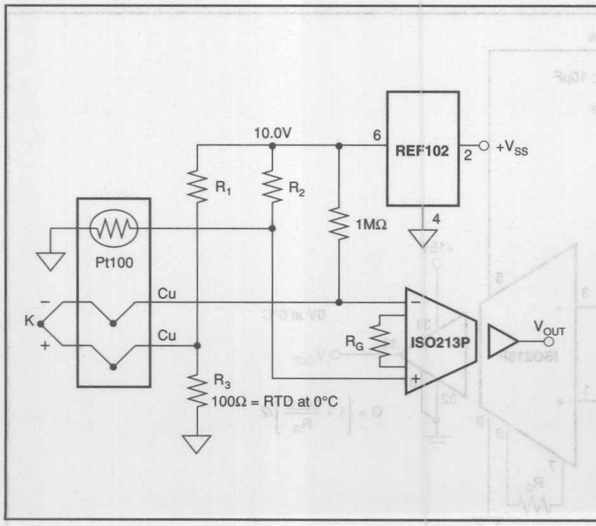


FIGURE 11. ECG Amplifier With Right-Leg Drive.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

FIGURE 12. Thermocouple Amplifier With Cold Junction Compensation and Down-Scale Burn-Out.

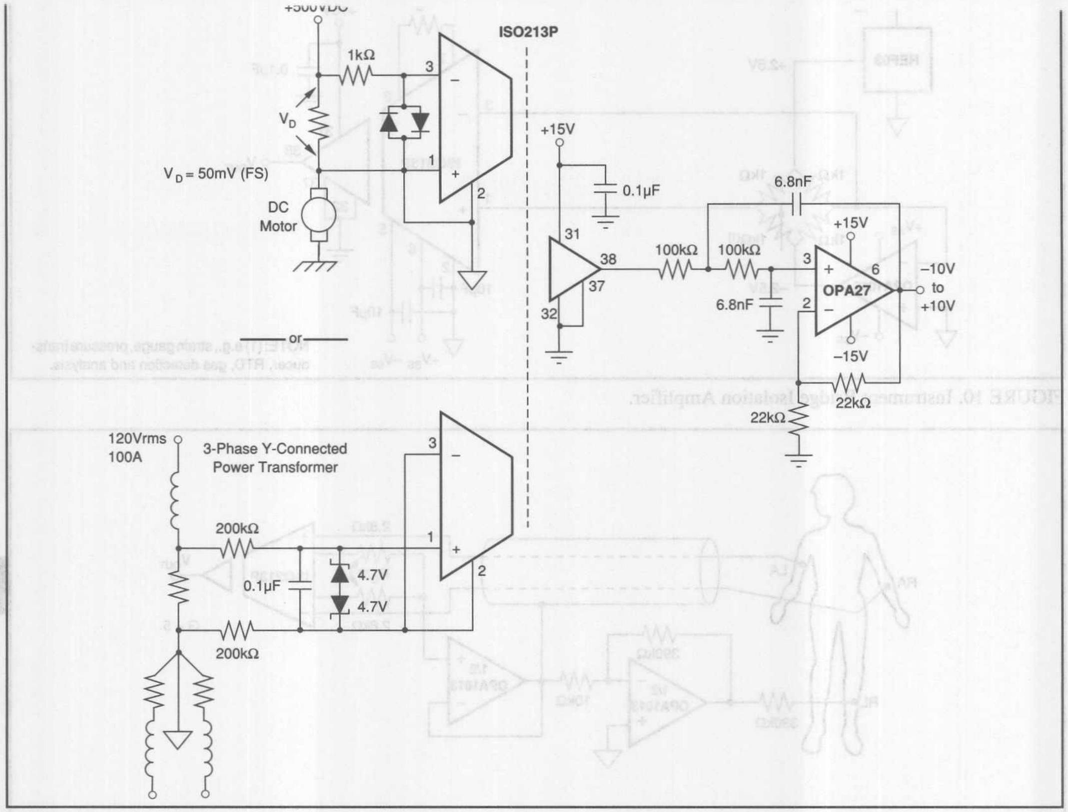


FIGURE 13. Isolated Current Monitoring Applications.

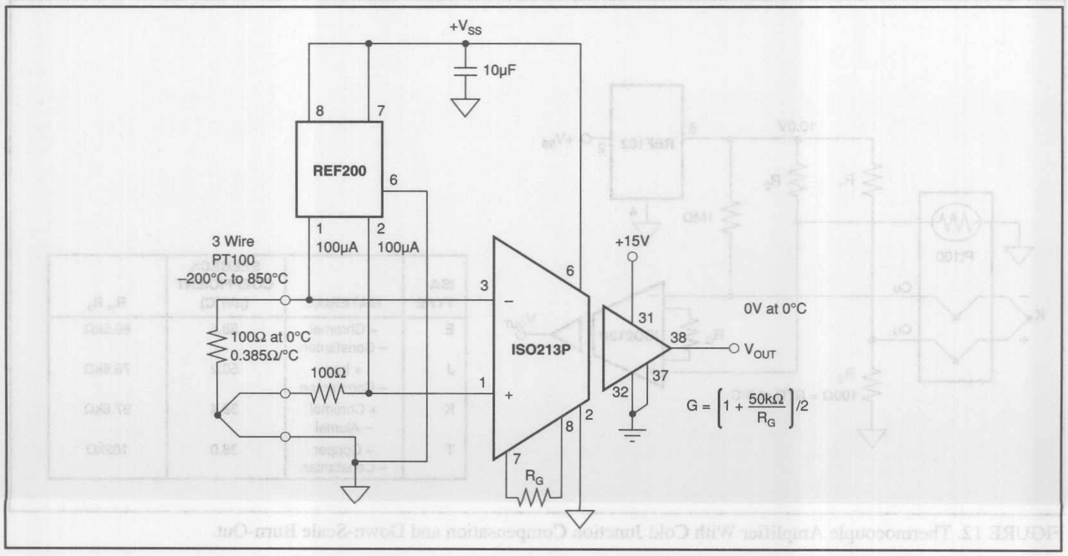


FIGURE 14. Isolated Temperature Sensing and Amplification.

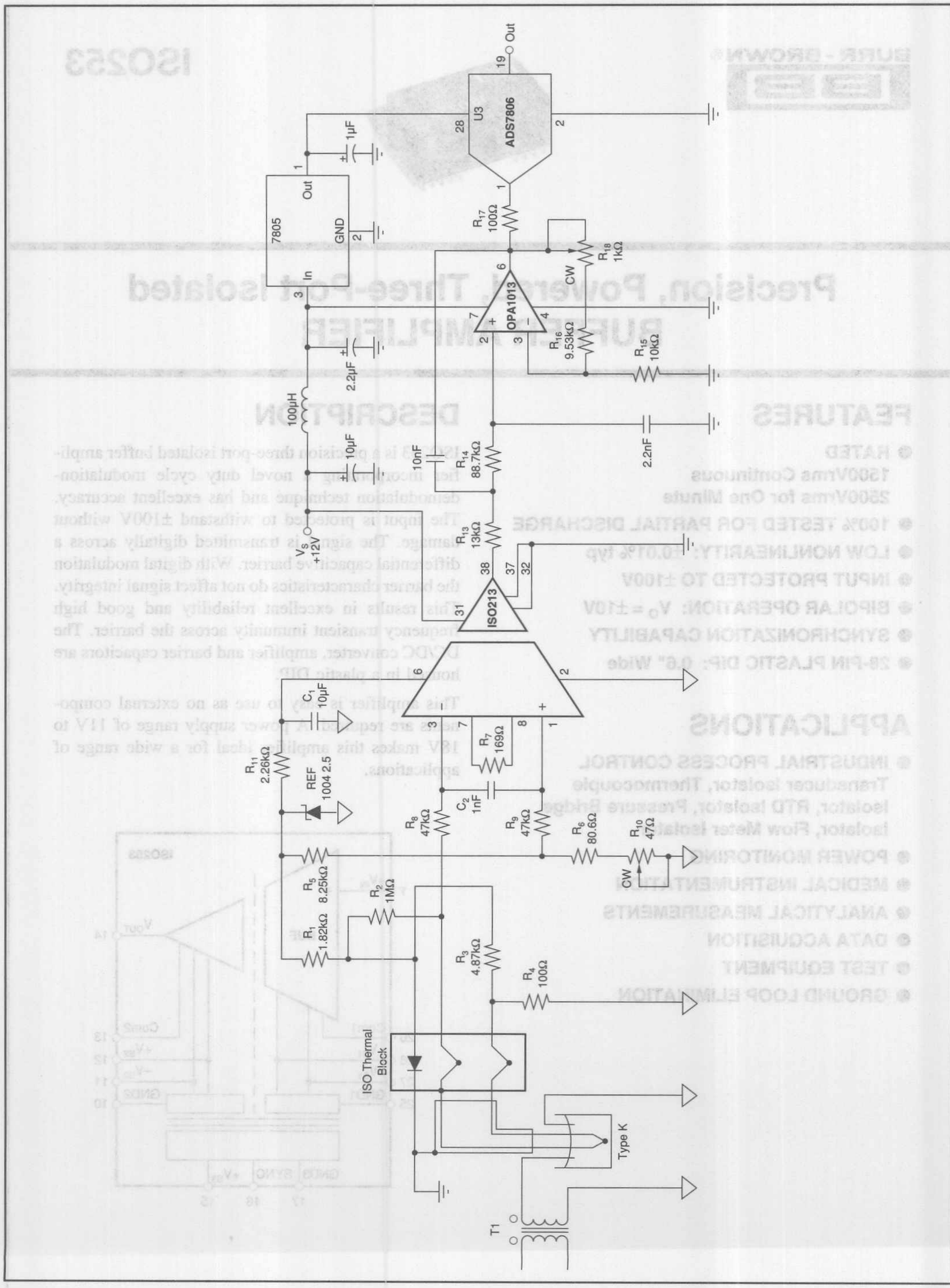


FIGURE 15. Complete Temperature Acquisition System.

ISOLATION PRODUCTS 5 ISO213

BURR - BROWN®

ISO253

Precision, Powered, Three-Port Isolated BUFFER AMPLIFIER

FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
- 100% TESTED FOR PARTIAL DISCHARGE
- LOW NONLINEARITY: ±0.01% typ
- INPUT PROTECTED TO ±100V
- BIPOLAR OPERATION: $V_O = \pm 10V$
- SYNCHRONIZATION CAPABILITY
- 28-PIN PLASTIC DIP: 0.6" Wide

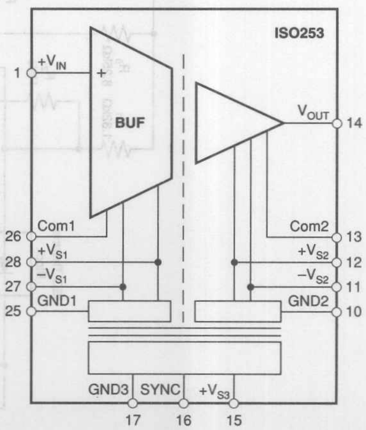
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- GROUND LOOP ELIMINATION

DESCRIPTION

ISO253 is a precision three-port isolated buffer amplifier incorporating a novel duty cycle modulation-demodulation technique and has excellent accuracy. The input is protected to withstand ±100V without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. The DC/DC converter, amplifier and barrier capacitors are housed in a plastic DIP.

This amplifier is easy to use as no external components are required. A power supply range of 11V to 18V makes this amplifier ideal for a wide range of applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25°C$, $V_{S3} = 15V$, $R_L = 2k\Omega$, and 220nF capacitors on all generated supplies, unless otherwise noted.

PARAMETER	CONDITIONS	ISO253P MIN	TYP	MAX	UNITS
ISOLATION					
Voltage Rated Continuous:					
AC	T_{MIN} to T_{MAX}	1500			Vrms
100% Test (AC 50Hz)	1s; Partial Discharge ≤ 5pC	2500			Vrms
Rated One Min		2500			Vrms
Isolation-Mode Rejection					
DC			120		dB
AC 50Hz	1500Vrms		95		dB
Barrier Impedance			$10^{14} \parallel 2$		Ω ǁ pF
Leakage Current	VISO = 240Vrms, 50Hz		1.4	2	μArms
GAIN					
Nominal Gain			1		V/V
Gain Error			0.15	±0.3	%
Gain vs Temperature			15		ppm/°C
Nonlinearity			0.01	±0.1	%
INPUT OFFSET VOLTAGE					
Initial Offset				±100	mV
vs Temperature			150		μV/°C
vs Supply			1		mV/V
INPUT					
Voltage Range		±10	±15		V
Resistance			200		kΩ
OUTPUT					
Voltage Range		±10			V
Current Drive		±5			mA
Capacitive Load Drive			0.1		μF
Ripple Voltage			25		mVp-p
FREQUENCY RESPONSE					
Small Signal Bandwidth			50		kHz
Slew Rate			0.25		V/μs
Settling Time, 0.1%			50		μs
POWER SUPPLIES					
Rated Voltage			15		V
Voltage Range		11		18	V
Quiescent Current		25	40	55	mA
Rated Output Voltage	No Load	13	14.5		V
	50mA Load On Two Supplies	12	13.2	16	V
Load Regulation			28		mV/mA
Line Regulation			1		V/V
SYNC Frequency		1		1.4	MHz
Output Voltage Ripple			50		mV
TEMPERATURE RANGE					
Operating		–40		85	°C
Storage		–40		85	°C

ABSOLUTE MAXIMUM RATINGS

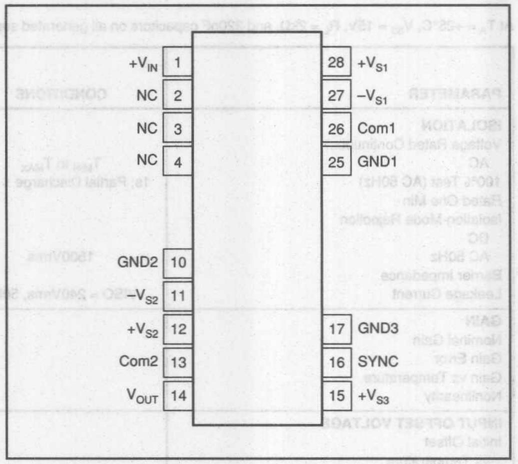
Supply Voltage	+18V
V_{IN}, Analog Input Voltage Range	±100V
Com1 to GND1	±1V
Com2 to GND2	±1V
Continuous Isolation Voltage:	1500Vrms
	2500Vrms one min
IMV, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Duration	Continuous to Common

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO253P	28-Pin Plastic DIP	335

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

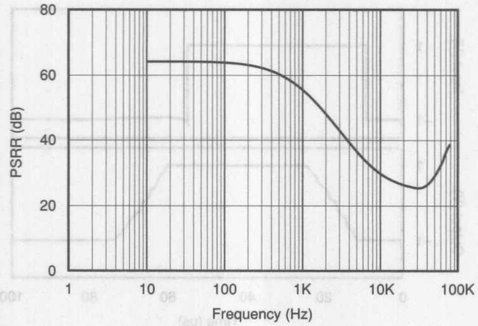
ORDERING INFORMATION

MODEL	PACKAGE
ISO253P	28-Pin Plastic DIP

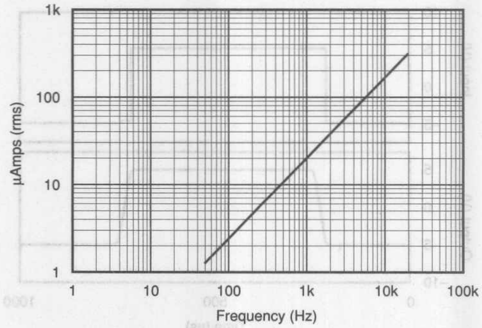
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, $+V_{S3} = 15V$, $R_L = 2k\Omega$, and 220nF capacitors on all generated supplies, unless otherwise noted.

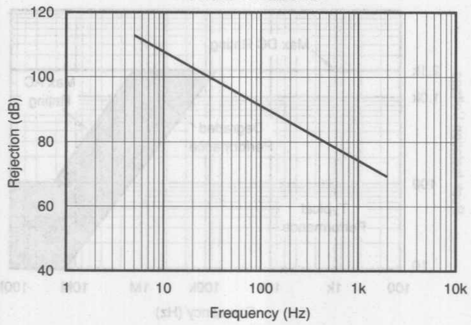
PSRR vs FREQUENCY



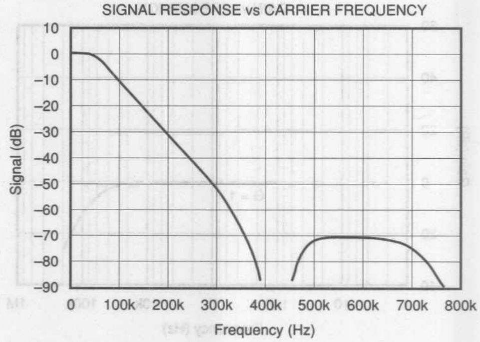
ISOLATION LEAKAGE CURRENT vs FREQUENCY
(V = 240Vrms)



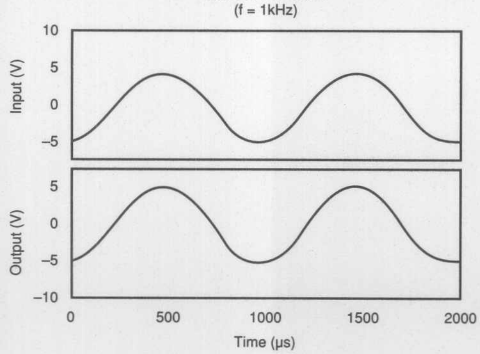
IMR vs FREQUENCY



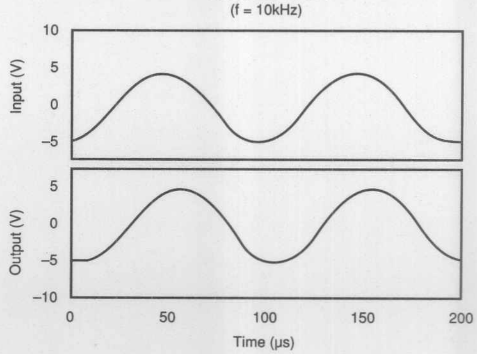
SIGNAL RESPONSE vs CARRIER FREQUENCY



SINE RESPONSE
(f = 1kHz)



SINE RESPONSE
(f = 10kHz)



ISO253

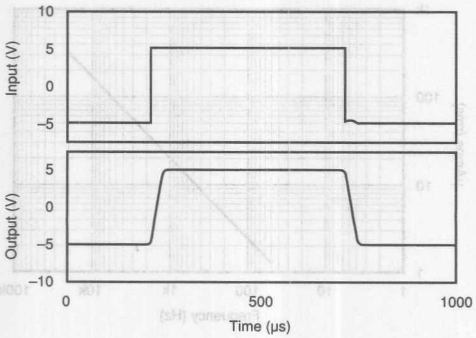
5

ISOLATION PRODUCTS

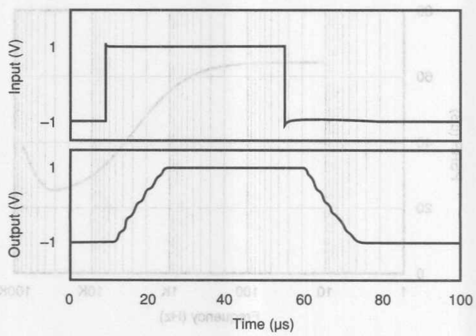
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $+V_{S3} = 15V$, $R_L = 2k\Omega$, and 220nF capacitors on all generated supplies, unless otherwise noted.

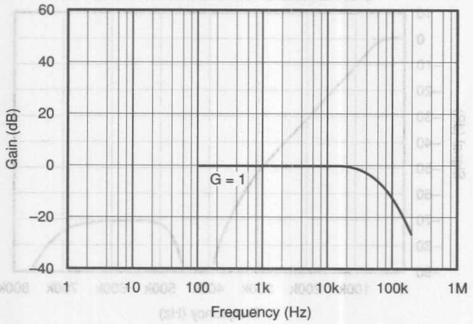
PULSE RESPONSE
(f = 1kHz)



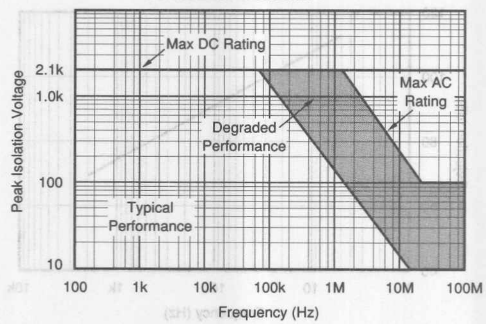
PULSE RESPONSE
(f = 10kHz)



GAIN vs FREQUENCY



ISOLATION MODE VOLTAGE
vs FREQUENCY



BASIC OPERATION

ISO253 is a precision, powered, three-port isolated buffer amplifier. The input and output sections are galvanically isolated by matched and EMI shielded capacitors built into the plastic package. The DC/DC converter input is also galvanically isolated from both the input and output supplies.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows proper power and signal connections. The power supply input pin $+V_{S3}$ should be bypassed with a 2.2µF tantalum capacitor and the outputs V_{S1} and V_{S2} with 220nF ceramic capacitors located as close to the amplifier as possible. All ground connections should be run independently to a common point. Signal Common on both input and output sections provide a high-impedance point for sensing signal ground in noisy applications. Com1 and Com2 must have a path to ground for signal current returns and should be maintained within ±1V of GND1 and GND2 respectively.

INPUT PROTECTION

The input of the buffer amplifier is protected for voltages up to ±100V. The input is a 200kΩ resistor to the summing node of the input amplifier.

DC/DC CONVERTER

ISO253 provides a reliable solution to the need for integral power. The high isolation rating being achieved by careful design and attention to the physical construction of the transformer. In addition to the high dielectric strength a low leakage coating increases the isolation voltage range. The soft start oscillator/driver design eliminates high inrush currents during turn-on. Input current sensing protects both the converter and the load from possible thermal damage during a fault condition. The DC/DC converter is synchronized to the amplifier and when multiple ISO253's are used, each channel can be synchronized via the SYNC pin.

The DC/DC converter consists of a free-running oscillator, control and switch driver circuitry, MOSFET switches, a transformer, rectifier diodes and filter capacitors all contained within the ISO253 package. The control circuitry consists of current limiting, soft start and synchronization features. In instances where several ISO253's are used in a system, beat frequencies developed between the ISO253's are a potential source of low frequency noise in the supply and ground paths. This noise may couple into the signal path and can be avoided by synchronizing the individual ISO253's together by tying the SYNC pins together or using the circuit in Figure 2 to drive the SYNC pins from an external source.

When connecting up to eight ISO253's without a driver the unit with the highest natural frequency will determine the synchronized running frequency. The SYNC pin is sensitive to capacitive loading: 150pF or less is recommended. If unused, the SYNC pin should be left open. Avoid shorting the SYNC pin directly to ground or supply potentials; otherwise damage may result.

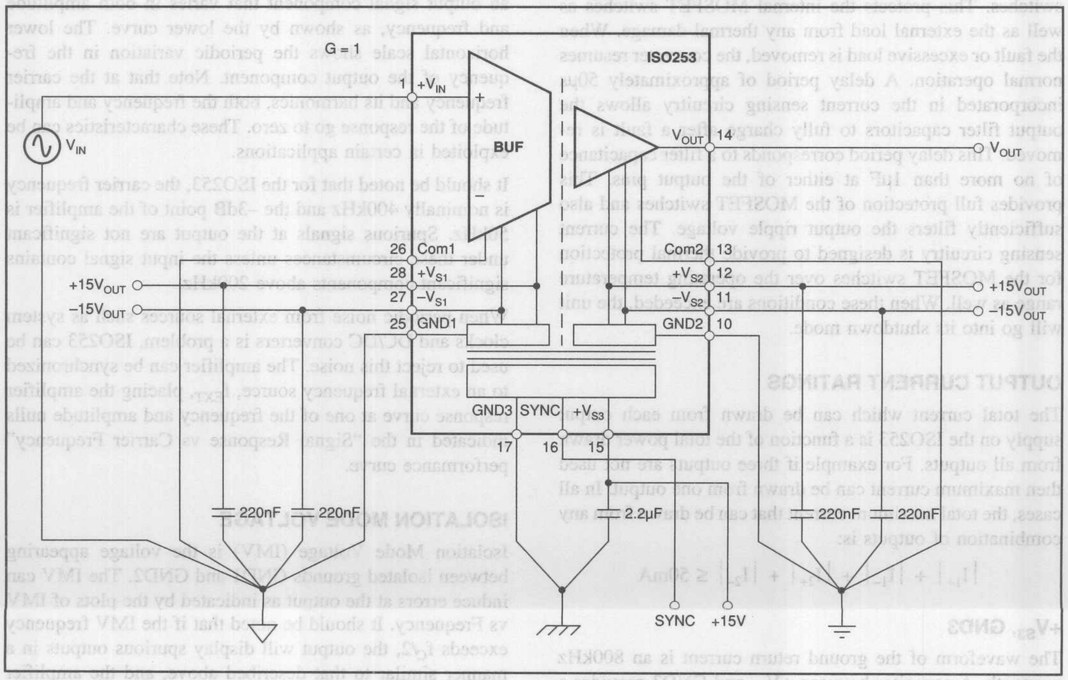


FIGURE 1. Basic Connections.

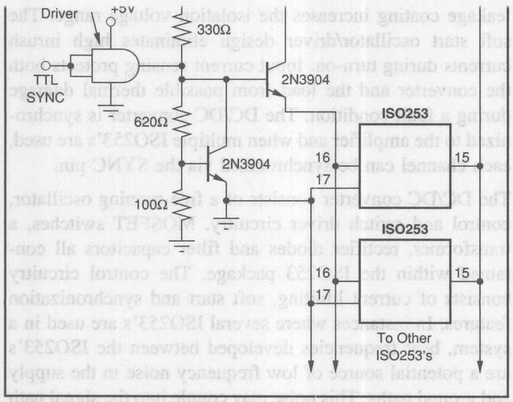


FIGURE 2. External SYNC drive.

Soft start circuitry protects the MOSFET switches during startup. This is accomplished by holding the gate-to-source voltage of both MOSFET switches low until the free-running oscillator is fully operational. In addition, soft start circuitry and input current sensing also protects the switches. This current limiting keeps the MOSFET switches operating in their safe operating area under fault conditions or excessive loads. When either of these conditions occur, the peak input current exceeds a safe limit. The result is an approximate 5% duty cycle, 300µs drive period to the MOSFET switches. This protects the internal MOSFET switches as well as the external load from any thermal damage. When the fault or excessive load is removed, the converter resumes normal operation. A delay period of approximately 50µs incorporated in the current sensing circuitry allows the output filter capacitors to fully charge after a fault is removed. This delay period corresponds to a filter capacitance of no more than 1µF at either of the output pins. This provides full protection of the MOSFET switches and also sufficiently filters the output ripple voltage. The current sensing circuitry is designed to provide thermal protection for the MOSFET switches over the operating temperature range as well. When these conditions are exceeded, the unit will go into its shutdown mode.

OUTPUT CURRENT RATINGS

The total current which can be drawn from each output supply on the ISO253 is a function of the total power drawn from all outputs. For example if three outputs are not used then maximum current can be drawn from one output. In all cases, the total maximum current that can be drawn from any combination of outputs is:

$$|I_{1+}| + |I_{1-}| + |I_{2+}| + |I_{2-}| \leq 50\text{mA}$$

$+V_{S3}$, GND3

The waveform of the ground return current is an 800kHz sawtooth. A capacitor between $+V_{S3}$ and GND3 provides a means.) Normal power down of the $+V_{S3}$ supply is not considered instantaneous. Should a rapid break in input power occur the internal transformers voltage will rapidly rise to maintain current flow and may cause internal damage to the ISO253.

SYNCHRONIZED OPERATION

ISO253 can be synchronized to an external signal source. This capability is useful in eliminating troublesome beat frequencies in multi-channel systems and in rejecting AC signals and their harmonics. To use this feature, tie all sync pins together or apply an external signal to the SYNC pin. ISO253 can be synchronized to an external oscillator over the range 1-1.4MHz (this corresponds to a modulation frequency of 500kHz to 700kHz as SYNC is internally divided by 2).

CARRIER FREQUENCY CONSIDERATIONS

ISO253 amplifiers transmit the signal across the ISO-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes more complex. The "Signal Response vs Carrier Frequency" performance curve describes this behavior graphically. The upper curve illustrates the response for input signals varying from DC to $f_C/2$. At input frequencies at or above $f_C/2$, the device generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go to zero. These characteristics can be exploited in certain applications.

It should be noted that for the ISO253, the carrier frequency is nominally 400kHz and the –3dB point of the amplifier is 50kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 200kHz.

When periodic noise from external sources such as system clocks and DC/DC converters is a problem, ISO253 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the "Signal Response vs Carrier Frequency" performance curve.

ISOLATION MODE VOLTAGE

Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds GND1 and GND2. The IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs in a manner similar to that described above, and the amplifier

Response vs Carrier Frequency" performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in "IMR vs Frequency" performance curve and compute the amplifier response to this input-referred error signal from the data given in the "Signal Response vs Carrier Frequency" performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/µs. For convenience, this is plotted in the typical performance curves for the ISO253 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/µs but falls below 20kV/µs, performance may be degraded. At rates of change above 20kV/µs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltage below 15V may decrease the dV/dT to 500V/µs for typical performance, but the maximum dV/dT of 20kV/µs remains unchanged.

Leakage current is determined solely by the impedance of the barrier and transformer capacitance and is plotted in the "Isolation Leakage Current vs Frequency" curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one.

Historically, Burr-Brown has chosen a deliberately conservative one: VTEST = (2 x ACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO253.

Partial Discharge

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. The inception voltage for these voids tends to be constant, so that the measurement of total charge being redistributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure. The bulk inception voltage, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the bulk extinction voltage provides a lower, more conservative voltage from which to derive a safe continuous rating. In production, measuring at a level somewhat below the expected inception voltage and then de-rating by a factor related to expectations about system transients is an accepted practice.

Partial Discharge Testing

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE in Germany, an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display less than or equal to 5pC partial discharge level in a 100% production test.

APPLICATIONS

The ISO253 isolation amplifiers are used in three categories of applications:

- Accurate isolation of signals from high voltage ground potentials
- Accurate isolation of signals from severe ground noise and
- Fault protection from high voltages in analog measurements

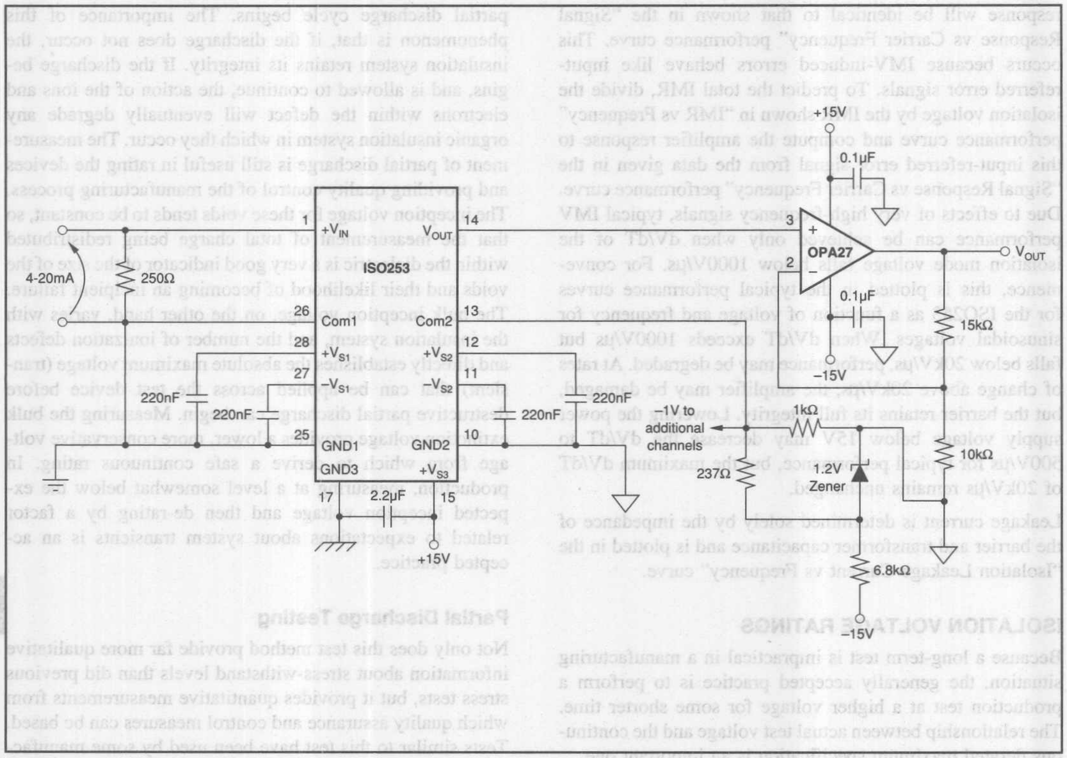


FIGURE 3. Process Current Input Isolator with Offset.

BURR - BROWN®

ISO254

Precision, Powered, Three-Port Isolated PROGRAMMABLE GAIN AMPLIFIER

FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
  100% TESTED FOR PARTIAL DISCHARGE
- PROGRAMMABLE GAINS OF 1, 10, 100, 1000
- LOW NONLINEARITY: ±0.01% typ
- LOW INPUT BIAS CURRENT: ±5nA max
- LOW INPUT OFFSET VOLTAGE: 625µV max
- INPUTS PROTECTED TO ±40V
- BIPOLAR OPERATION: $V_O = \pm 10V$
- SYNCHRONIZATION CAPABILITY
- 28-PIN PLASTIC DIP: 0.6" Wide

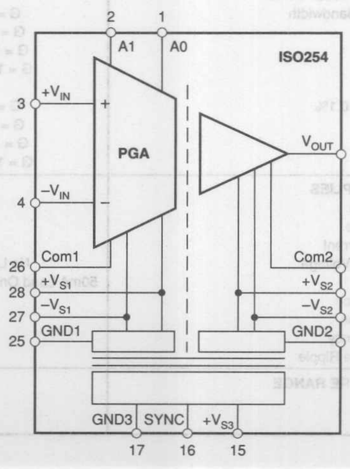
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- GROUND LOOP ELIMINATION

DESCRIPTION

ISO254 is a precision three-port isolated programmable gain instrumentation amplifier incorporating a novel duty cycle modulation-demodulation technique and has excellent accuracy. Internal input protection can withstand up to ±40V input differential without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. The DC/DC converter, amplifier and barrier capacitors are housed in a plastic DIP.

This amplifier is easy to use as no external components are required. A power supply range of 11V to 18V makes this amplifier ideal for a wide range of applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PARAMETER	CONDITIONS	ISO254P MIN	TYP	MAX	UNITS
ISOLATION					
Voltage Rated Continuous:					
AC	T_{MIN} to T_{MAX}	1500			Vrms
100% Test (AC 50Hz)	1s; Partial Discharge ≤ 5pC	2500			Vrms
Rated One Min		2500			Vrms
Isolation-Mode Rejection					
DC			120		dB
AC 50Hz	1500Vrms		95		dB
Barrier Impedance			10^{14} || 2		Ω || pF
Leakage Current	VISO = 240Vrms, 50Hz		1.4	2	µArms
GAIN					
Gain Error	G = 1		0.15	±0.3	%
	G = 10		0.15		
	G = 100		0.15	±0.3	%
	G = 1000		0.2		
Gain vs Temperature	G = 1		±15		ppm/°C
	G = 10		±15		ppm/°C
	G = 100		±15		ppm/°C
	G = 1000		±15		ppm/°C
Nonlinearity	G = 1		±0.01	±0.102	%
	G = 10		±0.01		
	G = 100		0.01	±0.104	%
	G = 1000		±0.01		
INPUT OFFSET VOLTAGE					
Initial Offset				±(0.125 +101/G)	mV
vs Temperature			±(1 + 510/G)		µV/°C
CMRR			90		dB
vs Supply			1		mV/V
INPUT					
Voltage Range		±10			V
Bias Current				±5	nA
vs Temperature			±8		pA/°C
Offset Current				±5	nA
vs Temperature			±8		pA/°C
OUTPUT					
Voltage Range		±10			V
Current Drive		±5			mA
Capacitive Load Drive			0.1		µF
Ripple Voltage			25		mVp-p
FREQUENCY RESPONSE					
Small Signal Bandwidth	G = 1		50		kHz
	G = 10		30		kHz
	G = 100		10		kHz
	G = 1000		1		kHz
Slew Rate			0.5		V/µs
Settling Time, 0.1%	G = 1		80		µs
	G = 10		380		µs
	G = 100		490		µs
	G = 1000		1650		µs
POWER SUPPLIES					
Rated Voltage			15		V
Voltage Range		11		18	V
Quiescent Current		25	40	55	mA
Rated Output Voltage	No Load	13	14.5		V
	50mA Load On Two Supplies	12	13.2	16	V
Load Regulation			35		mV/mA
Line Regulation			1		V/V
SYNC Frequency		1	1.4		MHz
Output Voltage Ripple			50		mV
TEMPERATURE RANGE					
Operating		–40		85	°C
Storage		–40		85	°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
V_{IN}, Analog Input Voltage Range	±40V
Com1 to GND1	±1V
Com2 to GND2	±1V
Continuous Isolation Voltage	1500Vrms
	2500Vrms one min
IMV, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Duration	Continuous to Common

ELECTROSTATIC DISCHARGE SENSITIVITY

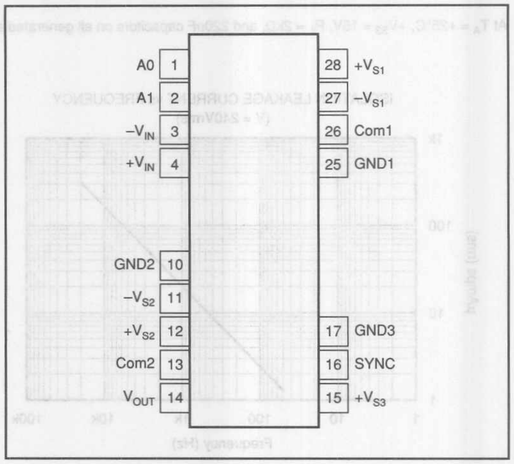
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ORDERING INFORMATION

MODEL	PACKAGE
ISO254P	28-Pin Plastic DIP

PIN CONFIGURATION



PACKAGE INFORMATION

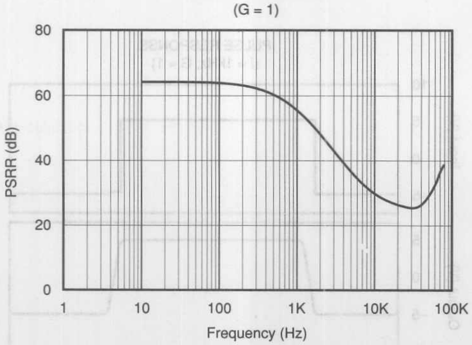
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO254P	28-Pin Plastic DIP	335

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

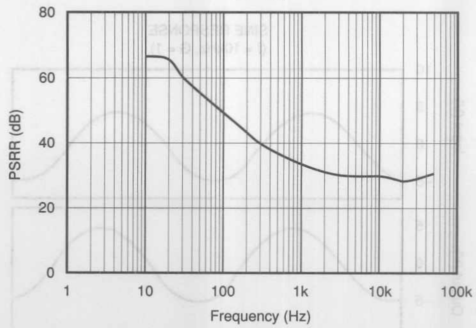
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, $+V_{S3}$ = 15V, R_L = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

PSRR vs FREQUENCY
(G = 1)

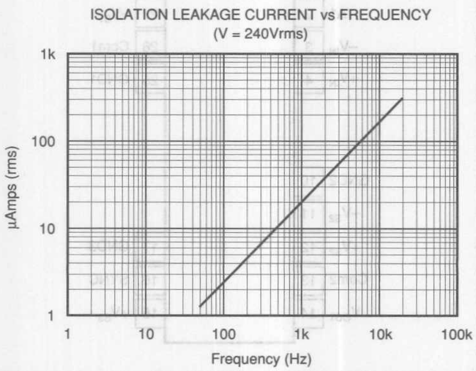


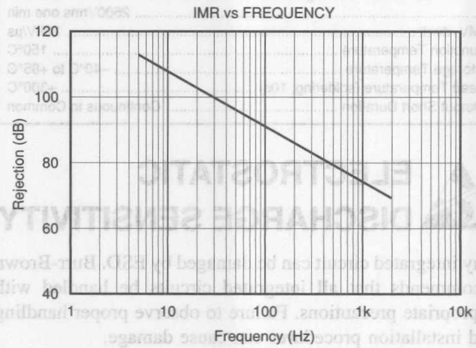
PSRR vs FREQUENCY
(G = 10)

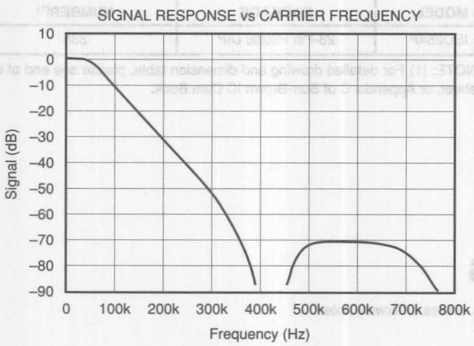


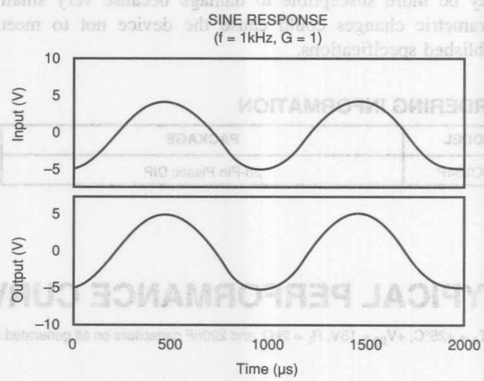
TYPICAL PERFORMANCE CURVES (CONT)

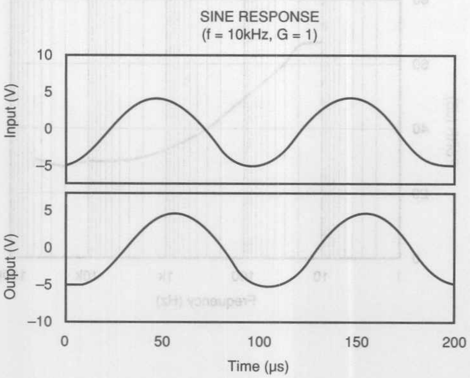
At T_A = +25°C, $+V_{S3}$ = 15V, R_L = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

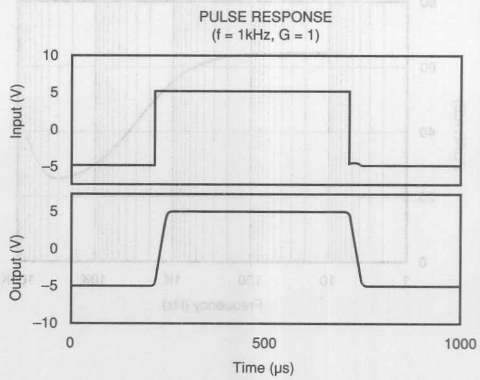








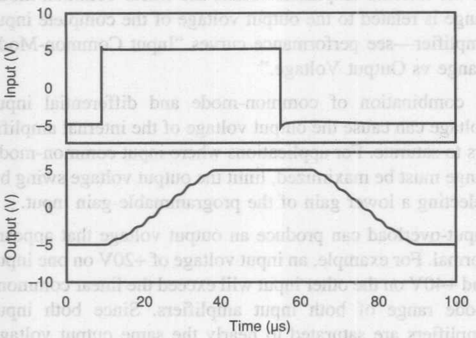




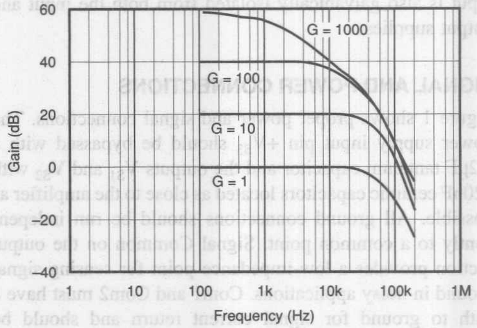
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $+V_{S3}$ = 15V, R_L = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

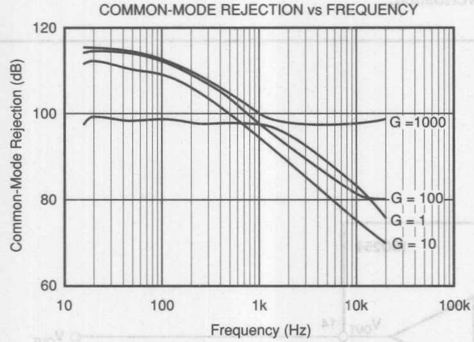
PULSE RESPONSE
(f = 10kHz, G = 1)



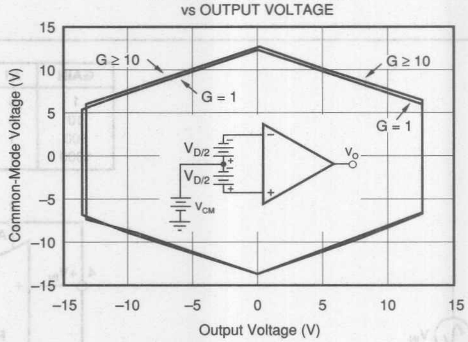
GAIN vs FREQUENCY



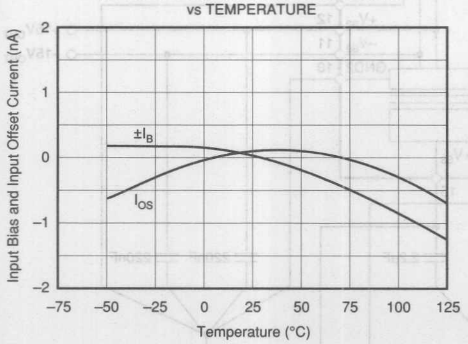
COMMON-MODE REJECTION vs FREQUENCY



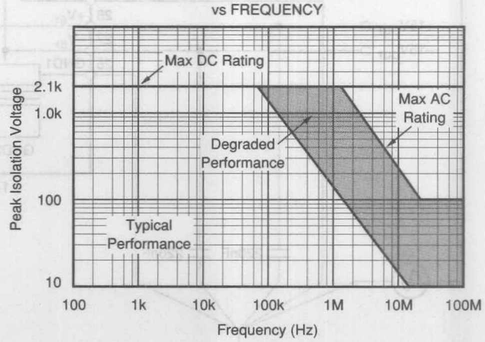
INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE



INPUT BIAS AND INPUT OFFSET CURRENT
vs TEMPERATURE



ISOLATION MODE VOLTAGE
vs FREQUENCY



mable-gain amplifier. The input and output sections are galvanically isolated by matched and EMI shielded capacitors built into the plastic package. The DC/DC converter input is also galvanically isolated from both the input and output supplies.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows proper power and signal connections. The power supply input pin $+V_{S3}$ should be bypassed with a 2.2µF tantalum capacitor and the outputs V_{S1} and V_{S2} with 220nF ceramic capacitors located as close to the amplifier as possible. All ground connections should be run independently to a common point. Signal Common on the output section provides a low-impedance point for sensing signal ground in noisy applications. Com1 and Com2 must have a path to ground for signal current return and should be maintained within ±1V of GND1 and GND2 respectively.

is approximately ±12.7V (or 2.3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the internal amplifiers. Thus, the linear common-mode range is related to the output voltage of the complete input amplifier—see performance curves "Input Common-Mode Range vs Output Voltage."

A combination of common-mode and differential input voltage can cause the output voltage of the internal amplifiers to saturate. For applications where input common-mode range must be maximized, limit the output voltage swing by selecting a lower gain of the programmable-gain input.

Input-overload can produce an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the programmable-gain amplifier will be near 0V even though both inputs are overloaded.

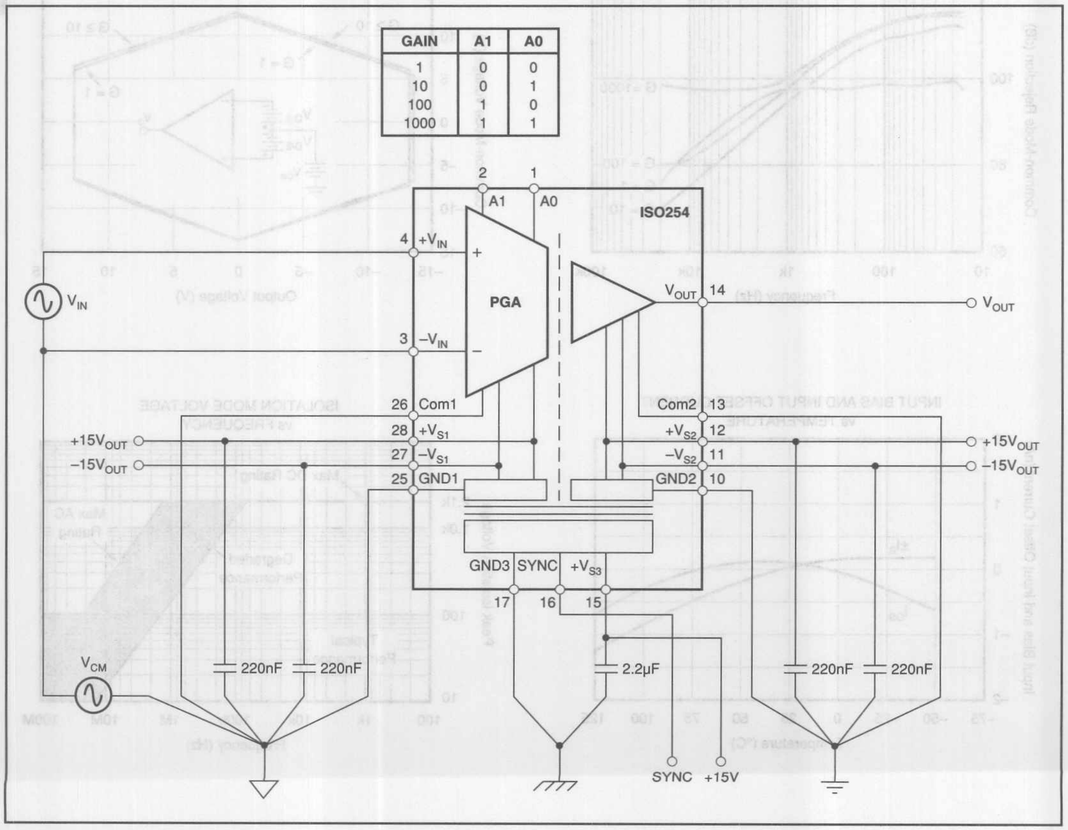


FIGURE 1. Basic Connections.

INPUT PROTECTION

The inputs of the programmable-gain amplifiers are individually protected for voltages up to ±40V. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The inputs are protected even if no power supply is present.

DC/DC CONVERTER

ISO254 provides a reliable solution to the need for integral power. The high isolation rating being achieved by careful design and attention to the physical construction of the transformer. In addition to the high dielectric strength a low leakage coating increases the isolation voltage range. The soft start oscillator/driver design eliminates high inrush currents during turn-on. Input current sensing protects both the converter and the load from possible thermal damage during a fault condition. The DC/DC converter is synchronized to the amplifier and when multiple ISO254's are used, each channel can be synchronized via the SYNC pin.

The DC/DC converter consists of a free-running oscillator, control and switch driver circuitry, MOSFET switches, a transformer, rectifier diodes and filter capacitors all contained within the ISO254 package. The control circuitry consists of current limiting, soft start and synchronization features. In instances where several ISO254's are used in a system, beat frequencies developed between the ISO254's are a potential source of low frequency noise in the supply and ground paths. This noise may couple into the signal path and can be avoided by synchronizing the individual ISO254's together by tying the SYNC pins together or using the circuit in Figure 2 to drive the SYNC pins from an external source.

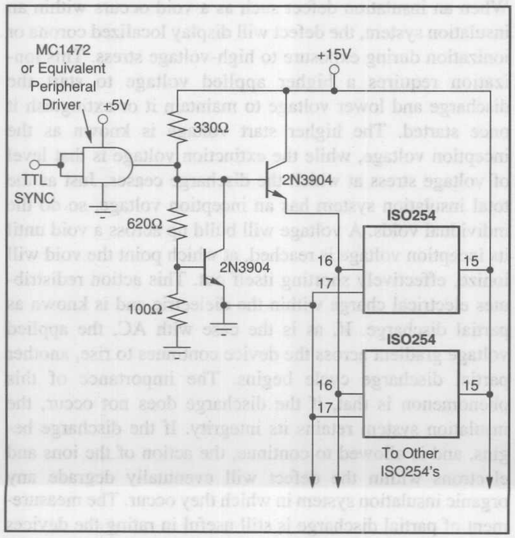


FIGURE 2. External SYNC drive.

When connecting up to eight ISO254's without a driver the unit with the highest natural frequency will determine the synchronized running frequency. The SYNC pin is sensitive to capacitive loading: 150pF or less is recommended. If unused, the SYNC pin should be left open. Avoid shorting the SYNC pin directly to ground or supply potentials; otherwise damage may result.

Soft start circuitry protects the MOSFET switches during startup. This is accomplished by holding the gate-to-source voltage of both MOSFET switches low until the free-running oscillator is fully operational. In addition, soft start circuitry and input current sensing also protects the switches. This current limiting keeps the MOSFET switches operating in their safe operating area under fault conditions or excessive loads. When either of these conditions occur, the peak input current exceeds a safe limit. The result is an approximate 5% duty cycle, 300µs drive period to the MOSFET switches. This protects the internal MOSFET switches as well as the external load from any thermal damage. When the fault or excessive load is removed, the converter resumes normal operation. A delay period of approximately 50µs incorporated in the current sensing circuitry allows the output filter capacitors to fully charge after a fault is removed. This delay period corresponds to a filter capacitance of no more than 1µf at either of the output pins. This provides full protection of the MOSFET switches and also sufficiently filters the output ripple voltage. The current sensing circuitry is designed to provide thermal protection for the MOSFET switches over the operating temperature range as well. When these conditions are exceeded, the unit will go into its shutdown mode.

OUTPUT CURRENT RATINGS

The total current which can be drawn from each output supply on the ISO254 is a function of the total power drawn from all outputs. For example if three outputs are not used then maximum current can be drawn from output. In all cases, the total maximum current that can be drawn from any combination of outputs is:

$$|I_{1+}| + |I_{1-}| + |I_{2+}| + |I_{2-}| \le 50\text{mA}$$

$+V_{S3}$, GND3

The waveform of the ground return current is an 800kHz sawtooth. A capacitor between $+V_{S3}$ and GND3 provides a bypass for the AC portion of this current. The power should never be instantaneously interrupted to the ISO254 (i.e., a break in the line to $+V_{S3}$ either by accidental or switch means.) Normal power down of the $+V_{S3}$ supply is not considered instantaneous. Should a rapid break in input power occur the internal transformers voltage will rapidly rise to maintain current flow and may cause internal damage to the ISO254.

SYNCHRONIZED OPERATION

ISO254 can be synchronized to an external signal source. This capability is useful in eliminating troublesome beat frequencies in multi-channel systems and in rejecting AC signals and their harmonics. To use this feature, tie all sync pins together or apply an external signal to the SYNC pin. ISO254 can be synchronized to an external oscillator over the range 1-1.4MHz (this corresponds to a modulation frequency of 500kHz to 700kHz as SYNC is internally divided by 2).

CARRIER FREQUENCY CONSIDERATIONS

ISO254 amplifiers transmit the signal across the ISO-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes more complex. The "Signal Response vs Carrier Frequency" performance curve describes this behavior graphically. The upper curve illustrates the response for input signals varying from DC to $f_C/2$. At input frequencies at or above $f_C/2$, the device generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go to zero. These characteristics can be exploited in certain applications.

It should be noted that for the ISO254, the carrier frequency is nominally 400kHz and the –3dB point of the amplifier is 50kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 200kHz.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO254 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the "Signal Response vs Carrier Frequency" performance curve.

ISOLATION MODE VOLTAGE

Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds GND1 and GND2. The IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs in a manner similar to that described above, and the amplifier response will be identical to that shown in the "Signal Response vs Carrier Frequency" performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in "IMR vs Frequency" performance curve and compute the amplifier response to this input-referred error signal from the data given in the "Signal Response vs Carrier Frequency" performance curve.

Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/µs. For convenience, this is plotted in the typical performance curves for the ISO254 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/µs but falls below 20kV/µs, performance may be degraded. At rates of change above 20kV/µs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltage below 15V may decrease the dV/dT to 500V/µs for typical performance, but the maximum dV/dT of 20kV/µs remains unchanged.

Leakage current is determined solely by the impedance of the barrier and transformer capacitance and is plotted in the "Isolation Leakage Current vs Frequency" curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one.

Historically, Burr-Brown has chosen a deliberately conservative one: VTEST = (2 x ACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO254.

Partial Discharge

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices

and providing quality control of the manufacturing process. The inception voltage for these voids tends to be constant, so that the measurement of total charge being redistributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure. The bulk inception voltage, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the bulk extinction voltage provides a lower, more conservative voltage from which to derive a safe continuous rating. In production, measuring at a level somewhat below the expected inception voltage and then de-rating by a factor related to expectations about system transients is an accepted practice.

Partial Discharge Testing

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE in Germany, an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display less than or equal to 5pC partial discharge level in a 100% production test.

APPLICATIONS

The ISO254 isolation amplifiers are used in three categories of applications:

- Accurate isolation of signals from high voltage ground potentials
- Accurate isolation of signals from severe ground noise and
- Fault protection from high voltages in analog measurements

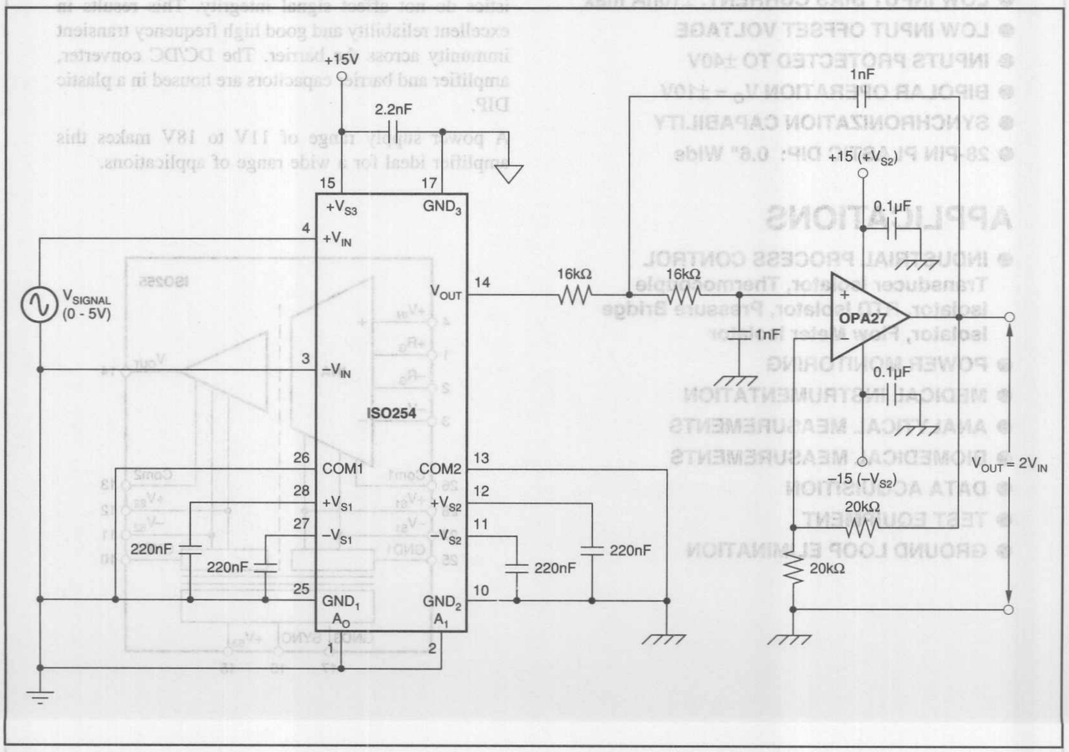


FIGURE 3. Noise Reduction in Data Acquisition System.

Precision, Powered, Three-Port Isolated INSTRUMENTATION AMPLIFIER

FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
  100% Tested for Partial Discharge
- GAINS OF 1 TO 10,000
- LOW NONLINEARITY: ±0.05% typ
- LOW INPUT BIAS CURRENT: ±10nA max
- LOW INPUT OFFSET VOLTAGE
- INPUTS PROTECTED TO ±40V
- BIPOLAR OPERATION V_O = ±10V
- SYNCHRONIZATION CAPABILITY
- 28-PIN PLASTIC DIP: 0.6" Wide

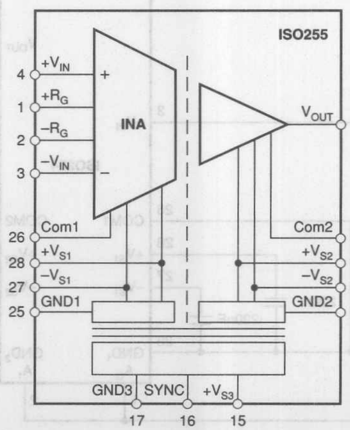
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- GROUND LOOP ELIMINATION

DESCRIPTION

ISO255 is a precision three-port isolated instrumentation amplifier incorporating a novel duty cycle modulation-demodulation technique and has excellent accuracy. Internal input protection can withstand up to ±40V input differential without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. The DC/DC converter, amplifier and barrier capacitors are housed in a plastic DIP.

A power supply range of 11V to 18V makes this amplifier ideal for a wide range of applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At $T_A = +25°C$, $V_{S3} = 15V$, $R_L = 2k\Omega$, and 220nF capacitors on all generated supplies, unless otherwise noted.

PARAMETER	CONDITIONS	ISO255P MIN	TYP	MAX	UNITS
ISOLATION					
Voltage Rated Continuous:					
AC	T_{MIN} to T_{MAX}	1500			Vrms
100% Test (AC 50Hz)	1s; Partial Discharge ≤ 5pC	2500			Vrms
Rated One Min		2500			Vrms
Isolation-Mode Rejection					
DC			120		dB
AC 50Hz	1500Vrms		95		dB
Barrier Impedance			$10^{14} \parallel 2$		Ω ∥ pF
Leakage Current	VISO = 240Vrms, 50Hz		1.4	2	μArms
GAIN					
Gain Equation			$1 + 50k\Omega/R_G$		V/V
Gain Error	G = 1		0.15	±0.35	%
	G = 10		0.15		
	G = 100		0.15	±0.95	%
	G = 1000		0.2		
Gain vs Temperature	G = 1		±50		ppm/°C
	G = 10		±50		ppm/°C
	G = 100		±50		ppm/°C
	G = 1000		±50		ppm/°C
Nonlinearity	G = 1		±0.05	±0.102	%
	G = 10		±0.05		
	G = 100		±0.05	±0.104	%
	G = 1000		±0.05		
INPUT OFFSET VOLTAGE					
Initial Offset				± (0.125 + 101/G)	mV
vs Temperature			± (1 + 520/G)		μV/°C
CMRR			90		dB
vs Supply			1		mV/V
INPUT					
Voltage Range		±10			V
Bias Current				±10	nA
vs Temperature			±40		pA/°C
Offset Current				±10	nA
vs Temperature			±40		pA/°C
OUTPUT					
Voltage Range		±10			V
Current Drive		±5			mA
Capacitive Load Drive			0.1		μF
Ripple Voltage			25		mVp-p
FREQUENCY RESPONSE					
Small Signal Bandwidth	G = 1		50		kHz
	G = 10		50		kHz
	G = 100		30		kHz
	G = 1000		4		kHz
Slew Rate	G = 10		0.2		V/μs
Settling Time, 0.1%	G = 1		20		μs
	G = 10		20		μs
	G = 100		30		μs
	G = 1000		240		μs
POWER SUPPLIES					
Rated Voltage			15		V
Voltage Range		11		18	V
Quiescent Current		25	40	55	mA
Rated Output Voltage	No Load	13	14.5		V
	50mA Load On Two Supplies	12	13.2	16	V
Load Regulation			28		mV/mA
Line Regulation			1		V/V
SYNC Frequency		1		1.4	MHz
Output Voltage Ripple			50		mV
TEMPERATURE RANGE					
Operating		–40		85	°C
Storage		–40		85	°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
V_{IN}, Analog Input Voltage Range	±40V
Com1 to GND1	±1V
Com2 to GND2	±1V
Continuous Isolation Voltage:	1500Vrms
	2500Vrms one min
IMV, dv/dt	20kV/μs
Junction Temperature	150°C
Storage Temperature	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Duration	Continuous to Common

ELECTROSTATIC DISCHARGE SENSITIVITY

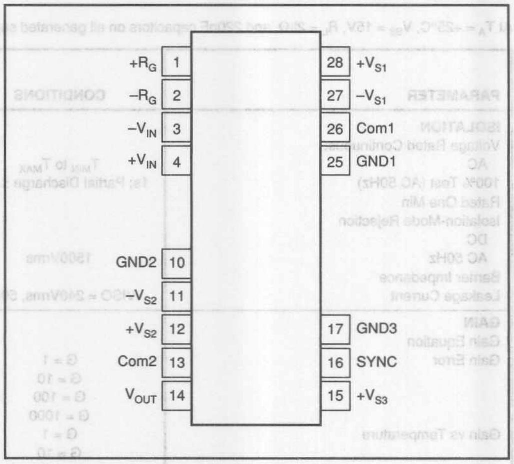
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ORDERING INFORMATION

MODEL	PACKAGE
ISO255P	28-Pin Plastic DIP

PIN CONFIGURATION



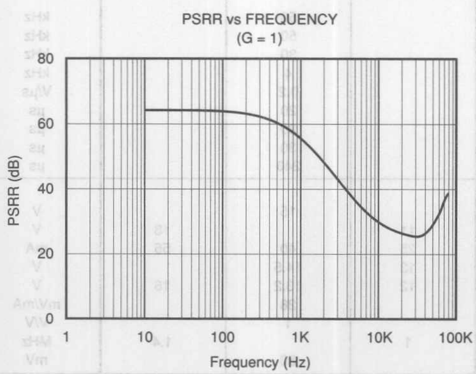
PACKAGE INFORMATION

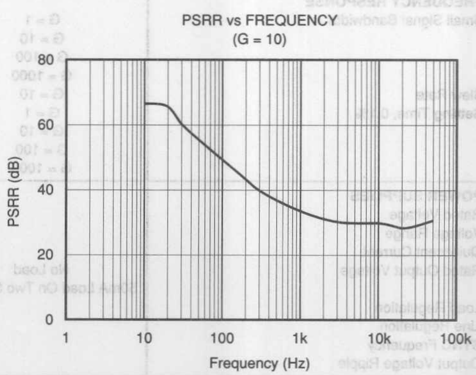
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ISO255P	28-Pin Plastic DIP	335

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

At T_A = +25°C, $+V_{S3}$ = 15V, R_L = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

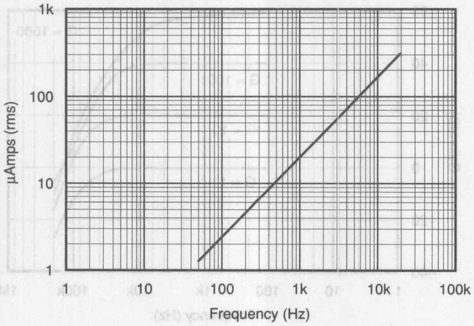




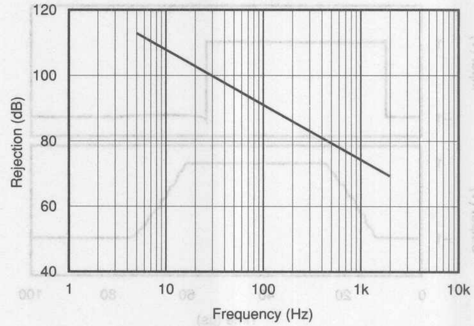
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $+V_{S3}$ = 15V, R_L = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

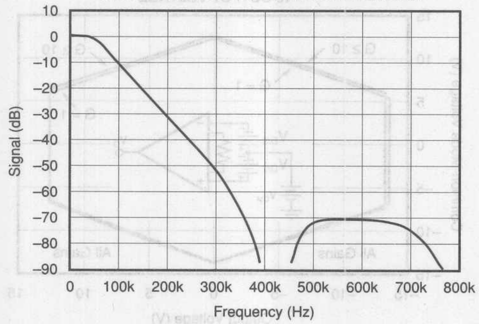
ISOLATION LEAKAGE CURRENT vs FREQUENCY
(V = 240Vrms)



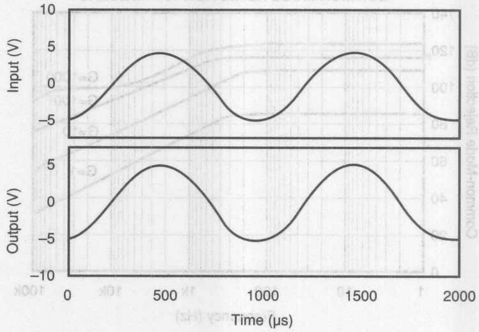
IMR vs FREQUENCY



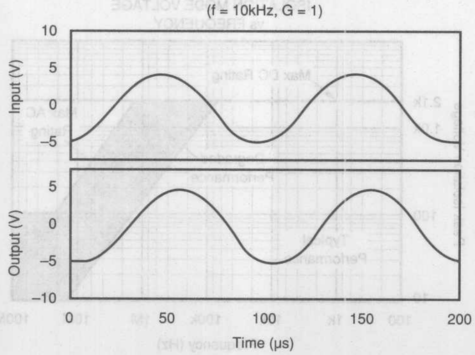
SIGNAL RESPONSE vs CARRIER FREQUENCY



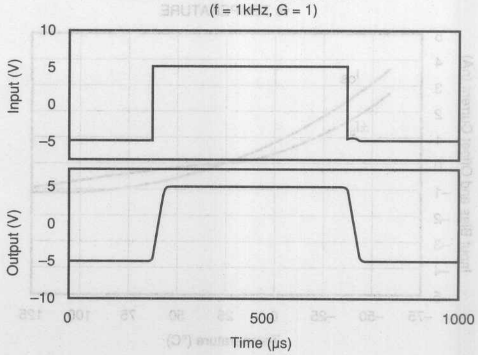
SINE RESPONSE
(f = 1kHz, G = 1)



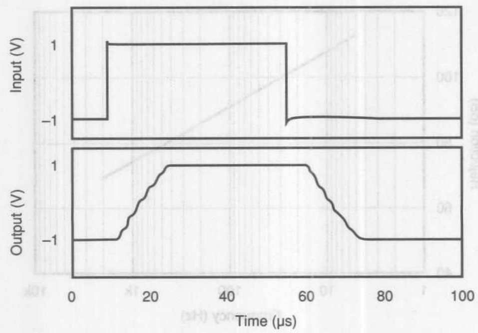
SINE RESPONSE
(f = 10kHz, G = 1)



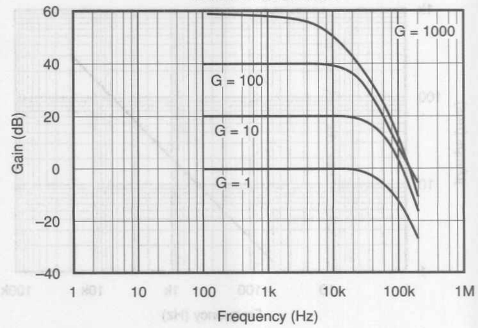
PULSE RESPONSE
(f = 1kHz, G = 1)



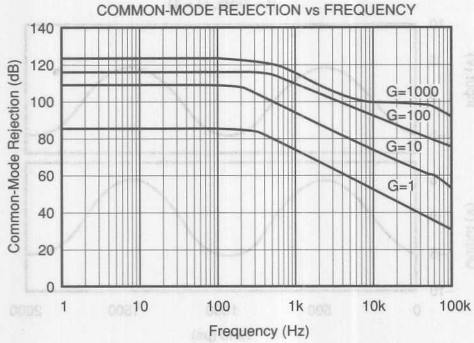
PULSE RESPONSE
(f = 10kHz, G = 1)



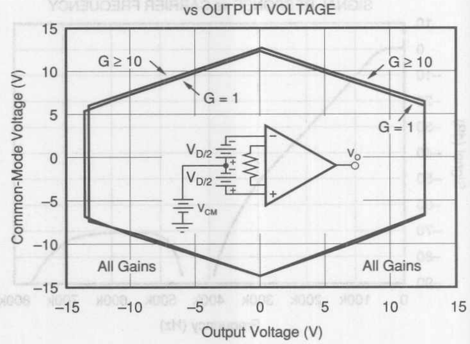
GAIN vs FREQUENCY



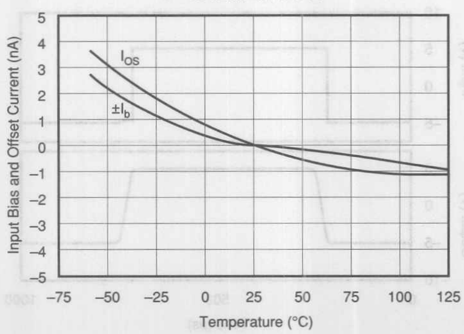
COMMON-MODE REJECTION vs FREQUENCY



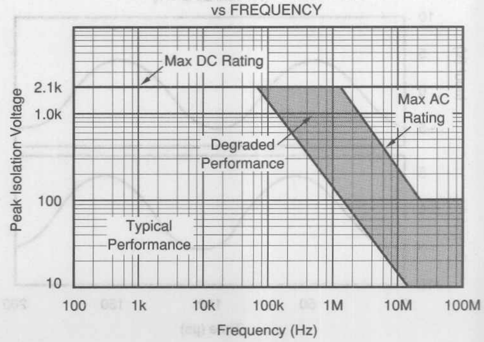
INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE



INPUT BIAS AND OFFSET CURRENT
vs TEMPERATURE



ISOLATION MODE VOLTAGE
vs FREQUENCY



ISO255 is a precision, powered, three-port isolated instrumentation amplifier. The input and output sections are galvanically isolated by matched and EMI shielded capacitors built into the plastic package. The DC/DC converter input is also galvanically isolated from both the input and output supplies.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows proper power and signal connections. The power supply input pin $+V_{S3}$ should be bypassed with a 2.2µF tantalum capacitor and the outputs V_{S1} and V_{S2} with 220nF ceramic capacitors located as close to the amplifier as possible. All ground connections should be run independently to a common point. Signal Common on the input section provides a low-impedance point for sensing signal ground in noisy applications. Com1 and Com2 must have a path to ground for signal current return and should be maintained within ±1V of GND1 and GND2 respectively.

SETTING THE GAIN

Gain of the ISO255 is set by a single external resistor, R_G, connected between pins 1 and 2:

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

The 50kΩ term in Equation 1 comes from the sum of the two absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the ISO255.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input circuitry of the ISO255 is approximately ±14V (or 1V from the power supplies). As the output voltage increases.

However, the linear input range will be limited by the output voltage swing of the internal amplifiers. Thus, the linear common-mode range is related to the output voltage of the complete input amplifier—see performance curves "Input Common-Mode Range vs Output Voltage."

A combination of common-mode and differential input voltage can cause the output voltage of the internal amplifiers to saturate. For applications where input common-mode range must be maximized, limit the output voltage swing by selecting a lower input gain.

Input-overload can produce an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the instrumentation amplifier will be near 0V even though both inputs are overloaded.

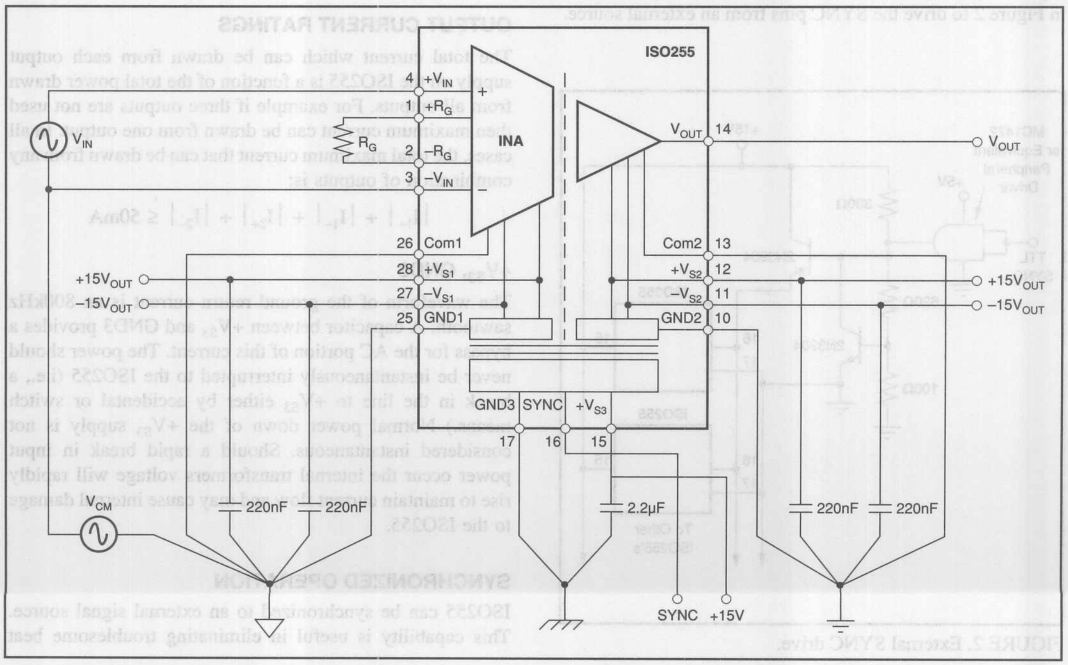


FIGURE 1. Basic Connections.

INPUT PROTECTION

The inputs of the amplifier are individually protected for voltages up to ±40V. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The inputs are protected even if no power supply is present.

DC/DC CONVERTER

ISO255 provides a reliable solution to the need for integral power. The high isolation rating being achieved by careful design and attention to the physical construction of the transformer. In addition to the high dielectric strength a low leakage coating increases the isolation voltage range. The soft start oscillator/driver design eliminates high inrush currents during turn-on. Input current sensing protects both the converter and the load from possible thermal damage during a fault condition. The DC/DC converter is synchronized to the amplifier and when multiple ISO255's are used, each channel can be synchronized via the SYNC pin.

The DC/DC converter consists of a free-running oscillator, control and switch driver circuitry, MOSFET switches, a transformer, rectifier diodes and filter capacitors all contained within the ISO255 package. The control circuitry consists of current limiting, soft start and synchronization features. In instances where several ISO255's are used in a system, beat frequencies developed between the ISO255's are a potential source of low frequency noise in the supply and ground paths. This noise may couple into the signal path and can be avoided by synchronizing the individual ISO255's together by tying the SYNC pins together or using the circuit in Figure 2 to drive the SYNC pins from an external source.

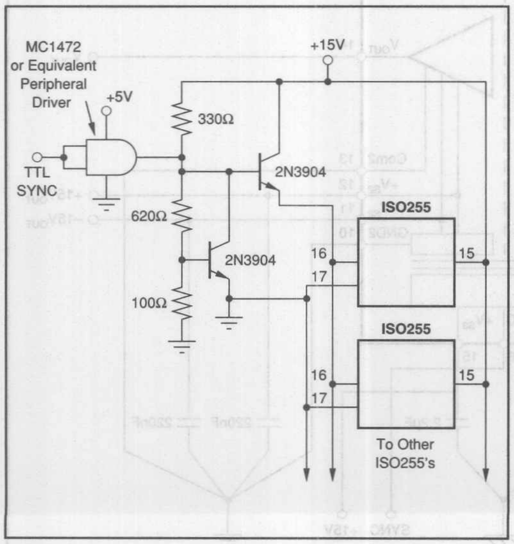


FIGURE 2. External SYNC drive.

When connecting up to eight ISO255's without a driver the unit with the highest natural frequency will determine the synchronized running frequency. The SYNC pin is sensitive to capacitive loading: 150pF or less is recommended. If unused, the SYNC pin should be left open. Avoid shorting the SYNC pin directly to ground or supply potentials; otherwise damage may result.

Soft start circuitry protects the MOSFET switches during startup. This is accomplished by holding the gate-to-source voltage of both MOSFET switches low until the free-running oscillator is fully operational. In addition, soft start circuitry and input current sensing also protects the switches. This current limiting keeps the MOSFET switches operating in their safe operating area under fault conditions or excessive loads. When either of these conditions occur, the peak input current exceeds a safe limit. The result is an approximate 5% duty cycle, 300μs drive period to the MOSFET switches. This protects the internal MOSFET switches as well as the external load from any thermal damage. When the fault or excessive load is removed, the converter resumes normal operation. A delay period of approximately 50μs incorporated in the current sensing circuitry allows the output filter capacitors to fully charge after a fault is removed. This delay period corresponds to a filter capacitance of no more than 1μF at either of the output pins. This provides full protection of the MOSFET switches and also sufficiently filters the output ripple voltage. The current sensing circuitry is designed to provide thermal protection for the MOSFET switches over the operating temperature range as well. When these conditions are exceeded, the unit will go into its shutdown mode.

OUTPUT CURRENT RATINGS

The total current which can be drawn from each output supply on the ISO255 is a function of the total power drawn from all outputs. For example if three outputs are not used then maximum current can be drawn from one output. In all cases, the total maximum current that can be drawn from any combination of outputs is:

$$|I_{1+}| + |I_{1-}| + |I_{2+}| + |I_{2-}| \leq 50\text{mA}$$

$+V_{S3}$, GND3

The waveform of the ground return current is an 800kHz sawtooth. A capacitor between $+V_{S3}$ and GND3 provides a bypass for the AC portion of this current. The power should never be instantaneously interrupted to the ISO255 (i.e., a break in the line to $+V_{S3}$ either by accidental or switch means.) Normal power down of the $+V_{S3}$ supply is not considered instantaneous. Should a rapid break in input power occur the internal transformers voltage will rapidly rise to maintain current flow and may cause internal damage to the ISO255.

SYNCHRONIZED OPERATION

ISO255 can be synchronized to an external signal source. This capability is useful in eliminating troublesome beat

frequencies in multi-channel systems and in rejecting AC signals and their harmonics. To use this feature, tie all sync pins together or apply an external signal to the SYNC pin. ISO255 can be synchronized to an external oscillator over the range 1-1.4MHz (this corresponds to a modulation frequency of 500kHz to 700kHz as SYNC is internally divided by 2).

CARRIER FREQUENCY CONSIDERATIONS

ISO255 amplifiers transmit the signal across the ISO-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes more complex. The "Signal Response vs Carrier Frequency" performance curve describes this behavior graphically.

It should be noted that for the ISO255, the carrier frequency is nominally 400kHz and the –3dB point of the amplifier is 60kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 200kHz.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO255 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the "Signal Response vs Carrier Frequency" performance curve.

ISOLATION MODE VOLTAGE

Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds GND1 and GND2. IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs, and the amplifier response will be identical to that shown in the "Signal Response vs Carrier Frequency" performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in "IMR vs Frequency" performance curve and compute the amplifier response to this input-referred error signal from the data given in the "Signal Response vs Carrier Frequency" performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/µs. For convenience, this is plotted in the typical performance curves for the ISO255 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/µs but falls below 20kV/µs, performance may be degraded. At rates of change above 20kV/µs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltage below 15V may decrease the dV/dT to 500V/µs for typical performance, but the maximum dV/dT of 20kV/µs remains unchanged.

Leakage current is determined solely by the impedance of the barrier and transformer capacitance and is plotted in the "Isolation Leakage Current vs Frequency" curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one.

Historically, Burr-Brown has chosen a deliberately conservative one: VTEST = (2 x ACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO255.

Partial Discharge

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. The inception voltage for these voids tends to be constant, so that the measurement of total charge being redistributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure. The bulk inception voltage, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the bulk

extinction voltage provides a lower, more conservative voltage from which to derive a safe continuous rating. In production, measuring at a level somewhat below the expected inception voltage and then de-rating by a factor related to expectations about system transients is an accepted practice.

Partial Discharge Testing

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE in Germany, an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display less than or equal to 5pC partial discharge level in a 100% production test.

APPLICATIONS

The ISO255 isolation amplifiers are used in three categories of applications:

- Accurate isolation of signals from high voltage ground potentials
- Accurate isolation of signals from severe ground noise and
- Fault protection from high voltages in analog measurements

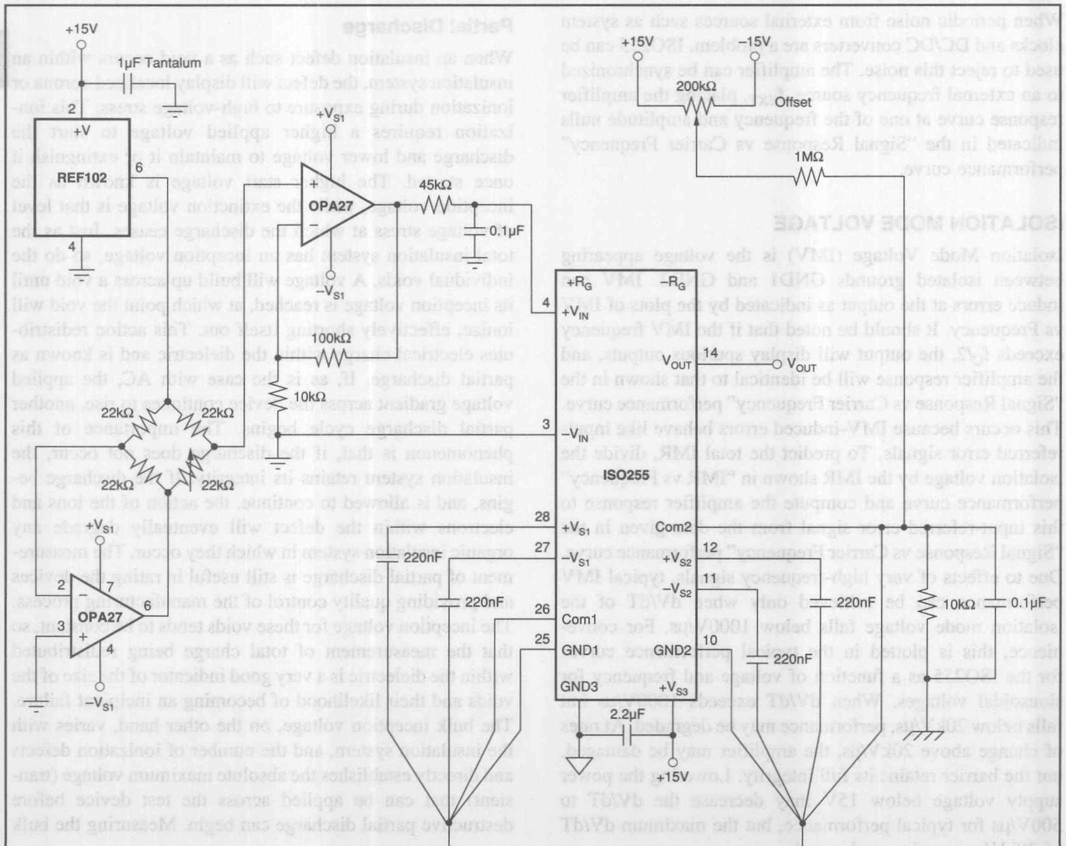


FIGURE 3. Conditioning a Bridge Circuit.

Precision, Powered, Three-Port Isolated OPERATIONAL AMPLIFIER

FEATURES

- RATED
  1500Vrms Continuous
  2500Vrms for One Minute
- 100% TESTED FOR PARTIAL DISCHARGE
- LOW NONLINEARITY: ±0.05% typ
- LOW INPUT BIAS CURRENT: ±5nA max
- INPUTS PROTECTED TO ±30V
- BIPOLAR OPERATION V_O = ±10V
- SYNCHRONIZATION CAPABILITY
- 28-PIN PLASTIC DIP: 0.6" Wide

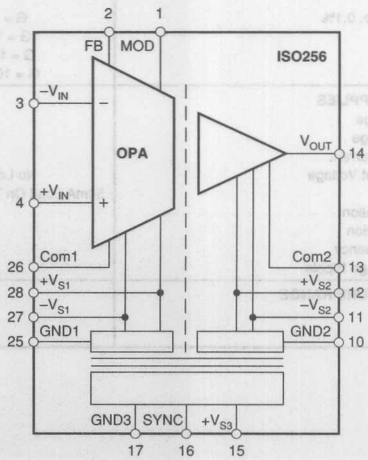
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- POWER MONITORING
- MEDICAL INSTRUMENTATION
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT
- GROUND LOOP ELIMINATION

DESCRIPTION

ISO256 is a precision three-port isolation operational amplifier incorporating an uncommitted operational amplifier for input conditioning and a novel duty cycle modulation-demodulation technique which has excellent accuracy. Internal input protection can withstand up to ±30V input differential without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. The DC/DC converter, amplifier and barrier capacitors are housed in a plastic DIP.

A power supply range of 11V to 18V makes this amplifier ideal for a wide range of applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

BURR-BROWN®
PDS-1311B

SPECIFICATIONS

At T_A = +25°C, V_{S3} = 15V, R_L = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

PARAMETER	CONDITIONS	ISO256P MIN	ISO256P TYP	ISO256P MAX	UNITS
ISOLATION					
Voltage Rated Continuous:					
AC	T_{MIN} to T_{MAX}	1500			Vrms
100% Test (AC 50Hz)	1s; Partial Discharge ≤ 5pC	2500			Vrms
Rated One Minute		2500			Vrms
Isolation-Mode Rejection					
DC			120		dB
AC 50Hz	1500Vrms		95		dB
Barrier Impedance			10^{14} || 2		Ω || pF
Leakage Current	VISO = 240Vrms, 50Hz		1.4	2	µArms
GAIN ISO AMP					
Gain Error	G = 1		0.15	±0.3	%
Gain vs Temperature	G = 1		±50		ppm/°C
Nonlinearity	G = 1		0.046	±0.1	%
INPUT OFFSET VOLTAGE OP AMP					
Initial Offset			60		µV
vs Temperature			± 1.2		µV/°C
vs Supply			3		µV/V
CMRR			115		dB
INPUT OP AMP					
Voltage Range		±10			V
Bias Current				±5	nA
vs Temperature			±60		pA/°C
Offset Current				±5	nA
vs Temperature			±85		pA/°C
INPUT ISO AMP					
Initial Offset			±50	±100	mV
vs Supply			1		mV/V
Input Resistance			200		kΩ
OUTPUT ISO AMP					
Voltage Range		±10			V
Current Drive		±5			mA
Capacitive Load Drive			0.1		µF
Ripple Voltage			10		mVp-p
FREQUENCY RESPONSE					
Small Signal Bandwidth	G = 1		20		kHz
	G = 10		20		kHz
	G = 100		4		kHz
	G = 1000		7		kHz
Slew Rate			0.2		V/µs
Settling Time, 0.1%	G = 1		100		µs
	G = 10		400		µs
	G = 100		600		µs
	G = 1000		950		µs
POWER SUPPLIES					
Rated Voltage			15		V
Voltage Range		11		18	V
Quiescent Current		25	40	55	mA
Rated Output Voltage	No Load	13	14.5		V
	50mA Load On Two Supplies	12	13.2	16	V
Load Regulation			28		mV/mA
Line Regulation			1		V/V
SYNC Frequency			1 to 1.4		MHz
Output Voltage Ripple			50		mV
TEMPERATURE RANGE					
Operating		–40		85	°C
Storage		–40		85	°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
V_{IN}, Analog Input Voltage Range	±40V
Com1 to GND1	±1V
Com2 to GND2	±1V
Continuous Isolation Voltage:	1500Vrms
	2500Vrms one min
IMV, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Duration	Continuous to Common

ELECTROSTATIC DISCHARGE SENSITIVITY

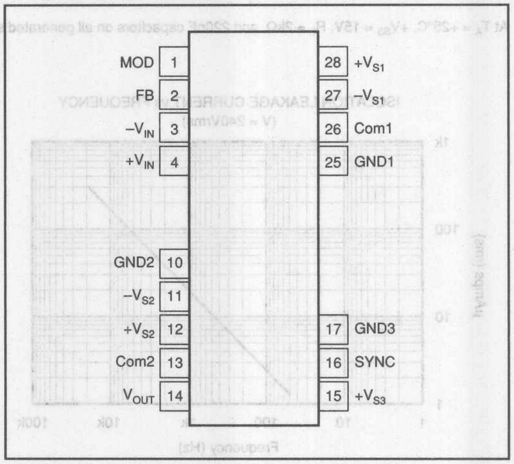
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ORDERING INFORMATION

MODEL	PACKAGE
ISO256P	28-Pin Plastic DIP

PIN CONFIGURATION



PACKAGE INFORMATION

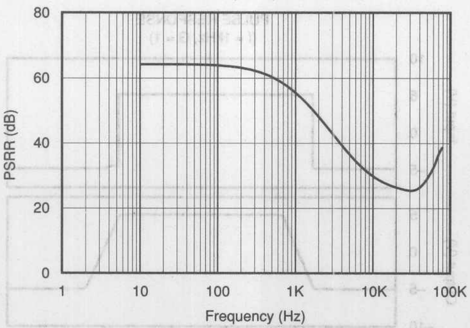
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[(1)]
ISO256P	28-Pin Plastic DIP	335

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

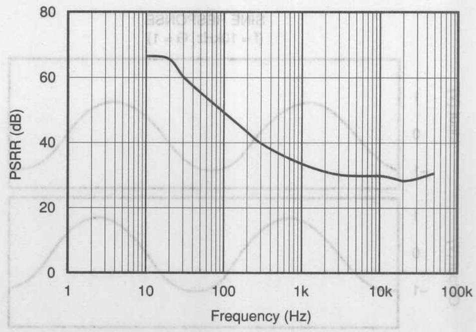
TYPICAL PERFORMANCE CURVES

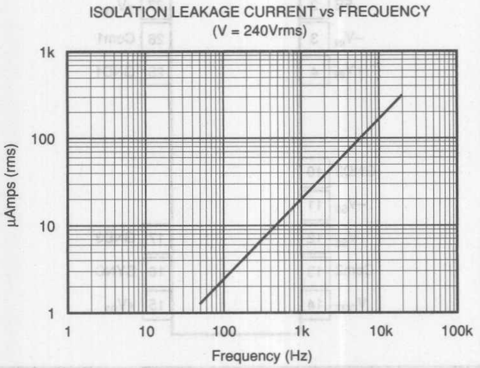
At T_A = +25°C, $+V_{S3}$ = 15V, R_L = 2kΩ, and 220nF capacitors on all generated supplies, unless otherwise noted.

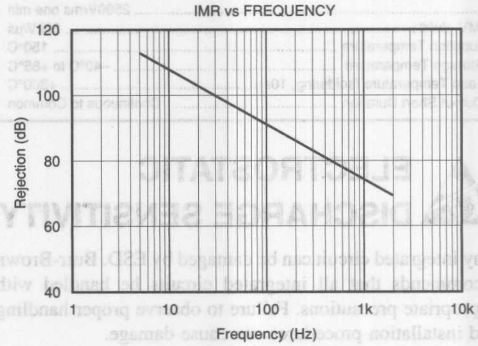
PSRR vs FREQUENCY
(G = 1)

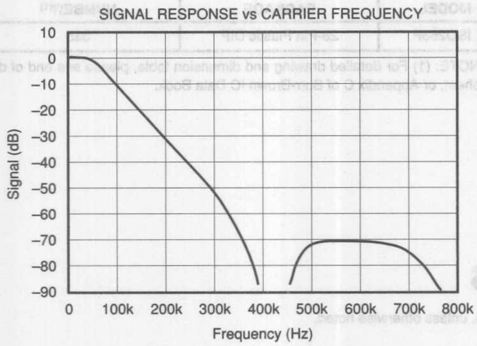


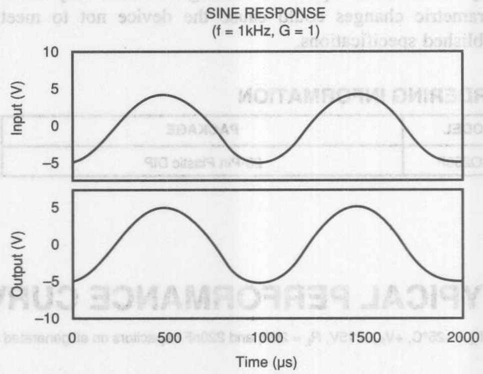
PSRR vs FREQUENCY
(G = 10)

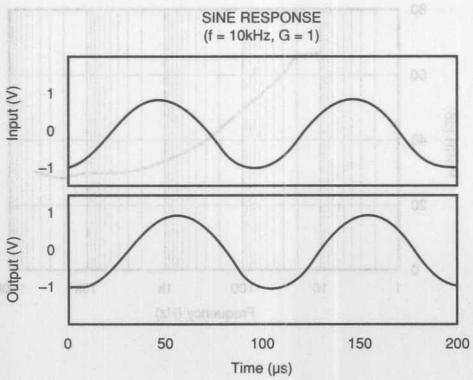


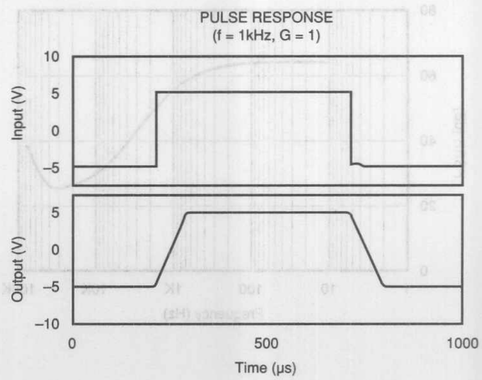

ISOLATION LEAKAGE CURRENT vs FREQUENCY
(V = 240Vrms)
µAmps (rms)
1k
100
10
1
1
10
100
1k
10k
100k
Frequency (Hz)


IMR vs FREQUENCY
Rejection (dB)
120
100
80
60
40
1
10
100
1k
10k
Frequency (Hz)


SIGNAL RESPONSE vs CARRIER FREQUENCY
Signal (dB)
10
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
0
100k
200k
300k
400k
500k
600k
700k
800k
Frequency (Hz)

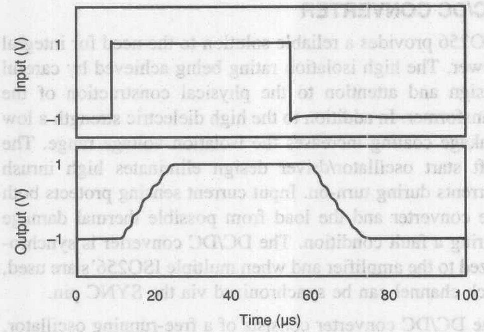

SINE RESPONSE
(f = 1kHz, G = 1)
Input (V)
10
5
0
−5
Output (V)
5
0
−5
−10
0
500
1000
1500
2000
Time (µs)


SINE RESPONSE
(f = 10kHz, G = 1)
Input (V)
1
0
−1
Output (V)
1
0
−1
0
50
100
150
200
Time (µs)

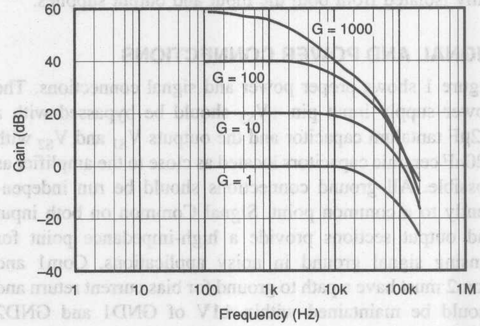

PULSE RESPONSE
(f = 1kHz, G = 1)
Input (V)
10
5
0
−5
Output (V)
5
0
−5
−10
0
500
1000
Time (µs)

At $T_A = +25°C$, $+V_{S3} = 15V$, $R_L = 2k\Omega$, and 220nF capacitors on all generated supplies, unless otherwise noted.

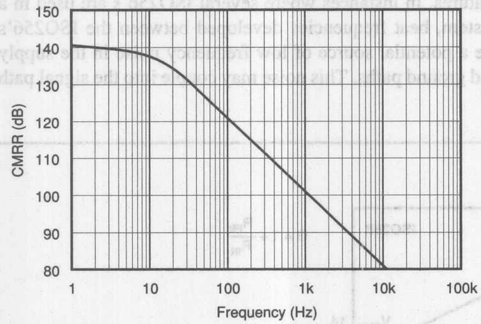
PULSE RESPONSE
(f = 10kHz, G = 1)



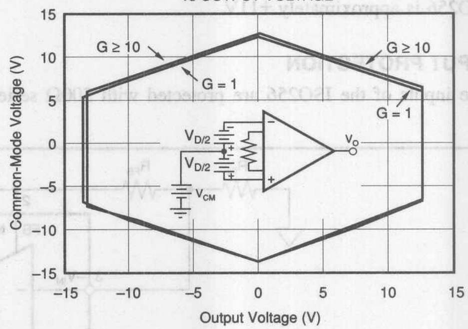
GAIN vs FREQUENCY



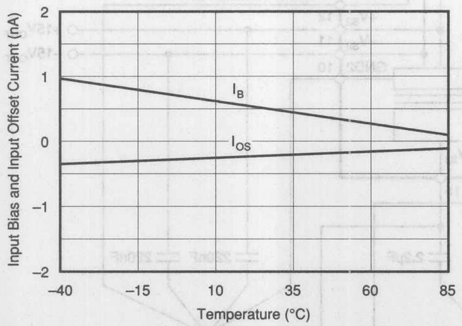
CMRR vs FREQUENCY



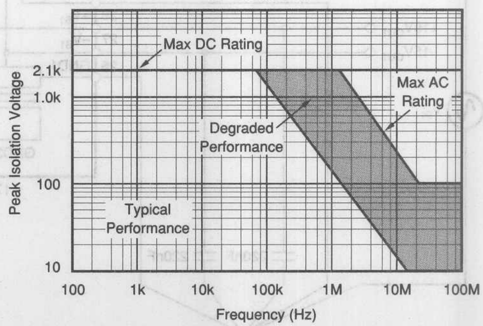
INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE



INPUT BIAS AND INPUT OFFSET CURRENT
vs TEMPERATURE



ISOLATION MODE VOLTAGE
vs FREQUENCY



BASIC OPERATION

ISO256 is a precision, powered, three-port isolated amplifier. The input and output sections are galvanically isolated by matched and EMI shielded capacitors built into the plastic package. The DC/DC converter input is also galvanically isolated from both the input and output supplies.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows proper power and signal connections. The power supply input pin $+V_{S3}$ should be bypassed with a 2.2µF tantalum capacitor and the outputs V_{S1} and V_{S2} with 220nF ceramic capacitors located as close to the amplifier as possible. All ground connections should be run independently to a common point. Signal Common on both input and output sections provide a high-impedance point for sensing signal ground in noisy applications. Com1 and Com2 must have a path to ground for bias current return and should be maintained within ±1V of GND1 and GND2 respectively.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input circuitry of the ISO256 is approximately ±11V.

INPUT PROTECTION

The inputs of the ISO256 are protected with 500Ω series resistors and diode clamps. The inputs can withstand ±30V differential inputs without damage. The protection diodes will of course conduct current when the inputs are overdriven. This may disturb the slewing rate in unity gain follower applications, but will not damage the op-amp.

DC/DC CONVERTER

ISO256 provides a reliable solution to the need for integral power. The high isolation rating being achieved by careful design and attention to the physical construction of the transformer. In addition to the high dielectric strength a low leakage coating increases the isolation voltage range. The soft start oscillator/driver design eliminates high inrush currents during turn-on. Input current sensing protects both the converter and the load from possible thermal damage during a fault condition. The DC/DC converter is synchronized to the amplifier and when multiple ISO256's are used, each channel can be synchronized via the SYNC pin.

The DC/DC converter consists of a free-running oscillator, control and switch driver circuitry, MOSFET switches, a transformer, rectifier diodes and filter capacitors all contained within the ISO256 package. The control circuitry consists of current limiting, soft start and synchronization features. In instances where several ISO256's are used in a system, beat frequencies developed between the ISO256's are a potential source of low frequency noise in the supply and ground paths. This noise may couple into the signal path

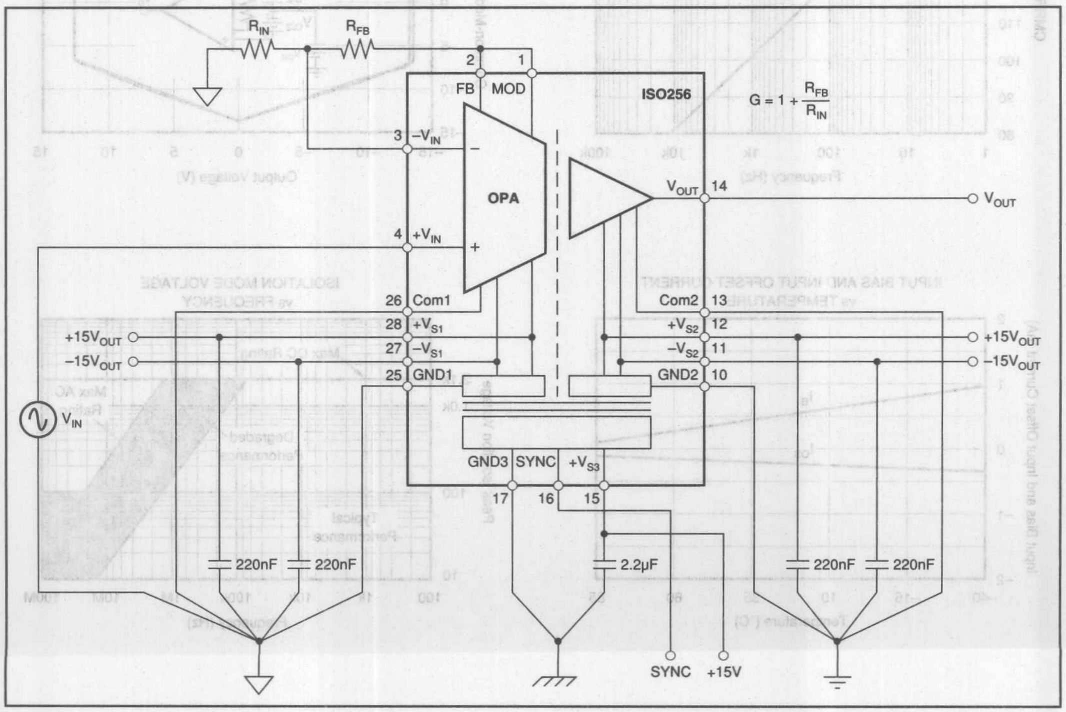


FIGURE 1. Basic Connections.

and can be avoided by synchronizing the individual ISO256's together by tying the SYNC pins together or using the circuit in Figure 2 to drive the SYNC pins from an external source.

When connecting up to eight ISO256's without a driver the unit with the highest natural frequency will determine the synchronized running frequency. The SYNC pin is sensitive to capacitive loading: 150pf or less is recommended. If unused, the SYNC pin should be left open. Avoid shorting the SYNC pin directly to ground or supply potentials; otherwise damage may result.

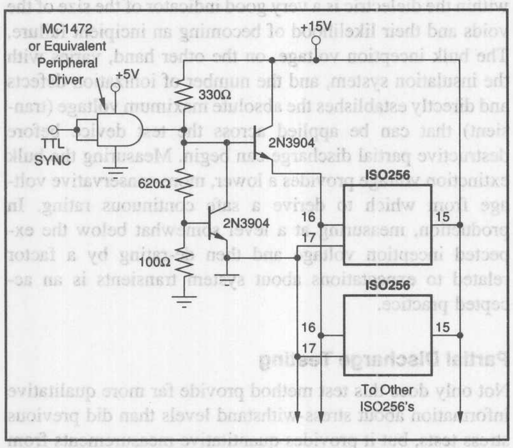


FIGURE 2. External SYNC drive.

Soft start circuitry protects the MOSFET switches during startup. This is accomplished by holding the gate-to-source voltage of both MOSFET switches low until the free-running oscillator is fully operational. In addition, soft start circuitry and input current sensing also protects the switches. This current limiting keeps the MOSFET switches operating in their safe operating area under fault conditions or excessive loads. When either of these conditions occur, the peak input current exceeds a safe limit. The result is an approximate 5% duty cycle, 300µs drive period to the MOSFET switches. This protects the internal MOSFET switches as well as the external load from any thermal damage. When the fault or excessive load is removed, the converter resumes normal operation. A delay period of approximately 50µs incorporated in the current sensing circuitry allows the output filter capacitors to fully charge after a fault is removed. This delay period corresponds to a filter capacitance of no more than 1µf at either of the output pins. This provides full protection of the MOSFET switches and also sufficiently filters the output ripple voltage. The current sensing circuitry is designed to provide thermal protection for the MOSFET switches over the operating temperature range as well. When these conditions are exceeded, the unit will go into its shutdown mode.

OUTPUT CURRENT RATINGS

The total current which can be drawn from each output supply on the ISO256 is a function of the total power drawn from all outputs. For example if three outputs are not used then maximum current can be drawn from one output. In all cases, the total maximum current that can be drawn from any combination of outputs is:

$$|I_{1+}| + |I_{1-}| + |I_{2+}| + |I_{2-}| \leq 50\text{mA}$$

$+V_{S3}$, GND3

The waveform of the ground return current is an 800kHz sawtooth. A capacitor between $+V_{S3}$ and GND3 provides a bypass for the AC portion of this current. The power should never be instantaneously interrupted to the ISO256 (i.e., a break in the line to $+V_{S3}$ either by accidental or switch means.) Normal power down of the $+V_{S3}$ supply is not considered instantaneous. Should a rapid break, in input power occur the internal transformers voltage will rapidly rise to maintain current flow and may cause internal damage to the ISO256.

SYNCHRONIZED OPERATION

ISO256 can be synchronized to an external signal source. This capability is useful in eliminating troublesome beat frequencies in multi-channel systems and in rejecting AC signals and their harmonics. To use this feature, tie all sync pins together or apply an external signal to the SYNC pin. ISO256 can be synchronized to an external oscillator over the range 1-1.4MHz (this corresponds to a modulation frequency of 500kHz to 700kHz as SYNC is internally divided by 2).

CARRIER FREQUENCY CONSIDERATIONS

ISO256 amplifiers transmit the signal across the ISO-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes more complex.

It should be noted that for the ISO256, the carrier frequency is nominally 400kHz and the –3dB point of the amplifier is 50kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 200kHz.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO256 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the "Signal Response vs Carrier Frequency" performance curve.

ISOLATION MODE VOLTAGE

Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds GND1 and GND2. IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs in a

Response vs Carrier Frequency" performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in "IMR vs Frequency" performance curve and compute the amplifier response to this input-referred error signal from the data given in the "Signal Response vs Carrier Frequency" performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/μs. For convenience, this is plotted in the typical performance curves for the ISO256 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/μs but falls below 20kV/μs, performance may be degraded. At rates of change above 20kV/μs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltage below 15V may decrease the dV/dT to 500V/μs for typical performance, but the maximum dV/dT of 20kV/μs remains unchanged.

Leakage current is determined solely by the impedance of the barrier and transformer capacitance and is plotted in the "Isolation Leakage Current vs Frequency" curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one.

Historically, Burr-Brown has chosen a deliberately conservative one: VTEST = (2 x ACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO256.

Partial Discharge

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. The inception voltage for these voids tends to be constant, so that the measurement of total charge being redistributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure. The bulk inception voltage, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the bulk extinction voltage provides a lower, more conservative voltage from which to derive a safe continuous rating. In production, measuring at a level somewhat below the expected inception voltage and then de-rating by a factor related to expectations about system transients is an accepted practice.

Partial Discharge Testing

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE in Germany, an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display less than or equal to 5pC partial discharge level in a 100% production test.

APPLICATIONS

The ISO256 isolation amplifiers are used in three categories of applications:

- Accurate isolation of signals from high voltage ground potentials
- Accurate isolation of signals from severe ground noise and
- Fault protection from high voltages in analog measurements

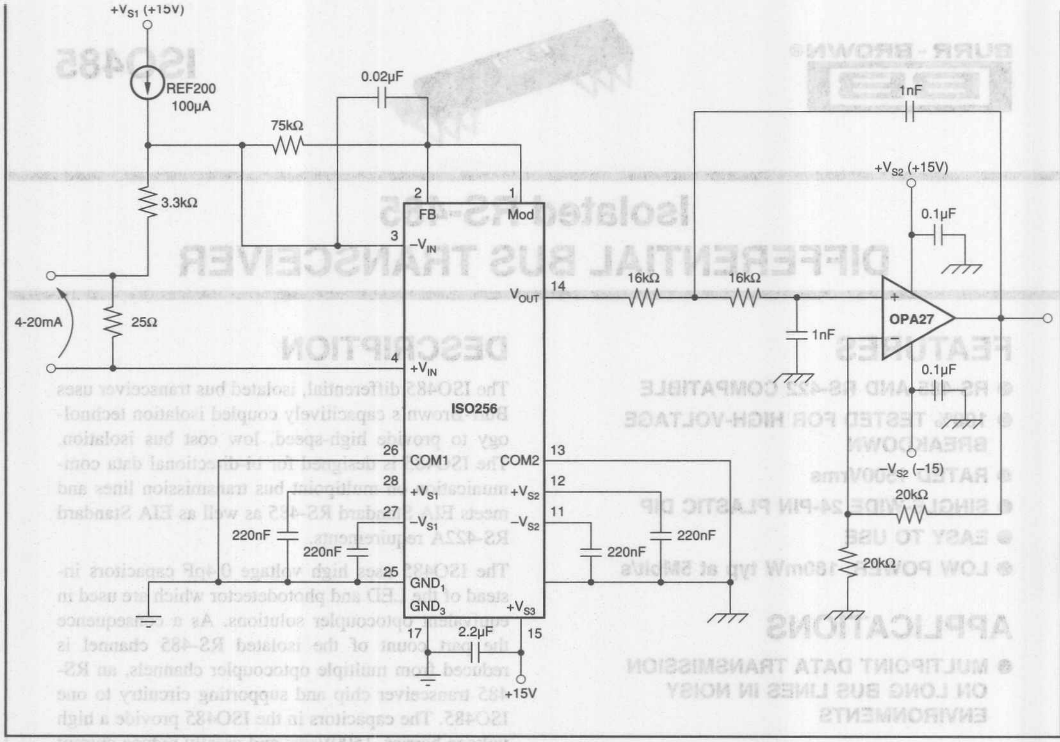
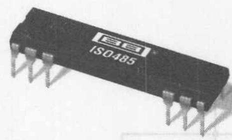


FIGURE 3. Isolated 4-20mA Current Receiver with O/P Filter.

BURR-BROWN®



ISO485

Isolated RS-485 DIFFERENTIAL BUS TRANSCEIVER

FEATURES

- RS-485 AND RS-422 COMPATIBLE
- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- SINGLE-WIDE 24-PIN PLASTIC DIP
- EASY TO USE
- LOW POWER: 180mW typ at 5Mbit/s

APPLICATIONS

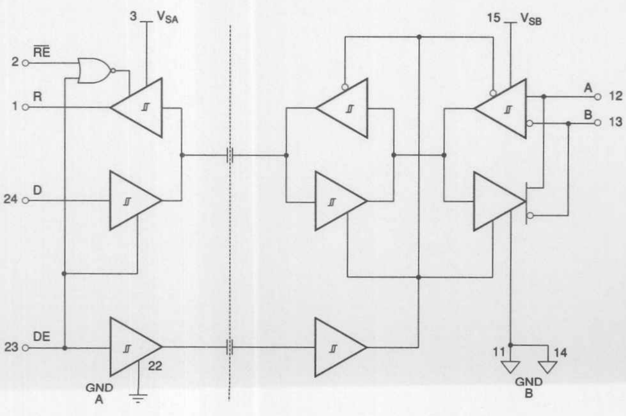
- MULTIPOINT DATA TRANSMISSION ON LONG BUS LINES IN NOISY ENVIRONMENTS

DESCRIPTION

The ISO485 differential, isolated bus transceiver uses Burr-Brown's capacitively coupled isolation technology to provide high-speed, low cost bus isolation. The ISO485 is designed for bi-directional data communication on multipoint bus transmission lines and meets EIA Standard RS-485 as well as EIA Standard RS-422A requirements.

The ISO485 uses high voltage 0.4pF capacitors instead of the LED and photodetector which are used in equivalent optocoupler solutions. As a consequence the part count of the isolated RS-485 channel is reduced from multiple optocoupler channels, an RS-485 transceiver chip and supporting circuitry to one ISO485. The capacitors in the ISO485 provide a high voltage barrier, 1500Vrms and greatly reduce current spikes on the power line.

The ISO485 combines a 3-state differential line driver and a differential-input line receiver both of which operate from a single 5V power supply. The driver differential outputs and the receiver differential input/output bus ports are designed to offer minimum loading to the bus whenever the driver is disabled or $V_S = 0V$.



TRUTH TABLE

DE	RE	RS-485 BUS
0	0	R_X
0	1	HIGH Z
1	0	HIGH Z
1	1	T_X

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25°C$, $V_S = 5V$, unless otherwise specified.

PARAMETER	CONDITION	ISO485P MIN	TYP	MAX	UNITS
DRIVER DC CHARACTERISTICS					
Input Voltage					
High MIN				2	V
Low MAX		0.8			V
Input Current					
High-Level	$V_{IN} = 2.4V$			±1	µA
Low-Level	$V_{IN} = 0.4V$			±1	µA
Output Voltage	$I_{OUT} = 0$	0		5	V
Differential Output Voltage	$I_{OA} - I_{OB} = 0$	1.5		5	V
	$R_{LOAD} = 100Ω$	2	2.5	5	V
	$R_{LOAD} = 54Ω$	1.5	2.5	5	V
Change In Magnitude of Differential Output Voltage	$R_{LOAD} = 54Ω$ or $100Ω$			±0.5	V
Common-Mode Output Voltage	$R_{LOAD} = 54Ω$ or $100Ω$			3	V
Change in Magnitude of Common-Mode Output Voltage	$R_{LOAD} = 54Ω$ or $100Ω$			±0.2	V
Output Current	$V_{OUT} = 7V$, output disabled			1	mA
	$V_{OUT} = -7V$, output disabled			–0.8	mA
Short-Circuit Output Current (1 sec max)	$V_{OUT} = -7V$		–250		mA
	$V_{OUT} = 0V$		–150		mA
	$V_{OUT} = V_S$		250		mA
	$V_{OUT} = 12V$		250		mA
DRIVER SWITCHING CHARACTERISTICS					
Propagation Delay Time, Low-to-High Level Output	$R_{LOAD} = 54Ω$			60	ns
Propagation Delay Time, High-to-Low Level Output	$R_{LOAD} = 54Ω$			60	ns
Input to Output Propagation Delay Skew	$R_{LOAD} = 54Ω$		10		ns
Output Rise Time	$R_{LOAD} = 54Ω$		10		ns
Output Fall Time	$R_{LOAD} = 54Ω$		10		ns
RECEIVER DC CHARACTERISTICS					
Differential-Input-Threshold Voltage					
High	$V_{OUT} = 2.7V$, $I_{OUT} = -0.4mA$			0.2	V
Low	$V_{OUT} = 0.5V$, $I_{OUT} = 8mA$	–0.2			V
Hysteresis			70		mV
High-Level Output Voltage	$V_{ID} = 200mV$, $I_{OH} = 400µA$	2.4			V
Low-Level Output Voltage	$V_{ID} = 200mV$, $I_{OL} = 8mA$			0.4	V
High-Impedance-State Output Current	$V_{OUT} = 1.4V$			±1	µA
Line Input Current	$V_{IN} = 12V$, other output = 0V		0.7		mA
	$V_{IN} = -7V$, other output = 0V		–0.6		mA
Enable-Input Current					
High	$V_{IH} = 2.7V$			1	µA
Low	$V_{IL} = 0.4V$			1	µA
Input Resistance		12			kΩ
Short-Circuit Output Current	1 sec max		40		mA
RECEIVER SWITCHING CHARACTERISTICS					
Propagation Delay Time,					
Low-to-High Level Output	$V_{ID} = -1.5V$ to $1.5V$, $C_L = 15pF$		35	60	ns
High-to-Low Level Output	$V_{ID} = -1.5V$ to $1.5V$, $C_L = 15pF$		30	60	ns
Input to Output Propagation Delay Skew			10		ns
Output Rise Time	$R_L = 54Ω$		8		ns
Output Fall Time	$R_L = 54Ω$		8		ns
TRANSCEIVER SPECIFICATIONS					
Maximum Data Rate		20	35		Mbits/s
Propagation Delay Driver to Receiver			75		ns
Driver Output Enable Time	$R_L = 110Ω$		155	200	ns
Driver Output Disable Time	$R_L = 110Ω$		185	280	ns
Propagation Delay Receiver to Driver			13		ns
Receiver Output Enable Time	$C_L = 15pF$		110	180	ns
Receiver Output Disable Time	$C_L = 15pF$		120	185	ns

PARAMETER	CONDITION	ISO485P MIN	TYP	MAX	UNITS
TRANSCEIVER SPECIFICATIONS (CONT)					
Supply Voltage					
V_SA		3	5	5.5	V
V_SB		4.75	5	5.25	V
Supply Current	DE RE RS-485 BUS				
V_SA	0 0 Rx			5	mA
V_SA	0 1 HIGH Z			0.4	mA
V_SA	1 0 HIGH Z			0.4	mA
V_SA	1 1 Tx			0.4	mA
V_SB	0 0 Rx			55	mA
V_SB	0 1 HIGH Z			55	mA
V_SB	1 0 HIGH Z			51	mA
V_SB	1 1 Tx			51	mA
RECOMMENDED OPERATING CONDITIONS					
Voltage at Any Bus Terminal	(separately or common-mode)	–7		12	V
High-Level Driver Input Voltage		2			V
Low-Level Driver Input Voltage				0.8	V
Differential Receiver Input Voltage				±12	V
Output Current High-Level					
	Driver			–60	mA
	Receiver			–400	µA
Output Current Low-Level					
	Driver			60	mA
	Receiver			8	mA
TEMPERATURE RANGE					
Operating		–40		85	°C
Storage		–40		125	°C
ISOLATION PARAMETERS					
Rated Voltage, Continuous	50Hz	1500			Vrms
Partial Discharge, 100% Test(1)	1s, 5pC	2400			Vrms
Creepage Distance (External) DIP = "P" Package			16		mm
Internal Isolation Distance			0.10		mm
Isolation Voltage Transient Immunity(2)			1.6		kV/µs
Barrier Impedance			$> 10^{14} \parallel 7$		Ω ‖ pF
Leakage Current	240Vrms, 60Hz		0.6		µArms

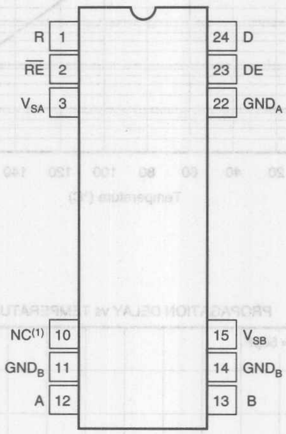
NOTES: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages, V_S	5.5V
Voltage at any bus terminal	–10 to 15V
Enable Input Voltage	0 to V_{CC} + 0.5V
Continuous total dissipation at 25°C free-air temp.	750mW
Lead solder temperature, 260°C for 10s, 1.6mm below seating plane	300°C
Junction Temperature	150°C
Package thermal transfer, θ_{JA}	75°C/W

PIN CONFIGURATION

Top View DIP



NOTE: (1) Pin 10 must be left unconnected.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO485P	24-Pin Single-Wide DIP	243-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	R	Data Received From Transmission Line
2	$\overline{RE}$	Receive Switch Controlling Receiving Of Data
3	V_{SA}	+5V Supply Pin For Side A
10	NC	This Pin MUST Be Left Unconnected
11	GND_B	Ground Pin For Side B. Also Connected To Pin 14
12	A	Data, Driver Out/Receiver In
13	B	Data, Driver Out/Receiver In
14	GND_B	Ground Pin For Side B. Also Connected To Pin 11
15	V_{SB}	+5V Supply Pin For Side B
22	GND_A	Ground Pin For Side A
23	DE	Driver Switch Controlling Output Of Data
24	D	Data To Be Transmitted

ELECTROSTATIC DISCHARGE SENSITIVITY

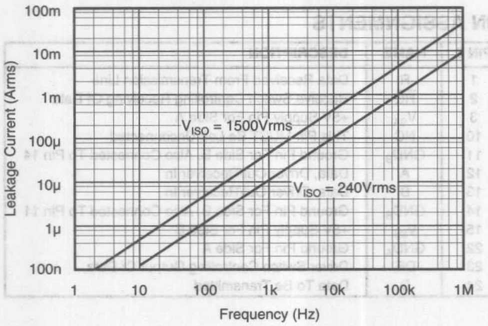
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

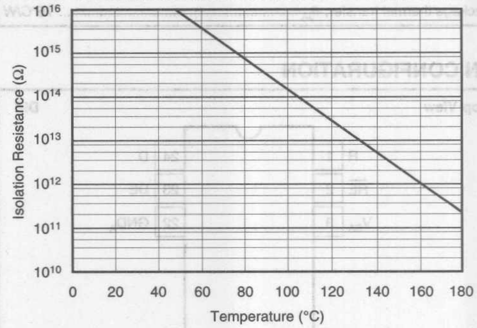
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, $V_S = +5V$, unless otherwise noted.

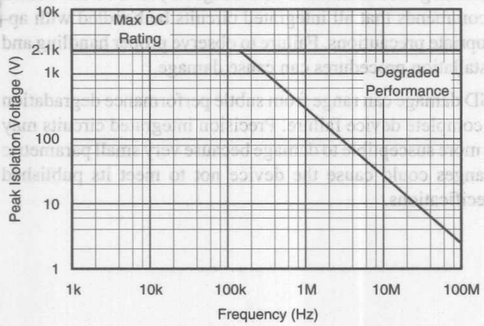
ISOLATION LEAKAGE CURRENT vs FREQUENCY



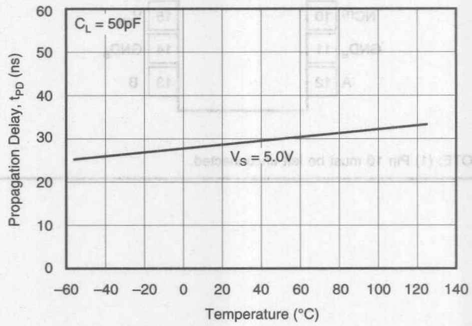
TYPICAL INSULATION RESISTANCE vs TEMPERATURE



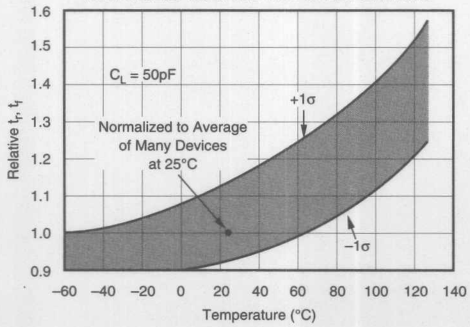
ISOLATION VOLTAGE vs FREQUENCY



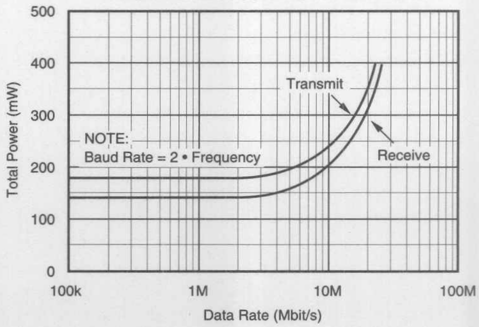
PROPAGATION DELAY vs TEMPERATURE



NORMALIZED RISE/FALL TIME vs TEMPERATURE



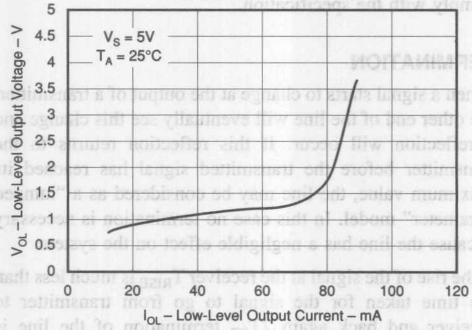
TYPICAL POWER DISSIPATION vs DATA RATE



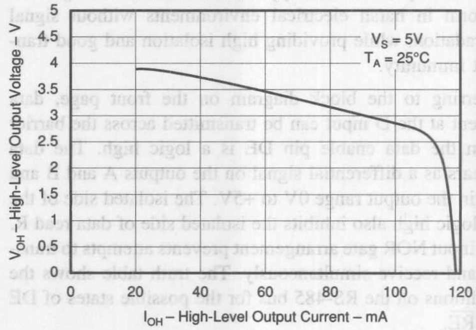
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = +5V$, unless otherwise noted.

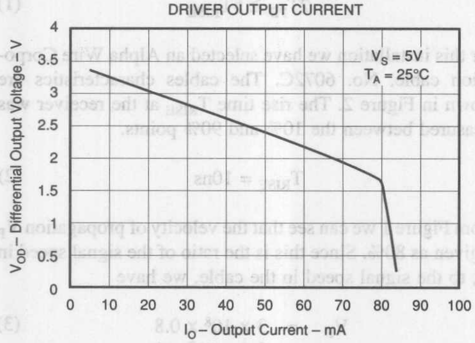
OUTPUT LOW VOLTAGE vs
DRIVER OUTPUT CURRENT



OUTPUT HIGH VOLTAGE vs
DRIVER OUTPUT CURRENT



OUTPUT VOLTAGE vs
DRIVER OUTPUT CURRENT



The ISO485 is a differential, isolated transceiver for half duplex multi-point communication, and complies with the EIA Interface Standards summarized in Table I. The signals transmitted across the isolation barrier can achieve transmission rates up to 35Mbit/s typical. The barrier is designed to perform in harsh electrical environments without signal degradation, while providing high isolation and good transient immunity.

Referring to the block diagram on the front page, data present at the D input can be transmitted across the barrier when the data enable pin DE is a logic high. The data appears as a differential signal on the outputs A and B and within the output range 0V to +5V. The isolated side of the DE logic high also inhibits the isolated side of data read R. The input NOR gate arrangement prevents attempts to transmit and receive simultaneously. The truth table shows the conditions on the RS-485 bus for the possible states of DE and $\overline{RE}$.

ISOLATION BARRIER

Data is transmitted by coupling complementary logic pulses to the receiver through two 0.4pF capacitors. These capacitors are built into the ISO485 package with Faraday shielding to guard against false triggering by external electrostatic fields.

The integrity of the isolation barrier of the ISO485 is verified by partial discharge testing. 2400Vrms, 50Hz, is applied across the barrier for one second while measuring any tiny discharge currents that may flow through the barrier. These current pulses are produced by localized ionization within the barrier. This is the most sensitive and reliable indicator of barrier integrity and longevity, and does not damage the barrier. A device fails the test if five or more current pulses of 5pC or greater are detected.

Conventional isolation barrier testing applies test voltage far in excess of the rated voltage to catastrophically break down a marginal device. A device that passes the test may be weakened, and lead to premature failure.

APPLICATION EXAMPLE

Consider an RS-485 network in an industrial area. The system specifications are:

- Distance between master controller and the farthest outstation 50 meters.
- System data rate is to be 30Mbit/s.
- One daisy-chain cable will link the master controller to the outstations.

The main design considerations in implementing this system are:

- Line loading and termination
- Selection of correct cable for requirements
- Attenuation and distortion of the signal
- Fault protection and fail-safe operation

RS-485 recommends a maximum of 32 unit loads on any one line: the unit loading being derived from the 12kΩ input impedance and the 12V maximum common-mode voltage. The ISO485 represents 1 unit load. We could, therefore, connect up to 31 outstations to the master controller and comply with the specification.

TERMINATION

When a signal starts to change at the output of a transmitter, the other end of the line will eventually see this change and a reflection will occur. If this reflection returns to the transmitter before the transmitted signal has reached its maximum value, the line may be considered as a "lumped parameter" model. In this case no termination is necessary because the line has a negligible effect on the system.

If the rise of the signal at the receiver T_{RISE} is much less than the time taken for the signal to go from transmitter to receiver and back again $2T_{PD}$ termination of the line is necessary. It is usual to terminate the line with its characteristic impedance, Z_O when the following rule applies:

$$2T_{PD} \geq 5T_{RISE} \quad (1)$$

For this installation we have selected an Alpha Wire Corporation cable, No. 6072C. The cables characteristics are shown in Figure 2. The rise time T_{RISE} at the receiver was measured between the 10% and 90% points.

$$T_{RISE} = 10\text{ns} \quad (2)$$

From Figure 1 we can see that the velocity of propagation V_P is given as 80%. Since this is the ratio of the signal speed in air, to the signal speed in the cable, we have

$$\begin{aligned} V_P &= 3 \times 10^8 \times 0.8 \\ &= 2.4 \times 10^8 \text{ m/s} \end{aligned} \quad (3)$$

therefore

$$\begin{aligned} T_{PD} &= 1/V_P \\ &= 4.2\text{ns/m} \end{aligned}$$

For the cable

$$\begin{aligned} 2T_{PD} &= 4.2 \times 10^{-9} \times 50 \times 2 \\ &= 42\text{us} \end{aligned}$$

Equation 1 holds, therefore the line must be terminated with its characteristic impedance.

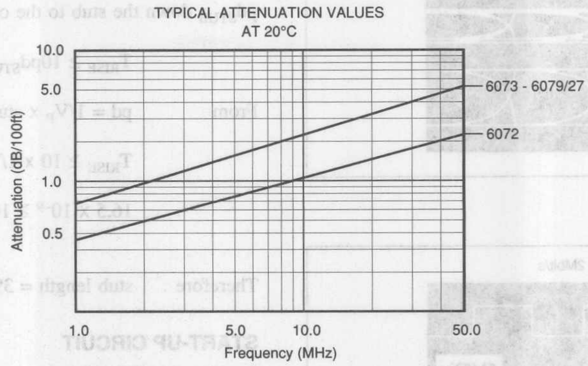
EYE PATTERNS AND Z_O

Eye patterns can be used to assess the signal distortion and noise on the transmission line. It is also a convenient method of determining the characteristic impedance of the line. The term 'eye' comes from the shape of the trace on the oscilloscope. See Figures 2 and 3.

The eye pattern was obtained using the non return zero pseudo-noise generator circuit shown in Figure 5. Figure 2 shows the effects of the termination resistor for the three cases: $Z_T > Z_O$, $Z_T = Z_O$, $Z_T < Z_O$ with $Z_T = Z_O$ the eye

pattern is clear. In practice a precision decade resistance box was used to determine the exact value of Z_T to use.

As the data rate is increased we can see from Figure 3 how the signal distortion also increases. From the graph in Figure 1 we can see that the specified attenuation figures given agree with those obtained by measurement; approximately –1.3db/100ft, at 30Mbit/s (15MHz).



TYPICAL ELECTRICAL CHARACTERISTICS

Capacitance

ALPHA WIRE CORP. NO.	CDR. to CDR. pF/ft	CDR. to CDR. (pF/m)	CDR. to (CDR. AND SHIELD) pF/ft	CDR. to (CDR. AND SHIELD) pF/m)	VP. %	Z_0 at 1MHz, Ω
6072C	8.7	(28, 5)	5.9	(52, 2)	80	150
6073C thru 6079/27C	12.5	(41, 0)	22.0	(72, 5)	80	150

FIGURE 1. Cable Characteristics.

PARAMETER		EIA-232	RS-432-A	RS-422-A	RS-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
Maximum Cable Length (m)		15	1200	1200	1200
Maximum Data Rate (bps)		20k	100k	10M	10M
Maximum Common-Mode Voltage (V)		±25	±6	6 to –0.25	12 to –7
Driver Output Levels (V)	Loaded	±5	±3.6	±2	±1.5
	Unloaded	±15	±6	±5	±5
Driver Load (Ω)		3k to 7k	450 (min)	100 (min)	60 (min)
Driver Slew Rate		30V/µs (max)	External Control	NA	NA
Driver Output Short Circuit Current Limit (mA)		500 to V_{CC}	150 to GND	150 to GND	150 to GND 250 to –7 or 12V
Driver Output Resistance High Z state (Ω)	Power on	NA	NA	NA	12k
	Power off	300	60k	60k	12k
Receiver Input Resistance (Ω)		3 to 7	4	4	12
Receiver Sensitivity		±3V	±200mV	±200mV	±200mV

TABLE I. Summary of EIA Interface Standards.

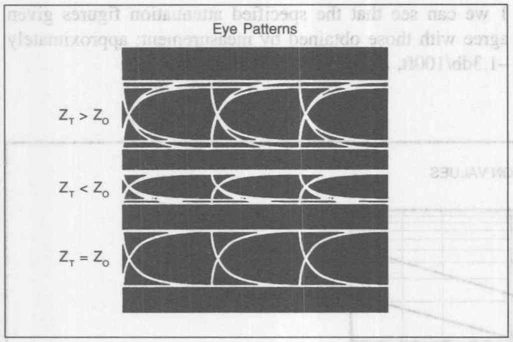


Figure 2. Eye Patterns.

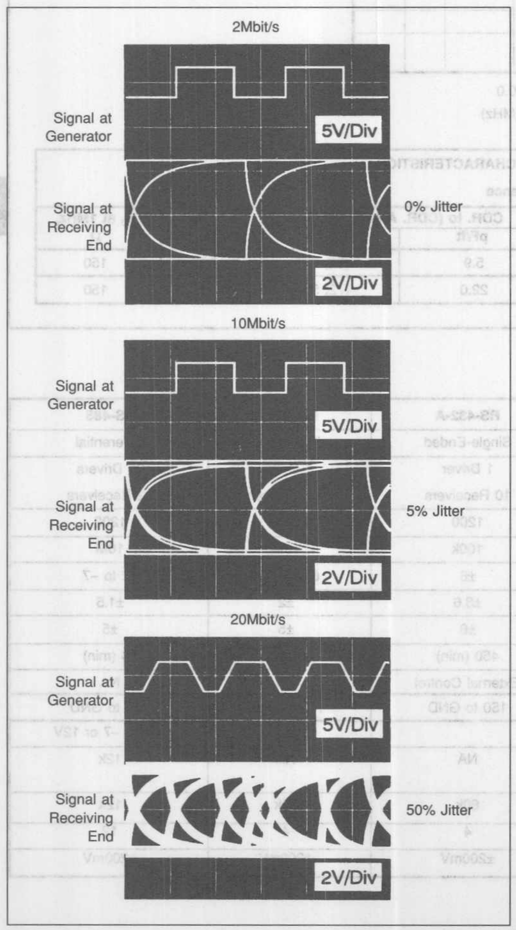


Figure 3. ISO485 Signal Distortion vs Data Rate.

STUB LENGTH

If the outstations are not to act as transmission lines, they too must meet the criteria determined by equation 1. They must be seen as a lumped parameter. As a rule-of-thumb, the transition time of the pulse from the transmitter, T_{RISE} should be ten times longer than the propagation delay, pd_{STUB} down the stub to the outstation.

$$T_{RISE} \geq 10pd_{STUB} \tag{4}$$

From $\quad pd = 1/V_P \times \text{stub length}$

$$T_{RISE} \geq 10 \times 1/V_P \times \text{stub length}$$

$$16.5 \times 10^{-9} \geq 10 \times \frac{1}{3 \times 10^8 \times 0.8} \times \text{stub length}$$

Therefore $\quad$ stub length = 396mm (15.6") maximum

START-UP CIRCUIT

Because the ISO485 is a capacitively coupled device, it is possible to power up an indeterminate state. The circuit of Figure 4 ensures that the ISO485 powers up in the receive mode, thus avoiding any conflict on the transmission line.

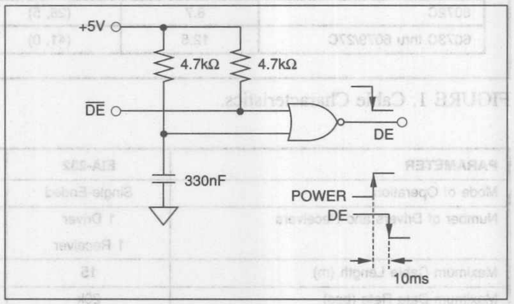


Figure 4. Start-up Circuit.

TRANSMIT/RECEIVE MODE

Because the ISO485 is a capacitively coupled device, indeterminate states can occur when the change from transmit to receive or, from receive to transmit is initiated. This is easily overcome by transmitting an edge prior to the data of interest. The four possible conditions which could happen are detailed in Figures 5a, 5b, 6a, and 6b. Thereafter, data is known and correct.

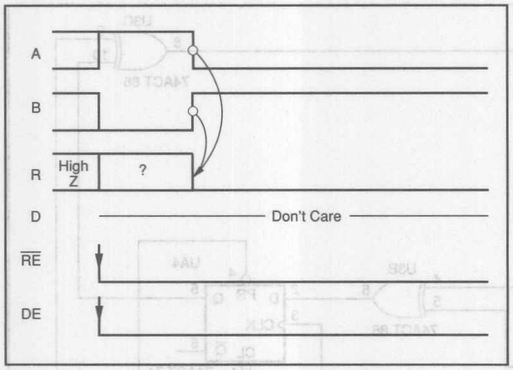


Figure 5a. Transmit to Receive.

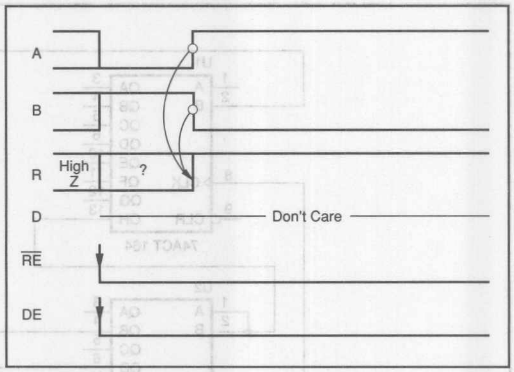


Figure 5b. Transmit to Receive.

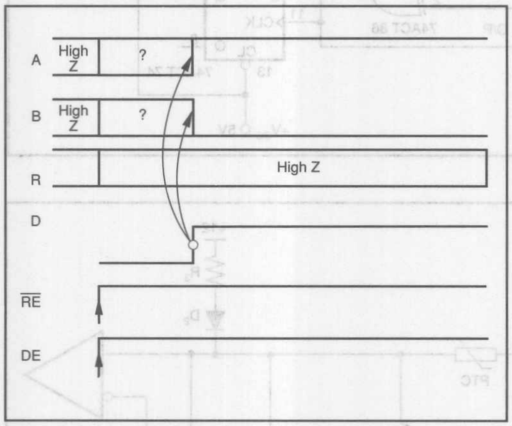


Figure 6a. Receive to Transmit

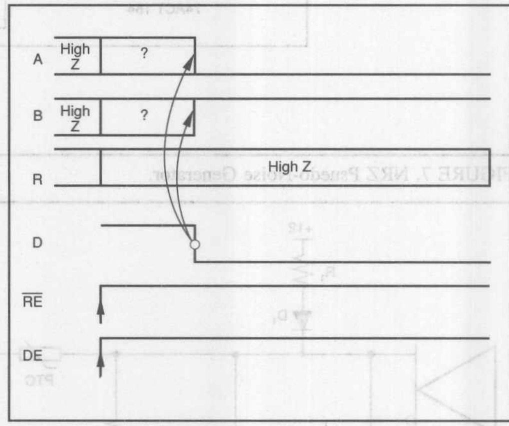


Figure 6b. Receive to Transmit.

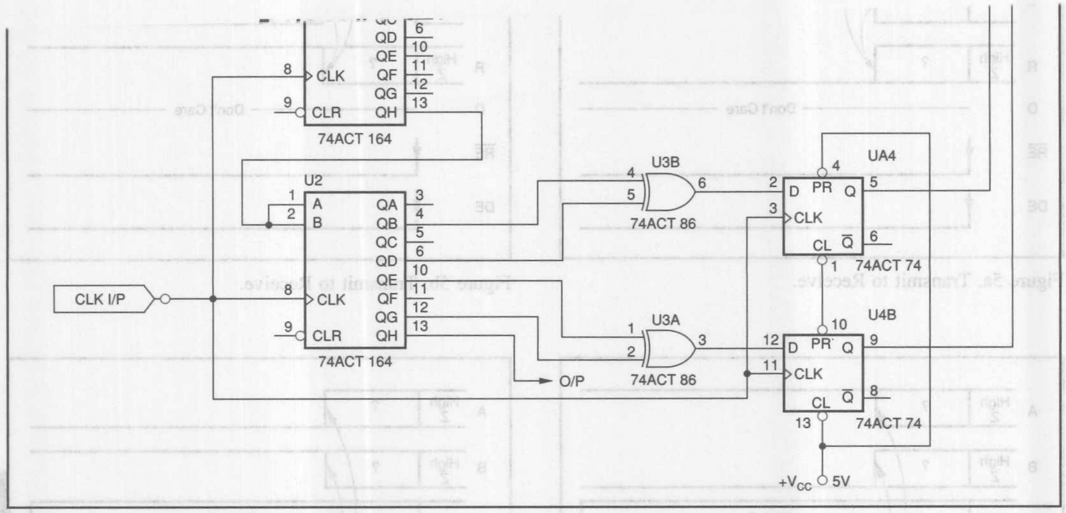
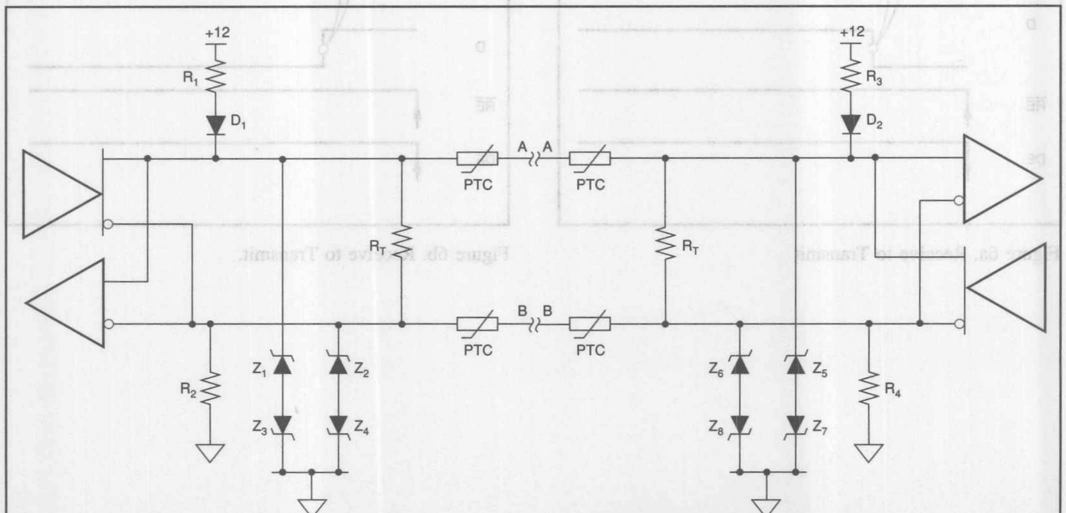


FIGURE 7. NRZ Psuedo-Noise Generator.



a) $R_1 = R_3$ and $R_2 = R_4$
For open circuit conditions this biases the line to a logic '1'

b) $Z_1 = Z_3 = Z_5 = Z_7$ = BZX85 = 12V
$Z_2 = Z_4 = Z_6 = Z_8$ = BZX85 = 6.8V
$D_1 = D_2$ = IN4048

The zener diode in conjunction with the ptc thermistors limit the current drawn on the line when taken beyond the +12V and –7V. The ptc thermistors also current limit on the line being shorted to the ground.

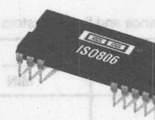
c) $R_1 = R_2 = 0.5 \times Z_0\left(1 + \frac{V_{CC}}{V_{TH}}\right)$

$R_T = Z_0\left(1 + \frac{V_{TH}}{V_{CC}}\right)$

NOTE: PTC = Positive Temperature Coefficient Thermistor.

FIGURE 8. RS-485 Line with Fail-Safe Protection.

BURR - BROWN®



ISO806

Isolated 12-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 1500Vrms ISOLATION CONTINUOUS
- 25µS CONVERSION TIME
- 12-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

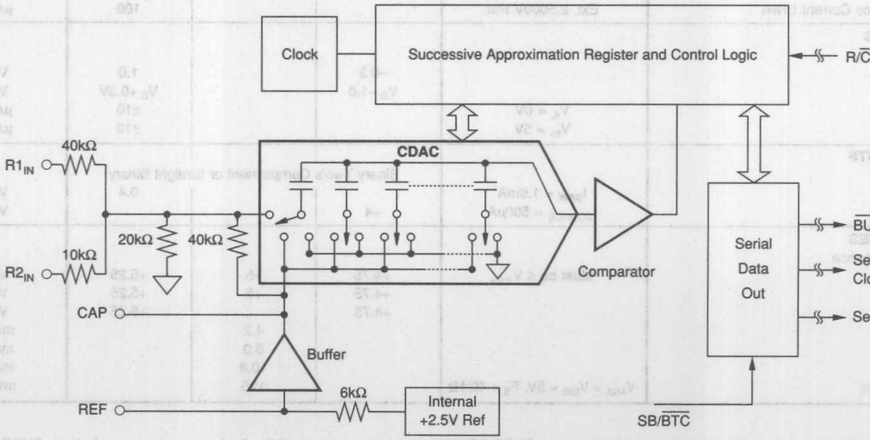
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

DESCRIPTION

The ISO806 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO806 contains a complete 12-bit capacitor based SAR, ADC with S/H, clock, reference, µP interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including ±10V, ±5V, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of –40°C to +85°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

PARAMETER	CONDITIONS	ISO806P MIN	TYP	MAX	UNITS
RESOLUTION				12	Bit
ANALOG INPUT					
Voltage Ranges			±10, 0 to +5, 0 to +4		V
Impedance			(See Table II)		
Capacitance			35		pF
THROUGHPUT SPEED					
Conversion Time				20	µs
Complete Cycle	Acquire and Convert			25	µs
Throughput Rate		40			kHz
DC ACCURACY					
Integral Linearity Error			±0.15	±0.9	LSB(1)
Differential Linearity Error			±0.15	±0.9	LSB
No Missing Codes			Guaranteed		Bits
Transition Noise(2)			0.1		LSB
Full Scale Error(3,4)				±0.5	%
Full Scale Error Drift			±7		ppm/°C
Full Scale Error Drift	Ext. 2.5000V Ref		±0.5		ppm/°C
Bipolar Zero Error(3)	±10V Range			±10	mV
Bipolar Zero Error Drift	±10V Range		±0.5		ppm/°C
Unipolar Zero Error(3)	0V to 5V, 0V to 4V Ranges			±3	mV
Unipolar Zero Error Drift	0V to 5V, 0V to 4V Ranges		±0.5		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_S)	+4.75V < V_S < +5.25V			±0.5	LSB
AC ACCURACY					
Spurious-Free Dynamic Range	f_{IN} = 1kHz, ±10V		90		dB(5)
Total Harmonic Distortion	f_{IN} = 1kHz, ±10V		–90		dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz, ±10V		73		dB
Signal-to-Noise	f_{IN} = 1kHz, ±10V		73		dB
Useable Bandwidth(6)			130		kHz
SAMPLING DYNAMICS					
Aperture Delay			40		ns
Aperture Jitter			20		ps
Overvoltage Recovery(7)			750		ns
REFERENCE					
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must use external buffer.)			1		µA
Internal Reference Drift			8		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref			100	µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		1.0	V
V_{IH}		V_D –1.0		V_D +0.3V	V
I_{IL}	V_{IL} = 0V			±10	µA
I_{IH}	V_{IH} = 5V			±10	µA
DIGITAL OUTPUTS					
Data Coding			Binary Two's Complement or Straight Binary		
V_{OL}	I_{SINK} = 1.6mA			0.4	V
V_{OH}	I_{SOURCE} = 500µA	+4			V
POWER SUPPLIES					
Specified Performance					
V_{DIG1}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
V_{DIG2}		+4.75		+5.25	V
I_{DIG1}			4.2		mA
I_{ANA}			5.0		mA
I_{DIG2}			10.8		mA
Power Dissipation	V_{ANA} = V_{DIG} = 5V, F_S = 40kHz		125		mW

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

PARAMETER	CONDITIONS	ISO806P MIN	TYP	MAX	UNITS
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C
Thermal Resistance, ϕ_{JA}					
Plastic DIP			75		°C/W
ISOLATION PARAMETERS					
Rated Voltage, Continuous	50Hz	1500			Vrms
Partial Discharge, 100% Test(8)	1s, 5pC	2500			Vrms
Creepage Distance (External) DIP = "P" Package			16		mm
Internal Isolation Distance			0.10		mm
Barrier Impedance			$>10^{13}$ ll 15		Ω ll pF
Leakage Current(9)	240Vrms, 60Hz			1.7	µArms
	240Vrms, 50Hz			1.4	µArms

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (9) Tested at 2500Vrms, 50Hz limit 10µA.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
CAP	V_{ANA} +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND and AGND1	±0.3V
DGND, AGND, and GND_{ISO}	1563Vrms
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO806P	Plastic DIP	215-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

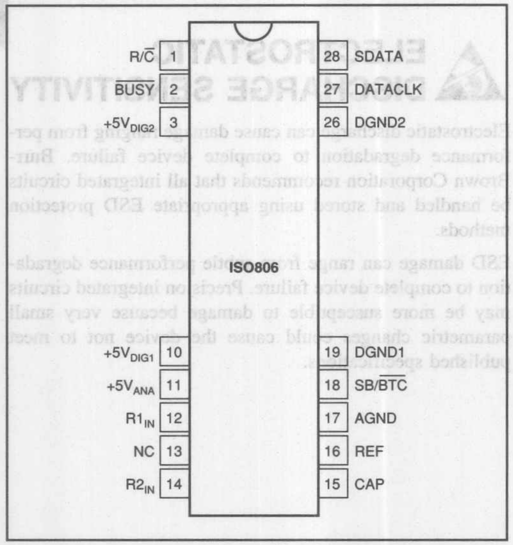
ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ISO806P	±0.9	70	–40°C to +85°C	Plastic DIP

			...convert. With BUSY high, a falling edge on R/C initiates a new conversion.
2	$\overline{BUSY}$	O	At the start of conversion BUSY goes LOW and stays LOW until conversion is complete.
3	$+5V_{DIG2}$		Isolated Digital Supply Volts.
10	$+5V_{DIG1}$		Digital Supply Volts.
11	$+5V_{ANA}$		Analog Supply Volts.
12	$R1_{IN}$		Analog Input.
13	NC		No Connection. Leave unconnected.
14	$R2_{IN}$		Analog Input.
15	CAP		Reference Buffer Output. 2.2μF tantalum capacitor to ground.
16	REF		Reference Input/Output. 2.2μF tantalum capacitor to ground.
17	AGND		Analog Ground.
18	SB/$\overline{BTC}$	I	Selects Straight Binary or Binary Two's Complement for Output Data Format.
19	DGND1		Digital Ground.
26	DGND2		Isolated Ground.
27	DATACLK	O	Data Clock Output.
28	SDATA	O	Serial Output Synchronized to DATACLK.

TABLE I. Pin Assignments.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	IMPEDANCE
±10V	V_{IN}	CAP	45.7kΩ
0V to 5V	AGND	V_{IN}	20.0kΩ
0V to 4V	V_{IN}	V_{IN}	21.4kΩ

TABLE II. Input Range Connections. See also Figure 3.

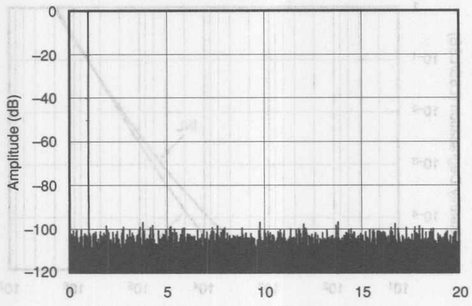
R/$\overline{C}$	$\overline{BUSY}$	DATACLK	OPERATION
$\downarrow$	1	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
0	$\uparrow$	X	New conversion initiated without acquisition of a new signal. Data will be invalid. R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	0	X	New convert commands ignored. Conversion "n" in progress.

TABLE III. Control Functions

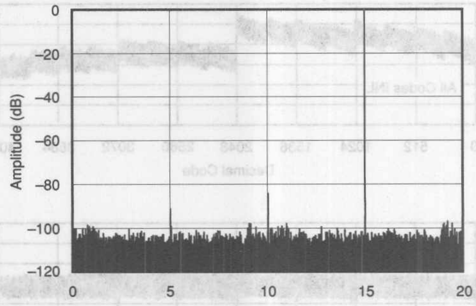
TYPICAL PERFORMANCE CURVES

T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

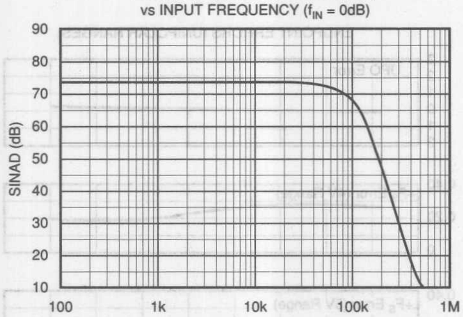
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 1kHz, 0dB)



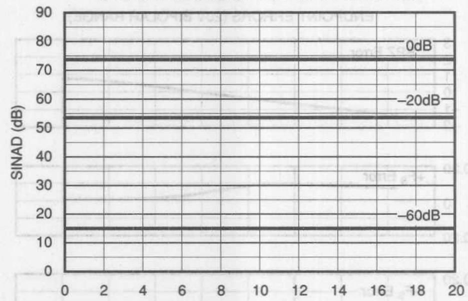
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 15kHz, 0dB)



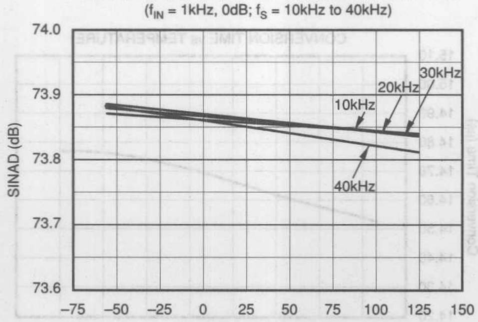
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = 0dB)



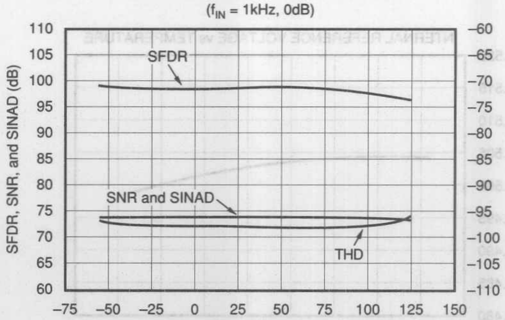
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY AND INPUT AMPLITUDE



SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
(f_{IN} = 1kHz, 0dB; f_S = 10kHz to 40kHz)



A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 1kHz, 0dB)



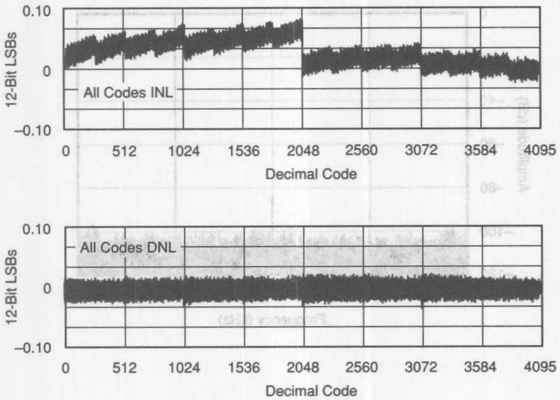
ISO806

5

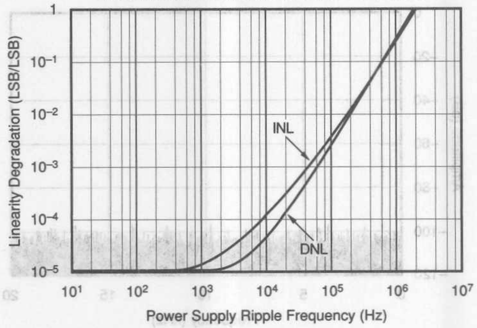
ISOLATION AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

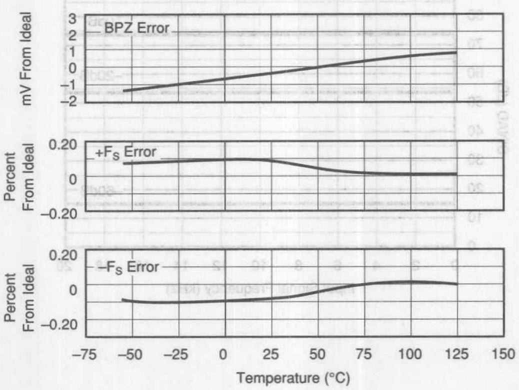
$T_A = +25°C$, $f_S = 40kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.



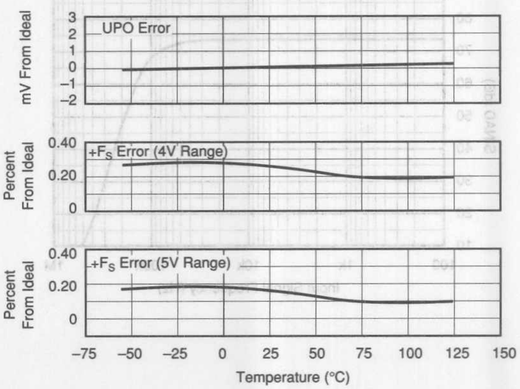
POWER SUPPLY RIPPLE SENSITIVITY
INL/DNL DEGRADATION PER LSB OF P-P RIPPLE



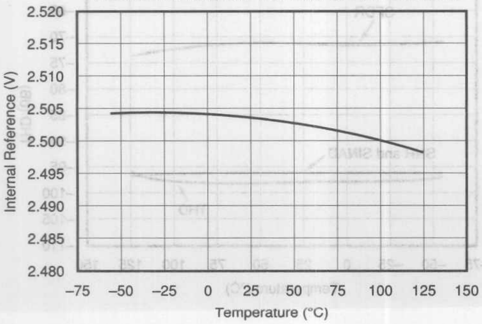
ENDPOINT ERRORS (20V BIPOLAR RANGE)



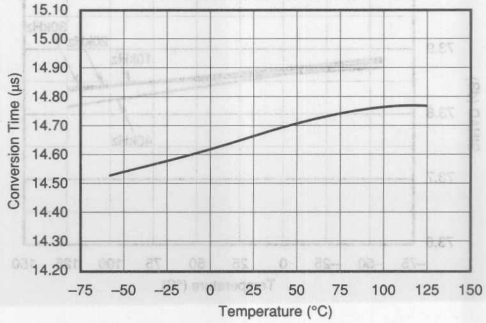
ENDPOINT ERRORS (UNIPOLAR RANGES)



INTERNAL REFERENCE VOLTAGE vs TEMPERATURE



CONVERSION TIME vs TEMPERATURE



BASIC OPERATION

SERIAL OUTPUT

Figure 1 shows a basic circuit to operate the ISO806 with a ±10V input range and serial output. Taking $R/\overline{C}$ (pin 1) LOW for 40ns (12µs max) will initiate a conversion and output valid data from the previous conversion on SDATA (pin 28) synchronized to 12 clock pulses output on DATACLK (pin 27). $\overline{BUSY}$ (pin 2) will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in Binary Two's Complement format, MSB first, and will be valid on both the rising and falling edges of the data clock. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ISO806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The $R/\overline{C}$ (pin 1) LOW for a minimum of 40ns immediately puts the sample/hold of the ISO806 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 2) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $R/\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ISO806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. $R/\overline{C}$ is level triggered.

READING DATA

The ISO806 outputs serial data in Straight Binary or Binary Two's Complement data output format. If $SB/\overline{BTC}$ (pin 18) is HIGH, the output will be in SB format, and if LOW, the output will be in BTC format. Refer to Table IV for ideal output codes.

Reading the data through the serial port will shift the internal output registers one bit per data clock pulse.

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT			
				BINARY TWO'S COMPLEMENT ($SB/\overline{BTC}$ LOW)		STRAIGHT BINARY ($SB/\overline{BTC}$ HIGH)	
Full-Scale Range	±10	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	1.22mV	976µV	BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
+Full Scale (FS – 1LSB)	9.99512V	4.99878V	3.999024V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0V	2.5V	2V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	–4.88mV	2.49878V	1.999024V	1111 1111 1111	FFF	0111 1111 1111	7FF
–Full Scale	–10V	0V	0V	1000 0000 0000	800	0000 0000 0000	000

Table IV. Output Codes and Ideal Input Voltages.

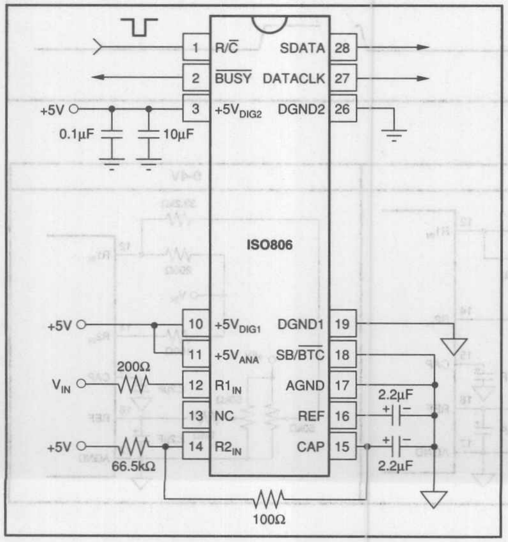


FIGURE 1. Basic ±10V Operation with Serial Output.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	0.04		12	µs
t_3	$\overline{BUSY}$ Delay from Start of Conversion		110		ns
t_4	$\overline{BUSY}$ LOW		14.7	20	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		90		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		14.7	20	µs
t_8	Acquisition Time		3		µs
t_{13}	Start of Conversion to DATACLK Delay		1.4		µs
t_{14}	DATACLK Period		1.1		µs
t_{15}	Data Valid to DATACLK HIGH Delay		75		ns
t_{16}	Data Valid after DATACLK LOW Delay		600		ns
$t_7 + t_8$	Throughput Time			25	µs

TABLE V. Conversion and Data Timing. T_A = –40°C to +85°C.

INTERNAL DATA CLOCK (During A Conversion)

The R/$\overline{C}$ (pin 1) LOW will initiate conversion 'n' and activate the internal data clock (typically 900kHz clock rate). The ISO806 will output 12 bits of valid data, MSB first, from conversion 'n-1' on SDATA (pin 28), synchronized to 12 clock pulses output on DATACLK (pin 27). The data will be valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 2) can be used to latch the data. After the 12th clock pulse, DATACLK will remain LOW until the next conversion is initiated, SDATA will also go LOW.

INPUT RANGES

The ISO806 offers three input ranges: standard ±10V and 0-5V, and a 0-4V range for complete, single supply systems. Figures 3a and 3b show the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full scale error[(1)] specifications are tested and guaranteed with the fixed resistors shown in Figure 3b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

pensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The input impedance, summarized in Table II, results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors used for each input range (see Figure 4). The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V.

Analog inputs above or below the expected range will yield either positive full scale or negative full scale digital outputs respectively. There will be no wrapping or folding over for analog inputs outside the nominal range.

Note: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

CALIBRATION

HARDWARE CALIBRATION

To calibrate the offset and gain of the ISO806 in hardware, install the resistors shown in Figure 3a. Table VI lists the hardware trim ranges relative to the input for each input range.

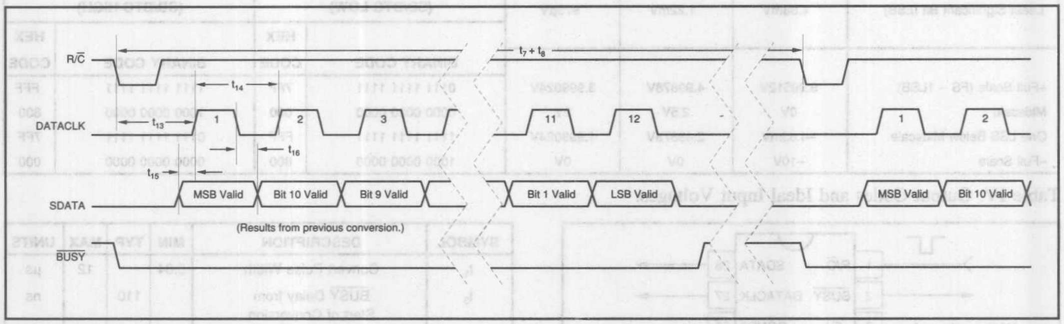


FIGURE 2. Serial Data Timing.

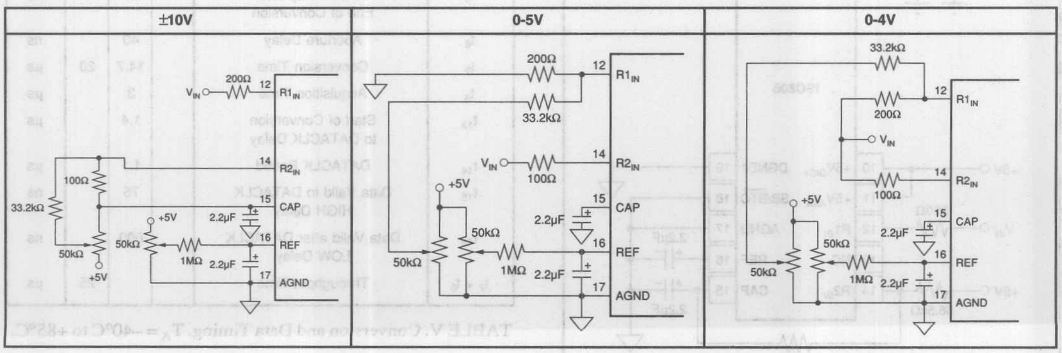


FIGURE 3a. Circuit Diagrams (With Hardware Trim).

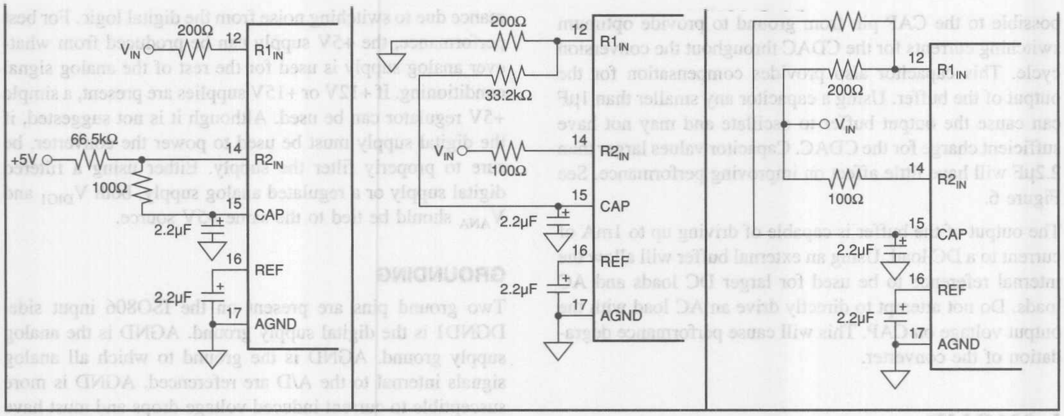


FIGURE 3b. Circuit Diagrams (Without Hardware Trim).

SOFTWARE CALIBRATION

To calibrate the offset and gain in software, no external resistors are required. However, to get the data sheet specifications for offset and gain, the resistors shown in Figure 3b are necessary. See the **No Calibration** section for more details on the external resistors. Refer to Table VII for the range of offset and gain errors with and without the external resistors.

NO CALIBRATION

See Figure 3b for circuit connections. Note that the actual voltage dropped across the external resistors is at least two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be considered when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors will be sufficient.

The external resistors shown in Figure 3b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. Not using the external resistors will result in offset and gain errors in addition to those listed in the electrical specifications section. Offset refers to the equivalent voltage of the digital output when converting with the input grounded. A positive gain error occurs when the equivalent output voltage of the digital output is larger than the analog input. Refer to Table VII for nominal ranges of gain and offset errors with and without the external resistors. Refer to Figure 4 for typical shifts in the transfer functions which occur when the external resistors are removed.

To further analyze the effects of removing any combination of the external resistors, consider Figure 5. The combination of the external and the internal resistors form a voltage divider which reduces the input signal to a 0.3125V to 2.8125V input range at the CDAC. The internal resistors are laser trimmed to high relative accuracy to meet full specifications. The actual input impedance of the internal resistor network looking into pin 12 or pin 14 however, is only accurate to ±20% due to process variations. This should be taken into account when determining the effects of removing the external resistors.

REFERENCE

The ISO806 operates with its internal 2.5V reference. The internal reference has approximately an 8ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5%).

The ISO806 also has an internal buffer for the reference voltage. See Figure 6 for characteristic impedances at the input and output of the buffer with all combinations of power down and reference down.

REF

REF (pin 16) is an input for an external reference or the output for the internal 2.5V reference. A 2.2μF tantalum capacitor should be connected as close as possible to the REF pin from ground. This capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference, degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads. See Figure 6.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 15) is the output of the internal reference buffer. A 2.2µF tantalum capacitor should be placed as close as possible to the CAP pin from ground to provide optimum switching currents for the CDAC throughout the conversion cycle. This capacitor also provides compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance. See Figure 6.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ISO806 uses 50% of its isolated power for the analog circuitry. The ISO806 front end should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG1} (pin 10) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG1} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Two ground pins are present on the ISO806 input side. DGND1 is the digital supply ground. AGND is the analog supply ground. AGND is the ground to which all analog signals internal to the A/D are referenced. AGND is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

The ground pin of the A/D should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

INPUT RANGE	OFFSET ADJUST RANGE (mV)	GAIN ADJUST RANGE (mV)
±10V	±15	±60
0 to 5V	±4	±30
0 to 4V	±3	±30

TABLE VI. Offset and Gain Adjust Ranges for Hardware Calibration (see Figure 3a).

INPUT RANGE (V)	OFFSET ERROR			GAIN ERROR		
	W/ RESISTORS	W/OUT RESISTORS		W/ RESISTORS	W/OUT RESISTORS	
	RANGE (mV)	RANGE (mV)	TYP (mV)	RANGE (% FS)	RANGE (% FS)	TYP
±10	$-10 \le BPZ \le 10$	$0 \le BPZ \le 35$	+15	$-0.4 \le G \le 0.4$ $0.15 \le G^{(1)} \le 0.15$	$-0.3 \le G \le 0.5$ $-0.1 \le G^{(1)} \le 0.2$	+0.05 +0.05
0 to 5	$-3 \le UPO \le 3$	$-12 \le UPO \le -3$	–7.5	$-0.4 \le G \le 0.4$ $0.15 \le G^{(1)} \le 0.15$	$-1.0 \le G \le 0.1$ $-0.55 \le G^{(1)} \le -0.05$	–0.2 –0.2
0 to 4	$-3 \le UPO \le 3$	$-10.5 \le UPO \le -1.5$	–6	$-0.4 \le G \le 0.4$ $-0.15 \le G^{(1)} \le 0.15$	$-1.0 \le G \le 0.1$ $-0.55 \le G^{(1)} \le -0.05$	–0.2 –0.2
Note: (1) High Grade.						

TABLE VII. Range of Offset and Gain Errors with and without External Resistors

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ISO806 is approximately 5-10% of the amount on similar ADCs with the charge redistribution DAC (CDAC) architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D. Any op amp sufficient for the signal in an application will be sufficient to drive the ISO806.

The resistive front end of the ISO806 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external over voltage protection circuitry.

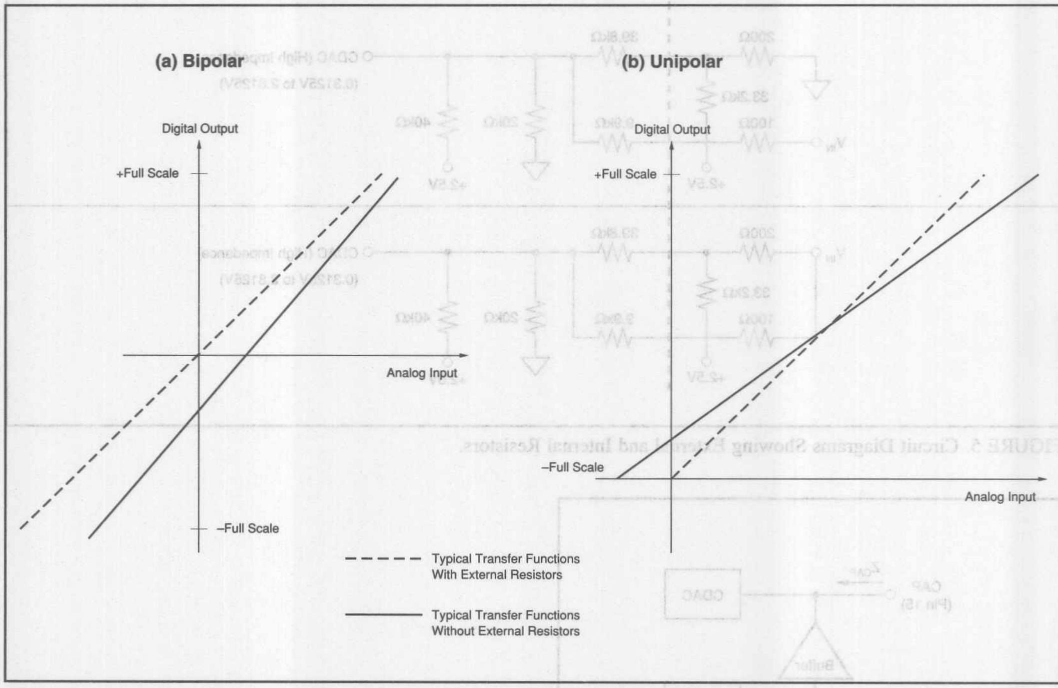


FIGURE 4. Typical Transfer Functions With and Without External Resistors.

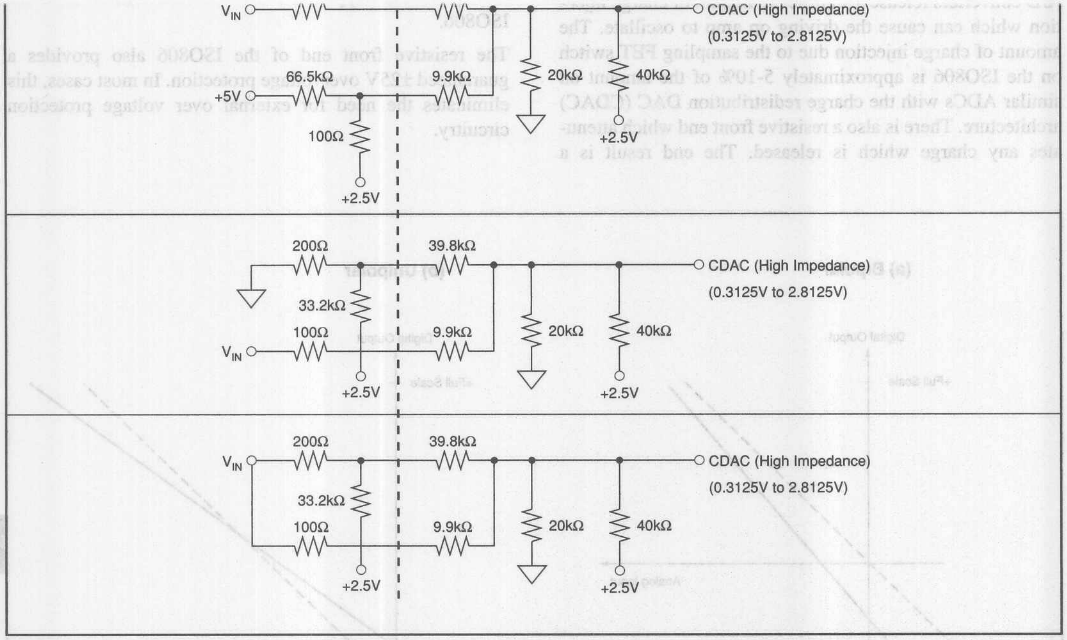
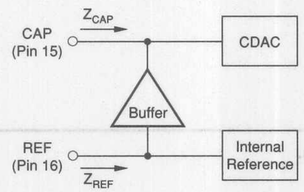


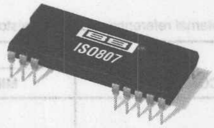
FIGURE 5. Circuit Diagrams Showing External and Internal Resistors.



	PWRD 0 REFD 0	PWRD 0 REFD 1	PWRD 1 REFD 0	PWRD 1 REFD 1
Z_{CAP} (Ω)	1	1	200	200
Z_{REF} (Ω)	6k	100M	6k	100M

FIGURE 6. Characteristic Impedances of Internal Buffer.

BURR - BROWN®



ISO807

Isolated 16-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 1500Vrms ISOLATION CONTINUOUS
- 25µS CONVERSION TIME
- 16-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

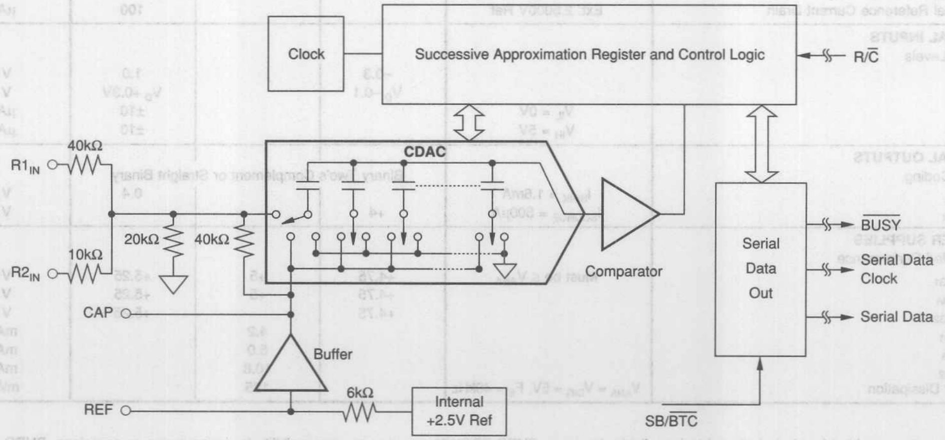
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

DESCRIPTION

The ISO807 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO807 contains a complete 16-bit capacitor based SAR, ADC with S/H, clock, reference, µP interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including ±10V, ±5V, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of –40°C to +85°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

PARAMETER	CONDITIONS	ISO807P MIN	TYP	MAX	UNITS
RESOLUTION				12	Bit
ANALOG INPUT					
Voltage Ranges			±10, 0 to +5, 0 to +4		V
Impedance			(See Table II)		
Capacitance			35		pF
THROUGHPUT SPEED					
Conversion Time				20	µs
Complete Cycle	Acquire and Convert			25	µs
Throughput Rate		40			kHz
DC ACCURACY					
Integral Linearity Error				±3	LSB(1)
Differential Linearity Error				+3, –2	LSB
No Missing Codes		15			Bits
Transition Noise(2)			0.8		LSB
Full Scale Error(3,4)				±0.5	%
Full Scale Error Drift			±7		ppm/°C
Full Scale Error Drift	Ext. 2.5000V Ref		±0.5		ppm/°C
Bipolar Zero Error(3)	±10V Range			±10	mV
Bipolar Zero Error Drift	±10V Range		±0.5		ppm/°C
Unipolar Zero Error(3)	0V to 5V, 0V to 4V Ranges			±3	mV
Unipolar Zero Error Drift	0V to 5V, 0V to 4V Ranges		±0.5		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_S)	+4.75V < V_S < +5.25V		±8		LSB
AC ACCURACY					
Spurious-Free Dynamic Range	f_{IN} = 1kHz, ±10V		100		dB(5)
Total Harmonic Distortion	f_{IN} = 1kHz, ±10V		–100		dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz, ±10V		88		dB
Signal-to-Noise	f_{IN} = 1kHz, ±10V		88		dB
Useable Bandwidth(6)			130		kHz
SAMPLING DYNAMICS					
Aperture Delay			40		ns
Aperture Jitter			20		ps
Overvoltage Recovery(7)			750		ns
REFERENCE					
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must use external buffer.)			1		µA
Internal Reference Drift			8		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref			100	µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		1.0	V
V_{IH}		V_D –0.1		V_D +0.3V	V
I_{IL}	V_{IL} = 0V			±10	µA
I_{IH}	V_{IH} = 5V			±10	µA
DIGITAL OUTPUTS					
Data Coding			Binary Two's Complement or Straight Binary		
V_{OL}	I_{SINK} = 1.6mA			0.4	V
V_{OH}	I_{SOURCE} = 500µA	+4			V
POWER SUPPLIES					
Specified Performance					
V_{DIG1}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
V_{DIG2}		+4.75		+5.25	V
I_{DIG1}			4.2		mA
I_{ANA}			5.0		mA
I_{DIG2}			10.8		mA
Power Dissipation	V_{ANA} = V_{DIG} = 5V, F_S = 40kHz		125		mW

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = -40°C$ to $+85°C$, $f_S = 40kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

PARAMETER	CONDITIONS	ISO807P MIN	TYP	MAX	UNITS
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C
Thermal Resistance, ϕ_{JA}					
Plastic DIP			75		°C/W
ISOLATION PARAMETERS					
Rated Voltage, Continuous	50Hz	1500			Vrms
Partial Discharge, 100% Test[8]	1s, 5pC	2500			Vrms
Creepage Distance (External) DIP = "P" Package			16		mm
Internal Isolation Distance			0.10		mm
Barrier Impedance			$>10^{13}$ ll 15		Ω ll pF
Leakage Current[9]	240Vrms, 60Hz			1.7	µArms
	240Vrms, 50Hz			1.4	µArms

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (9) Tested at 2500Vrms, 50Hz limit 10µA.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
CAP	V_{ANA} +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND and AGND1	±0.3V
DGND, AGND, and GND_{ISO}	1563Vrms
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ISO807P	Plastic DIP	215-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

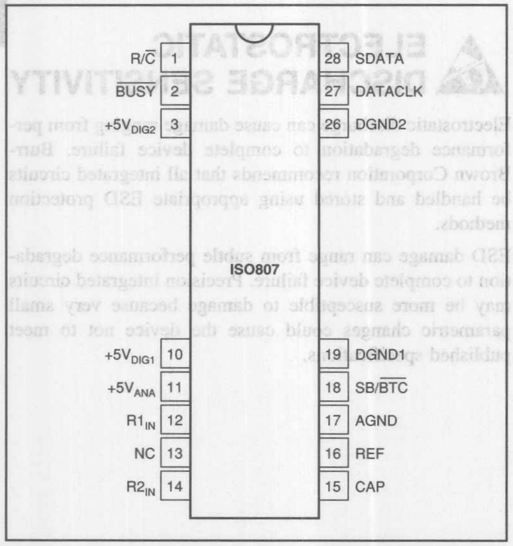
ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ISO807P	±3	83	–40°C to +85°C	Plastic DIP

1	R/$\overline{C}$	I	Read/Convert. With BUSY high, a falling edge on R/$\overline{C}$ initiates a new conversion.
2	$\overline{BUSY}$	O	At the start of conversion BUSY goes LOW and stays LOW until conversion is complete.
3	$+5V_{DIG2}$		Isolated Digital Supply Volts.
10	$+5V_{DIG1}$		Digital Supply Volts.
11	$+5V_{ANA}$		Analog Supply Volts.
12	$R1_{IN}$		Analog Input.
13	NC		No Connection. Leave unconnected.
14	$R2_{IN}$		Analog Input.
15	CAP		Reference Buffer Output. 2.2µF tantalum capacitor to ground.
16	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
17	AGND		Analog Ground.
18	SB/$\overline{BTC}$	I	Selects Straight Binary or Binary Two's Complement for Output Data Format.
19	DGND1		Digital Ground.
26	DGND2		Isolated Ground.
27	DATACLK	O	Data Clock Output.
28	SDATA	O	Serial Output Synchronized to DATACLK.

TABLE I. Pin Assignments.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	IMPEDANCE
±10V	V_{IN}	CAP	45.7kΩ
0V to 5V	AGND	V_{IN}	20.0kΩ
0V to 4V	V_{IN}	V_{IN}	21.4kΩ

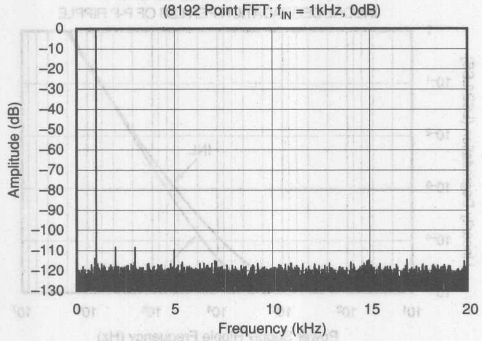
TABLE II. Input Range Connections. See also Figure 3.

R/$\overline{C}$	$\overline{BUSY}$	DATACLK	OPERATION
↓	1	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
0	↑	X	New conversion initiated without acquisition of a new signal. Data will be invalid. R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	0	X	New convert commands ignored. Conversion "n" in progress.

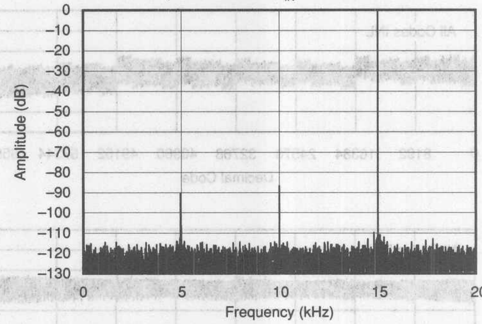
TABLE III. Control Functions

$T_A = +25°C$, $f_S = 40kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

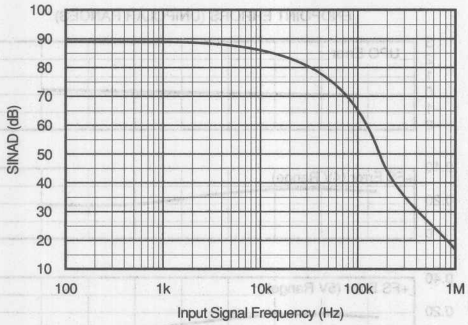
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 1kHz, 0dB)



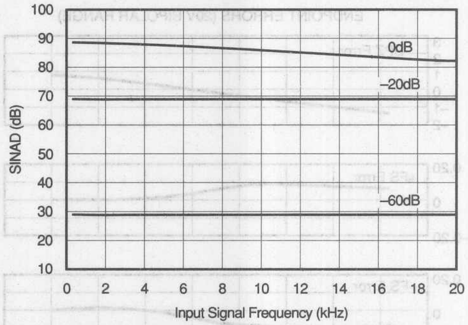
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 15kHz, 0dB)



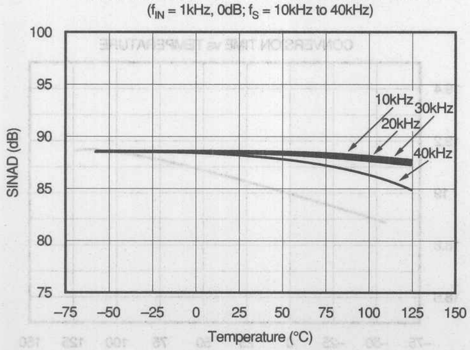
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = 0dB)



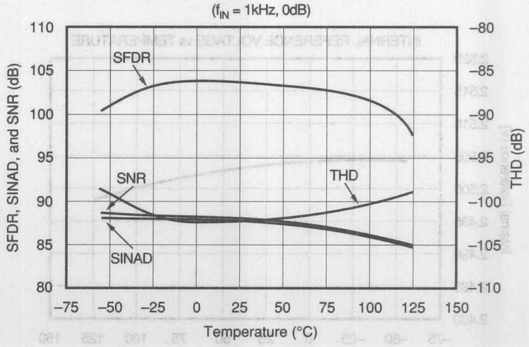
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY AND INPUT AMPLITUDE



SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
(f_{IN} = 1kHz, 0dB; f_S = 10kHz to 40kHz)

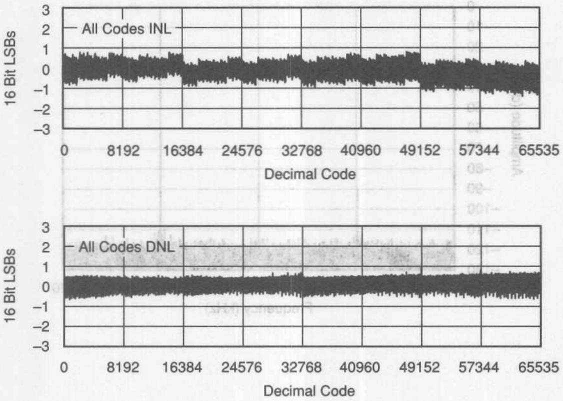


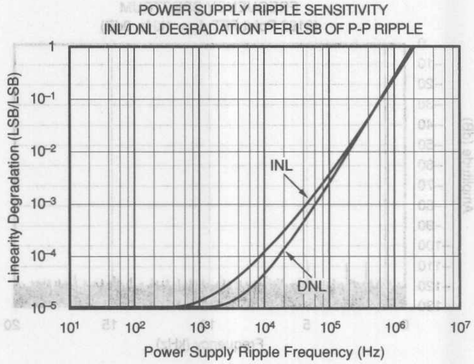
A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 1kHz, 0dB)

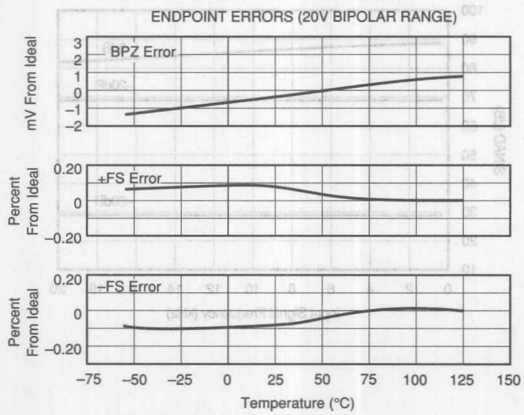


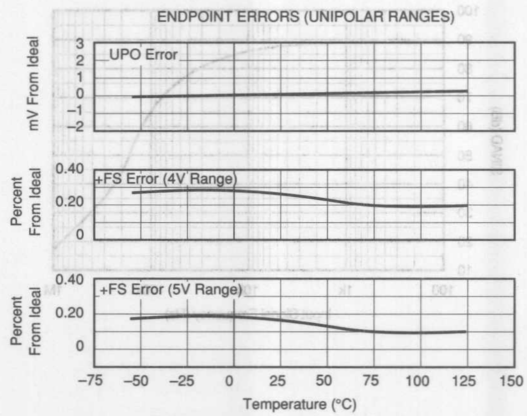
TYPICAL PERFORMANCE CURVES (CONT)

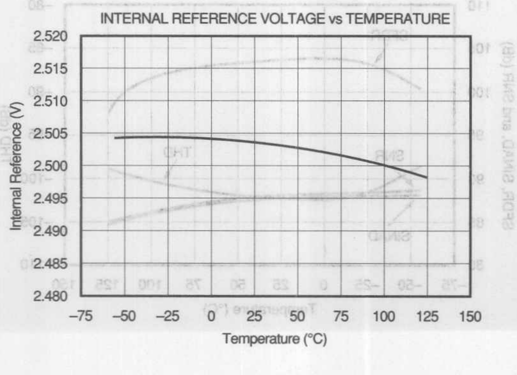
$T_A = +25°C$, $f_S = 40kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

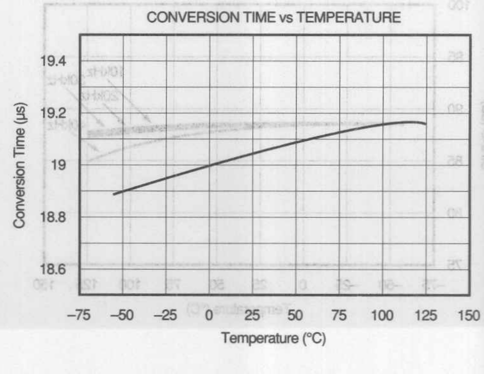












BASIC OPERATION

SERIAL OUTPUT

Figure 1 shows a basic circuit to operate the ISO807 with a ±10V input range and serial output. Taking R/$\overline{\text{C}}$ (pin 1) LOW for 40ns (12µs max) will initiate a conversion and output valid data from the previous conversion on SDATA (pin 28) synchronized to 16 clock pulses output on DATACLK (pin 27). $\overline{\text{BUSY}}$ (pin 2) will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in Binary Two's Complement format, MSB first, and will be valid on both the rising and falling edges of the data clock. $\overline{\text{BUSY}}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{\text{BUSY}}$ is LOW.

The ISO807 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The R/$\overline{\text{C}}$ (pin 1) LOW for a minimum of 40ns immediately puts the sample/hold of the ISO807 in the hold state and starts conversion 'n'. $\overline{\text{BUSY}}$ (pin 2) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{\text{BUSY}}$ LOW will be ignored. R/$\overline{\text{C}}$ must go HIGH before $\overline{\text{BUSY}}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ISO807 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. R/$\overline{\text{C}}$ is level triggered.

READING DATA

The ISO807 outputs serial data in Straight Binary or Binary Two's Complement data output format. If SB/$\overline{\text{BTC}}$ (pin 18) is HIGH, the output will be in SB format, and if LOW, the output will be in BTC format. Refer to Table IV for ideal output codes.

Reading the data through the serial port will shift the internal output registers one bit per data clock pulse.

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT			
				BINARY TWO'S COMPLEMENT (SB/$\overline{\text{BTC}}$ LOW)		STRAIGHT BINARY (SB/$\overline{\text{BTC}}$ HIGH)	
Full-Scale Range	±10	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	305µV	76µV	61µV	BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
+Full Scale (FS – 1LSB)	9.999695V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	–305µV	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full Scale	–10V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

Table IV. Output Codes and Ideal Input Voltages.

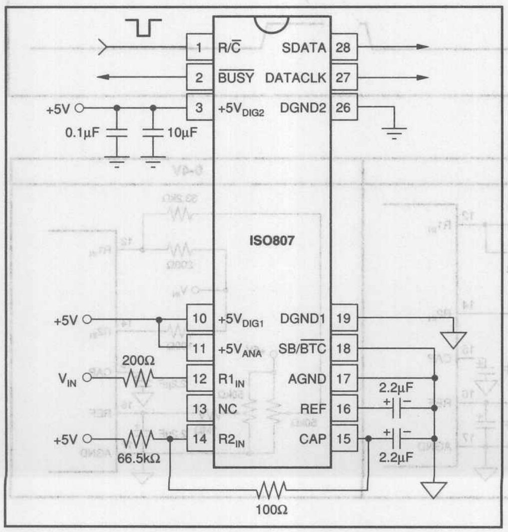


FIGURE 1. Basic ±10V Operation with Serial Output.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	0.04		12	µs
t_3	$\overline{\text{BUSY}}$ Delay from Start of Conversion		110		ns
t_4	$\overline{\text{BUSY}}$ LOW		18.8	20	µs
t_5	$\overline{\text{BUSY}}$ Delay after End of Conversion		90		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		18.8	20	µs
t_8	Acquisition Time		5		µs
t_{13}	Start of Conversion to DATACLK Delay		1.4		µs
t_{14}	DATACLK Period		1.1		µs
t_{15}	Data Valid to DATACLK HIGH Delay		75		ns
t_{16}	Data Valid after DATACLK LOW Delay		600		ns
$t_7 + t_8$	Throughput Time			25	µs

TABLE V. Conversion and Data Timing. T_A = –40°C to +85°C.

INTERNAL DATA CLOCK (During A Conversion)

The R/$\overline{C}$ (pin 1) LOW will initiate conversion 'n' and activate the internal data clock (typically 900kHz clock rate). The ISO807 will output 16 bits of valid data, MSB first, from conversion 'n-1' on SDATA (pin 28), synchronized to 16 clock pulses output on DATACLK (pin 27). The data will be valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 2) can be used to latch the data. After the 16th clock pulse, DATACLK will remain LOW until the next conversion is initiated, SDATA will also go LOW.

INPUT RANGES

The ISO807 offers three input ranges: standard ±10V and 0-5V, and a 0-4V range for complete, single supply systems. Figures 3a and 3b show the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full scale error(1) specifications are tested and guaranteed with the fixed resistors shown in Figure 3b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

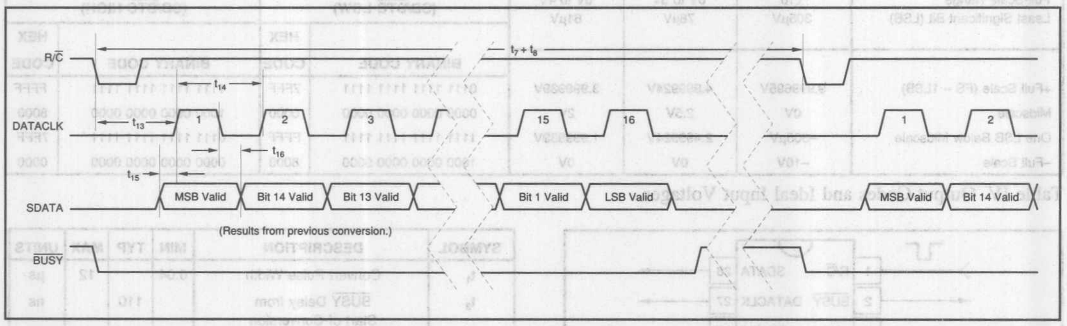


FIGURE 2. Serial Data Timing.

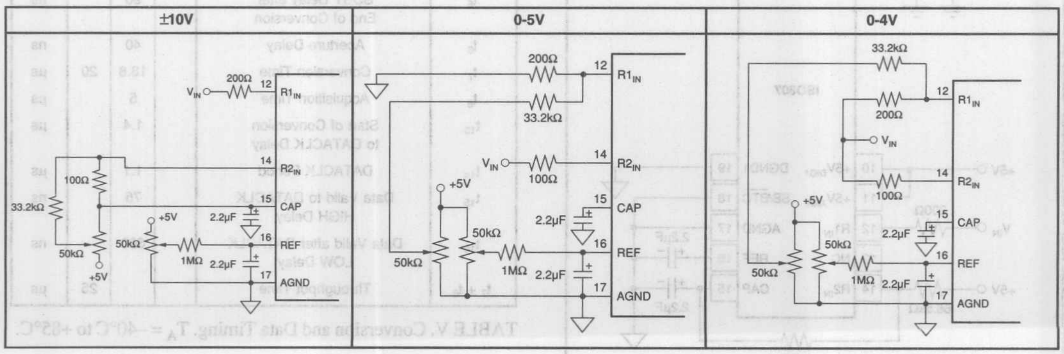


FIGURE 3a. Circuit Diagrams (With Hardware Trim).

pensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The input impedance, summarized in Table II, results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors used for each input range (see Figure 4). The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V.

Analog inputs above or below the expected range will yield either positive full scale or negative full scale digital outputs respectively. There will be no wrapping or folding over for analog inputs outside the nominal range.

Note: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

CALIBRATION

HARDWARE CALIBRATION

To calibrate the offset and gain of the ISO807 in hardware, install the resistors shown in Figure 3a. Table VI lists the hardware trim ranges relative to the input for each input range.

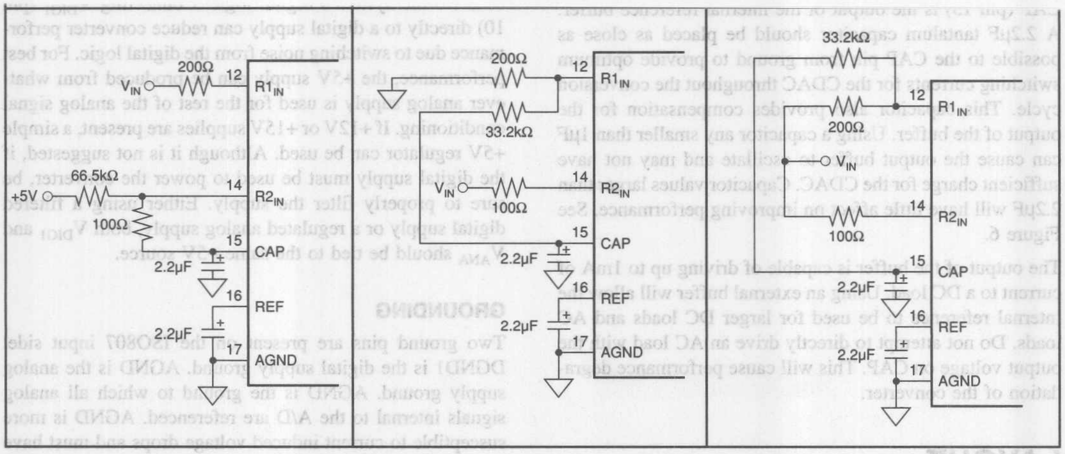


FIGURE 3b. Circuit Diagrams (Without Hardware Trim).

SOFTWARE CALIBRATION

To calibrate the offset and gain in software, no external resistors are required. However, to get the data sheet specifications for offset and gain, the resistors shown in Figure 3b are necessary. See the **No Calibration** section for more details on the external resistors. Refer to Table VII for the range of offset and gain errors with and without the external resistors.

NO CALIBRATION

See Figure 3b for circuit connections. Note that the actual voltage dropped across the external resistors is at least two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be considered when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors will be sufficient.

The external resistors shown in Figure 3b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. Not using the external resistors will result in offset and gain errors in addition to those listed in the electrical specifications section. Offset refers to the equivalent voltage of the digital output when converting with the input grounded. A positive gain error occurs when the equivalent output voltage of the digital output is larger than the analog input. Refer to Table VII for nominal ranges of gain and offset errors with and without the external resistors. Refer to Figure 4 for typical shifts in the transfer functions which occur when the external resistors are removed.

To further analyze the effects of removing any combination of the external resistors, consider Figure 5. The combination of the external and the internal resistors form a voltage divider which reduces the input signal to a 0.3125V to 2.8125V input range at the CDAC. The internal resistors are laser trimmed to high relative accuracy to meet full specifications. The actual input impedance of the internal resistor network looking into pin 12 or pin 14 however, is only accurate to ±20% due to process variations. This should be taken into account when determining the effects of removing the external resistors.

REFERENCE

The ISO807 operates with its internal 2.5V reference. The internal reference has approximately an 8ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5%).

The ISO807 also has an internal buffer for the reference voltage. See Figure 6 for characteristic impedances at the input and output of the buffer with all combinations of power down and reference down.

REF

REF (pin 16) is an input for an external reference or the output for the internal 2.5V reference. A 2.2μF tantalum capacitor should be connected as close as possible to the REF pin from ground. This capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference, degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads. See Figure 6.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 15) is the output of the internal reference buffer. A 2.2µF tantalum capacitor should be placed as close as possible to the CAP pin from ground to provide optimum switching currents for the CDAC throughout the conversion cycle. This capacitor also provides compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance. See Figure 6.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ISO807 uses 50% of its isolated power for the analog circuitry. The ISO807 front end should be considered as an analog component.

INPUT RANGE	OFFSET ADJUST RANGE (mV)	GAIN ADJUST RANGE (mV)
±10V	±15	±60
0 to 5V	±4	±30
0 to 4V	±3	±30

TABLE VI. Offset and Gain Adjust Ranges for Hardware Calibration (see Figure 3a).

INPUT RANGE (V)	OFFSET ERROR W/ RESISTORS RANGE (mV)	OFFSET ERROR W/OUT RESISTORS RANGE (mV)	OFFSET ERROR W/OUT RESISTORS TYP (mV)	GAIN ERROR W/ RESISTORS RANGE (% FS)	GAIN ERROR W/OUT RESISTORS RANGE (% FS)	GAIN ERROR W/OUT RESISTORS TYP
±10	−10 ≤ BPZ ≤ 10	0 ≤ BPZ ≤ 35	+15	−0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	−0.3 ≤ G ≤ 0.5 −0.1 ≤ G(1) ≤ 0.2	+0.05 +0.05
0 to 5	−3 ≤ UPO ≤ 3	−12 ≤ UPO ≤ −3	−7.5	−0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	−1.0 ≤ G ≤ 0.1 −0.55 ≤ G(1) ≤ −0.05	−0.2 −0.2
0 to 4	−3 ≤ UPO ≤ 3	−10.5 ≤ UPO ≤ −1.5	−6	−0.4 ≤ G ≤ 0.4 −0.15 ≤ G(1) ≤ 0.15	−1.0 ≤ G ≤ 0.1 −0.55 ≤ G(1) ≤ −0.05	−0.2 −0.2

Note: (1) High Grade.

TABLE VII. Range of Offset and Gain Errors with and without External Resistors

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG1} (pin 10) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG1} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Two ground pins are present on the ISO807 input side. DGND1 is the digital supply ground. AGND is the analog supply ground. AGND is the ground to which all analog signals internal to the A/D are referenced. AGND is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

The ground pin of the A/D should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ISO807 is approximately 5-10% of the amount on similar ADCs with the charge redistribution DAC (CDAC) architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D. Any op amp sufficient for the signal in an application will be sufficient to drive the ISO807.

The resistive front end of the ISO807 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external over voltage protection circuitry.

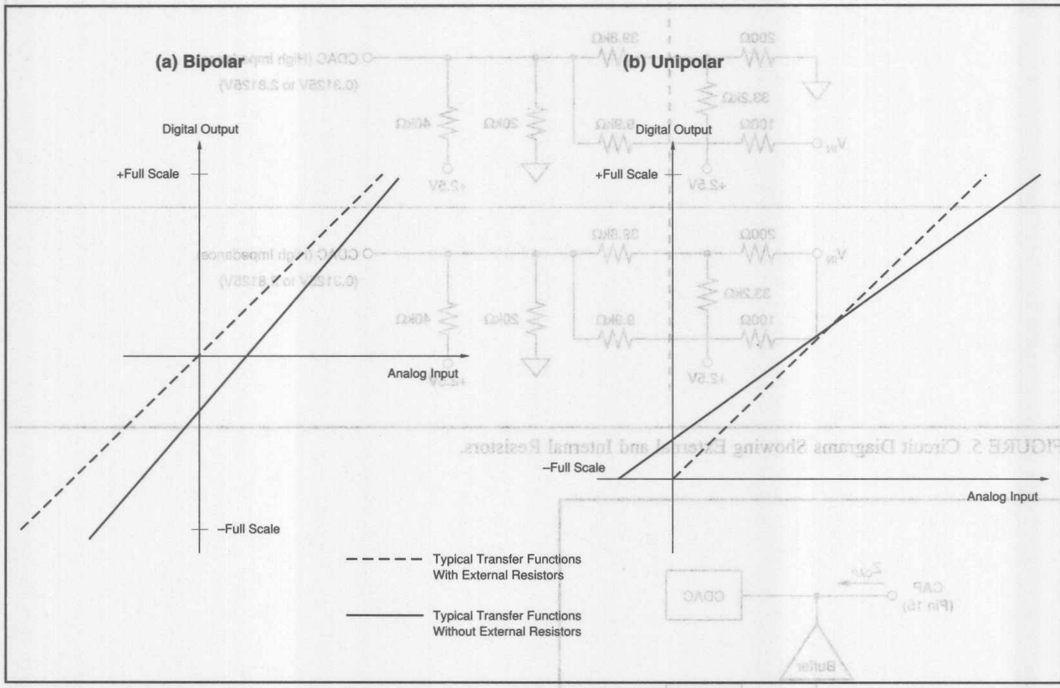


FIGURE 4. Typical Transfer Functions With and Without External Resistors.

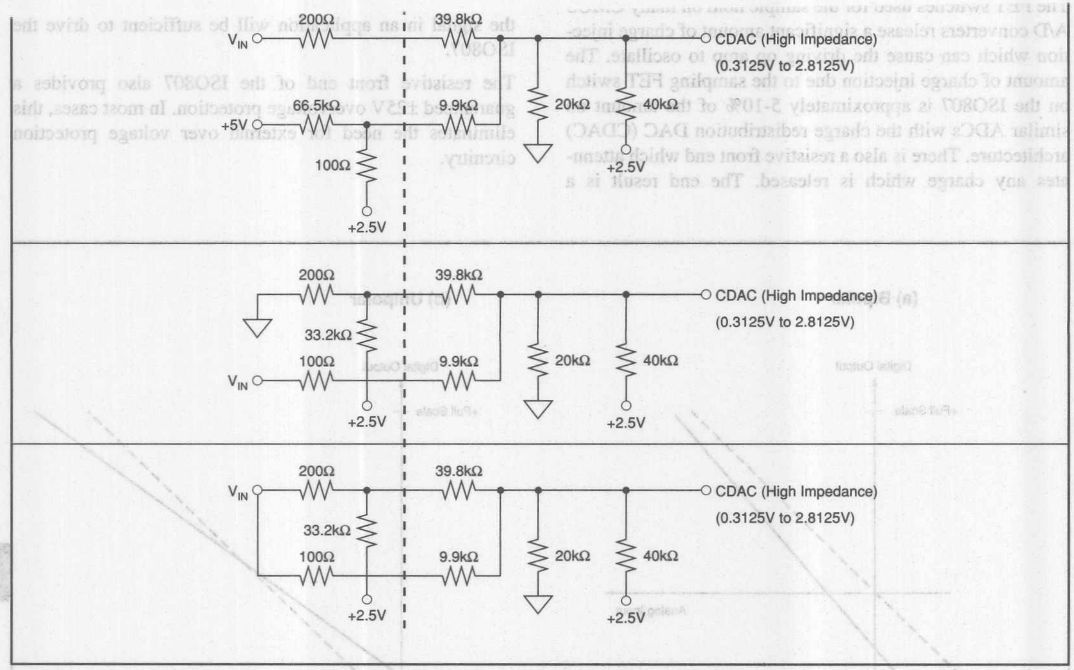
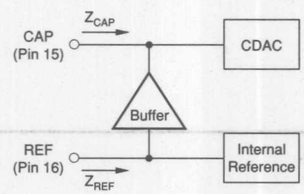


FIGURE 5. Circuit Diagrams Showing External and Internal Resistors.



	PWRD 0 REFD 0	PWRD 0 REFD 1	PWRD 1 REFD 0	PWRD 1 REFD 1
Z_{CAP} (Ω)	1	1	200	200
Z_{REF} (Ω)	6k	100M	6k	100M

FIGURE 6. Characteristic Impedances of Internal Buffer.

BURR - BROWN®

ISO808

Isolated 12-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 100kHz SAMPLING RATE
- 1500Vrms ISOLATION CONTINUOUS
- 10µS CONVERSION TIME
- 12-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

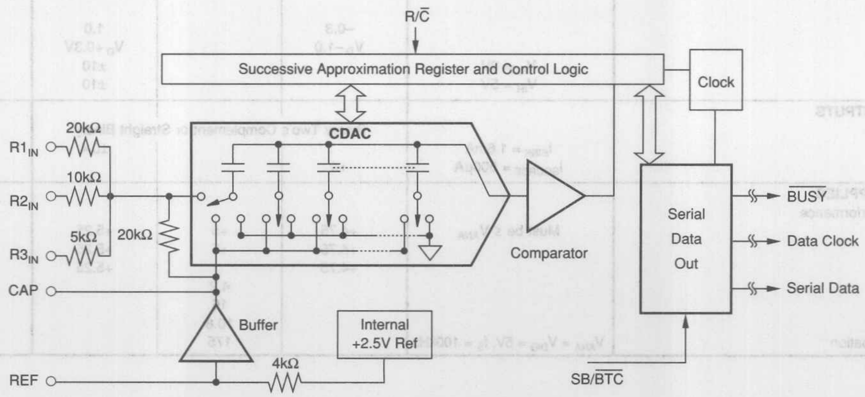
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

DESCRIPTION

The ISO808 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO808 contains a complete 12-bit capacitor based SAR, ADC with S/H, clock, reference, µP interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including ±10V, ±5V, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of –40°C to +85°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

PARAMETER	CONDITIONS	ISO808P MIN	ISO808P TYP	ISO808P MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Ranges			±10V, 0V to 5V, etc. (See Table I)		
Impedance			See Table I		
Capacitance			35		pF
THROUGHPUT SPEED					
Conversion Time			5.7	8	µs
Complete Cycle	Acquire and Convert			10	µs
Throughput Rate		100			kHz
DC ACCURACY					
Integral Linearity Error				±0.9	LSB(1)
Differential Linearity Error				±0.9	LSB
No Missing Codes			Guaranteed		
Transition Noise(2)			0.1		LSB
Full Scale Error(3,4)				±0.5	%
Full Scale Error Drift			±7		ppm/°C
Full Scale Error Drift	Ext. 2.5000V Ref		±2		ppm/°C
Bipolar Zero Error(3)	Bipolar Ranges			±10	mV
Bipolar Zero Error Drift	Bipolar Ranges			±2	ppm/°C
Unipolar Zero Error(3)	Unipolar Ranges			±5	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±0.5	LSB
AC ACCURACY					
Spurious-Free Dynamic Range	f_{IN} = 45kHz ±10V		90		dB(5)
Total Harmonic Distortion	f_{IN} = 45kHz ±10V		–90		dB
Signal-to-(Noise+Distortion)	f_{IN} = 45kHz ±10V		73		dB
Signal-to-Noise	f_{IN} = 45kHz ±10V		73		dB
Full-Power Bandwidth(6)			250		kHz
SAMPLING DYNAMICS					
Aperture Delay			40		ns
Aperture Jitter			Sufficient to meet AC specs		ns
Overvoltage Recovery(7)			150		ns
REFERENCE					
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must use external buffer)			1		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref			100	µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		1.0	V
V_{IH}		V_D –1.0		V_D +0.3V	V
I_{IL}	V_{IL} = 0V			±10	µA
I_{IH}	V_{IH} = 5V			±10	µA
DIGITAL OUTPUTS					
Data Coding			Binary Two's Complement or Straight Binary		
V_{OL}	I_{SINK} = 1.6mA			±0.4	V
V_{OH}	I_{SOURCE} = 500µA	+4			V
POWER SUPPLIES					
Specified Performance					
V_{DIG1}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
V_{DIG2}		+4.75		+5.25	V
I_{DIG1}			4.2		mA
I_{ANA}			16		mA
I_{DIG2}			10.8		mA
Power Dissipation	V_{ANA} = V_{DIG} = 5V, f_S = 100kHz		175		mW

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

PARAMETER	CONDITIONS	ISO808P MIN	TYP	MAX	UNITS
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C
Thermal Resistance, ϕ_{JA}					
Plastic DIP			75		°C/W
ISOLATION PARAMETERS					
Rated Voltage, Continuous	50Hz	1500			Vrms
Partial Discharge, 100% Test[8]	1s, 5pC	2500			Vrms
Creepage Distance (External) DIP = "P" Package			16		mm
Internal Isolation Distance			0.10		mm
Barrier Impedance			$>10^{13} \parallel 15$		Ω ∥ pF
Leakage Current[9]	240Vrms, 60Hz			1.7	µArms
	240Vrms, 50Hz			1.4	µArms

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (9) Tested at 2500Vrms, 50Hz limit 10µA.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
$R3_{IN}$	±25V
CAP	V_{ANA} +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND and AGND	±0.3V
DGND, AGND, and GND_{ISO}	1563Vrms
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	700mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ISO808P	28-Pin Plastic DIP	215-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

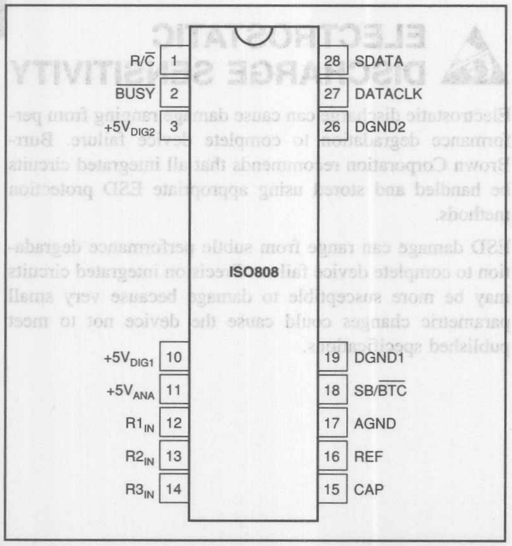
ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE (°C)	PACKAGE
ISO808P	±0.9	70	–40°C to +85°C	28-Pin Plastic DIP

1	$R\overline{C}$	I	Read/$\overline{\text{Convert}}$. With $\overline{\text{BUSY}}$ high, a falling edge on $R/\overline{C}$ initiates a new conversion.
2	$\overline{\text{BUSY}}$	O	At the start of conversion $\overline{\text{BUSY}}$ goes LOW and stays LOW until conversion is complete.
3	$+5V_{DIG2}$		Isolated Digital Supply Volts.
10	$+5V_{DIG1}$		Digital Supply Volts.
11	$+5V_{ANA}$		Analog Supply Volts.
12	$R1_{IN}$		Analog Input.
13	$R2_{N}$		Analog Input.
14	$R3_{N}$		Analog Input.
15	CAP		Reference Buffer Output. 2.2µF tantalum capacitor to ground.
16	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
17	AGND		Analog Ground.
18	$SB/\overline{BTC}$	I	Selects Straight Binary or Binary Two's Compliment for output data format.
19	DGND1		Digital Ground.
26	DGND2		Isolated Ground.
27	DATACLK	O	Data Clock Output.
28	SDATA	O	Serial Output Synchronized to DATACLK.

TABLE I. Pin Assignments.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ TO	IMPEDANCE
±10V	V_{IN}	AGND	CAP	22.9kΩ
±5V	AGND	V_{IN}	CAP	13.3kΩ
±3.33	V_{IN}	V_{IN}	CAP	10.7kΩ
0V to 10V	AGND	V_{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V_{IN}	10.0kΩ
0V to 4V	V_{IN}	AGND	V_{IN}	10.7kΩ

TABLE I. Input Range Connections. See Figure 3 for complete information.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		4500	ns
t_2	$\overline{\text{BUSY}}$ Delay		120		ns
t_3	$\overline{\text{BUSY}}$ LOW			8	µs
t_4	$\overline{\text{BUSY}}$ Delay after End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		5.7	8	µs
t_7	Acquisition Time			2	µs
$t_6 + t_7$	Throughput Time		9	10	µs
t_8	$R/\overline{C}$ LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid after DATACLK LOW Delay	100	125		ns

TABLE II. Conversion and Data Timing. $T_A = -40°C$ to $+85°C$.

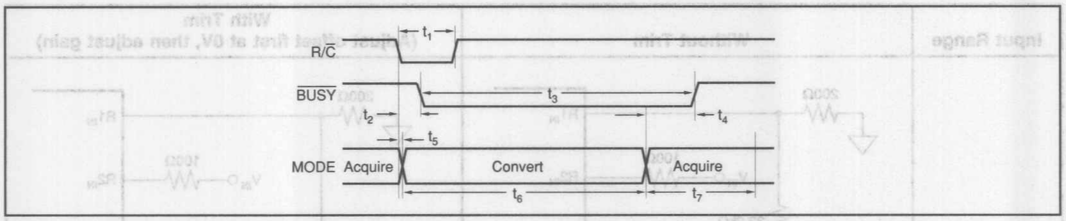


FIGURE 1. Basic Conversion Timing.

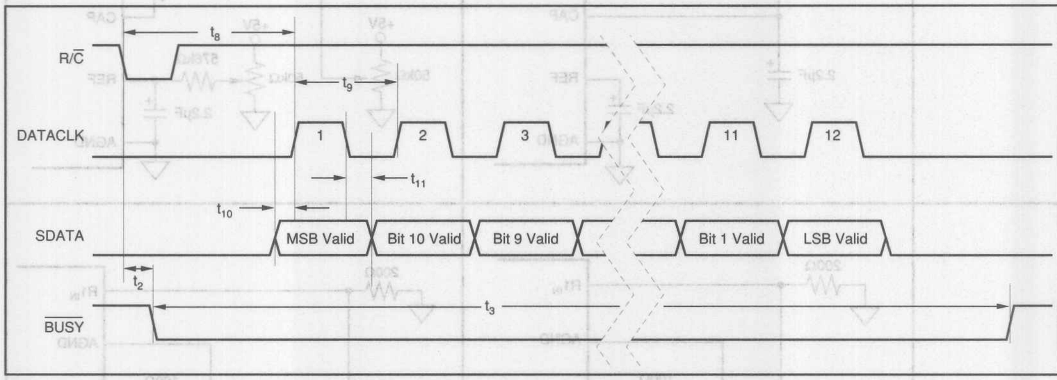


FIGURE 2. Serial Data Timing.

SPECIFIC FUNCTION	R/C̄	BUSY	DATACLK	SB/BTC	OPERATION
Initiate Conversion and Output Data	0	1	Output	X	Initiates Conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
	1 > 0	1	Output	X	Initiates Conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
Incorrect Conversions	0	0 > 1	X	X	R/C̄ must be HIGH or a new conversion will be initiated without time for acquisition.
Selecting Output Format	X	X	X	0	Serial Data is output in Binary Two's Complement format.
	X	X	X	1	Serial Data is output in Straight Binary format.

TABLE III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT: BINARY TWO'S COMPLEMENT (SB/BTC LOW) HEX BINARY CODE	CODE	DIGITAL OUTPUT: STRAIGHT BINARY (SB/BTC HIGH) HEX BINARY CODE	CODE
Full-Scale Range	±10	±5	±3.33V	0V to 5V	0V to 10V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	2.44mV	1.63mV	1.22mV	2.44mV	0.98mV				
+Full Scale (FS – 1LSB)	9.99512V	4.99756V	3.33171V	4.99878V	9.99756V	3.99902V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0V	0V	0V	2.5V	5V	2V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	–4.88mV	–2.44mV	–1.63mV	2.49878V	4.99756V	1.99902V	1111 1111 1111	FFF	0111 1111 1111	7FF
–Full Scale	–10V	–5V	–3.333333V	0V	0V	0V	1000 0000 0000	800	0000 0000 0000	000

TABLE IV. Output Codes and Ideal Input Voltages.

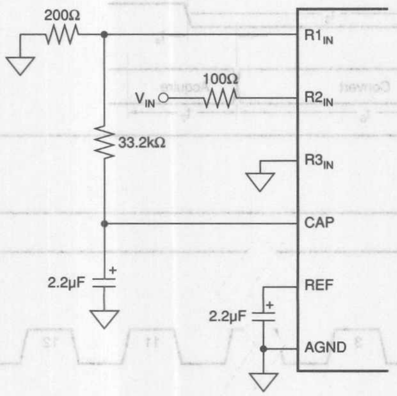
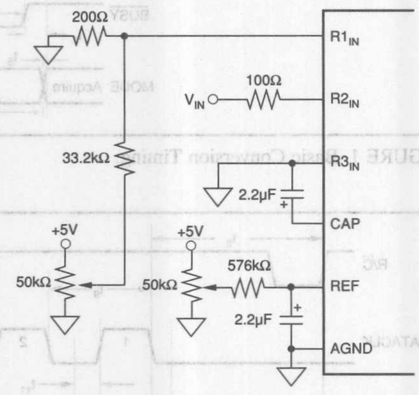
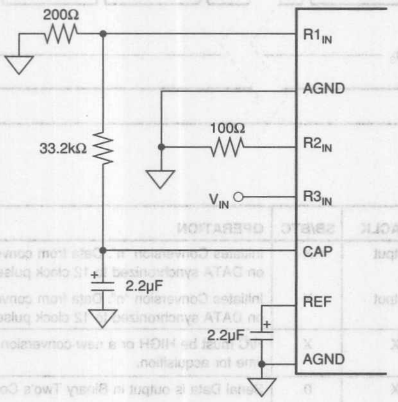
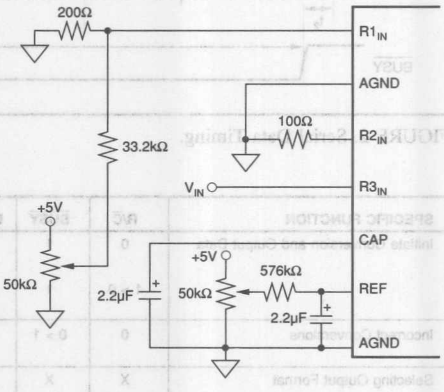
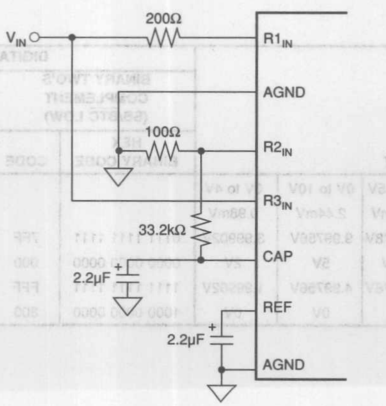
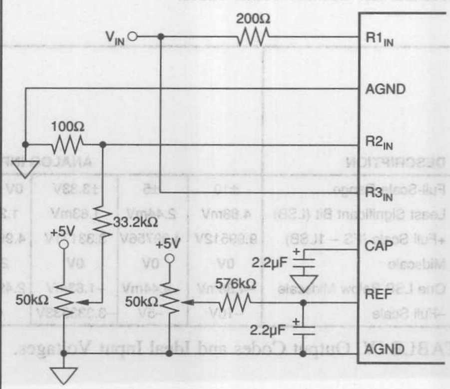
<table>
<tr><th>Input Range</th><th>Without Trim</th><th>With Trim
(Adjust offset first at 0V, then adjust gain)</th></tr>
<tr><td>0V – 10V</td><td>
</td><td>
</td></tr>
<tr><td>0V – 5V</td><td>
</td><td>
</td></tr>
<tr><td>0V – 4V</td><td>
</td><td>
</td></tr>
</table>

FIGURE 3a. Offset/Gain Circuits for Unipolar Input Ranges.

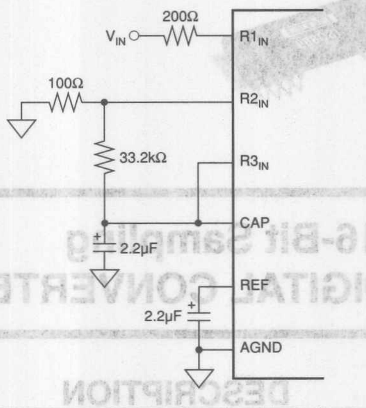
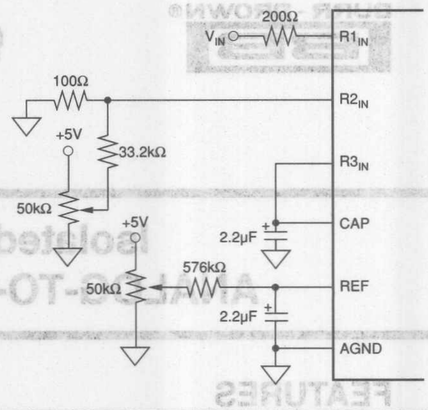
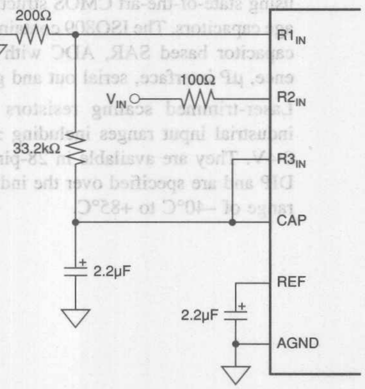
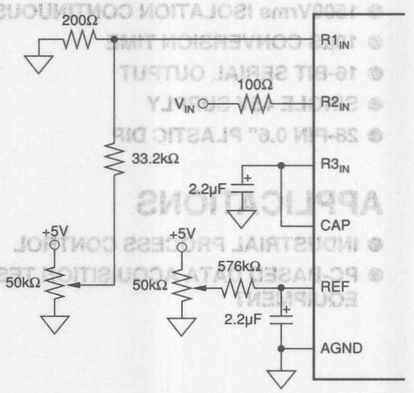
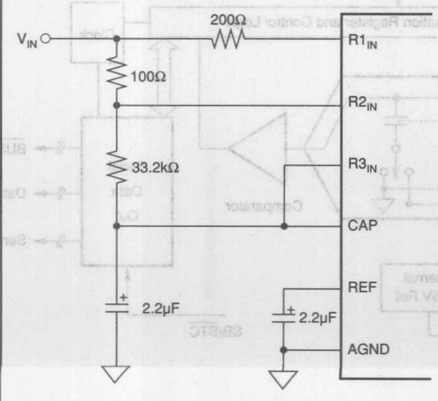
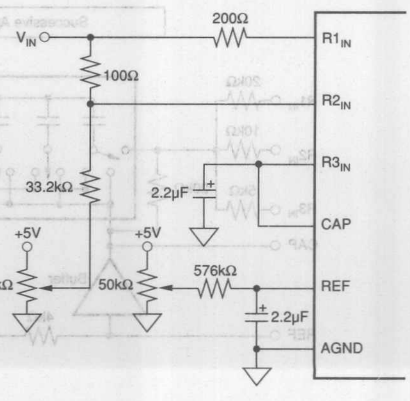
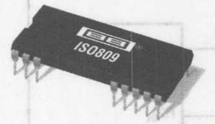
<table>
<tr><th>Input Range</th><th>Without Trim</th><th>With Trim
(Adjust offset first at 0V, then adjust gain)</th></tr>
<tr><td>±10V</td><td>
</td><td>
</td></tr>
<tr><td>±5V</td><td>
</td><td>
</td></tr>
<tr><td>±3.33V</td><td>
</td><td>
</td></tr>
</table>

FIGURE 3b. Offset/Gain Circuits for Bipolar Input Ranges.

BURR - BROWN®



ISO809

Isolated 16-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 100kHz SAMPLING RATE
- 1500Vrms ISOLATION CONTINUOUS
- 10µS CONVERSION TIME
- 16-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

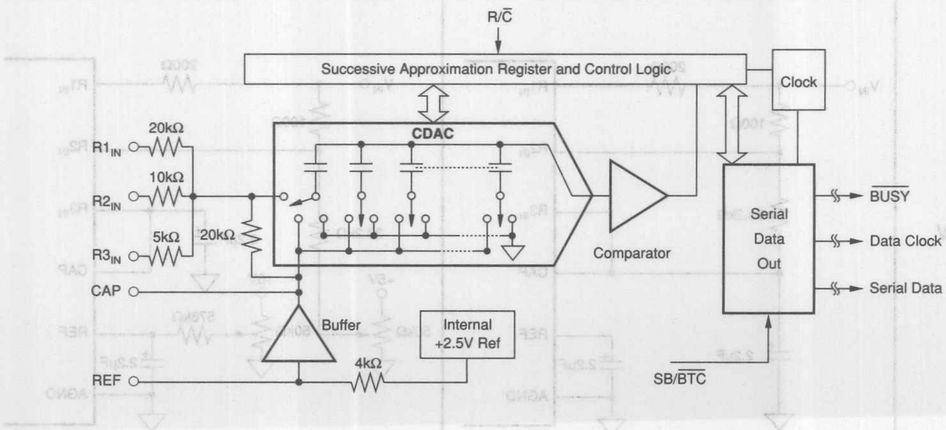
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

DESCRIPTION

The ISO809 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO809 contains a complete 16-bit capacitor based SAR, ADC with S/H, clock, reference, µP interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including ±10V, ±5V, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of –40°C to +85°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At $T_A = -40°C$ to $+85°C$, $f_S = 100kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

PARAMETER	CONDITIONS	ISO809P MIN	TYP	MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Ranges			±10V, 0V to 5V, etc. (See Table I)		
Impedance			See Table I		
Capacitance			35		pF
THROUGHPUT SPEED					
Conversion Time			7.6	8	µs
Complete Cycle	Acquire and Convert			10	µs
Throughput Rate		100			kHz
DC ACCURACY					
Integral Linearity Error				±4	LSB(1)
Differential Linearity Error				±4	LSB
No Missing Codes		15			
Transition Noise(2)			1.3		LSB
Full Scale Error(3,4)				±0.5	%
Full Scale Error Drift			±7		ppm/°C
Full Scale Error Drift	Ext. 2.5000V Ref		±2		ppm/°C
Bipolar Zero Error(3)	Bipolar Ranges			±10	mV
Bipolar Zero Error Drift	Bipolar Ranges		±2		ppm/°C
Unipolar Zero Error(3)	Unipolar Ranges			3	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2		ppm/°C
Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_D$)	$+4.75V < V_D < +5.25V$			8	LSB
AC ACCURACY					
Spurious-Free Dynamic Range	$f_{IN} = 45kHz$ ±10V		100		dB(5)
Total Harmonic Distortion	$f_{IN} = 45kHz$ ±10V		–100		dB
Signal-to-(Noise+Distortion)	$f_{IN} = 45kHz$ ±10V		88		dB
Signal-to-Noise	$f_{IN} = 45kHz$ ±10V		88		dB
Full-Power Bandwidth(6)			250		kHz
SAMPLING DYNAMICS					
Aperture Delay			40		ns
Aperture Jitter			Sufficient to meet AC specs		ns
Overvoltage Recovery(7)			150		ns
REFERENCE					
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must use external buffer)			1		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref			100	µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		1.0	V
V_{IH}		V_D –1.0		V_D +0.3V	V
I_{IL}	$V_{IL} = 0V$			±10	µA
I_{IH}	$V_{IH} = 5V$			±10	µA
DIGITAL OUTPUTS					
Data Coding			Binary Two's Complement or Straight Binary		
V_{OL}	$I_{SINK} = 1.6mA$			±0.4	V
V_{OH}	$I_{SOURCE} = 500\mu A$	+4			V
POWER SUPPLIES					
Specified Performance					
V_{DIG1}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
V_{DIG2}		+4.75	+5	+5.25	V
I_{DIG1}			4.2		mA
I_{ANA}			21		mA
I_{DIG2}			10.8		mA
Power Dissipation	$V_{ANA} = V_{DIG} = 5V$, $f_S = 100kHz$		175		mW

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

PARAMETER	CONDITIONS	ISO809P MIN	TYP	MAX	UNITS
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C
Thermal Resistance, ϕ_{JA}					
Plastic DIP			75		°C/W
ISOLATION PARAMETERS					
Rated Voltage, Continuous	50Hz	1500			Vrms
Partial Discharge, 100% Test(8)	1s, 5pC	2500			Vrms
Creepage Distance (External) DIP = "P" Package			16		mm
Internal Isolation Distance			0.10		mm
Barrier Impedance			$>10^{13} \parallel 15$		Ω ‖ pF
Leakage Current(9)	240Vrms, 60Hz			1.2	µArms
	240Vrms, 50Hz			1.0	µArms

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (9) Tested at 2500Vrms, 50Hz limit 10µA.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
$R3_{IN}$	±25V
CAP	V_{ANA} +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND and AGND	±0.3V
DGND, AGND, and GND_{ISO}	1563Vrms
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	700mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO809P	28-Pin Plastic DIP	215-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

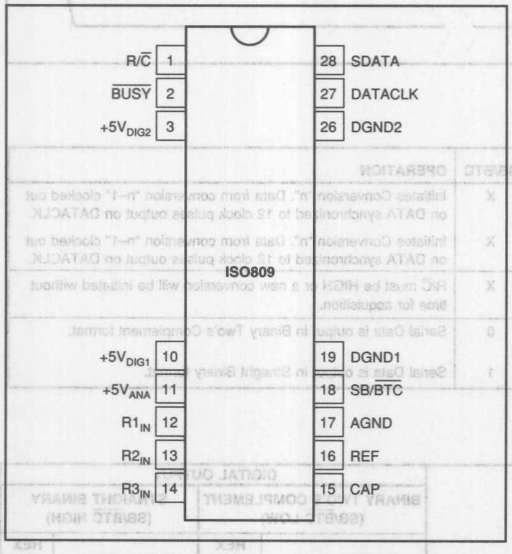
ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE (°C)	PACKAGE
ISO809P	±4	83	–40°C to +85°C	28-Pin Plastic DIP

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	$R/\overline{C}$	I	Read/$\overline{\text{Convert}}$. With $\overline{\text{BUSY}}$ high, a falling edge on $R/\overline{C}$ initiates a new conversion.
2	$\overline{\text{BUSY}}$	O	At the start of conversion $\overline{\text{BUSY}}$ goes LOW and stays LOW until conversion is complete.
3	$+5V_{DIG2}$		Isolated Digital Supply Volts.
10	$+5V_{DIG1}$		Digital Supply Volts.
11	$+5V_{ANA}$		Analog Supply Volts.
12	$R1_{IN}$		Analog Input.
13	$R2_{N}$		Analog Input.
14	$R3_{N}$		Analog Input.
15	CAP		Reference Buffer Output. 2.2µF tantalum capacitor to ground.
16	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
17	AGND		Analog Ground.
18	$SB/\overline{BTC}$	I	Selects Straight Binary or Binary Two's Complement for output data format.
19	DGND1		Digital Ground.
26	DGND2		Isolated Ground.
27	DATACLK	O	Data Clock Output.
28	SDATA	O	Serial Output Synchronized to DATACLK.

TABLE I. Pin Assignments.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ TO	IMPEDANCE
±10V	V_{IN}	AGND	CAP	22.9kΩ
±5V	AGND	V_{IN}	CAP	13.3kΩ
±3.33	V_{IN}	V_{IN}	CAP	10.7kΩ
0V to 10V	AGND	V_{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V_{IN}	10.0kΩ
0V to 4V	V_{IN}	AGND	V_{IN}	10.7kΩ

TABLE I. Input Range Connections. See Figure 3 for complete information.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		4500	ns
t_2	$\overline{\text{BUSY}}$ Delay		120		ns
t_3	$\overline{\text{BUSY}}$ LOW			8	µs
t_4	$\overline{\text{BUSY}}$ Delay after End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		5.7	8	µs
t_7	Acquisition Time			2	µs
$t_6 + t_7$	Throughput Time		9	10	µs
t_8	$R/\overline{C}$ LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid after DATACLK LOW Delay	100	125		ns

TABLE II. Conversion and Data Timing. $T_A = -40°C$ to $+85°C$.

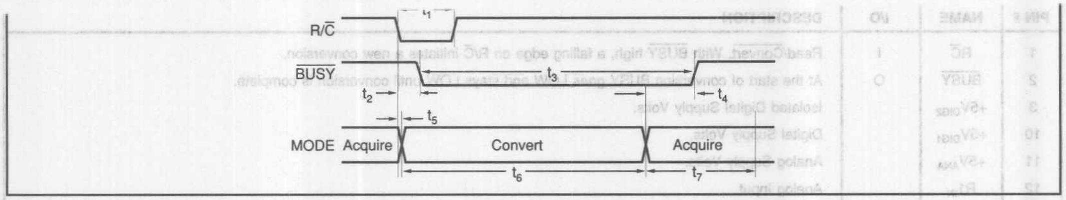


FIGURE 1. Basic Conversion Timing.

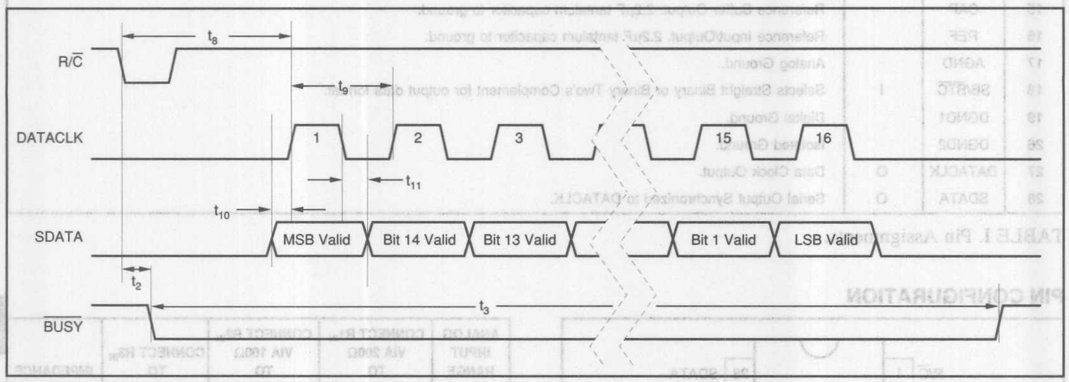


FIGURE 2. Serial Data Timing.

SPECIFIC FUNCTION	R/C̄	BUSY	DATACLK	SB/BTC	OPERATION
Initiate Conversion and Output Data	0	1	Output	X	Initiates Conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
	1 > 0	1	Output	X	Initiates Conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
Incorrect Conversions	0	0 > 1	X	X	R/C̄ must be HIGH or a new conversion will be initiated without time for acquisition.
Selecting Output Format	X	X	X	0	Serial Data is output in Binary Two's Complement format.
	X	X	X	1	Serial Data is output in Straight Binary format.

TABLE III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT: BINARY TWO'S COMPLEMENT (SB/BTC LOW) BINARY CODE	HEX CODE	DIGITAL OUTPUT: STRAIGHT BINARY (SB/BTC HIGH) BINARY CODE	HEX CODE
Full-Scale Range	±10	±5	±3.33V	0V to 10V	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	305µV	153µV	102µV	153µV	76µV	61µV				
+Full Scale (FS – 1LSB)	9.999695V	4.999847V	3.333231V	9.999847V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	–305µV	–153µV	–102µV	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full Scale	–10V	–5V	–3.333333V	0V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

TABLE IV. Output Codes and Ideal Input Voltages.

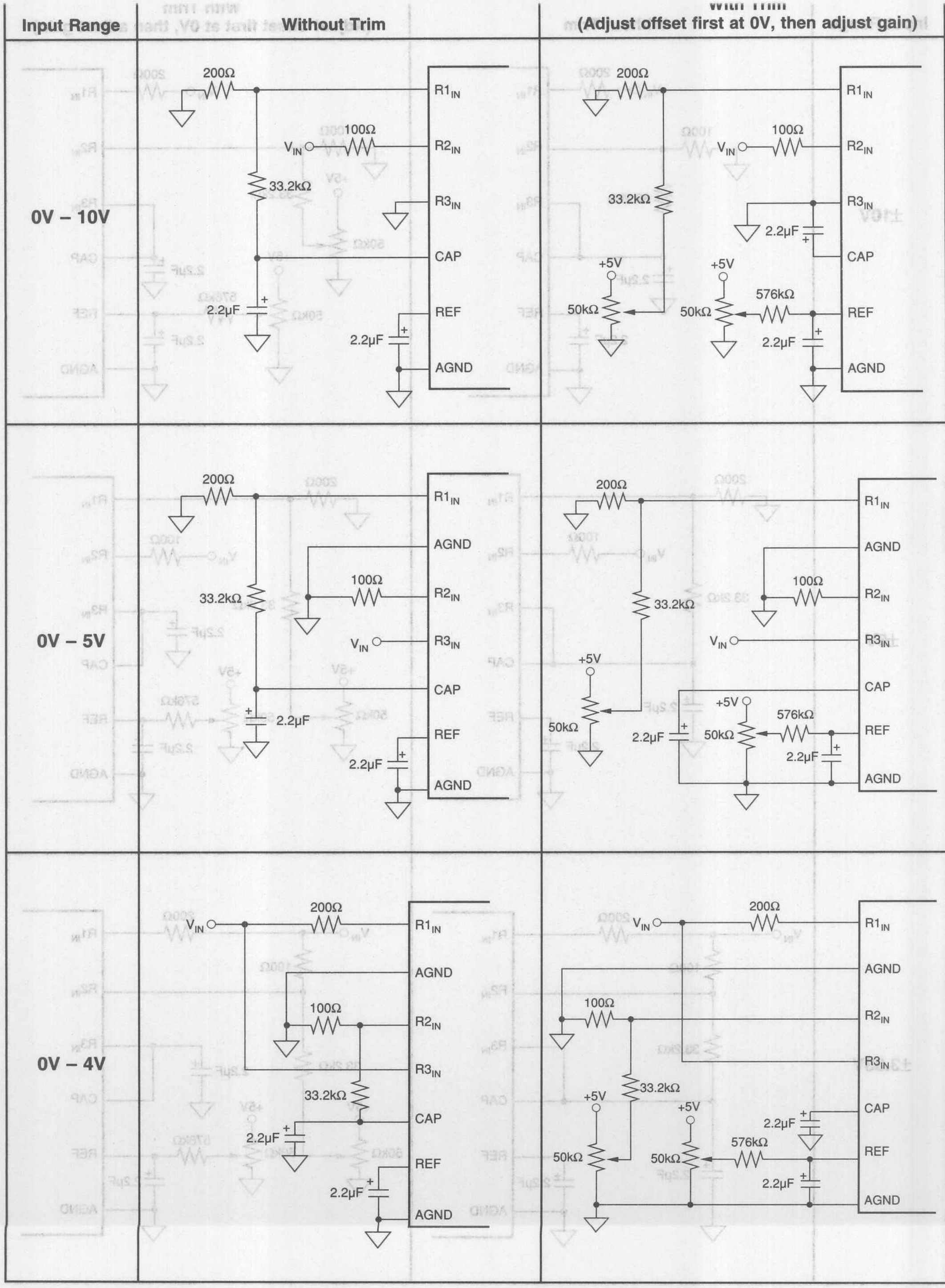


FIGURE 3a. Offset/Gain Circuits for Unipolar Input Ranges.

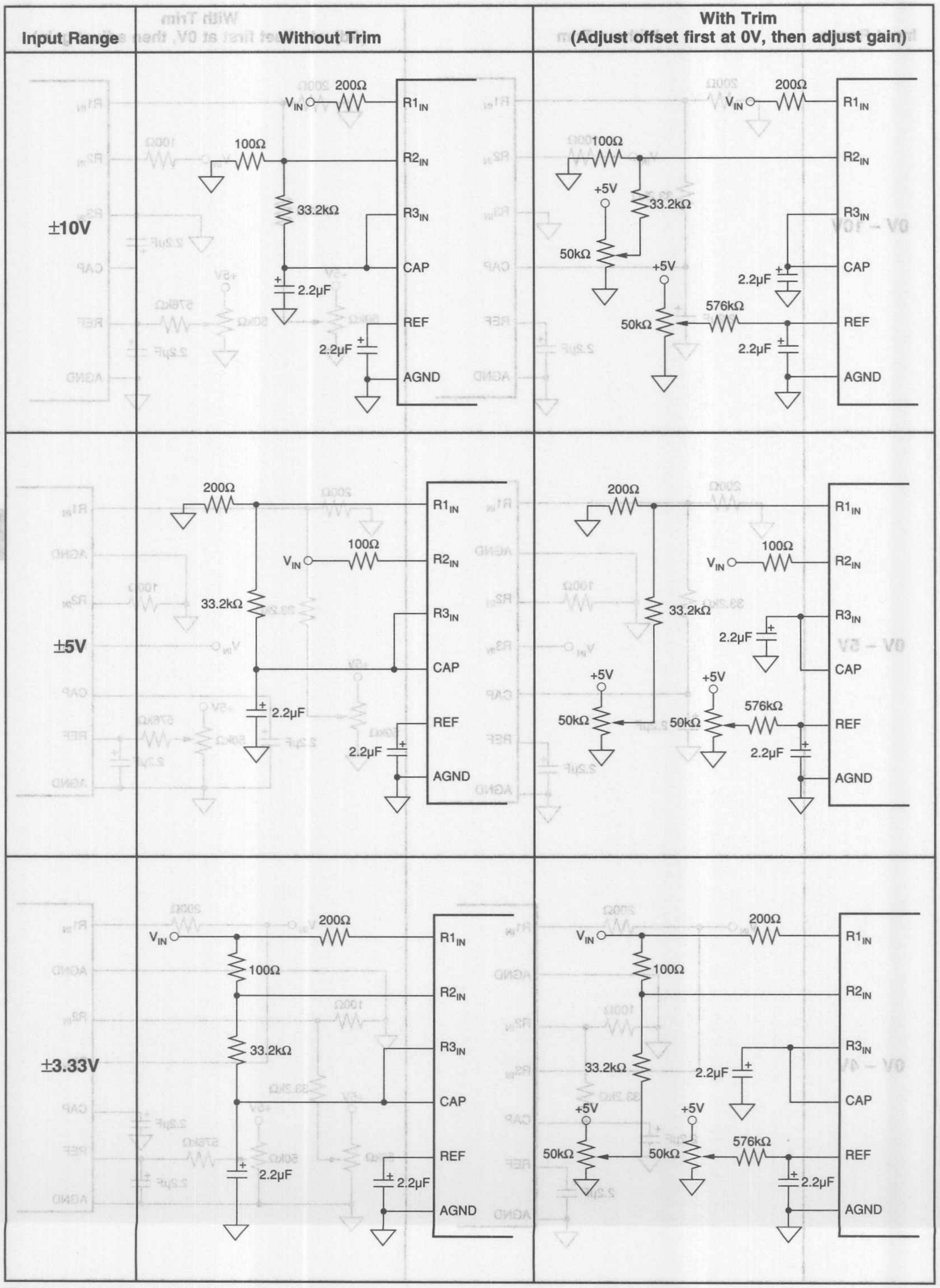


FIGURE 3b. Offset/Gain Circuits for Bipolar Input Ranges.

BURR - BROWN®

IXR100

Isolated, Self-Powered, Temperature Sensor Conditioning 4-20mA TWO-WIRE TRANSMITTER

FEATURES

- 1500Vrms ISOLATION
- TRUE TWO-WIRE OPERATION : Power and Signal on One Wire Pair
- RESISTANCE OR VOLTAGE INPUT
- DUAL MATCHED CURRENT SOURCES: 400µA at 7V
- WIDE SUPPLY RANGE 12V TO 36V
- PT100 RTD LINEARIZATION

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: All Types of Isolated Transmitters; Pt100 RTD Thermocouple Inputs Current Shunt (mV) Inputs
- ISOLATED DUAL CURRENT SOURCES
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY MONITORING
- GROUND LOOP ELIMINATION

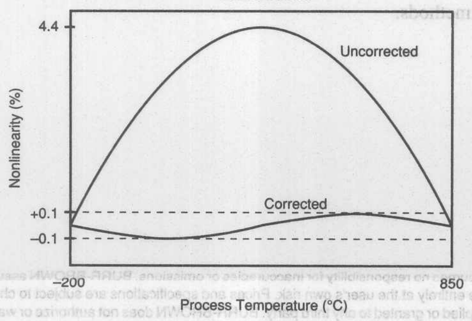
DESCRIPTION

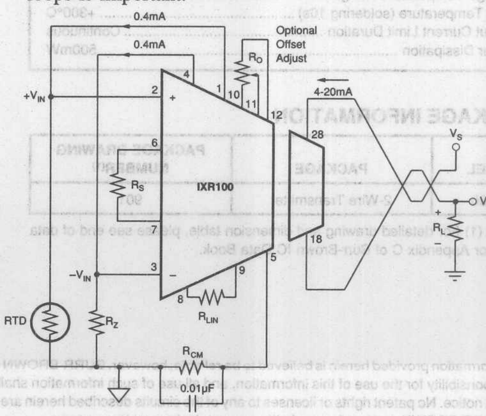
The IXR100 is an isolated 2-wire transmitter featuring loop powered operation and resistive temperature sensor conditioning (excitation and linearization). It contains a DC/DC convertor, high accuracy instrumentation amplifier with single resistor programmable span and linearization, and dual matched excitation current sources. This combination is ideally suited to a range of transducers such as thermocouples, RTDs, thermistors and strain gages. The small size makes it ideal for use in head mounted isolated temperature transmitters as well as rack and rail mounted equipment.

The isolated two-wire transmitter allows signal transmission and device power to be supplied on a single wire-pair by modulating the power supply current with the isolated signal source. The transmitter is resistant to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers and industrial equipment.

It can be used by OEMs producing isolated transmitter modules or by data acquisition system manufacturers. The IXR100 is also useful for general purpose isolated current transmission where the elimination of ground loops is important.

Pt100 NONLINEARITY CORRECTION USING IXR100





International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

At V_S = +24V, T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	IXR100 MIN	TYP	MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS					
Output Current	Linear Operating Region	4		20	mA
Output Current Limit			32		mA
Loop Supply Voltage		11.6		36	VDC
Load Resistance		$R_{LOAD} = (V_S - 11.6)/I_O$			Ω
ZERO					
Initial Error (1)	V_{IN} = 0, R_S = ∞			300	µA
vs Temperature				200	ppm FSR/°C
SPAN					
Output Current Equation	R_S in Ω, V_{IN} in V		I_O = 4mA + [0.016 + (40/R_S)] (V_{IN})		
Span Equation			S = [0.016 + (40/R_S)]		A/V
Untrimmed Error	(1)	−2.5		0	%
vs Temperature	Excluding TCR of R_S		50	100	ppm/°C
Nonlinearity : EMF Input	(2)		0.01	0.025	%FSR
: Pt100 Input	(3)		0.1		%FSR
INPUT					
Voltage Range	R_S = ∞		1		V
Common-Mode Range	V_{IN+}, V_{IN-} with Respect to COM	2		4	V
Offset Voltage			0.5	2.5	mV
vs Temperature			3	5	µV/°C
vs Supply			100		dB
CURRENT SOURCES					
Magnitude			0.4		mA
Accuracy				1	%
vs Temperature			50	100	ppm/°C
Match				0.5	%
vs Temperature			25	50	ppm/°C
DYNAMIC RESPONSE					
Settling Time	To 0.1% of Span		500		ms
TEMPERATURE RANGE					
Operating		−20		+70	°C
Storage		−40		+85	°C
ISOLATION	V_{ISO}	1000 JP			Vrms
Isolation Voltage	V_{ISO}	1500 KP			Vrms

NOTES: (1) Can be adjusted to zero. (2) End point span non-linearity. (3) End point, corrected span non-linearity with a Pt100 RTD input operated from −200°C to +850°C.

ABSOLUTE MAXIMUM RATINGS

Power Supply (+V_S −I_{OUT})	40V
Input Voltage (Com to V_{IN})	9V
Storage Temperature Range	−40°C to +85°C
Lead Temperature (soldering 10s)	+300°C
Output Current Limit Duration	Continuous
Power Dissipation	500mW

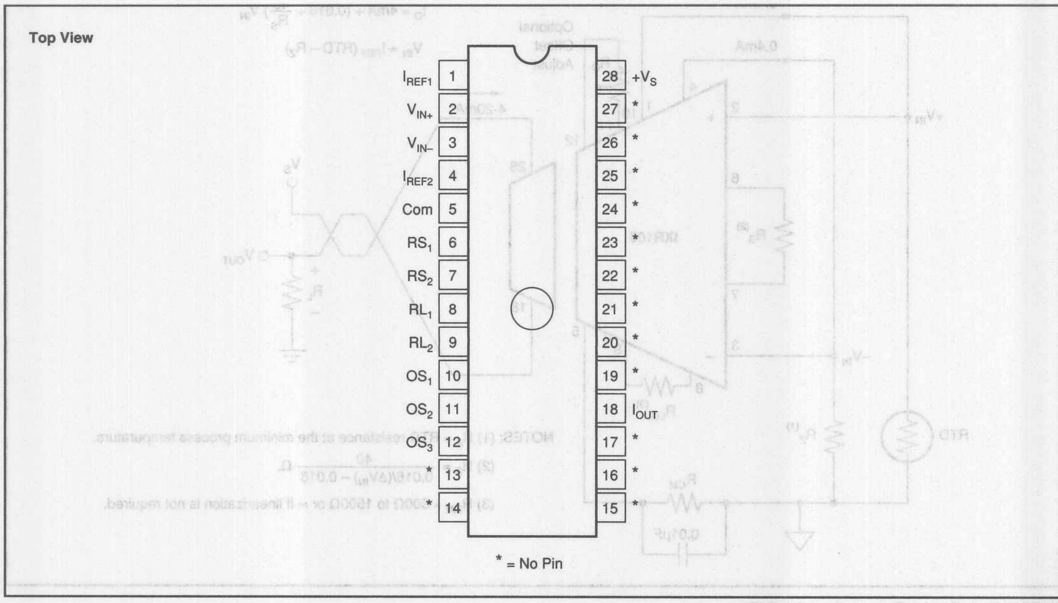
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
IXR100	2-Wire Transmitter	901

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



DISCUSSION OF PERFORMANCE

The IXR100 makes the design of isolated two wire 4 to 20mA transmitters easy and provides exceptional performance at very low cost. It combines several unique features not previously available in a single package. These include galvanic isolation, sensor excitation and linearization, excellent DC performance, and low zero and span drift. The IXR100 functions with voltages as low as 11.6V at the device. This allows operation with power supplies at or below 15V. When used with the RCV420 the complete 4 to 20mA current loop requires only 13.1V. If series diode protection is desired the minimum loop supply voltage is still only about 13.7V. This is especially useful in systems where the available supplies are only 15V.

BASIC CONNECTION

The basic connection of the IXR100 is shown in Figure 1. A differential voltage applied between pins 2 and 3 will cause a current of 4 to 20mA to circulate in the two wire output loop pins 28 and 18. Pins 1 and 4 supply the current excitation for resistive sensors. Pins 6 and 7 are provided for the connection of an external span resistor which increases the gain. Pins 8 and 9 provide linearity correction. Pins 10, 11 and 12 adjust the output offset current.

FUNCTIONAL DESCRIPTION

The IXR100 comprises of several functions:

- Sensor excitation
- Internal voltage regulator
- Input amplifier and V/I converter
- Linearization circuit
- DC/DC Converter

SENSOR EXCITATION

Sensor Excitation consists of two matched 0.4mA current sources. One is used to excite the resistive sensor and the other is used to excite the zero balance resistor R_Z. When the linearity correction feature is used these current sources are modulated together so that three wire operation of a Pt100 RTD is possible.

INTERNAL VOLTAGE REGULATOR

The circuitry within the IXR100 regulates the supply voltage to the DC/DC Converter, Input Amplifier, Linearization Amplifier and V/I Converter and removes the normal variations in V_S from these stages as the output spans from 4 to 20mA.

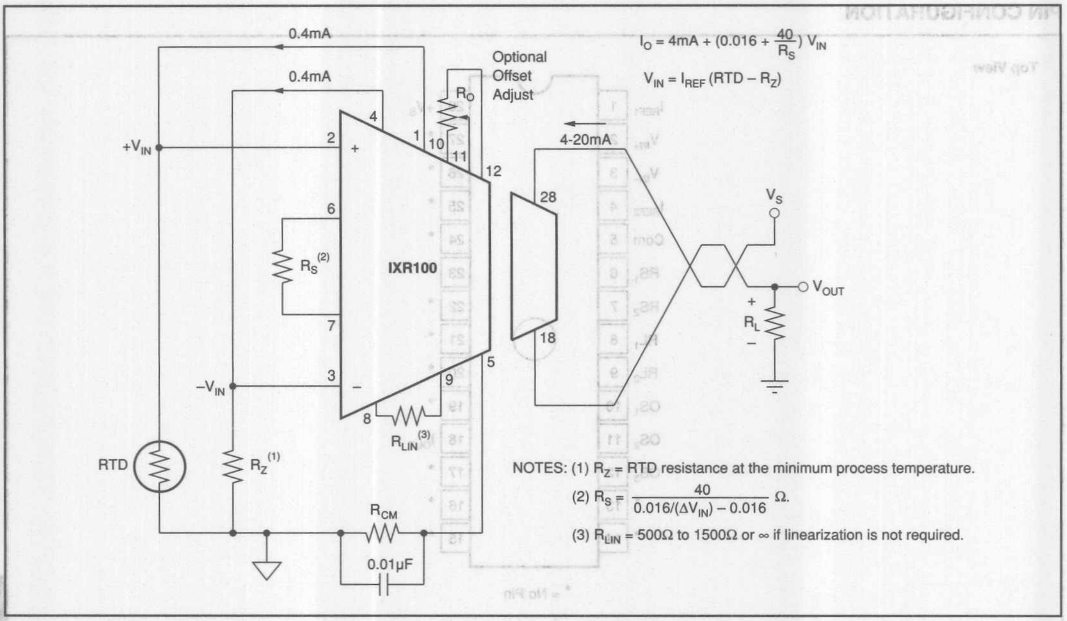


FIGURE 1. Basic Connection for RTD.

INPUT AMPLIFIER AND V/I CONVERTER

The Input Amplifier is an instrumentation amplifier whose gain is set by R_S, it drives the V/I Converter to produce a 4 to 20mA output current. The Input Amplifier has a common mode voltage range of 2 to 4V with respect to COM (pin 5). Normally this requirement is satisfied by returning the currents from the RTD and zero balance resistor R_Z to COM through a common mode resistor R_{CM}. For most applications a single value of 3.9kΩ may be used. When used with RTDs having large values of resistance R_{CM} must be chosen so that the inputs of the amplifier remain within its rated common mode range. R_{CM} should be bypassed with a 0.01µF or larger capacitor.

LINEARIZATION CIRCUIT

The Linearity Correction Circuit is unique in several ways. A single external resistor will provide up to 50 times improvement in the basic RTD linearity. Terminal based non-linearity can be reduced to less than ±0.1% for all RTD temperature spans. The Linearization circuit also contains an instrumentation amplifier internally connected to the $\pm V_{IN}$ pins. The gain of this stage is set by R_{LIN}. The output controls the excitation current sources to produce an increasing excitation current as V_{IN} increases. An important feature is that the Linearity Correction is made directly to the RTD output independent of the gain of the Input Amplifier. This provides minimal interaction between R_S and R_Z. This feature can be useful at the systems level by reducing data acquisition system processor overhead previously used to linearize sensor response in software/firmware.

DC/DC CONVERTER

The DC/DC Converter transfers power from the 2 wire current loop across the barrier to the circuitry used on the input side of the isolation barrier.

PIN DESCRIPTIONS

I_{REF1}, I_{REF2}

These pins provide a matched pair of current sources for sensor excitation. These current sources provide excellent thermal tracking, and when the linearization feature is used, are modulated by an equal amount. Their nominal current value is 0.4mA and their compliance voltage is:

$$V_{IN}+ < V_{IREF} < (Com + 7V)$$

$$I_{REF} = 400\mu A + \frac{V_{REF}}{2R_{LIN}}$$

$+V_{IN}$, $-V_{IN}$

These are the inputs to both the input amplifier and the linearization amplifier. Because the IXR100 has been optimized for RTD applications, the two sets of inputs are internally connected.

R_{S1}, R_{S2}

The resistor connected across these terminals determines the gain of the IXR100. For normal 4-20mA outputs:

$$R_S = \frac{40}{0.016/(\Delta V_{IN}) - 0.016} \Omega \quad (1)$$

R_{L1}, R_{L2}

The resistor connected between these terminals determines the gain of the linearization circuit and the amount of correction applied to the RTD. Its value may be determined in several ways. Two of which are shown as follows.

1. Empirically by interactively adjusting R_{LIN}, R_S and R_Z to achieve best fit 4 to 20mA output. R_Z is used to set 4mA at minimum input, R_S is adjusted for 12mA with a half span input, and R_{LIN} is adjusted to give 20mA with a full span input. This may require a few iterations but is probably the most practical method for field calibration. R_{LIN} will range between 500Ω and 1500Ω for 100Ω sensors (Pt100, D100, SAMA). Initially it may seem a little strange adjusting R_S for 12mA and R_{LIN} for 20mA. However, convergence is achieved much more quickly as the linearized curve passes through zero and has less effect at the mid span and the linearity trim resistor tends to adjust the transfer function more at the full span than the mid point.
2. Using Table I and linear interpolation for values of span not given in the table. This will yield very accurate results for the Pt100 sensor and acceptable results for D100 and SAMA sensors.

ZERO ADJUST (OPTIONAL) O_{S1}, O_{S2}, O_{S3}

The IXR100 has provision for adjusting the output offset current as shown in Figure 2. In many applications the already low offset will not need to be known at all. This trim effects the V/I converter stage and does not introduce V_{OS} drift errors that occur when the trim is performed at the input stage. If possible use R_Z to trim sensor output error to zero and use the offset control to trim the output to 4mA when V_{IN} = 0V. The offset adjustment can be made with a

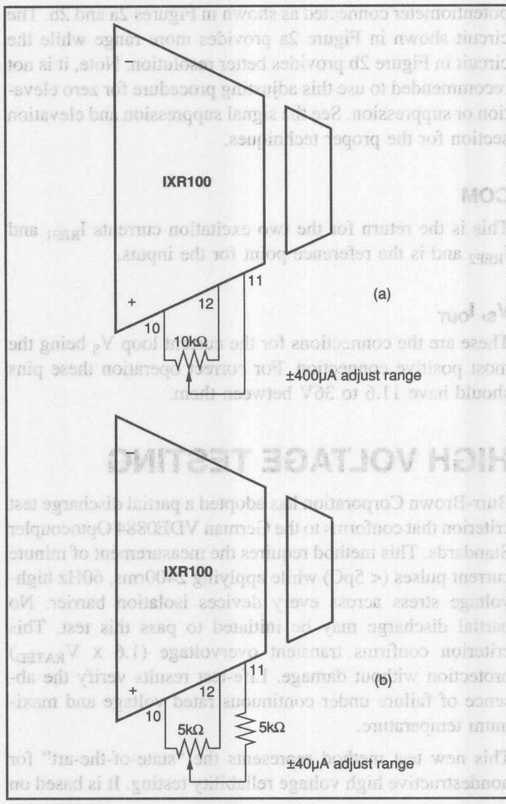


FIGURE 2. Basic Connection for Zero Adjust.

SPAN ΔT (°C)

T_{MIN} (°C)	50	100	200	300	400	500	600	700	800	900	1000
–200	573	653	839	995	1083	1131	1152	1159	1159	1154	1140
–150	745	855	1059	1158	1197	1206	1205	1196	1175	1151	1127
–100	983	1105	1228	1251	1249	1231	1207	1182	1156	1129	
–50	1233	1284	1286	1262	1236	1208	1180	1152	1125	1097	
0	1302	1287	1273	1229	1201	1173	1145	1117	1089		
50	1263	1249	1220	1192	1164	1136	1108	1081	1054		
100	1225	1211	1183	1155	1127	1100	1073	1046			
150	1188	1174	1146	1119	1091	1064	1038	1011			
200	1151	1137	1110	1083	1056	1030	1003				
250	1114	1101	1074	1048	1021	995	969				
300	1079	1066	1039	1013	987	962					
350	1044	1031	1005	979	954	928					
400	1009	996	971	946	921						
450	975	963	938	913	888						
500	942	930	905	881							
550	909	897	873	849							
600	877	865	841								
650	845	834	810								
700	814	803									
750	784	773									
800	754										

NOTES: (1) Linear interpolation between two horizontal or vertical values yields acceptable values. (2) Although not optimum, these values will also yield acceptable results with D100 and SAMA 100Ω nominal sensors. (3) Double R_{LIN} value for PT200.

TABLE I. R_{LIN} Values for Pt100 Sensor.

circuit shown in Figure 2a provides more range while the circuit in Figure 2b provides better resolution. Note, it is not recommended to use this adjusting procedure for zero elevation or suppression. See the signal suppression and elevation section for the proper techniques.

COM

This is the return for the two excitation currents I_{REF1} and I_{REF2} and is the reference point for the inputs.

V_S, I_{OUT}

These are the connections for the current loop V_S being the most positive connection. For correct operation these pins should have 11.6 to 36V between them.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (< 5pC) while applying 2400rms, 60Hz high-voltage stress across every devices isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 x V_{RATED}) protection without damage. Life-test results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state-of-the-art" for nondestructive high voltage reliability testing. It is based on dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier.

The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01µs-0.1µs current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the "inception voltage". Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage".

We have designed and characterized the package to yield an inception voltage in excess of 2400Vrms so that transient overvoltages below this level will not cause any damage. The extinction voltage is above 1500Vrms so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated level. Older high voltage test methods relied on applying a large enough overvoltage (above rating) to catastrophically break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

APPLYING THE IXR100

The IXR100 has been designed primarily to correct nonlinearities inherent in RTD sensors. It may also be used in other applications where its excellent performance makes it superior to other devices available. Examples are shown in the Applications Section.

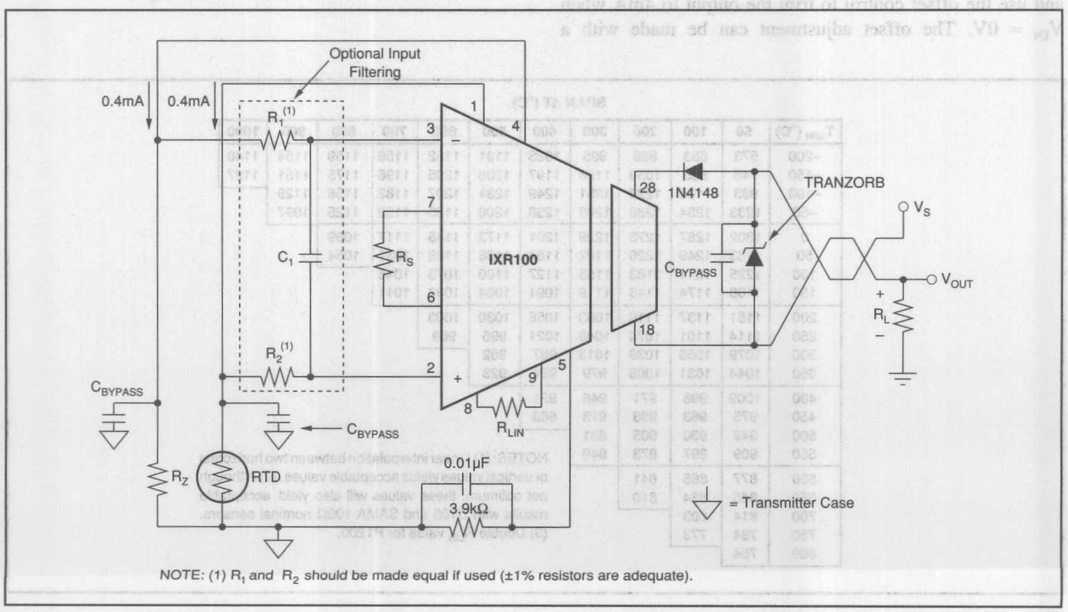


FIGURE 3. Transient and RFI Protection Circuit.

RFI AND TRANSIENT SUPPRESSION

Radio frequency interference and transients are a common occurrence in 4-20mA loops, especially when long wiring lengths are involved. RFI usually appears as a temporary change in output and results from rectification of the radio signal by one or more stages in the amplifier. For sensors which are closely coupled to the IXR100 and are contained in a common metal housing, the usual entry for RFI is via the 4-20mA loop wiring. Coaxial bypass capacitors may be used with great effectiveness to bring these leads into the transducer housing while suppressing the RFI. Values of 100 to 1000pF are generally recommended. For sensors remote from the IXR100, coaxial capacitors can also be used to filter the excitation and signal leads. Additional low-pass filtering at the IXR100 input helps suppress RFI. The easiest way to do this is with the optional differential RC filter shown in Figure 4. Typical values for R_1 and R_2 are 100-1000Ω, and for C_1 are 100-1000pF.

Transient suppression for negative voltages can be provided by the reverse-polarity protection diodes discussed later. However, positive transients cannot be handled by these diodes and do frequently occur in field-mounted loops. A shunt zener diode is of some help, but most zener diodes suffer from limited current-handling capacity and slow turn-on. Both of these characteristics can lead to device failure before the zener conducts. One type of zener, called the TRANZORB and available from General Semiconductor Industries, is especially effective in protecting against high-energy transients such as those induced by lightning or motor contactors. Choose a TRANZORB with a voltage rating close to, but exceeding, the maximum V_S which the IXR100 will see. In combination, the coaxial bypass capacitors and TRANZORB provide a very high level of protection against transients and RFI.

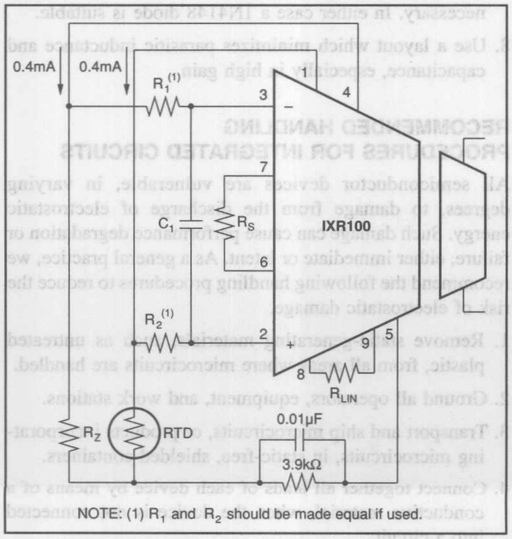


Figure 4. Optional Bandwidth-Limiting Circuitry.

INPUT BANDWIDTH LIMITING

Filtering at the input to the IXR100 is recommended where possible and can be done as shown in Figure 4. C_1 connected to pins 3 and 4 will reduce the bandwidth with a f_{-3dB} frequency given by:

$$f_{-3dB} = 0.159/(R_1 + R_2 + RTD + R_Z)\ (C_1 + 3pF)$$

This method has the disadvantage of having f_{-3dB} vary with R_1, R_2, RTD, and R_Z may require large values of R_1, and R_2. R_1 and R_2 should be matched to prevent zero errors due to input bias current.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (span elevation) or elevated zero range (span suppression). This is easily accomplished with the IXR100 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figure 5. In this example the sensor voltage is derived from RT (a thermistor, RTD or other variable resistance element) excited by one of the 0.4mA current sources. The other current source is used to create the elevated zero range voltage. Figures 6a, 6b, 6c and 6d show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments.

NOTE: Use of the optional offset null (pins 10, 11, and 12) for elevation or suppression is not recommended. This trim technique is used only to trim the IXR100's output offset current.

MAJOR POINTS TO CONSIDER WHEN USING THE IXR100

1. The leads to R_S and R_{LIN} should be kept as short as possible to reduce noise pick-up and parasitic resistance. If the linearity correction feature is not desired, the R_{LIN} pins are left open.
2. $+V_S$ should be bypassed with a 0.01µF capacitor as close to the unit as possible (pins 18 to 28).
3. Always keep the input voltages within their range of linear operation, +2V to +4V ($\pm V_{IN}$ measured with respect to pin 5).

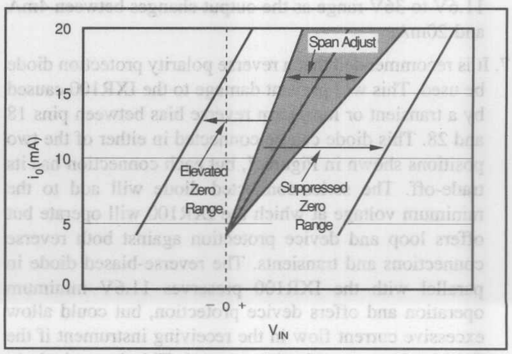


Figure 5. Elevation and Suppression Graph.

ISOLATION PRODUCTS 5 IXR100

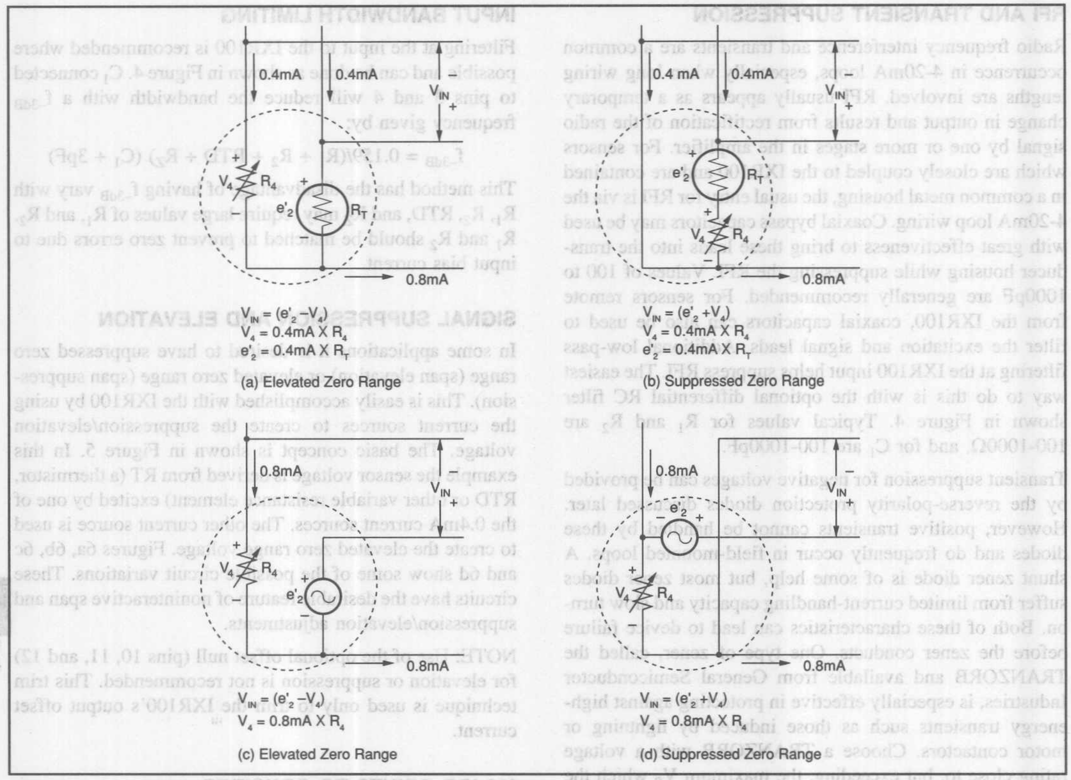


FIGURE 6. Elevation and Suppression Circuits.

4. The maximum input signal level (ΔV_{IN}) is 1V with R_S open and is less as R_S decreases in value.
5. Always return the current references to COM (pin 5) through an appropriate value of R_{CM} to keep V_{CM} within its operating range. Also, operate the current sources within their rated compliance voltage:

$$V_{IN} + \leq V_{IREF} \leq (\text{Com} + 7V)$$

6. Always choose R_L, (including line resistance) so that the voltage between pins 18 and 28 ($+V_S$) remains within the 11.6V to 36V range as the output changes between 4mA and 20mA.
7. It is recommended that a reverse polarity protection diode be used. This will prevent damage to the IXR100 caused by a transient or long-term reverse bias between pins 18 and 28. This diode can be connected in either of the two positions shown in Figure 7, but each connection has its trade-off. The series-connected diode will add to the minimum voltage at which the IXR100 will operate but offers loop and device protection against both reverse connections and transients. The reverse-biased diode in parallel with the IXR100 preserves 11.6V minimum operation and offers device protection, but could allow excessive current flow in the receiving instrument if the field leads are accidently reversed. This is particularly important if the receiving equipment has particularly low resistance or uses higher voltage supplies. In general, the series diode is recommended unless 12V operation is necessary. In either case a 1N4148 diode is suitable.
8. Use a layout which minimizes parasitic inductance and capacitance, especially in high gain.

RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice, we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove static-generating materials, such as untreated plastic, from all areas where microcircuits are handled.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.

5. Control relative humidity to as high a value as practical (50% recommended).

RTD APPLICATIONS

The IXR100 has been designed with RTD applications specifically in mind. The following information provides additional information for those applications.

TWO- AND THREE-WIRE CONNECTIONS

The IXR100 performs well with two-wire and three-wire RTD connections commonly encountered in industrial monitoring and control.

In two-wire applications, the voltage drop between the RTD and the IXR100 can be nulled by proper adjustment of R_Z, but care must be taken that this voltage drop does not vary with ambient conditions. Such variation will appear as an apparent variation in the RTD resistance and therefore as a change in measured temperature. Also, the linearity correction will interpret this change as a variation and attempt to linearize both the actual RTD signal and the resistance changes in the signal lines. For these reasons, the line resistance between the RTD and the IXR100 should be minimized by keeping line lengths short and/or using large-gauge wires. This limitation does not apply for three-wire connections.

In three-wire applications, shown in Figure 7, the RTD and R_Z lead arrangements set up a pseudo-Kelvin connection to the RTD. This occurs because the currents through the three wires are set up in opposing directions and cancel IR drops in the RTD leads. The current sources are both modulated equally, so that use of the linearity correction does not affect the cancellation. This action is true so long as the three wires are of the same length and gauge. Because most RTD leads are twisted and bundled, this requirement is usually met with no difficulty. Care must be taken that intermediate connections such as screw terminals do not violate this assumption by introducing unequal line resistances.

RTD ZERO ELEVATION AND SUPPRESSION

The IXR100 may be operated in zero-elevated and zero-suppressed ranges by simply offsetting R_Z. It may also be used in increase-decrease applications by interchanging the physical locations of the RTD and R_Z as shown in Figure 8. Use the same values of R_Z, R_{LIN} and R_S. Again, because the current sources are matched and are modulated equally, this connection has no effect on IXR100 performance, especially in three-wire applications.

OPEN CIRCUIT DETECTION

In some applications of the IXR100, the RTD will be located remotely. In these cases, it is possible for open circuits to develop. The IXR100 responds in the following manner to breaks in each lead. The following connections refer to the RTD connections shown in Figure 7.

TERMINAL OPEN	I_{OUT}(1)
1	32mA
2	3.6mA
3	32mA

NOTE: (1) Approximate value.

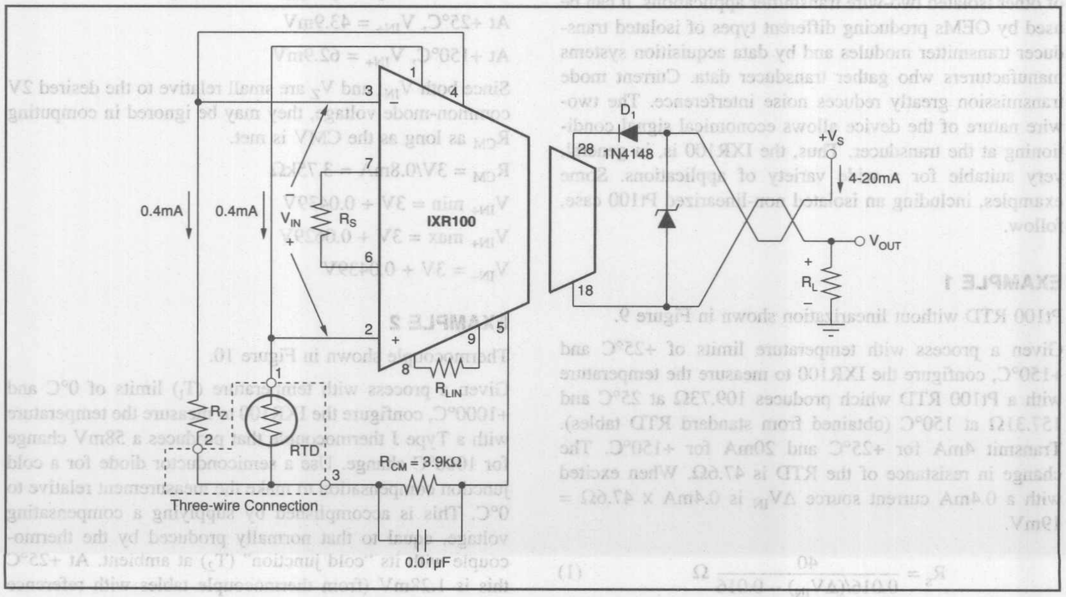


FIGURE 7. Basic 3-Wire RTD Connection for Increase-Increase Action.

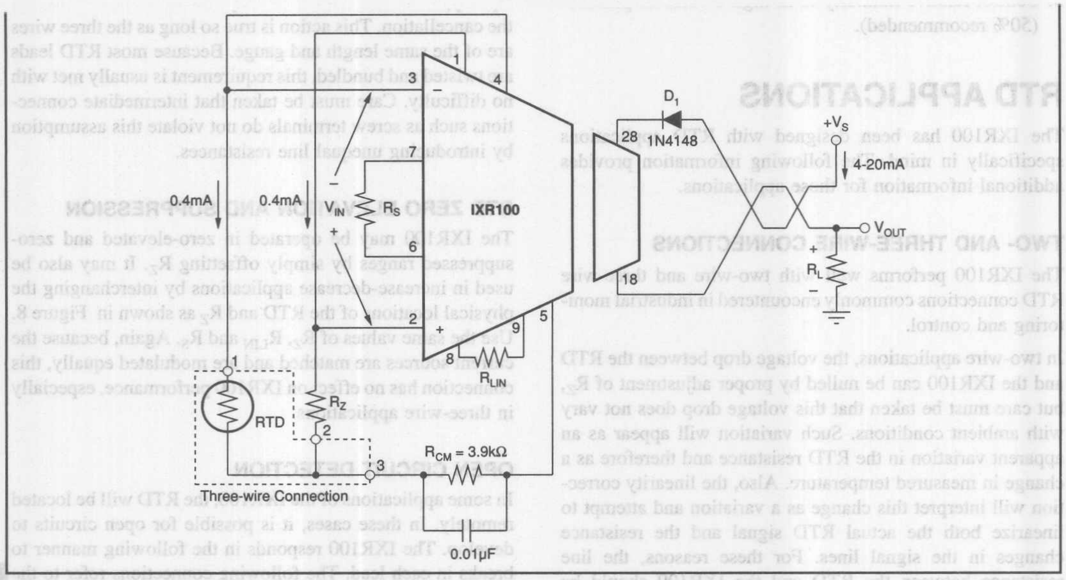


FIGURE 8. Basic 3-Wire RTD Connection for Increase-Decrease Action.

OTHER APPLICATIONS

In instances where the linearization capability of the IXR100 is not required, it can still provide improved performance in several applications. Its small size, wide compliance voltage, low zero and span drift, high PSRR, high CMRR and excellent linearity makes the IXR100 ideal for a variety of other isolated two-wire transmitter applications. It can be used by OEMs producing different types of isolated transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus, the IXR100 is, in general, very suitable for a wide variety of applications. Some examples, including an isolated non-linearized Pt100 case, follow.

EXAMPLE 1

Pt100 RTD without linearization shown in Figure 9.

Given a process with temperature limits of +25°C and +150°C, configure the IXR100 to measure the temperature with a Pt100 RTD which produces 109.73Ω at 25°C and 157.31Ω at 150°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C. The change in resistance of the RTD is 47.6Ω. When excited with a 0.4mA current source ΔV_{IN} is 0.4mA x 47.6Ω = 19mV.

$$R_S = \frac{40}{0.016/(\Delta V_{IN}) - 0.016}\ \Omega \qquad (1)$$

From Equation (1), R_S = 48.5Ω. Span adjustment (calibration) is accomplished by trimming R_S.

In order to make the lower range limit of 25°C correspond to the output lower range limit at 4mA, the input circuitry shown in Figure 9 is used. V_{IN} must be 0V at 25°C and R_Z is chosen to be equal to the RTD resistance at 25°C, or 109.73Ω. Computing R_{CM} and checking CMV:

At +25°C, V_{IN+} = 43.9mV

At +150°C, V_{IN+} = 62.9mV

Since both V_{IN+} and V_Z are small relative to the desired 2V common-mode voltage, they may be ignored in computing R_{CM} as long as the CMV is met.

R_{CM} = 3V/0.8mA = 3.75kΩ

V_{IN+} min = 3V + 0.0439V

V_{IN+} max = 3V + 0.0629V

V_{IN-} = 3V + 0.0439V

EXAMPLE 2

Thermocouple shown in Figure 10.

Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the IXR100 to measure the temperature with a Type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At +25°C this is 1.28mV (from thermocouple tables with reference junction at 0°C). Typically, at T_2 = +25°C, V_D = 0.6V and

$\Delta V_D/\Delta T = -2mV/°C$. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta V_D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At +25°C this is approximately $-52\mu V/°C$ (obtained from standard thermocouple table); therefore,

$$\Delta V_{TC}/\Delta T = (\Delta V_D/\Delta T)(R_6/(R_5 + R_6)) \quad (2)$$

$$-52\mu V/°C = (-2000\mu V/°C)(R_6/(R_5+R_6))$$

R_5 is chosen as $3.74k\Omega$ to be much larger than the resistance of the diode. Solving for R_6 yields 100Ω.

Transmit 4mA for $T_1 = 0°C$ and 20mA for $T_1 = +1000°C$. Note: $V_{IN} = V_{IN+} - V_{IN-}$ indicates that T_1 is relative to T_2. The input full scale span is 58mV. R_S is found from Equation (1) and equals 153.9Ω.

R_4 is chosen to make the output 4mA at $T_{TC} = 0°C$ (V_{TC} = 1.28mV) and $T_D = 25°C$ ($V_D = 0.6V$).

V_{TC} will be $-1.28mV$ when $T_{TC} = 0°C$ and the reference junction is at +25°C. V_4 must be computed for $T_D = +25°C$ to make $V_{IN} = 0V$.

$V_{D(25°C)} = 600mV$

$V_{IN(25°C)} = 600mV\ (100/3740) = 16.0mV$

$V_{IN} = V_{IN+} - V_{IN-} = V_{TC} + V_4 - V_{IN-}$

With $V_{IN} = 0$ and $V_{TC} = -1.28mV$,

$V_4 = V_{IN+} - V_{TC}$

$V_4 = 16.0mV - (-1.28mV)$

$0.4mA\ (R_4) = 17.28mV$

$R_4 = 43.2\Omega$

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to the upper or lower limit when the thermocouple impedance goes very high. The circuits of Figures 10, 11 and 12 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the + input (large impedance) will cause I_O to go to its lower range limit value (about 3.6mA). If up scale indication is desired, the circuit of Figure 13 should be used. When the T_C opens, the output will go to its upper range limit value (about 32mA or higher).

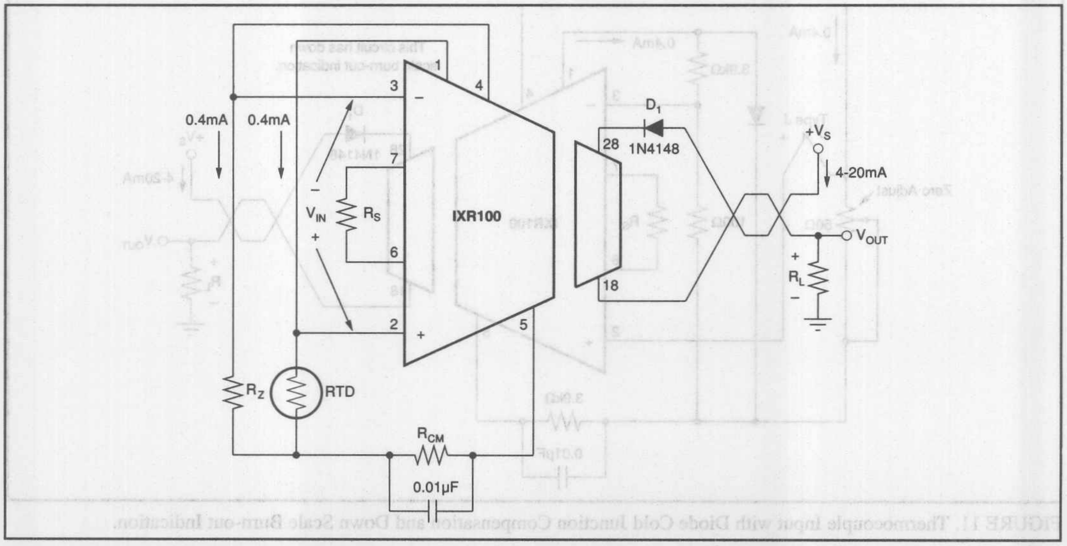


FIGURE 9. Pt100 RTD Without Linearization.

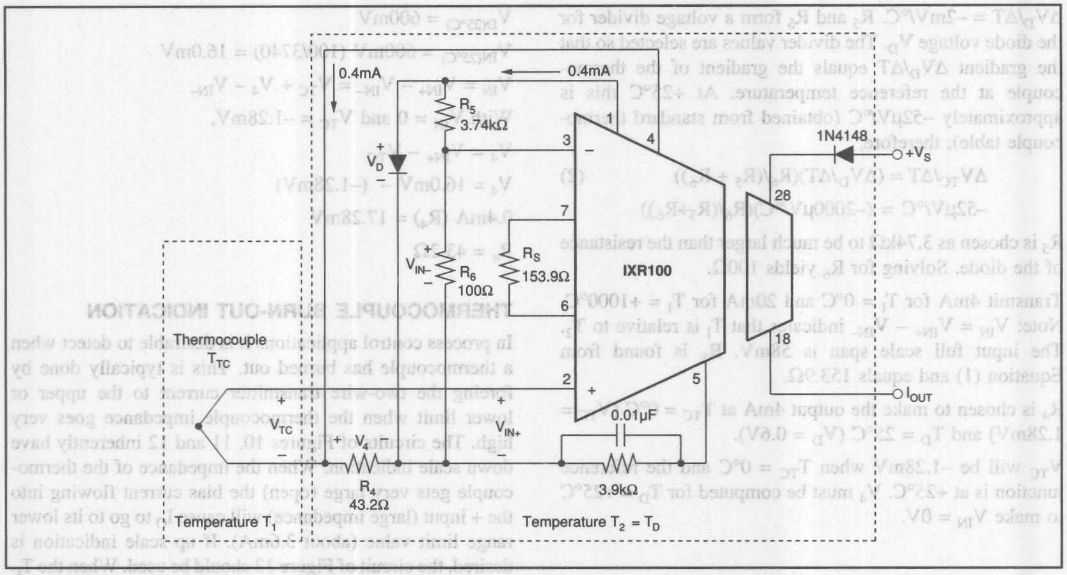


FIGURE 10. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

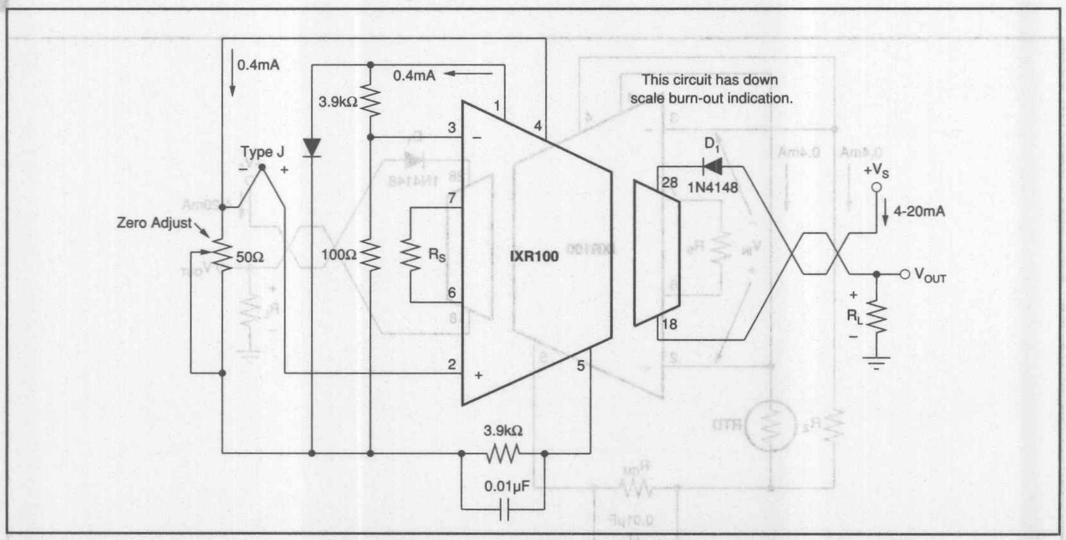


FIGURE 11. Thermocouple Input with Diode Cold Junction Compensation and Down Scale Burn-out Indication.

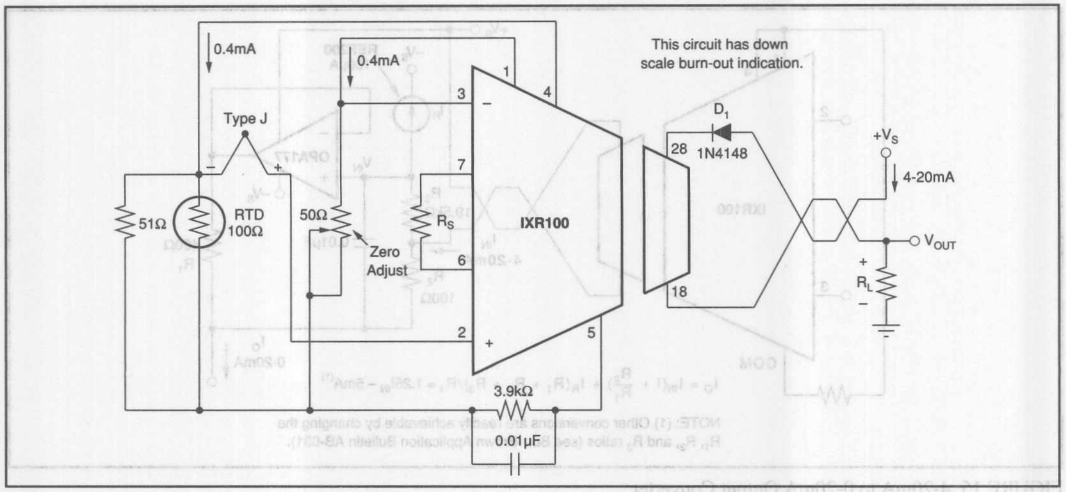


FIGURE 12. Thermocouple Input with RTD Cold Junction Compensation and Down Scale Burn-out Indication.

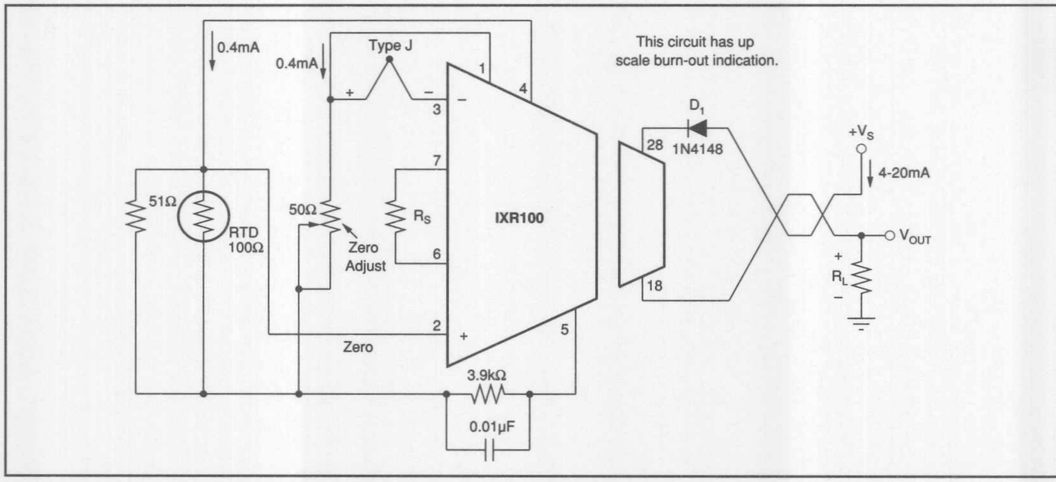


FIGURE 13. Thermocouple Input with RTD Cold Junction Compensation and Up Scale Burn-out Indication.

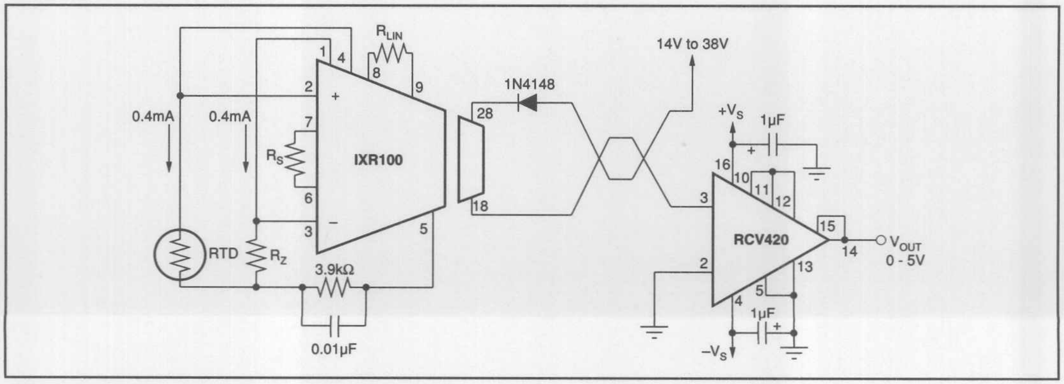
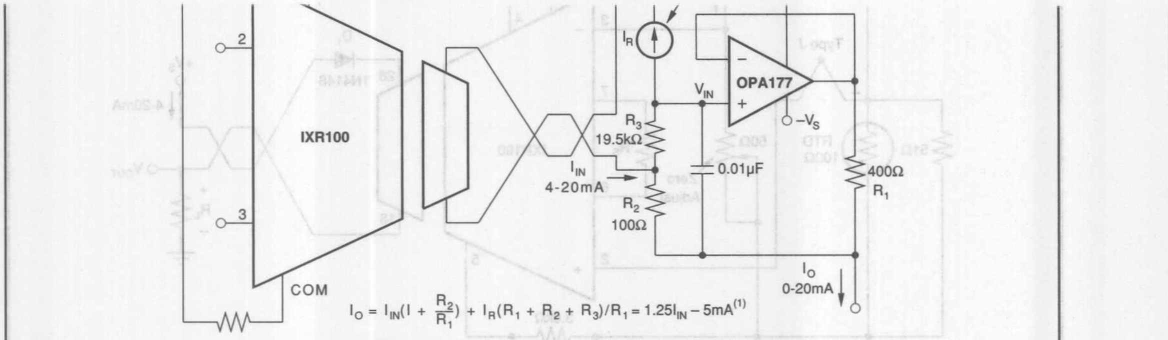


FIGURE 14. Isolated 4-20mA Instrument Loop.

ISOLATION PRODUCTS 5 IXR100

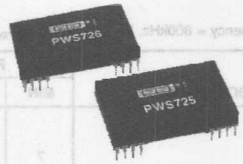


$$I_O = I_{IN}(1 + \frac{R_2}{R_1}) + I_R(R_1 + R_2 + R_3)/R_1 = 1.25I_{IN} - 5mA^{(1)}$$

NOTE: (1) Other conversions are readily achievable by changing the R_1, R_2, and R_3 ratios (see Burr-Brown Application Bulletin AB-031).

FIGURE 15. 4-20mA to 0-20mA Output Converter.

BURR - BROWN®



PWS725A
PWS726A

ABRIDGED DATA SHEET

For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 10736

Isolated, Unregulated DC/DC CONVERTERS

FEATURES

- ISOLATED ±7 TO ±18VDC OUTPUT FROM SINGLE 7 TO 18VDC SUPPLY
- ±15mA OUTPUT AT RATED VOLTAGE ACCURACY
- HIGH ISOLATION VOLTAGE PWS725A, 1500Vrms PWS726A, 3500Vrms
- LOW LEAKAGE CAPACITANCE: 9pF
- LOW LEAKAGE CURRENT: 2µA max, at 240VAC 50/60Hz
- HIGH RELIABILITY DESIGN
- AVAILABLE WITH OUTPUT SYNCHRONIZATION SIGNAL FOR USE WITH ISO120 AND ISO121
- PROTECTED AGAINST OUTPUT FAULTS
- COMPACT
- LOW COST
- EASY TO APPLY—FEW EXTERNAL PARTS

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS EQUIPMENT
- TEST EQUIPMENT
- DATA ACQUISITION

DESCRIPTION

The PWS725A and PWS726A convert a single 7 to 18VDC input to bipolar voltages of the same value as the input voltage. The converters are capable of providing ±15mA at rated voltage accuracy and up to ±40mA without damage. (See Output Current Rating.)

The PWS725A and PWS726A converters provide reliable, engineered solutions where isolated power is required in critical applications. The high isolation voltage rating is achieved through use of a specially-designed transformer and physical spacing. An additional high dielectric-strength, low leakage transformer coating increases the isolation rating of the PWS726A.

Reliability and performance are designed in. The bifilar wound, wirebonded transformer simultaneously provides lower output ripple than competing designs, and a higher performance/cost ratio. The soft-start oscillator/driver design assures full operation of the oscillator before either MOSFET driver turns on, protects the switches, and eliminates high inrush currents during turn-on. Input current sensing protects both the converter and the load from possible thermal damage during a fault condition.

Special design features make these converters especially easy to apply. The compact size allows dense circuit layout while maintaining critical isolation requirements. The Input Sync connection allows frequency synchronization of multiple converters. The Output Sync is available to synchronize ISO120 and ISO121 isolation amplifiers. The Enable input allows control over output power in instances where shutdown is desired to conserve power, such as in battery-powered equipment, or where sequencing of power turn-on/turn-off is desired.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

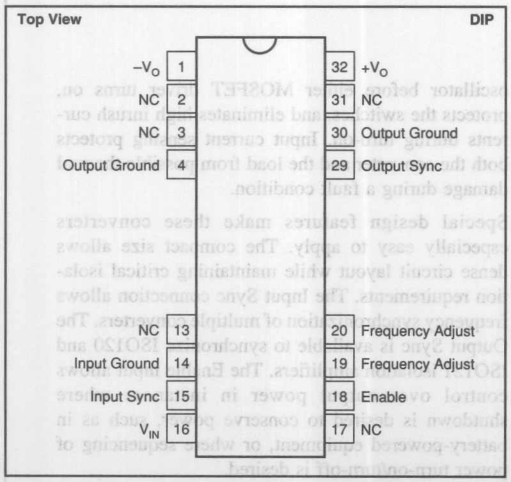
ELECTRICAL

T_A = +25°C, C_L = 1µF ceramic, V_{IN} = 15VDC, operating frequency = 800kHz, V_{OUT} = ±15VDC, C_{IN} = 1µF ceramic, I_{OUT} = ±15mA, unless otherwise specified.

PARAMETER	CONDITIONS	PWS725A MIN	PWS725A TYP	PWS725A MAX	PSW726A MIN	PSW726A TYP	PSW726A MAX	UNITS
INPUT								
Rated Voltage			15			*		VDC
Input Voltage Range		7		18	*		*	VDC
Input Current	I_O = ±15mA		77			*		mA
Input Current Ripple	No External Filtering		150			*		mAp-p
	L-C Input Filter, L_{IN} = 100µH, C_{IN} = 1µF(1)		5			*		mAp-p
	C Only, C_{IN} = 1µF		60					mAp-p
ISOLATION								
Test Voltages	Input to Output, 10 seconds	4000			8000			VDC
	Input to Output, 60 seconds, min	1500			3500			Vrms
Rated Voltage	Input to Output, Continuous, AC 60Hz			1500			3500	Vrms
	Input to Output, Continuous DC			2121			4950	VDC
Isolation Impedance	Input to Output		10^{12} || 9			*		Ω || pF
Leakage Current	Input to Output, 240Vrms, 60Hz		1.2	2.0		*	*	µA
OUTPUT								
Rated Output Voltage		14.25	15	15.75	*	*	*	VDC
Output Current	Balanced Loads		15	40		*	*	mA
	Single-Ended			80			*	mA
Load Regulation	Balanced Loads, ±10mA < I_{OUT} < ±40mA			0.4			*	%/mA
Ripple Voltage (400kHz)	No External Capacitor		60			*		mVp-p
	L_O = 10µH, C_O = 1µF (Figure 1)		10			*		mVp-p
	L_O = 0µH, C_O Filter Only				See Performance Curves			
Output Switching Noise	L_O = 10µH, C_O = 1µF		1			*		mVp-p
Output Capacitive Load	L_O = 100µH, C Filter			10			*	µF
	C Filter Only			1			*	µF
Voltage Balance, V+, V–			0.04					%
Sensitivity to ΔV_{IN}			1.15					V/V
Output Voltage Temp. Coefficient			10					mV/°C
Output Sync Signal	Square Wave, 50% Duty Cycle		30			*		Vp-p
TEMPERATURE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	*		*	°C
Storage		–25		+125	*		*	°C

* Specification same as PWS725A.

PIN CONFIGURATION

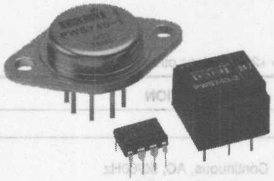


PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PWS725A	32-Pin Ceramic DIP	210
PWS726A	32-Pin Ceramic DIP	210

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®



PWS740

ABRIDGED DATA SHEET

For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 10758

Distributed Multi-Channel Isolated DC-TO-DC CONVERTER

FEATURES

- ISOLATED ±7 TO ±20VDC OUTPUTS
- BARRIER 100% TESTED AT 1500VAC, 60Hz
- LOWEST POSSIBLE COST PER CHANNEL
- MINIMUM PC BOARD SPACE
- 80% EFFICIENCY (8 CHANNELS, RATED LOADS)
- FLEXIBLE USE WITH PWS745 COMPONENTS

APPLICATIONS

- INDUSTRIAL MEASUREMENT AND CONTROL
- DATA ACQUISITION SYSTEMS
- TEST EQUIPMENT

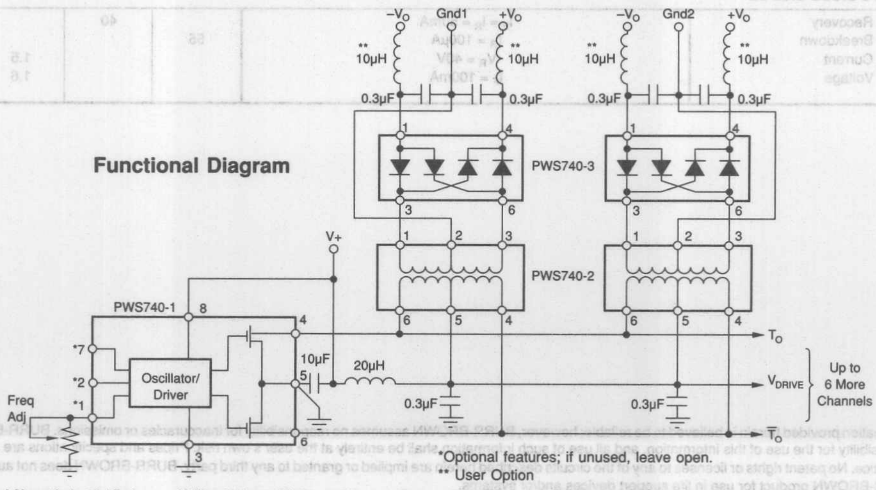
DESCRIPTION

The PWS740 is a multichannel, isolated DC-to-DC converter with a 1500VAC continuous isolation rating. The outputs track the input voltage to the converter over the range of 7 to 20VDC. The converter's modular design, comprising three components, minimizes the cost of isolated multichannel power for the user.

The PWS740-1 is a high-frequency (400kHz nominal) oscillator/driver, handling up to eight channels. This part is a hybrid containing an oscillator and two power FETs. It is supplied in a TO-3 case to provide the power dissipation necessary at full load. Transformer impedance limits the maximum input current to about 700mA at 15V input, well within the unit's thermal limits. A TTL-compatible ENABLE pin provides output shut-down if desired. A SYNC pin allows synchronization of several PWS740-1s.

The PWS740-2 is a trifilar-wound isolation transformer using a ferrite core and is encapsulated in a plastic package, allowing a higher isolation voltage rating. The PWS740-3 is a high-speed rectifier bridge in a plastic 8-pin mini-DIP package. One PWS740-2 and one PWS740-3 are used per isolated channel.

Functional Diagram

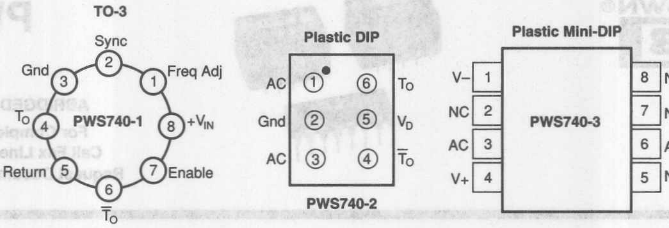


*Optional features; if unused, leave open.
** User Option

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

V_{IN} = 15V, output load on each of 8 channels = ±15mA, T_A = +25°C unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
PWS740 SYSTEM					
ISOLATION					
Rated Voltage	Continuous, AC, 50/60Hz			1500	VACrms
	Continuous, DC			2121	VDC
Test Voltage	10s, minimum	4000			VACrms
Impedance	Measured from Pin 2 to Pin 5 of the PWS740-2		10^{12} || 3		Ω || pF
Leakage Current	240VACrms, 60Hz Per Channel		0.5	1.5	μA
INPUT					
Rated Voltage			15		VDC
Voltage Range		7		20	VDC
Current	±30mA Output Load on 8 Channels, V_{IN} = 15V		520		mA
	Rated Output Load on 8 Channels, V_{IN} = 15V		300		mA
Current Ripple	Full Output Load on 8 Channels, V_{IN} = 15V with π Filter on Input		1		mA
OUTPUT					
Rated Voltage	±15mA Output Load on 8 Channels	14	15	16	VDC
Voltage at Min Load	±1mA/Channel		30		VDC
Voltage Range	±15mA Output Load on Each Channel	±7		±20	VDC
V_{OUT} vs Temp	±15mA Output Load on Each Channel		±0.05		V/°C
Load Regulation	±3mA < Output Load < ±30mA		0.25		V/mA
Tracking Regulation	V_{OUT}/V_{IN}		1.2		V/V
Ripple Voltage	See Typical Performance Curves				
Noise Voltage	See Theory of Operation				
Current | $+I_{OUT}$ | + | $-I_{OUT}$ |	Each Channel			60	mA
TEMPERATURE					
Specification		–25		+85	°C
Operation		–25		+85	°C
PWS740-1 OSCILLATOR/DRIVER					
Frequency	V_{IN} = 15V	350	400	470	kHz
Supply		7	15	20	V
Enable	Drivers On	2		V_S	V
	Drivers Off	0		0.8	V
PWS740-2 ISOLATION TRANSFORMER					
Isolation Test Voltage	10s, minimum	4000			VACrms
	60s, minimum	1500			VACrms
Rated Isolation Voltage	Continuous			1500	VACrms
Isolation Impedance			10^{12} || 3		Ω || pF
Isolation Leakage	240VAC		0.5	1.5	μA
Primary Inductance	400kHz, Pin 1 to Pin 5		300		μH
Winding Ratio	Primary/Secondary		68/76		
PWS740-3 DIODE BRIDGE					
Reverse Recovery	$I_F = I_R$ = 50mA		40		ns
Reverse Breakdown	I_R = 100μA	55			V
Reverse Current	V_R = 40V			1.5	μA
Forward Voltage	I_F = 100mA			1.6	V



(Drawings Not to Scale)

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PWS740-1 Driver	TO-3	030
PWS740-2 Transformer	6-Pin Plastic DIP	216
PWS740-3 Rectifier	8-Pin Plastic DIP	006

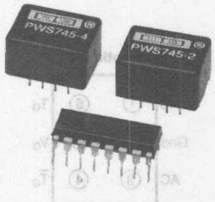
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BURR - BROWN®



PWS745

ABRIDGED DATA SHEET
For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 11095

Multi-Channel Isolated DC/DC CONVERTER COMPONENTS

FEATURES

- COMPACT SIZE
- LOW COST PER CHANNEL
- DRIVES UP TO 8 CHANNELS
- 750/1500VAC ISOLATION
- FLEXIBLE USE WITH PWS740/PWS750 COMPONENTS
- 0.4 IN. MAXIMUM MOUNTING HEIGHT

APPLICATIONS

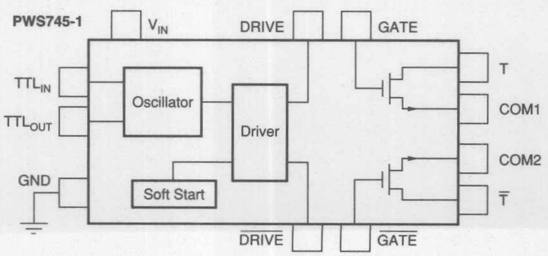
- INDUSTRIAL CONTROL
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- POINT-OF-USE POWER CONVERSION
- 5V TO ±15V FROM DIGITAL SUPPLIES

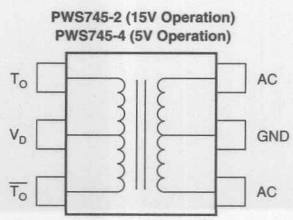
DESCRIPTION

The PWS745 is a set of components useful in the construction of single or multi-channel isolated DC/DC converters. By themselves, or in combination with the PWS740 and PWS750 families of components, they allow compact, optimal, and low-cost solutions to many power supply problems.

The PWS745-1 DIP oscillator/driver can be used to drive up to eight channels of independently isolated power. The switching MOSFETs are built into the driver to allow simple low-cost assembly of the multi-channel converter. The PWS745-1 also is capable of operating at 5VDC and can be easily synchronized with TTL level signals. While offering the user an alternative to the TO-3 package of the PWS740, the PWS745-1 also allows the user to select varying levels of power, isolation voltage, mounting technology and system configuration by choosing among the several component families. For example, the PWS745-1 can directly drive the PWS740, PWS745, or PWS750 transformers. It also can drive the FETs of a PWS750 distributed power system. The operating frequency is compatible with the ISO120 family of isolation amplifiers and is capable of multi-channel synchronized operation to eliminate troublesome beat frequencies.

The PWS745-2 is a 15V to ±15V output version, while the PWS745-4 is the 5V to ±15V output version. The PWS740-3 high-speed bridge provides a convenient rectifier for the selected transformer output.





International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{IN} = 15VDC, Output Load = ±15mA (PWS745-2) and T_A = 25°C unless otherwise noted.
Or V_{IN} = 5VDC, Output Load = ±12mA (PWS745-4) and T_A = 25°C unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWS745-1 OSCILLATOR/DRIVER					
Frequency: Internal OSC	TTL_{IN} = 0V	550	600	650	kHz
External OSC		500	600	1000	kHz
Supply: 15V Operation		10	15	18	V
5V Operation		4.5	5	5.5	V
Current	No Load		10		mA
	Max Load		650		mA
Current Ripple	C_{BYPASS} = 1µF		2.5		mAp-p
TTL_{IN}: I_{IH}				10	nA
I_{IL}			–1		µA
V_{IH}		2			V
V_{IL}				0.8	V
Frequency		1		2	MHz
TTL_{OUT}: I_{OL}				15	mA
Frequency			600		kHz
T, $\overline{T}$ Drive Current				50	mA
T, $\overline{T}$ Drive Voltage: High		3		7	V
Low				0.7	V
PWS745-2					
Voltage, Rated Continuous AC 60Hz		750			Vrms
100% Test(1)	60Hz, 1s	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms, 60Hz			150	µArms
PWS745-4					
Voltage, Rated Continuous AC 60Hz		750			Vrms
100% Test(1)	60Hz, 1s	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms, 60Hz			150	µArms
TEMPERATURE RANGE					
Specification		–40		85	°C
Operation		–40		85	°C
Storage		–40		85	°C

NOTES: (1) Tested at 1.6 rated, fail on 5pc partial discharge leakage current on five successive pulses.

Junction Temperature .... 150°C
Storage Temperature .... 85°C
Lead Temperature (soldering, 10s) .... 300°C
Transformer Output Short to Common .... Continuous
Max Load, Sum of All Transformer Outputs 500mA

Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION

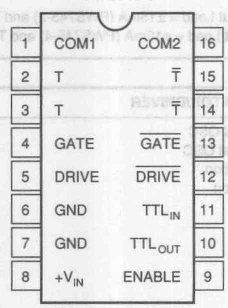
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
PWS745-1	16-Pin Plastic DIP	129
PWS745-2	8-Pin Plastic	250
PWS745-4	8-Pin Plastic	250

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

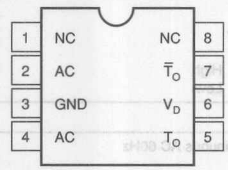
ELECTROSTATIC DISCHARGE SENSITIVITY

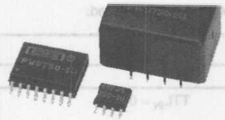
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



PWS745-2/PWS745-4





ABRIDGED DATA SHEET
For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 10838

Isolated, Unregulated DC/DC CONVERTER COMPONENTS

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- COMPACT-SURFACE MOUNT
- MULTICHANNEL OPERATION
- 5V OR 15V INPUT OPTIONS
- FLEXIBLE USE WITH PWS740/PWS745 COMPONENTS

DESCRIPTION

The PWS750 consists of three building blocks for building a low cost DC/DC converter. With them you can optimize DC/DC converter PC board layout or build a multichannel isolated DC/DC converter. All parts are surface mount, requiring minimal space to build the converter. The modular design minimizes the cost of isolated power.

The PWS750-1U is a high-frequency (800kHz nominal) driver that can drive N-channel MOSFETs up to the size of a 1.3A 2N7010. The recommended MOSFET for individual transformer drivers is the 2N7008. The PWS750-1U is supplied in a 16-pin double-wide SO package.

APPLICATIONS

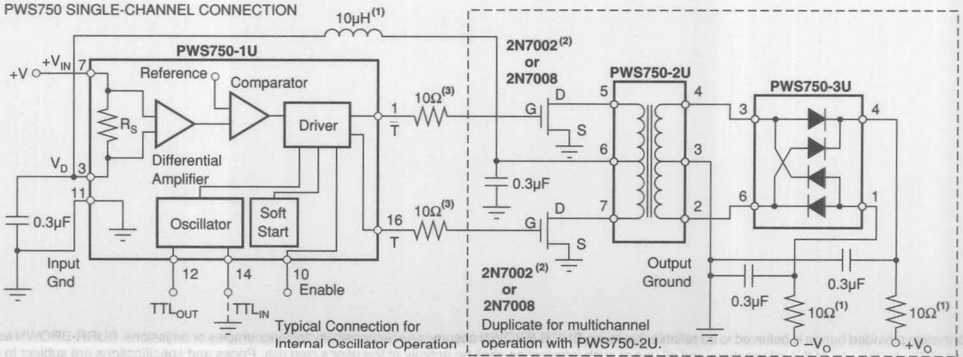
- INDUSTRIAL PROCESS CONTROL EQUIPMENT
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- VENDING MACHINES

The PWS750-2U and PWS750-4U are split-bobbin wound isolation transformers using a ferrite core. They are encapsulated in plastic packages, allowing a high isolation voltage rating.

The PWS750-3U is a high-speed monolithic diode bridge in a plastic 8-pin SO package.

One PWS750-1U can be used to drive up to four channels (15V nominal operation). One PWS750-2U and PWS750-3U and two 2N7002 (surface mount) or 2N7008 (TO-92) MOSFETs made by Siliconix are used per isolated channel. When a PWS750-4U is used as the transformer (5V input), then two TN0604s made by Supertex must be used, due to the higher currents of the primary (lower RDS on) and the lower V_{GS} threshold. With 5V operation only one channel can be directly driven by the PWS750-1U (a simple FET booster circuit can be used for multichannel operation; see Figure 3).

PWS750 SINGLE-CHANNEL CONNECTION



NOTES: (1) User option. (2) Use TN0604 for 5V to ±15V operation. (3) Multichannel Operation.

SPECIFICATIONS

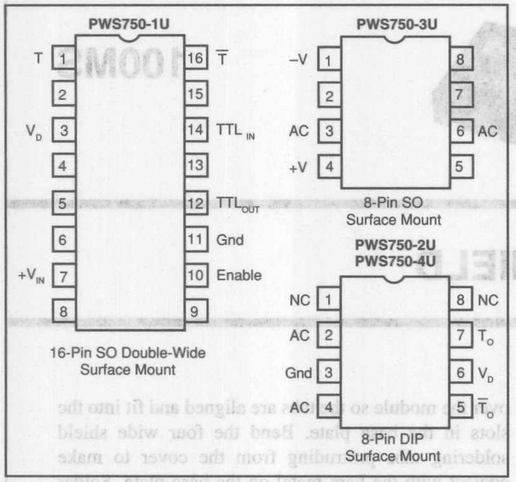
ELECTRICAL

At T_A = 25°C; $+V_{IN}$ = +15V; and I_{OUT} = ±15mA balanced loads unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWS750-1U OSCILLATOR					
Frequency: Internal OSC	TTL_{IN} = 0V	725	800	875	kHz
External OSC		1		2.5	MHz
Supply: 15V Operation		10	15	18	V
5V Operation		4.5	5	5.5	V
T, $\overline{T}$ Drive Current				50	mApk
T, $\overline{T}$ Drive Voltage, High		3		7	V
Low				0.7	V
TTL_{IN}, I_{IH}			10		nA
I_{IL}			–1		µA
V_{IH}		2			V
V_{IL}				0.8	V
TTL_{OUT}, I_{OL}				15	mA
PWS750-2U $+V_{IN}$ TO $\pm V_{OUT}$ ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz		750			Vrms
100% Test [1]	60Hz, 1s, <5pC PD	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1	1.5	µArms
Winding Ratio	Primary/Secondary		48/48		
PWS750-3U DIODE BRIDGE					
Reverse Recovery	$I_F = I_R$ = 50mA		40		ns
Reverse Breakdown	I_R = 100µA	55			V
Reverse Current	V_R = 40V			1.5	µA
Forward Voltage	I_F = 100mA			1.6	V
PWS750-4U $+5V_{IN}$ to $\pm 15V_{OUT}$ ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz		750			Vrms
100% Test [1]	60Hz, 1s, <5pC PD	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1	1.5	µArms
Winding Ratio	Primary/Secondary		24/70		
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating	Derated performance	–40		+85	°C
Storage		–40		+85	°C

NOTES: (1) Tested at 1.6 x rated, fail on 5pC partial discharge leakage current on five successive pulses at 60HZ.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Junction Temperature	150°C
Storage Temperature	–40°C to +85°C
Lead temperature (soldering, SOIC, 3s)	+260°C
Max Load, Sum of Both Outputs (PWS750-2U, 4U)	60mA

ORDERING INFORMATION

PWS750-XU

Basic Model Number

Components

1U : High-Frequency Driver

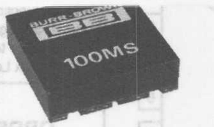
2U, 4U : Isolation Transformer

3U : High-Speed Monolithic Diode Bridge

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PWS750-1U	16-Pin SOIC	258
PWS750-2U	8-Pin Plastic	226
PWS750-3U	8-Pin SO	182
PWS750-4U	8-Pin Plastic	226

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



EMI SHIELD

DESCRIPTION

The 100MS is an epoxy encapsulated electromagnetic/electrostatic interference (EMI) shield for use with circuits where sensitivity to EMI is critical. It was designed to attenuate EMI by converting electromagnetic field energy into heat that is absorbed by the shield and by shunting electrostatic fields to common. The 100MS may be used in applications to either confine or exclude EMI. Its cavity was designed for 28.45mm x 28.45mm x 7.24mm, 20-pin hybrid packages. The shields in the cover and base plate are in two separate halves to maintain the electrical isolation between the adjacent rows of pins of the module it encloses. Because of the spacing between the shield halves and epoxy flow holes, the 100MS provides a partial, but adequate low reluctance path for electromagnetic flux. The 100MS is well suited for use with isolation modules such as the Burr-Brown 3656, 722, and 724.

ASSEMBLY INSTRUCTIONS

Assemble the base plate to the module by pushing the pins of the module through the beveled holes in the base plate until the base plate and bottom of the module are in contact with each other. Place the cover over the module so the tabs are aligned and fit into the slots in the base plate. Bend the four wide shield soldering tabs protruding from the cover to make contact with the bare metal on the base plate. Solder these four tabs to insure the integrity of their connection to the base plate.

The 100MS and the module it contains are mounted and secured to a printed circuit board (PCB) by soldering the two narrow PCB solder tabs to the appropriate common. The PCB solder tab closest to the input side of the module should be soldered to the input common. The other tab should be soldered to the output common. Figure 2 illustrates the assembly of the 100MS.

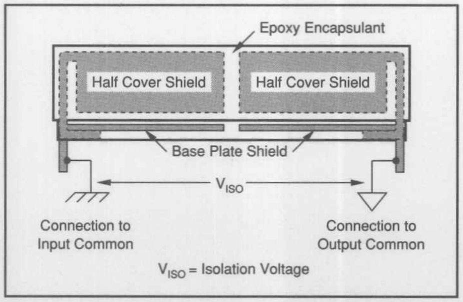


FIGURE 1. Cross-Sectional Side View of 100MS.

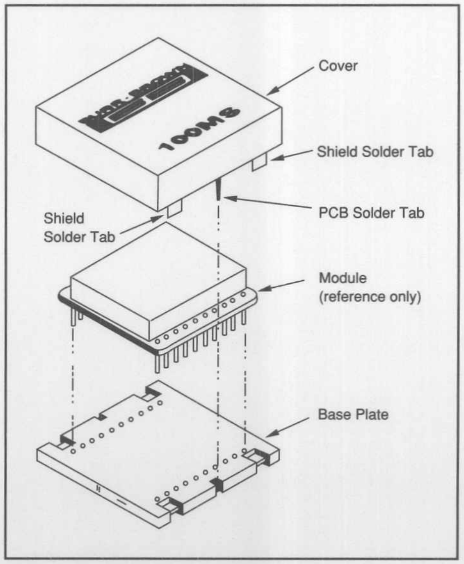


FIGURE 2. Assembly Diagram.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

Specifications apply between solder tabs.

PARAMETER	CONDITIONS	100MS MIN	TYP	MAX	UNITS
Isolation Voltage					
Rated Continuous, DC		3500			VDC
Rated Continuous, AC		2000			Vrms
Test	10 Seconds	8000			VDC
Capacitance			5		pF
Resistance			10^{10}		Ω
Leakage Current	120V, 60Hz		0.23		μA

NOTE: Temperature changes (ΔT/Δt) greater than 1°C per minute below 0°C and long term storage above 100°C are not recommended.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
100MS	EMI Shield	124

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

APPLICATIONS INFORMATION

MULTIPLE DEVICE ORIENTATION

A typical application for the 100MS is shown in Figure 3. Using multiple devices within 30mm of each other can cause them to interact by forming beat frequency interference outputs. The 100MS can reduce this interference by as much as a factor of 200:1 depending on the distance between the devices and their relative orientation.

Minimum EMI results when the gaps of both shields are paralleled as in Figure 3a.

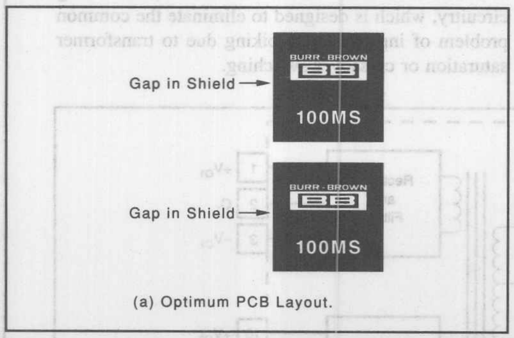


FIGURE 3a. Optimum PCB Layout. Orientation for minimum EMI.

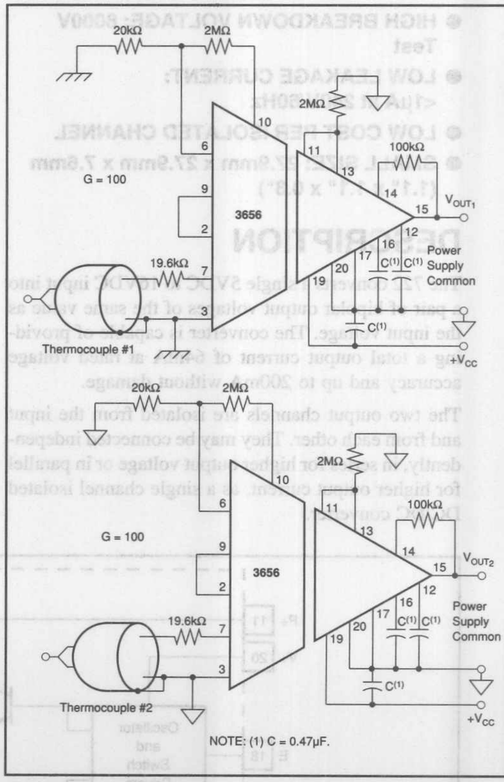
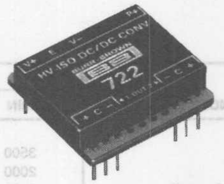


FIGURE 3b. Isolated Data Acquisition Input Circuitry. Orientation for Minimum EMI.

BURR - BROWN®



722

DUAL ISOLATED DC/DC CONVERTER

FEATURES

- DUAL ISOLATED ±5V TO ±16V OUTPUTS
- HIGH BREAKDOWN VOLTAGE: 8000V Test
- LOW LEAKAGE CURRENT: <1µA at 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE: 27.9mm x 27.9mm x 7.6mm (1.1" x 1.1" x 0.3")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION

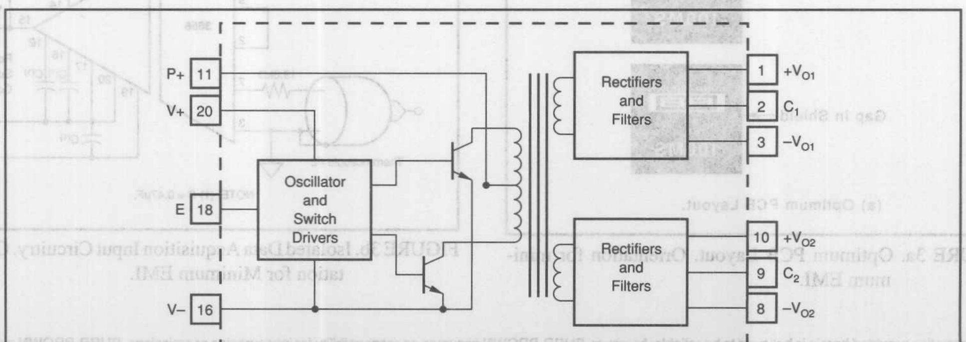
DESCRIPTION

The 722 converts a single 5VDC to 16VDC input into a pair of bipolar output voltages of the same value as the input voltage. The converter is capable of providing a total output current of 64mA at rated voltage accuracy and up to 200mA without damage.

The two output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage or in parallel for higher output current, as a single channel isolated DC/DC converter.

Integrated circuit construction of the 722 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 900kHz oscillator drives switching circuitry, which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{IN} = 15VDC, C = 0.47μF, R_1 selected per Typical Performance Curve.

PARAMETER	CONDITIONS	722			722BG			722MG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
Rated Input Voltage			15			*			*		VDC
Input Voltage Range(1)		5		16	*		*	*		*	VDC
Input Current	Total Output Current = 12mA		50			*			*		mA
	Total Output Current = 64mA		105	120		*	*		*	*	mA
	Total Output Current = 64mA at T_A = +85°C		120			*			*		mA
	Total Output Current = 160mA		—	—		225	275		—	—	mA
Input Ripple(2)	Total Output Current = 12mA		3			*			*		mA, pk
	Total Output Current = 64mA		6			*			*		mA, pk
	Total Output Current = 160mA		—			12			—		mA, pk
ISOLATION											
Test Voltages	Input-to-Output, 5 seconds, min			8000			*			*	Vpk
	Input-to-Output, 1 minute, min			—			—			2500	Vrms
	Channel-to-Channel, 5 seconds, min			5000			*			*	Vpk
Rated Voltages	Input-to-Output, continuous			3500			*			*	V
	Channel-to-Channel, continuous			2000	*		*			*	V
Isolation Impedance	Input-to-Output		10 || 6			*			*		GΩ || pF
Leakage Current(3)	Input-to-Output, 240V, 60Hz			1			*			*	μA
OUTPUT											
Rated Output Voltages(4)	I_{LOAD} = 3mA per Output	15.4		16.2	*		*	*		*	VDC
	I_{LOAD} = 16mA per Output	14.3		16.2	*		*	*		*	VDC
	I_{LOAD} = 40mA per Output	—	—	—	13.7	14.2	16.2	—	—	—	VDC
Output Current	Total of All Outputs			200			*			*	mA
	Any One Output(5)	3		100	*		*	*		*	mA
Load Regulation			(5)			*			*		
Ripple Voltage	I_{LOAD} = 3mA per Output		15			*			*		mVpk
	I_{LOAD} = 16mA per Output		35	100		*	*		*	*	mVpk
	I_{LOAD} = 40mA per Output		—			50			*		mVpk
Tracking Error between Dual Outputs	Balanced Loads		±100			*			*		mVDC
Sensitivity to Input Voltage Changes			1.13			*			*		V/V
Output Voltage Temperature Coefficient	$T_A = T_{SPECIFICATION\ RANGE}$		±0.02			*			*		%/°C
TEMPERATURE											
Specification	$I_{LOAD} \leq$ 16mA per Output	–25		+85	*		*	*		*	°C
	$I_{LOAD} \leq$ 40mA per Output	–25		+60	*		*	*		*	°C
Storage		–55		+125	*		*	*		*	°C
Junction Temperature				+125			*			*	°C

*Specifications same as 722.

NOTES: (1) For ambient temperature above +70°C the input voltage is 12.5V (max). The input voltage remains 16V (max) if case temperature is kept below +85°C. (2) External capacitor across "P+" to "V–" pins and 12" of #24 wire to V_{IN}. (3) Reference UL544, paragraph 27.5, Leakage Current. (4) See "Typical Performance Curves." (5) A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
722	20-Pin	102

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

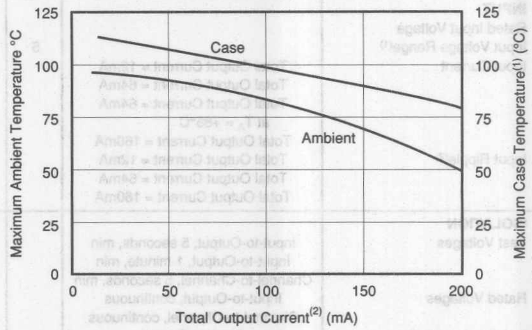
MODEL	PACKAGE	TEMPERATURE RANGE(1)
722	20-Pin	–25°C to +85°C
722BG	20-Pin	–25°C to +85°C
722MG	20-Pin	–25°C to +85°C

NOTE: (1) –25°C to +60°C for $I_{LOAD} \leq$ 40mA per Output.

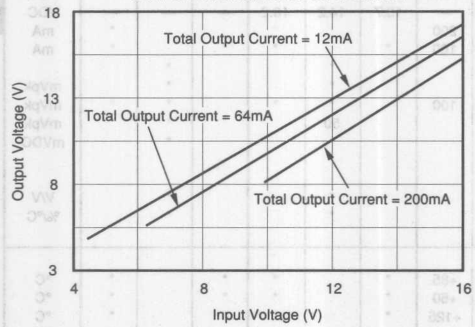
SELECTION OF R_1 OR EXTERNAL VOLTAGE V+ FOR MINIMUM INTERNAL POWER DISSIPATION

		MAXIMUM OUTPUT CURRENT FROM ANY SINGLE OUTPUT		
		<16mA	16mA to 30mA	30mA
Input Voltage (V)	>13	1.3kΩ	820Ω	510Ω
	11 to 13	820Ω	510Ω	200Ω
	9 to 11	510Ω	200Ω	0Ω
	8 to 9	200Ω	0Ω	—
	<8	0Ω	—	—
	$V+_{EXT}$	6.5V	7.5V	9.0V

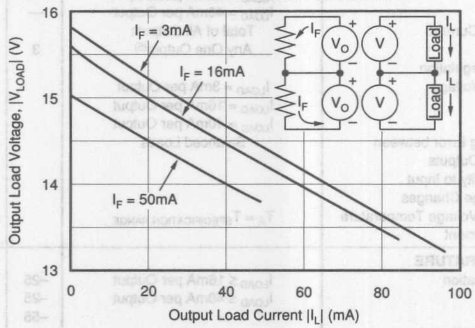
MAXIMUM SAFE OPERATING TEMPERATURE vs TOTAL OUTPUT CURRENT



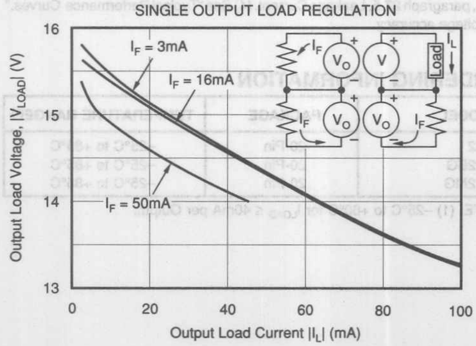
OUTPUT VOLTAGE vs INPUT VOLTAGE



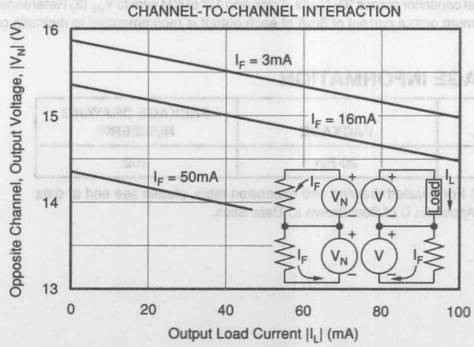
SINGLE-CHANNEL LOAD REGULATION



SINGLE OUTPUT LOAD REGULATION



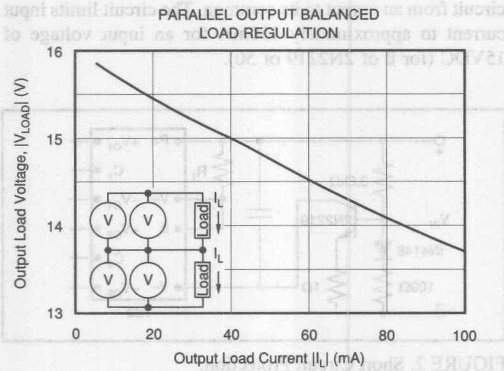
CHANNEL-TO-CHANNEL INTERACTION

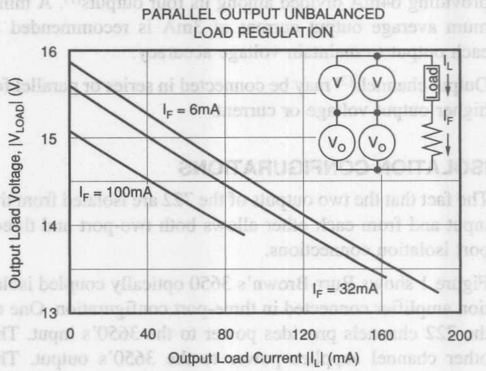


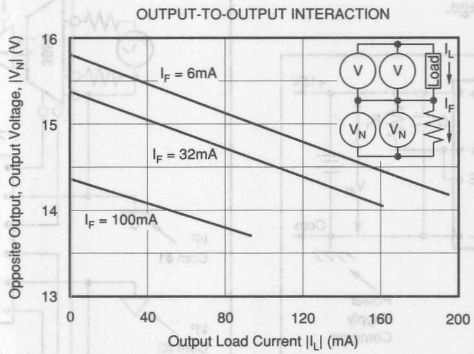
NOTES: (1) Using a 104mm x 19mm x 1.6mm aluminum strip mounted to the bottom of the case with heat sink compound. (2) Total output current is the sum of the currents for each individual output.

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_{IN} = 15VDC$, $C = 0.47\mu F$. R_1 selected per Typical Performance Curve.







INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 722 are shown in Figures 1 and 3. Primary power (V_{IN}) is applied at the "P+" and "V–" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V–"; the only requirement is that "P+" and "V+" must be positive with respects to "V–".

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor, R_1. The value of R_1 as a function of V_{IN} is shown in the Typical Performance Curves section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5V to +7.5V positive with respect to "V–." If a separate source is used, the "V+" input must be applied before the "P+" input to avoid possible damage to the unit. "P+" and "V+" must remain positive with respect to "V–" at all times (including transients). If necessary, diode clamps should be put across these inputs.

The "E" pin enables the converter when connected to "V+" and disables it when connected to "V–."

An external capacitor, "C" (0.47μF ceramic), is used to reduce input ripple. It should be connected as close to the "P+" and "V–" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 722 is not internally shielded, external shielding may be appropriate in applications where RFI at the 900kHz nominal oscillator frequency is a problem.

Each output is filtered with an internal 0.22μF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10μF between each output and its common.

DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 722 is capable of providing 64mA divided among its four outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

The fact that the two outputs of the 722 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows Burr-Brown's 3650 optically coupled isolation amplifier connected in three-port configuration. One of the 722 channels provides power to the 3650's input. The other channel supplies power to the 3650's output. The amplifier's input and output are isolated from each other and the system's power supply common. In this configuration, the 722's channel-to-channel isolation specification applies to the amplifier input-to-output voltage.

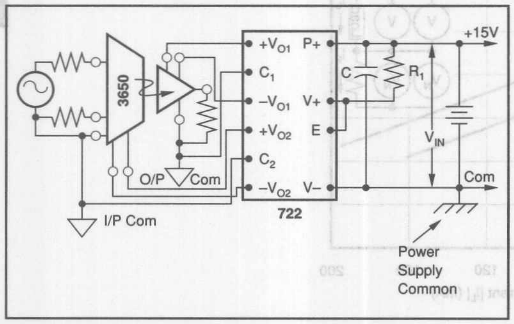


FIGURE 1. Three-Port Isolation.

Figure 3 illustrates how the 722 may provide isolated input power to the input stage of two 3650's connected in the two-port configuration. Power for the output stage is provided by the system +15V and –15V supplies. Input stages are isolated from each other and from the system supply. In this situation, the 722's input-to-output isolation specification applies to the amplifier's input-to-output voltages, while the channel-to-channel 722 specification applies to the voltage existing between "I/P Com #1" and "I/P Com #2."

NOTES: (1) "Output" denotes a single output terminal (+V or –V) and its associated common. (2) "Channel" denotes a pair of outputs (+V and –V) and their associated common.

SHORT CIRCUIT PROTECTION

The circuit in Figure 2 may be added to the input of the 722 to protect it from damage in situations where too much current is demanded from the outputs—such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for ß of 2N2219 of 50).

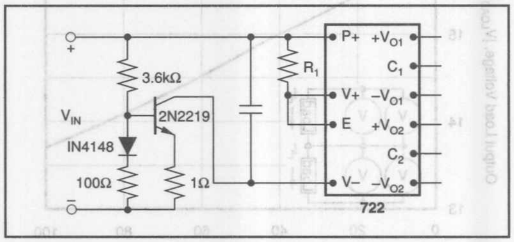


FIGURE 2. Short Circuit Protection.

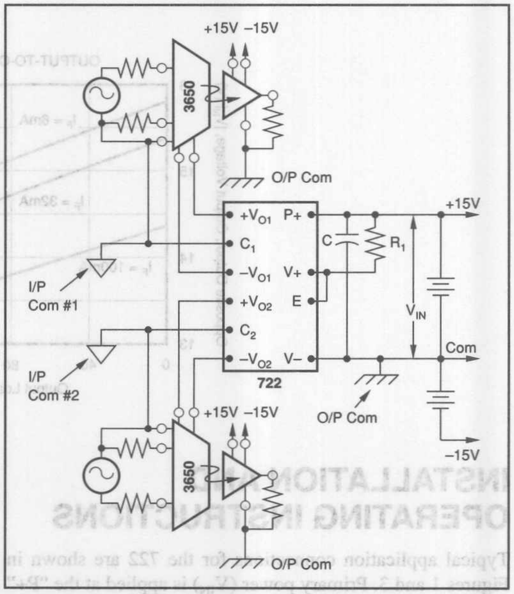
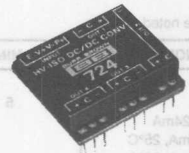


FIGURE 3. Two-Port Isolation with Two 3650's.

BURR - BROWN®

724



QUAD ISOLATED DC/DC CONVERTER

FEATURES

- QUAD ISOLATED ±8V OUTPUTS
- HIGH BREAKDOWN VOLTAGE: 3000V Test
- LOW LEAKAGE CURRENT: <1μA at 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE: 27.9mm X 27.9mm X 6.6mm (1.1" X 1.1" X 0.26")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION

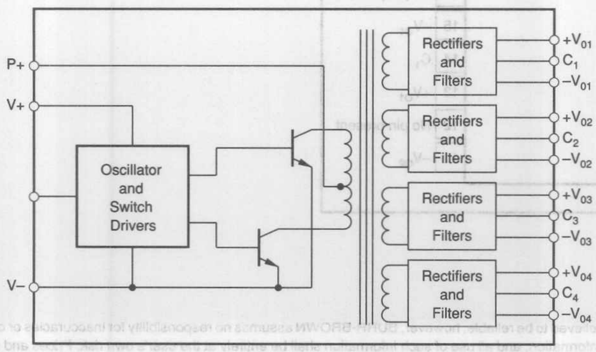
DESCRIPTION

The 724 converts a single 5VDC to 16VDC input into four pairs of bipolar output voltages of approximately half the output voltage. The converter is capable of providing a total output current of 128mA at rated voltage accuracy and up to 500mA without damage.

The four output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage, or in parallel for higher output current as a single channel isolated DC/DC converter.

Integrated circuit construction of the 724 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, and low leakage coating used on the internal assembly.

A self-contained 800kHz oscillator drives switching circuitry, which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.



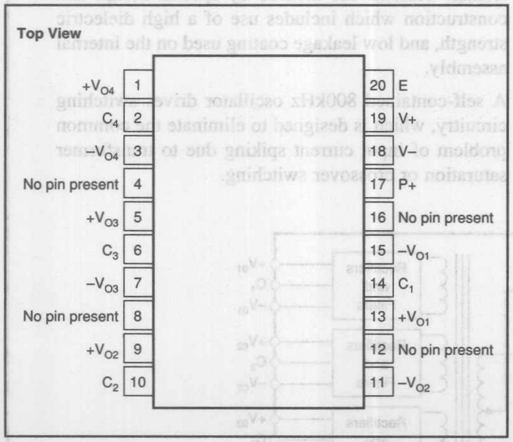
International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At 25°C with V_{IN} = 15V, R_1 = 1.3kΩ, C = 0.47µF, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Input Voltage		5	15	16	VDC
Input Current	ΣI_{OUT} = 24mA		50		mA
	ΣI_{OUT} = 128mA, 25°C		110	125	mA
	ΣI_{OUT} = 128mA, 25°C		120		mA
Input Ripple (1, 5)	ΣI_{OUT} = 24mA, C = 0.47µF		10		mA, pk
	ΣI_{OUT} = 128mA, C = 0.47µF			25	mA, pk
ISOLATION					
Test Voltage (2)	Input-to-Output, 5s min			3000	VDC
	Channel-to-Channel, 5s min			3000	VDC
Rated Voltage (2)	Input-to-Output, Continuous			1000	VDC
	Channel-to-Channel, Continuous			1000	VDC
Isolation Impedance	Input-to-Output		10 || 6		GΩ || pF
Leakage Current	Input-to-Output, 240V/60Hz			1.0	µA
OUTPUT					
Voltage (3)	At 15V Input I_L = 3mA	8.0	8.5	9.0	V
	I_L = 16mA	7.5	7.9	8.3	V
Current for Rated Voltage	Total of All Outputs			128	mA
	Any One Output (4)	3			
Total Safe Nondestructive Current	Total of All Outputs			500	mA
	Any One Output			200	mA
Load Regulation (3)			(4)		
Ripple Voltage (5)	I_L = 3mA		35		mV, pk
	I_L = 16mA			200	mV, pk
Difference of $+V_O$ and $-V_O$	$+I_L = -I_L$		±30		mV
Sensitivity to Input Voltage Change			0.63		V/V
Output Voltage Change Over Temperature	–25°C to +85°C		2		%
TEMPERATURE RANGE					
Operating		–25		+85	°C
Storage		–55		+125	°C

NOTES: (1) 0.47µF external capacitor across "P+" to "V–" pins and 12" of #24 wire to V_{IN}. (2) See "Isolation Voltage Ratings" on page 5. The input to output and channel to channel continuous AC rating is 700Vrms. (3) See "Typical Performance Curves." (4) A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy. (5) Test bandwidth 10MHz, max.

CONNECTION DIAGRAMS

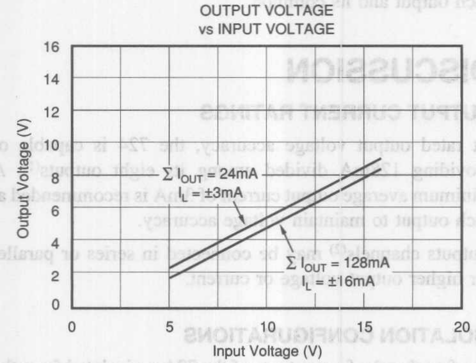


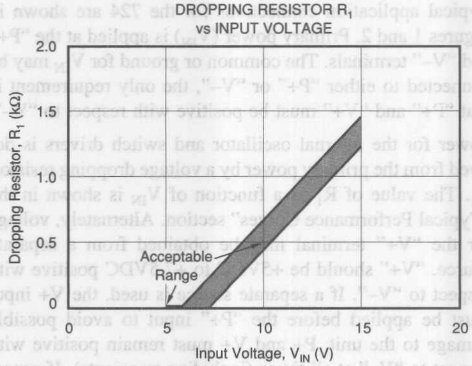
PACKAGE INFORMATION

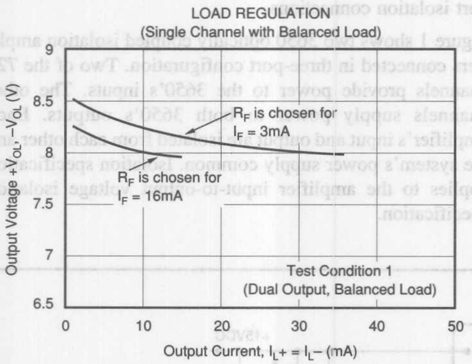
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
724	20-Pin	102

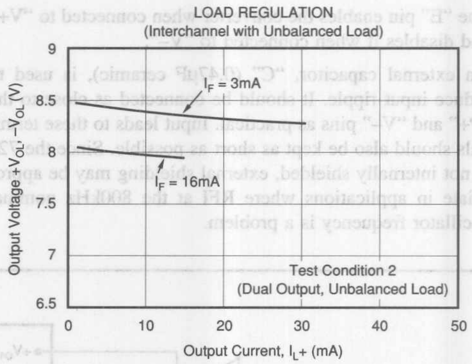
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

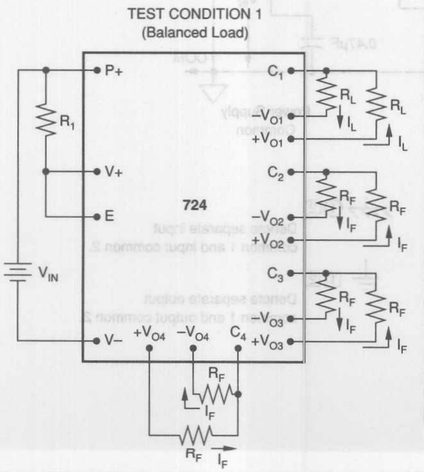
All specifications typical at 25°C, unless otherwise noted.

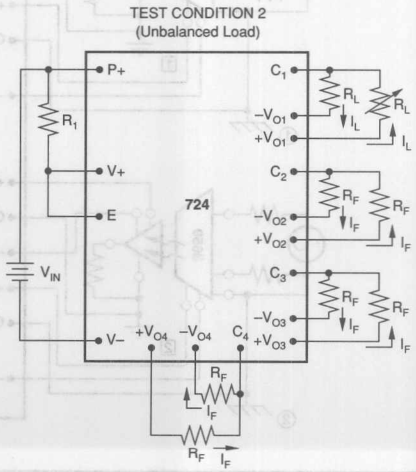












INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 724 are shown in Figures 1 and 2. Primary power (V_{IN}) is applied at the "P+" and "V–" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V–", the only requirement is that "P+" and "V+" must be positive with respect to "V–".

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor, R_1. The value of R_1 as a function of V_{IN} is shown in the "Typical Performance Curves" section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5VDC to +7.5VDC positive with respect to "V–". If a separate source is used, the V+ input must be applied before the "P+" input to avoid possible damage to the unit. P+ and V+ must remain positive with respect to "V–" at all times (including transients). If necessary, diode clamps should be put across these inputs.

The "E" pin enables the converter when connected to "V+" and disables it when connected to "V–".

An external capacitor, "C" (0.47µF ceramic), is used to reduce input ripple. It should be connected as close to the "P+" and "V–" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 724 is not internally shielded, external shielding may be appropriate in applications where RFI at the 800kHz nominal oscillator frequency is a problem.

Each output is filtered with an internal 0.047µF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10µF between each output and its common.

DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 724 is capable of providing 128mA divided among its eight outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Outputs channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

The fact that the four outputs of the 724 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows two 3650 optically coupled isolation amplifiers connected in three-port configuration. Two of the 724 channels provide power to the 3650's inputs. The other channels supply power to both 3650's outputs. Each amplifier's input and output are isolated from each other and the system's power supply common. Isolation specification applies to the amplifier input-to-output voltage isolation specification.

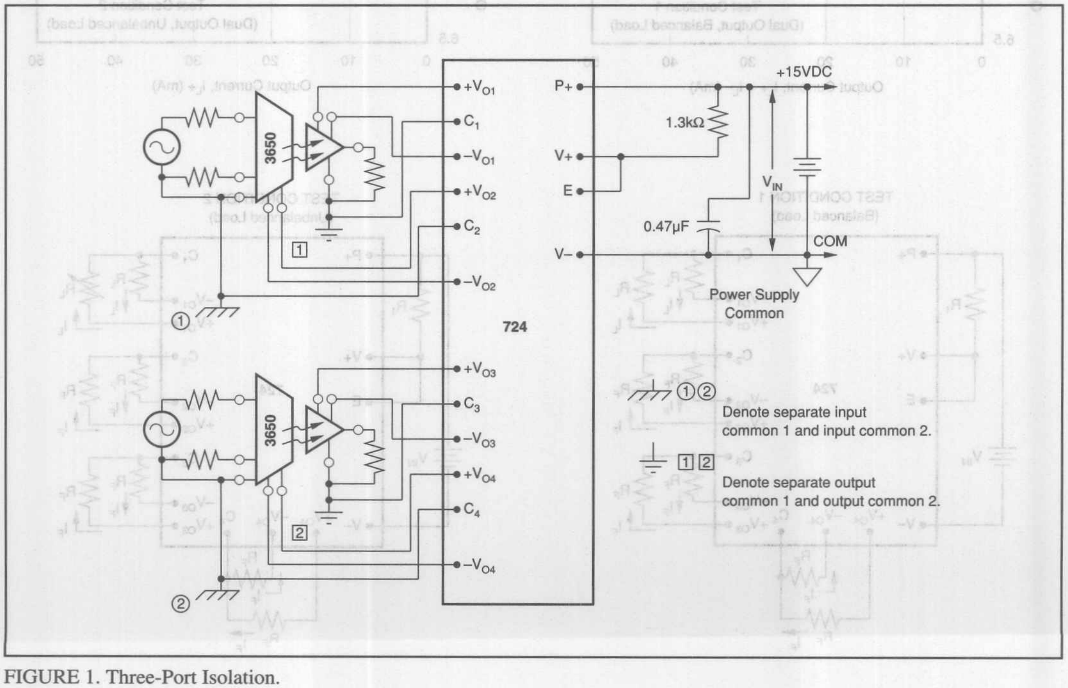


FIGURE 1. Three-Port Isolation.

Figure 2 illustrates how the 724 may provide isolated input power to the input stage of four 3650s connected in the two-port configuration. Power for the four output stages is provided by the system +15VDC and –15VDC supplies. Input stages are isolated from each other and from the system supply. In this situation, the 724's isolation specification applies to amplifier's input-to-output voltage and to the voltage existing between any two I/P COM terminals.

ISOLATION VOLTAGE RATINGS

Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration), it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated maximum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{TEST} = (2 \times V_{CONTINUOUS\ RATING}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.[3] Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 724 to protect it from damage in situations where too much current is demanded from the outputs—such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

NOTES: (1) "Output" denotes a single output terminal (+V or –V) and its associated common. (2) "Channel" denotes a pair of outputs (+V and –V) and their associated common. (3) Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111.

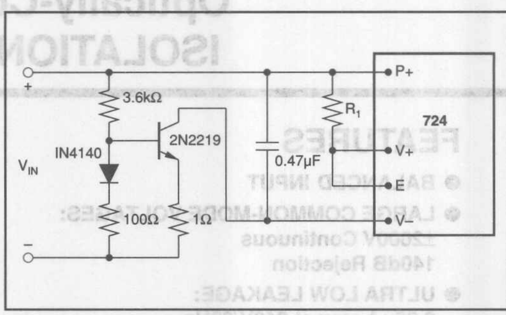


FIGURE 3. Short Circuit Protection.

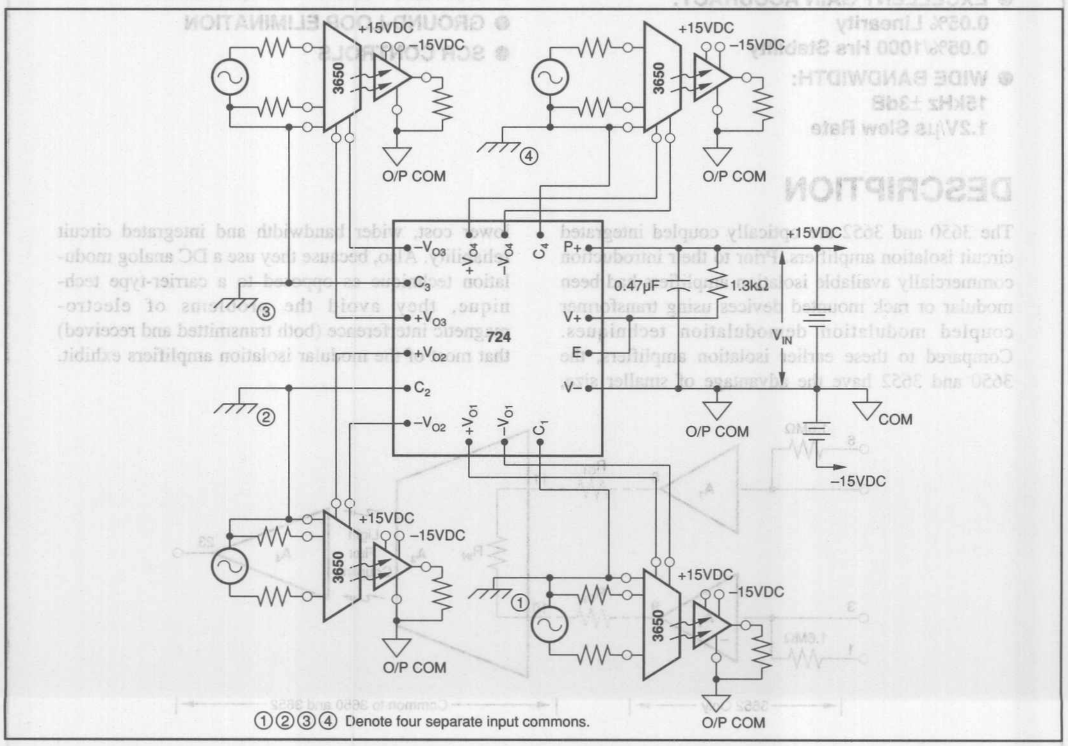
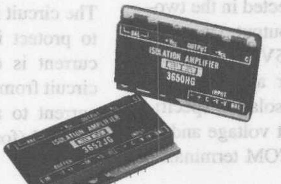


FIGURE 2. Two-Port Isolation with Four 3650s.

BURR - BROWN®



3650
3652

Optically-Coupled Linear ISOLATION AMPLIFIERS

FEATURES

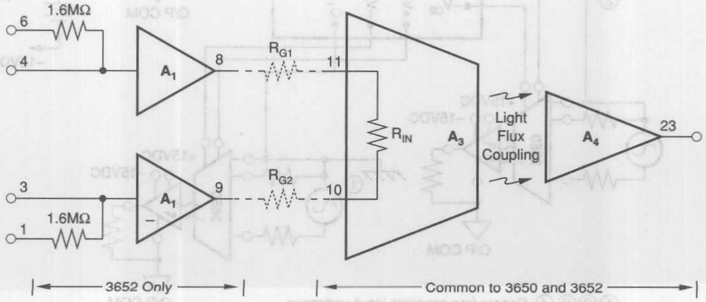
- BALANCED INPUT
- LARGE COMMON-MODE VOLTAGES:
  ±2000V Continuous
  140dB Rejection
- ULTRA LOW LEAKAGE:
  0.35μA max at 240V/60Hz
  1.8pF Leakage Capacitance
- EXCELLENT GAIN ACCURACY:
  0.05% Linearity
  0.05%/1000 Hrs Stability
- WIDE BANDWIDTH:
  15kHz ±3dB
  1.2V/μs Slew Rate

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- DATA ACQUISITION
- INTERFACE ELEMENT
- BIOMEDICAL MEASUREMENTS
- PATIENT MONITORING
- TEST EQUIPMENT
- CURRENT SHUNT MEASUREMENT
- GROUND-LOOP ELIMINATION
- SCR CONTROLS

DESCRIPTION

The 3650 and 3652 are optically coupled integrated circuit isolation amplifiers. Prior to their introduction commercially available isolation amplifiers had been modular or rack mounted devices using transformer coupled modulation demodulation techniques. Compared to these earlier isolation amplifiers, the 3650 and 3652 have the advantage of smaller size, lower cost, wider bandwidth and integrated circuit reliability. Also, because they use a DC analog modulation technique as opposed to a carrier-type technique, they avoid the problems of electromagnetic interference (both transmitted and received) that most of the modular isolation amplifiers exhibit.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At +25°C and ±15VDC supply voltages, unless otherwise specified.

MODEL	3650MG, HG(1)	3650JG	3650KG(1)	3652MG, HG(1)	3652JG
ISOLATION					
Isolation Voltage					
Rated Continuous, min	2000Vp or VDC				
Tested Voltage, min, 10s Duration	5000Vp				
Isolation Mode Rejection, G = 10					
DC	140dB				
60Hz, 5000Ω Source Unbalance	120dB				
Leakage Current, 240V/60Hz	0.35µA, max				
Isolation Impedance					
Capacitance	1.8pF				
Resistance	$10^{12}\Omega$				
GAIN					
Gain Equation					
for Current Sources	$G_1 = 10^6$V/Amp			$G_1 = 1.0057 \times 10^6$V/Amp(2)	
for Voltage Sources	$G_V1 = \frac{10^6}{R_{G1} + R_{G2} + R_{IN}}$ V/V			$\frac{10^6}{R_{G1} + R_{G2} + R_{IN} + R_O}$ V/V	
Input Resistance, R_{IN}, max	25Ω			25Ω	
Buffer Output Impedance, R_O	Not Applicable			90Ω ±30Ω	
Gain Equation Error, max(3)	1.5%	0.5%	0.5%	1.5%(4)	0.5%(4)
Gain Nonlinearity	±0.05% typ ±0.2% max	±0.03% typ ±0.1% max	±0.02% typ ±0.05% max	±0.05% typ ±0.2% max	±0.05% typ ±0.1% max
Gain vs Temperature	300ppm/°C	100ppm/°C	50ppm/°C	300ppm/°C	200ppm/°C
Gain vs Time	±0.05%/1000hrs			±0.05%/1000hrs	
Frequency Response					
Slew Rate	0.7V/µs min, 1.2V/µs typ				
±3dB Frequency	15kHz				
Settling Time					
to ±0.01%	400µs				
to ±0.1%	200µs				
INPUT STAGE(5)					
Input Offset Voltage					
at 25°C, max(3)	±5mV	±1mV	±0.5mV	±5mV	±2mV
vs Temperature, max	±25µV/°C	±10µV/°C	±5µV/°C	±50µV/°C	±25µV/°C
vs Supply	100µV/V			100µV/V	
vs Time	50µV/1000hrs			100µV/1000hrs	
Input Bias Current					
at 25°C	10nA typ, 40nA max			10pA typ, 50pA max	
vs Temperature	0.3nA/°C			Doubles Every +10°C	
vs Supply	0.2nA/V			1pA/V	
Input Offset Current				10pA	
vs Temperature	Effects Included			Doubles Every +10°C	
vs Supply	In Output Offset			1pA/V	
Input Impedance					
Differential	"R_{IN}" = 25Ω max			$10^{11}\Omega$	
Common-Mode	$10^9\Omega$			$10^{11}\Omega$	
Input Noise					
Voltage, 0.05Hz to 100Hz	4µVp-p			8µVp-p	
10Hz to 10kHz	4µVrms			5µVrms	
Input Voltage Range					
Common-Mode, Linear Operation,	±(|V| –5)V			±(|V| –5)	
w/o damage, at +, –	±V			±V	
at +I, –I	Not Applicable(6)			±300V for 10ms(7)	
at $+I_R$, $-I_R$	Not Applicable(6)			±3000V for 10ms(7)	
Differential, w/o damage, at +, –	±V			±V	
Differential, w/o damage, at +I, –I	Not Applicable			±600V for 10ms(7)	
Differential, w/o damage, at $+I_R$, $-I_R$	Not Applicable			±6000V for 10ms(7)	
Common-Mode Rejection, 60Hz	90dB at 60Hz, 5kΩ Imbalance			80dB at 60Hz, 5kΩ Imbalance	
Power Supply (Input Stage Only)					
Voltage (at "+V" and "–V")	±8V to ±18V			±8V to ±18V	
Current					
Quiescent	±1.2mA(8)			±3mA(8)	
with ±10V Output(7)	+6.5mA or –6.5mA, typ +12mA or –12mA, max			+8.5mA or –8.5mA, typ +16mA, or –16mA, max	

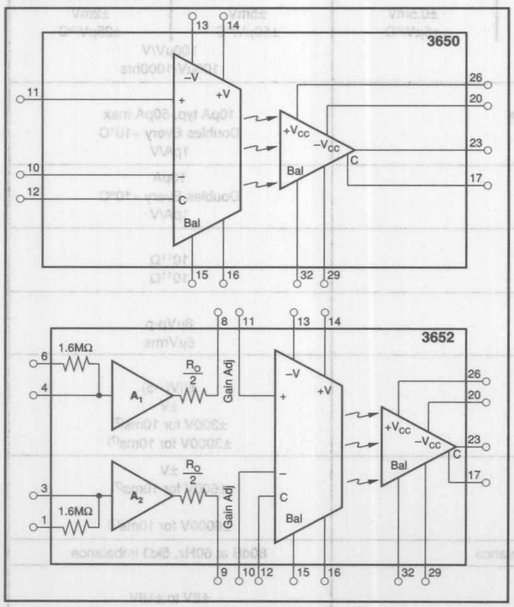
SPECIFICATIONS (CONT)

At +25°C and ±15VDC supply voltages, unless otherwise specified.

MODEL	3650MG, HG(1)	3650JG	3650KG	3652MG, HG(1)	3652JG
OUTPUT STAGE					
Output Voltage, min		±10V			±10V
Output Current, min		±5mA			±5mA
Output Offset Voltage					
at 25°C, max(3)	±25mV	±10mV	±10mV	±25mV	±10mV
vs Temperature, max	±900μV/°C	±450μV/°C	±300μV/°C	±900μV/°C	±450μV/°C
vs Supply		±500μV/V			±500μV/V
vs Time		±1mV/1000hrs			±1mV/1000hrs
Output Noise Voltage					
0.05Hz to 100Hz		50μVp-p			50μVp-p
10Hz to 1kHz		65μVrms			65μVrms
Power Supply (Output Stage Only)					
Voltage ("$+V_{CC}$" and "$-V_{CC}$")			±8V to ±18V		
Current					
Quiescent			±2.3mA typ, ±6mA max		
with ±5mA Output, max			±11mA		
TEMPERATURE(9)					
Specification			0°c to +85°C		
Operating			−40°C to +100°C		
Storage			−55°C to +125°C		

NOTES: (1) All electrical and mechanical specifications of the 3650MG and 3652MG are identical to the 3650HG and 3652HG, respectively, except that the following specifications apply to the 3650MG and 3652MG: (a) Isolation test voltage duration increased from 10 seconds minimum to 60 seconds minimum; (b) Input offset voltage at 25°C, max: ±10mV; vs temperature max: ±100μV/°C; (c) Output offset voltage at 25°C, max; ±50mV; vs temperature max; ±1.8mV/°C. (2) If used as 3650, see Installation and Operating Instructions. (3) Trimmable to zero. (4) Gain error terms specified for inputs applied through buffer amplifiers (i.e., ±1 or $\pm I_R$ pins). (5) Input stage specifications at +I and −I inputs for 3652 unless otherwise noted. (6) Maximum safe input current at either input is 10mA. (7) Continuous rating is 1/3 pulse rating. (8) Load current is drawn from one supply lead at a time: other supply current at quiescent level. For 3652 add 0.2mA/V of positive CMV. (9) dT/dt < 1°C/minute below 0°C, and long-term storage above 100°C is not recommended. Also limit the repeated thermal cycles to be within the 0°C to +85°C temperature range.

PIN CONFIGURATIONS



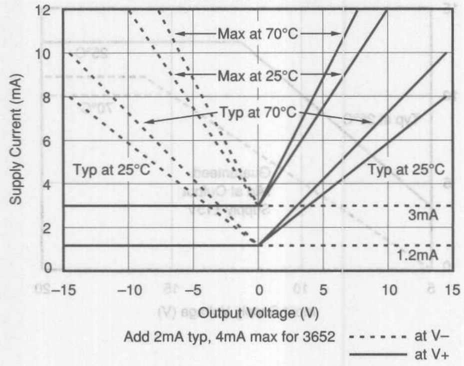
PACKAGE INFORMATION

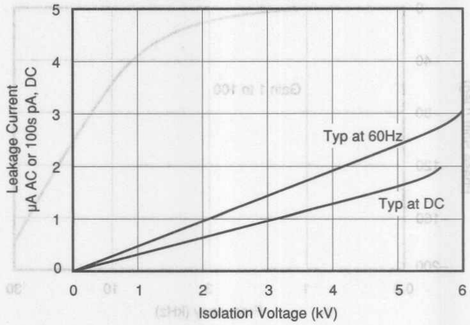
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
3650	32-Pin DIP	77
3652	32-Pin DIP	77

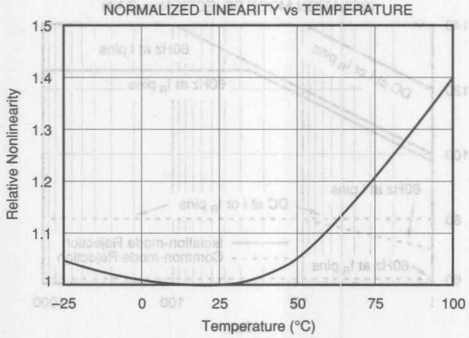
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

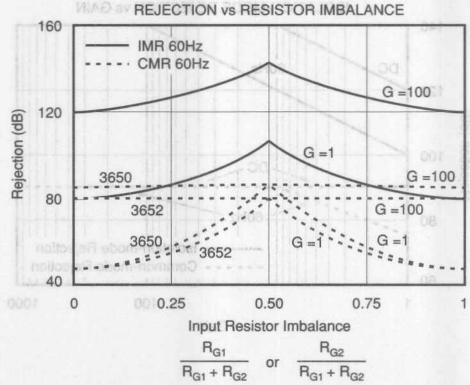
TYPICAL PERFORMANCE CURVES

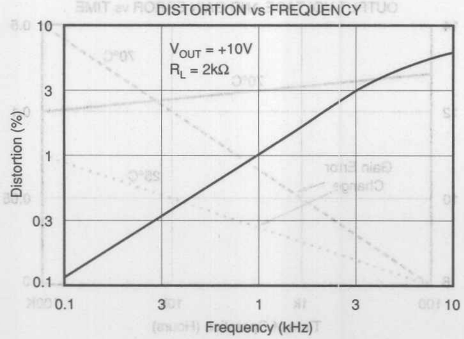
Typical at +25°C and ±15VDC power supplies, unless otherwise noted.

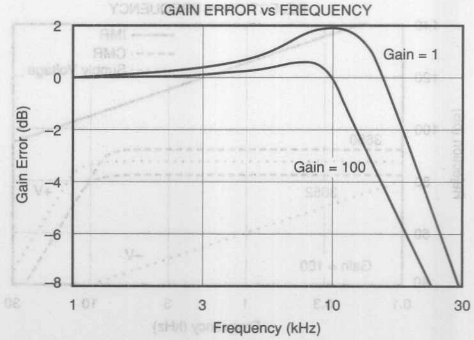










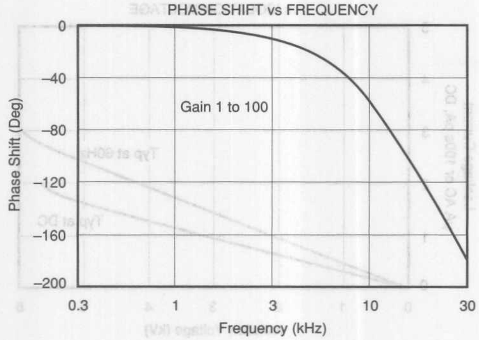


3650/3652

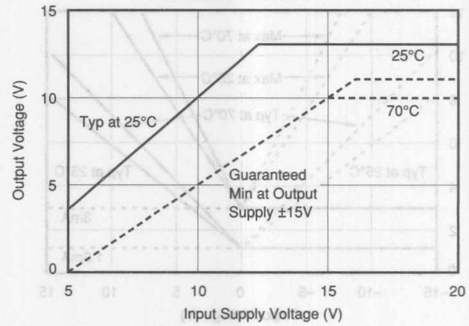
5

ISOLATION AMPLIFIERS

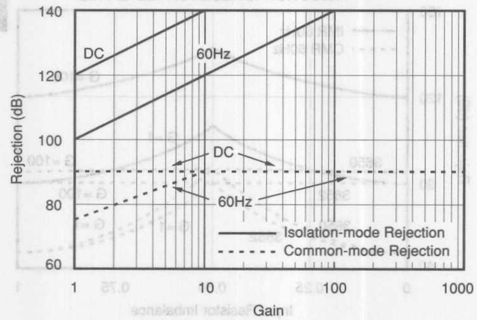
PHASE SHIFT vs FREQUENCY



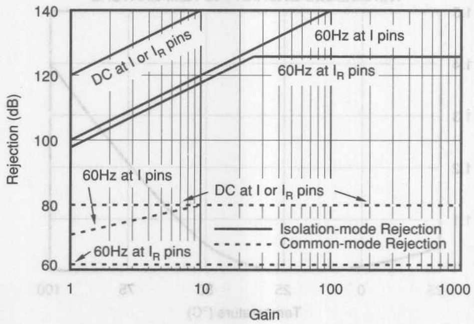
OUTPUT VOLTAGE SWING
vs INPUT SUPPLY VOLTAGE



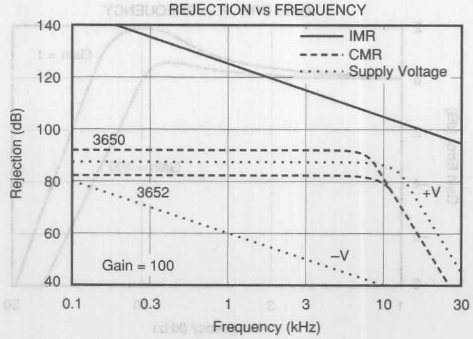
3650 COMMON-MODE AND
ISOLATION-MODE REJECTION vs GAIN



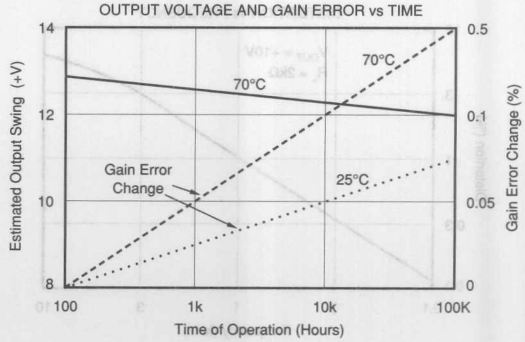
3652 COMMON-MODE AND
ISOLATION-MODE REJECTION vs GAIN



REJECTION vs FREQUENCY



OUTPUT VOLTAGE AND GAIN ERROR vs TIME



ISOLATION-MODE VOLTAGE, V_{ISO}

The isolation-mode voltage is the voltage which appears across the isolation barrier, i.e., between the input common and the output common. (See Figure 1.)

Two isolation voltages are given in the electrical specifications: "rated continuous" and "test voltage". Since it is impractical on a production basis to test a "continuous" voltage (infinite test time is implied), it is a generally accepted practice to test at a significantly higher voltage for some reasonable length of time. For the 3650 and 3652, the "test voltage" is equal to 1000V plus two times the "rated continuous" voltage. Thus, for a continuous rating of 2000V, each unit is tested at 5000V.

COMMON-MODE VOLTAGE, V_{CM}

The common-mode voltage is the voltage midway between the two inputs of the amplifier measured with respect to input common. It is the algebraic average of the voltage applied at the amplifiers' input terminals. In the circuit in Figure 1, $(V_+ + V_-)/2 = V_{CM}$. (NOTE: Many applications involve a large system "common-mode voltage." Usually in such cases the term defined here as "V_{CM}" is negligible and the system "common-mode voltage" is applied to the amplifier as "V_{ISO}" in Figure 1.)

ISOLATION-MODE REJECTION

The isolation-mode rejection is defined by the equation in Figure 1. The isolation-mode rejection is not infinite because there is some leakage across the isolation barrier due to the isolation resistance and capacitance.

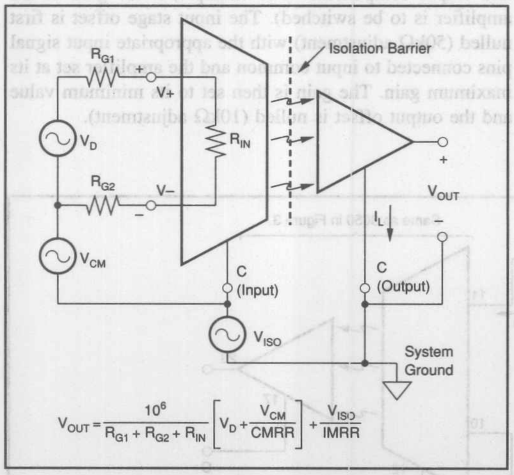


FIGURE 1. Illustration of Isolation-Mode and Common-Mode Specifications.

NOTE: (1) The only effect of decreased LED output is a slight decrease in full scale swing capability. See Typical Performance Curves.

straightline expressed as a percent of peak-to-peak full scale output (i.e. ±10mV at 20Vp-p ≈ 0.05%).

THEORY OF OPERATION

Prior to the introduction of the 3650 family optical isolation had not been practical in linear circuits. A single LED and photodiode combination, while useful in a wide range of digital isolation applications, has fundamental limitations—primarily nonlinearity and instability as a function of time and temperature.

The 3650 and 3652 use a unique technique to overcome the limitations of the single LED and photodiode isolator. Figure 2 is an elementary equivalent circuit for the 3650, which can be used to understand the basic operation without considering the cluttering details of offset adjustment and biasing for bipolar operation.

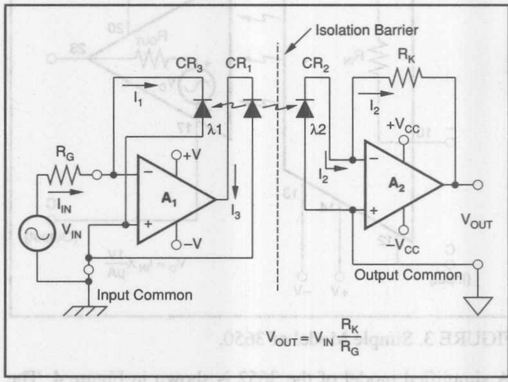


FIGURE 2. Simplified Equivalent Circuit of Linear Isolator.

Two matched photodiodes are used—one in the input (CR_3) and one in the output stage (CR_2)—to greatly reduce nonlinearities and time-temperature instabilities. Amplifier A_1, LED CR_1, and photodiode CR_3 are used in a negative feedback configuration such that $I_1 = I_{IN} R_G$ (where R_G is the user supplied gain setting resistor). Since CR_2 and CR_3 are closely matched, and since they receive equal amounts of light from the LED CR_1 (i.e., $\lambda_1 = \lambda_2$), $I_2 = I_1 = I_{IN}$. Amplifier A_2 is connected as a current-to-voltage converter with $V_{OUT} = I_2 R_K$ where R_K is an internal 1MΩ scaling resistor. Thus the overall transfer function is:

$$V_{OUT} = V_{IN} \frac{10^6}{R_G}, \ (R_G \text{ in } \Omega s)$$

This improved isolator circuit overcomes the primary limitations of the single LED and photodiode combination. The transfer function is now virtually independent of any degradation in the LED output as long as the two photodiodes and optics are closely matched(1). Linearity is now a

function of the accuracy of the matching and is further enhanced by the use of negative feedback in the input stage. Advanced laser trimming techniques are used to further compensate for residual matching errors.

A model of the 3650 suitable for simple circuit analysis is shown in Figure 3. The output is a current dependent voltage source, V_D, whose value depends on the input current. Thus, the 3650 is a transconductance amplifier with a gain of one volt per microamp. When voltage sources are used, the input current is derived by using gain setting resistors in series with the voltage source (see Installation and Operating Instructions for details). R_{IN} is the differential input impedance. The common-mode and isolation impedances are very high and are assumed to be infinite for this model.

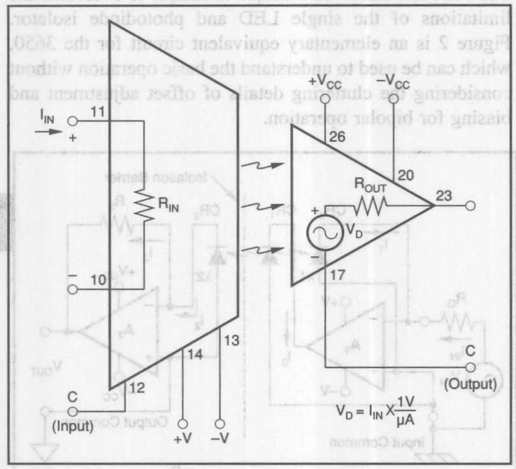


FIGURE 3. Simple Model of 3650.

A simplified model of the 3652 is shown in Figure 4. The isolation and output stages are identical to the 3650. Additional input circuitry consisting of FET buffer amplifiers and input protection resistors have been added to give higher differential and common-mode input impedance ($10^{11}\Omega$), lower bias currents (50pA) and overvoltage protection. The $+I_R$ and $-I_R$ inputs have a 10ms pulse rating of 6000V differential and 3000V common-mode (see Definitions for a discussion of common-mode and isolation-mode voltages.) The addition of the buffer amplifiers also creates a voltage-in voltage-out transfer function with the gain set by R_{G1} and R_{G2}.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

The power supply connections for the 3650 and 3652 are shown in Figure 5. When a DC/DC converter is used for isolated power, it is placed in parallel with the isolation barrier of the amplifier. This can lower the isolation impedance and degrade the isolation-mode rejection of the overall circuit. Therefore, a high quality, low leakage DC/DC converter such as the Burr-Brown Model 722 should be used.

OFFSET VOLTAGE ADJUSTMENTS

The offset nulling circuits are identical for the 3650 and 3652 and are shown in Figure 5. The offset adjust circuitry is optional and the units will meet the stated specifications with the BAL terminals unconnected. Provisions are available to null both the input and output stage offsets. If the amplifier is operated at a fixed gain, normally only one adjustment will be used: the output stage (10kΩ adjustment) for low gains and the input stage (50kΩ adjustment) for high gains, (>10).

Use the following procedure if it is desired to null both input and output components. (For example, if the gain of the amplifier is to be switched). The input stage offset is first nulled (50kΩ adjustment) with the appropriate input signal pins connected to input common and the amplifier set at its maximum gain. The gain is then set to its minimum value and the output offset is nulled (10kΩ adjustment).

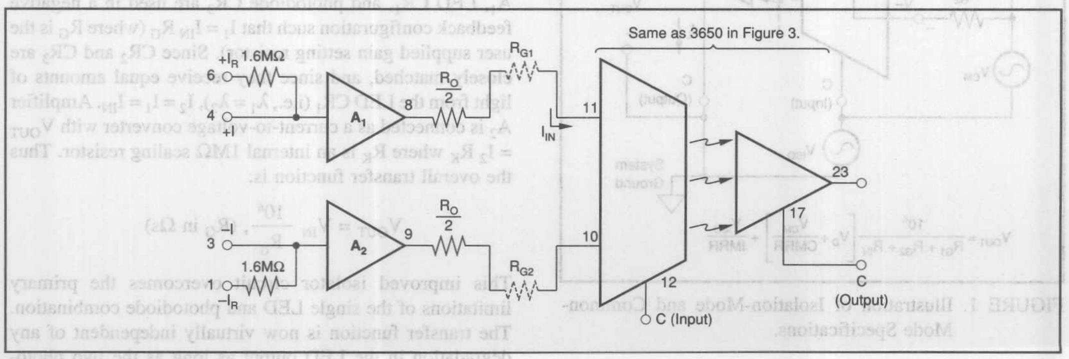


FIGURE 4. Simple Model of 3652.

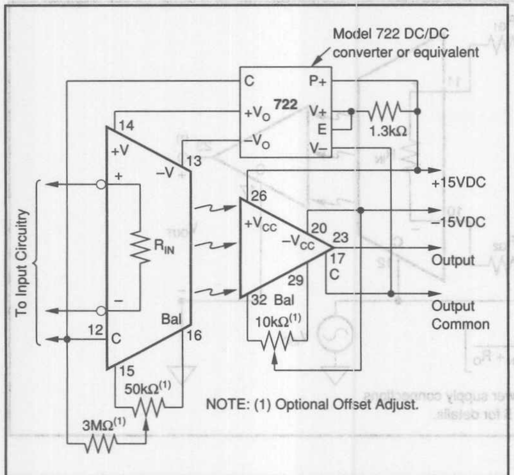
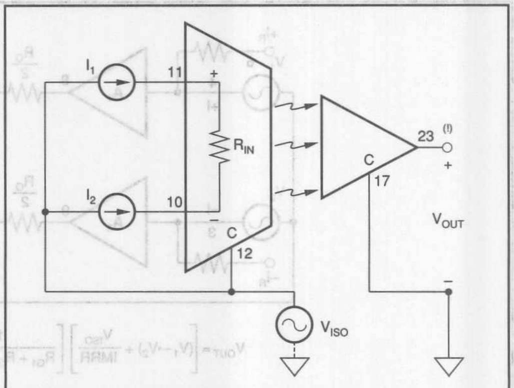


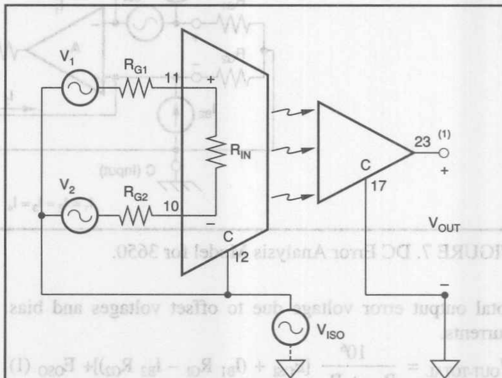
FIGURE 5. Power and Offset Adjust Connections.



$$V_{OUT} = (I_1 - I_2) \times 10^6 V/A + V_{ISO} \times IMRR^{(2)}$$

NOTE: (1) The offset adjustment circuitry and power supply connections have been omitted for simplicity. Refer to Figure 5 for details. (2) IMRR here is in pA/V, typically 5pA/V at 60Hz and 1pA/V at DC.

FIGURE 6a. 3650 with Differential Current Sources.



$$V_{OUT} = \left[(V_1 - V_2) + \frac{V_{ISO}}{IMRR}\right]\left[\frac{10^6\Omega}{R_{G1} + R_{G2} + R_{IN} + R_O}\right]$$

NOTE: (1) The offset adjustment circuitry and power supply connections have been omitted for simplicity. Refer to Figure 5 for details.

FIGURE 6b. 3650 with Differential Voltage Sources.

INPUT CONFIGURATIONS

Some possible input configurations for the 3650 and 3652 are shown in Figures 6a, 6b, 6c. Differential input sources are used in these examples. For situations with nondifferential inputs, the appropriate source term should be set to zero in the gain equations and replaced with a short in the diagrams.

Figure 6a shows the 3650 connected as a transconductance amplifier with input current sources. Voltage sources are shown in Figure 6b. In this case the voltages are converted to currents by R_{G1} and R_{G2}. As shown by the equations, they perform as gain setting resistors in the voltage transfer function. When a single voltage source is used, it is recommended (but not essential) that the gain setting resistor remain split into two equal halves in order to minimize errors due to bias currents and common-mode rejection (see Typical Performance Curves).

Figure 6c illustrates the connections for the 3652 when the FET buffer amplifiers, A_1 and A_2, are used. This configuration provides an isolation amplifier with high input impedance (both common-mode and differential, and good common-mode and isolation-mode rejection. It is a true isolated instrumentation amplifier which has many benefits for noise rejection when source impedance imbalances are present.

In the 3652, the voltage gain of the buffer amplifiers is slightly less than unity, but the gain of the output stage has been raised to compensate for this so that the overall transfer function from the ±I or $\pm I_R$ inputs to the output is correct. It should be noted that A_1 and A_2 are buffer amplifiers. No summing can be done at the ±I or $\pm I_R$ inputs. Figure 6c shows the +I and –I inputs used. If more input voltage protection is desired, then the $+I_R$ and $-I_R$ inputs should be used. This will increase the input noise due to the contribution from the 1.6MΩ resistors, but will provide additional differential and common-mode protection (10ms rating of 3kV).

ERROR ANALYSIS

A model of the 3650 suitable for DC error analysis of offset voltage, voltage drift versus temperature, bias current, etc., is shown in Figure 7.

A_1 and A_2, the input and output stage amplifiers, are considered to be ideal. Separate external generators are used to model the offset voltages and bias currents. R_{IN} is assumed to be small relative to R_{G1} and R_{G2} and is therefore omitted from the gain equation. The feedback configuration, optics and component matching are such that $I_1 = I_2 = I_3 = I_4$. A simple circuit analysis gives the following expression for the

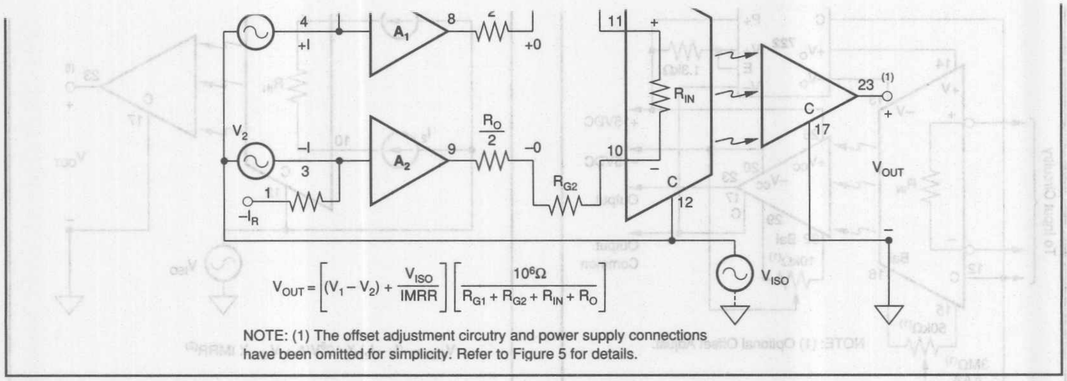


FIGURE 6c. 3652 with Differential Voltage Sources.

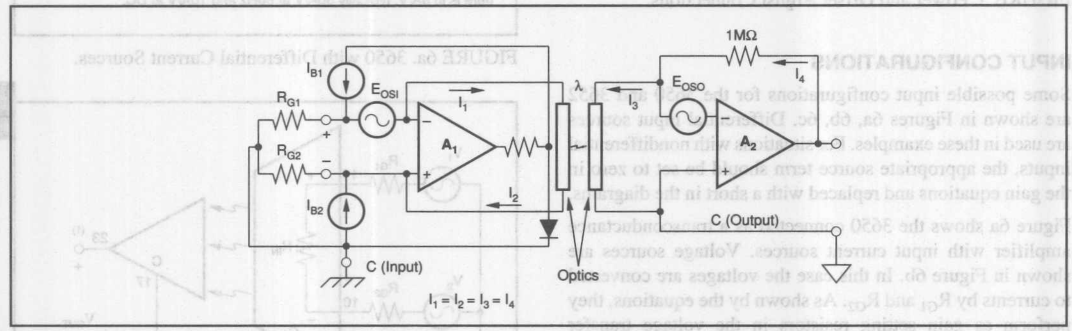


FIGURE 7. DC Error Analysis Model for 3650.

total output error voltage due to offset voltages and bias currents.

$$V_{OUT\text{-}TOTAL} = \frac{10^6}{R_{G1} + R_{G2}} [E_{OSI} + (I_{B1} R_{GI} - I_{B2} R_{G2})] + E_{OSO} \quad (1)$$

Offset current is defined as the difference between the two bias currents I_{B1} and I_{B2}. If $I_{B1} = I_B$ and $I_{B2} = I_B + I_{OSI}$

then, for $R_{G1} = R_{G2}$, $V_{OUT} - I_B = \dfrac{10^6 I_{OS}}{2}$

This component of error is not a function of gain and is therefore included as a part of E_{OSO} specifications. The output errors due to the output stage bias current are also included in E_{OSO}. This results in a very simple equation for the total error:

$$V_{OUT\text{-}TOTAL} = \frac{10^6 E_{OSI}}{2R_{GI}} + E_{OSO} \text{ (for } R_{G1} = R_{G2}\text{).} \quad (2)$$

In summary, it should be noted that equation (2) should be used only when $R_{G1} = R_{G2}$. When $R_{G1} \neq R_{G2}$, equation (1) applies.

The effects of temperature may be analyzed by replacing the offset terms with their corresponding temperature gradient terms:

$$V_{OUT} \rightarrow \Delta V_{OUT}/\Delta T,\ E_{OSI} \rightarrow \Delta E_{OSI}/\Delta T, \text{ etc.}$$

For a complete analysis of the effects of temperature, gain variations must also be considered.

OUTPUT NOISE

The total output noise is given by:

$$E_N \text{ (RMS)} = \sqrt{(E_{NI}G)^2 + (E_{NO})^2}$$

where E_N (RMS) = Total output noise

E_{NI} = RMS noise of the input stage

E_{NO} = RMS noise of the output stage

$G = 10^6/(R_{G1} + R_{G2})$

E_{NO} includes the noise contribution due to the optics and the noise currents of the output stage. Errors created by the noise current of the input stage are insignificant compared to other noise sources and are therefore omitted.

COMMON-MODE AND ISOLATION-MODE REJECTION

The expression for the output error due to common-mode and isolation mode voltage is:

$$V_{OUT} = G\left[\frac{V_{CM}}{CMRR} + \frac{V_{ISO}}{IMRR}\right]$$

GUARDING AND PROTECTION

To preserve the excellent inherent isolation characteristics of these amplifiers, the following recommended practice should be noted.

1. Use shielded twisted pair of cable at the input as with any instrumentation amplifier.
2. Care should be taken to minimize external capacitance. A symmetrical layout of external components to achieve balanced capacitance from the input terminals to output common will preserve high IMR.
3. External components and conductor patterns should be at a distance equal to or greater than the distance between the input and output terminals to prevent HV breakdown.
4. Though not an absolute requirement, the use of laminated or conformally coated printed circuit boards is recommended.

APPLICATIONS

Figure 8 shows a system where isolation amplifiers (3650) are used to measure the armature current and the armature voltage of a motor.

The armature current of the motor is converted to a voltage by the calibrated shunt R_S and then amplifier (adjustable gain) and isolated by the 3650.

The armature voltage is sensed by the voltage divider (adjustable) shown and then amplified and isolated by the 3650.

The 3650 provides the advantage of accurate current measurement in the presence of high common-mode voltage. Both 3650s provide the advantage of isolating the motor ground from the control system ground. Isolated power is provided by an isolated DC/DC converter (BB Model 722 or equivalent).

The 3652 is ideally suited for patient monitoring applications as shown in Figure 9. The fact that it is a true balanced input instrumentation amplifier with very high differential and common-mode impedance means that it can greatly reduce the common-mode noise pick up due to imbalance in lead impedances that often appear in patient monitoring situations. The 3kV and 6kV shown in Figure 9 are the 10ms pulse ratings of the $+I_R$ and $-I_R$ inputs for the common-mode and differential input voltages with respect to input common. The rating of the isolation barrier is 2000Vpk continu-

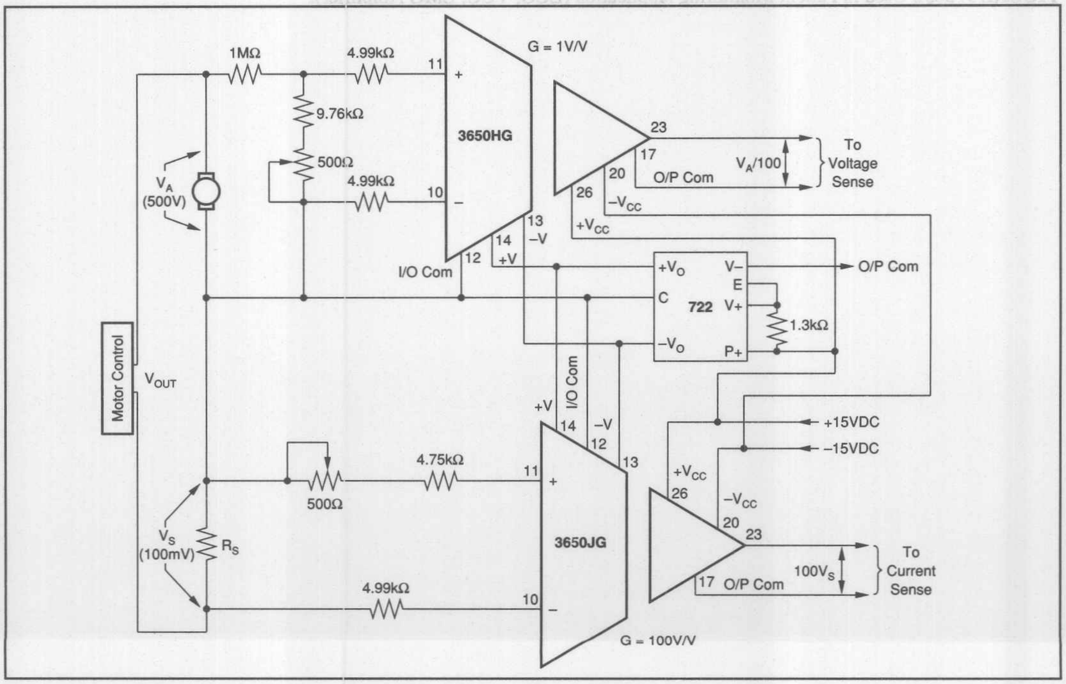


FIGURE 8. Isolated Armature Current and Voltage Sensor.

ous. The nonrecurrent pulse rating of the isolation barrier is 5000Vpk, since each unit is factory tested at 5000Vpk. If the isolation barrier is to be subjected to higher voltages a gas filled surge voltage protection device can be used. For multichannel operation, two 3652s can be powered by one Model 722 isolated DC/DC converter. The total leakage current for both channels at 240V 60Hz would still be less than 2μA.

The block diagram in Figure 10 shows the use of isolation amplifiers in SCR control application.

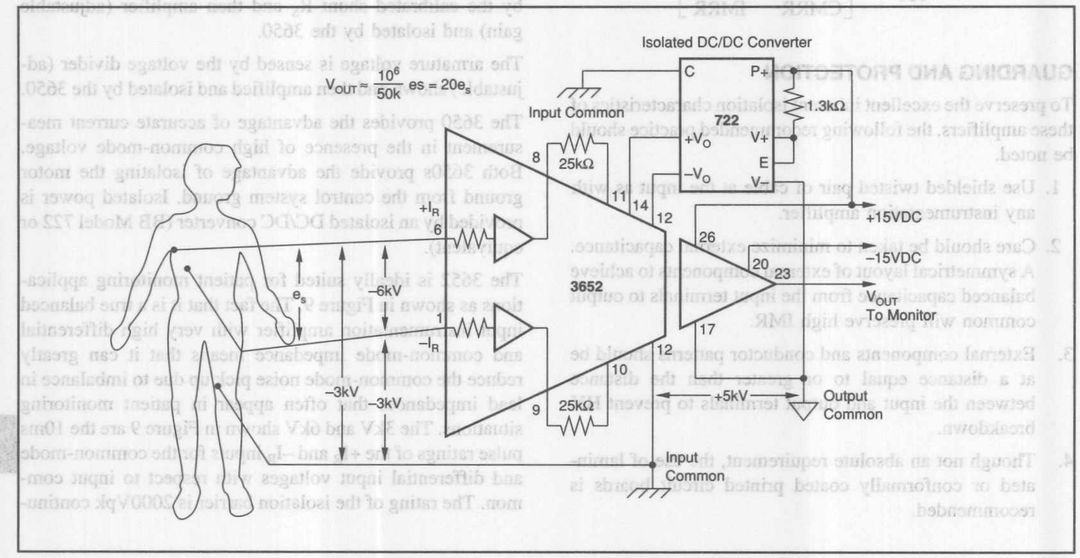


FIGURE 9. 3652 Used in Patient Monitoring Application (ECG, VCG, EMG Amplifier).

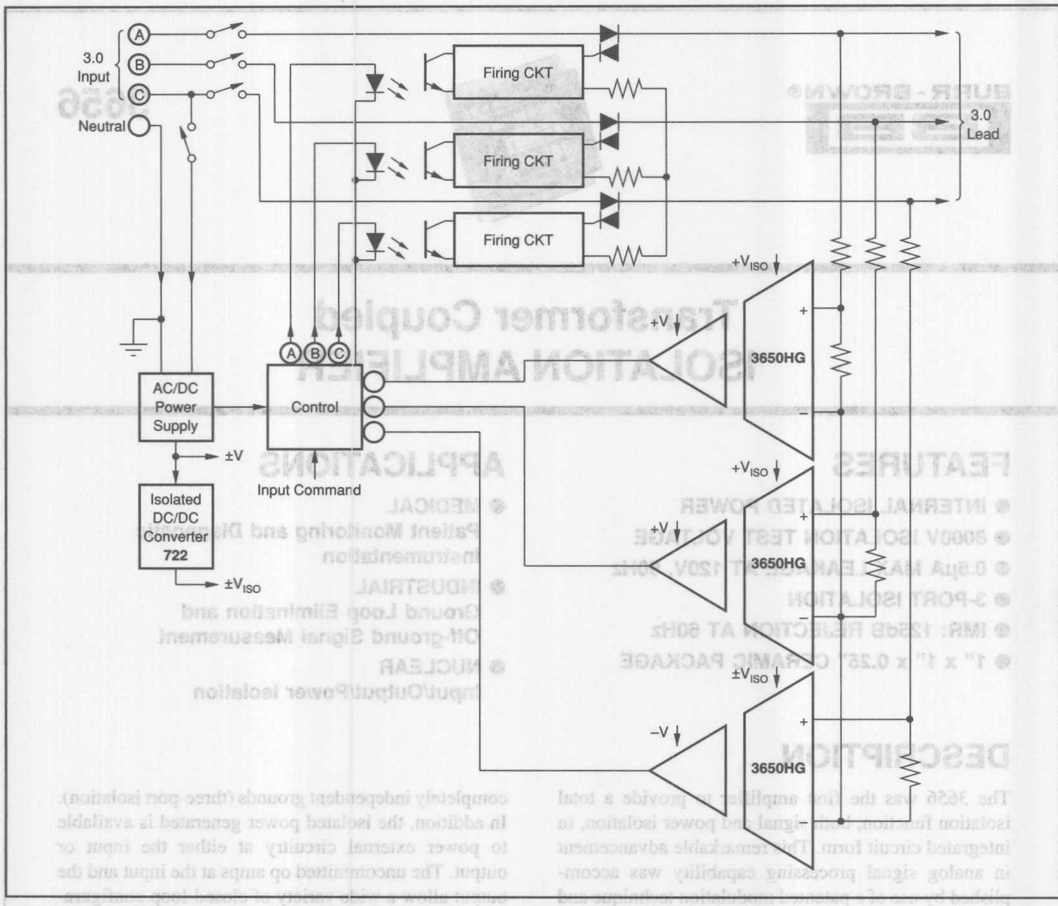
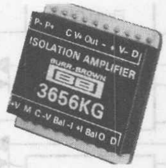


FIGURE 10. 3-Phase Bidirectional SCR Control with Voltage Feedback.

BURR - BROWN®



3656

Transformer Coupled
ISOLATION AMPLIFIER

FEATURES

- INTERNAL ISOLATED POWER
- 8000V ISOLATION TEST VOLTAGE
- 0.5μA MAX LEAKAGE AT 120V, 60Hz
- 3-PORT ISOLATION
- IMR: 125dB REJECTION AT 60Hz
- 1" x 1" x 0.25" CERAMIC PACKAGE

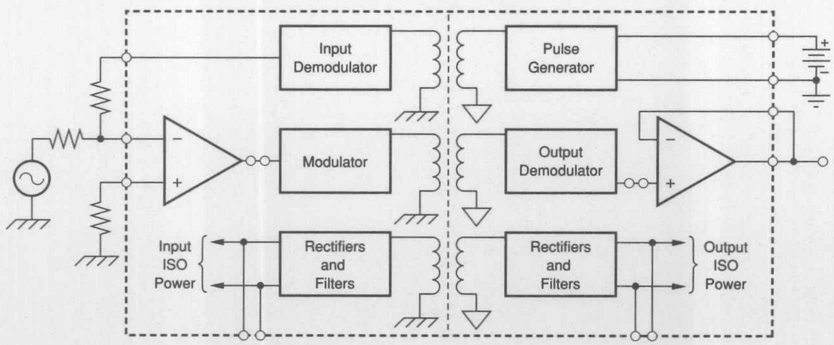
APPLICATIONS

- **MEDICAL**
  Patient Monitoring and Diagnostic Instrumentation
- **INDUSTRIAL**
  Ground Loop Elimination and Off-ground Signal Measurement
- **NUCLEAR**
  Input/Output/Power Isolation

DESCRIPTION

The 3656 was the first amplifier to provide a total isolation function, both signal and power isolation, in integrated circuit form. This remarkable advancement in analog signal processing capability was accomplished by use of a patented modulation technique and miniature hybrid transformer.

Versatility and performance are outstanding features of the 3656. It is capable of operating with three completely independent grounds (three-port isolation). In addition, the isolated power generated is available to power external circuitry at either the input or output. The uncommitted op amps at the input and the output allow a wide variety of closed-loop configurations to match the requirements of many different types of isolation applications.



This product is covered by the following United States patents: 4,066,974; 4,103,267; 4,082,908. Other patents pending may also apply upon the allowance and issuance of patents thereon. The product may also be covered in other countries by one or more international patents corresponding to the above-identified U.S. patents.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At +25°C, V± = 15VDC and 15VDC between P+ and P–, unless otherwise specified.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG MIN	TYP	MAX	UNITS
ISOLATION					
Voltage					
Rated Continuous(1), DC		3500 (1000)			VDC
Test, 10s(1)		8000 (3000)			VDC
Test, 60s(1)	G_1 = 10V/V	2000 (700)			Vrms
Rejection					
DC			160		dB
60Hz, < 100Ω in I/P Com(2)			125		dB
60Hz, 5kΩ in I/P Com(2)					
3656HG		108			dB
3656AG, BG, JG, KG		112			dB
Capacitance(1)			6 (6.3)		pF
Resistance(1)			10^{12} (10^{12})		Ω
Leakage Current	120V, 60Hz		0.28	0.5	µA
GAIN					
Equations	See Text				
Accuracy of Equations					
Initial(3) 3656HG	G < 100V/V			1.5	%
3656AG, JG, KG				1	%
3656BG				0.3	%
vs Temperature 3656HG				480	ppm/°C
3656AG, JG				120	ppm/°C
3656BG, KG				60	ppm/°C
vs Time			0.02 (1 + log khrs.)		%
Nonlinearity	$R_A + R_F = R_B \geq 2M\Omega$				
External Supplies Used at					
Pins 12 and 16, 3656HG	Unipolar or Bipolar Output			±0.15	%
3656AG, JG, KG				±0.1	%
3656BG				±0.05	%
Internal Supplies Used for Output Stage	Bipolar Output Voltage Swing, Full Load(4)		±0.15		%
OFFSET VOLTAGE(5), RTI					
Initial(3), 3656HG	15Vp between P+ and P–			$\pm[4 + (40/G_1)]$	mV
3656AG, JG				$\pm[2 + (20/G_1)]$	mV
3656BG, KG				$\pm[1 + (10/G_1)]$	mV
vs Temperature, 3656HG				$\pm[200 + (1000/G_1)]$	µV/°C
3656JG				$\pm[50 + (750/G_1)]$	µV/°C
3656AG				$\pm[25 + (500/G_1)]$	µV/°C
3656KG				$\pm[10 + (350/G_1)]$	µV/°C
3656BG				$\pm[5 + (350/G_1)]$	µV/°C
vs Supply Voltage	Supply between P+ and P–				
3656HG				$\pm[0.6 + (3.5/G_1)]$	mV/V
3656AG, BG, JG, KG				$\pm[0.3 + (2.1/G_1)]$	mV/V
vs Current(6)			$\pm[0.1 + (10/G_1)]$	$\pm[0.2 + (20/G_1)]$	mV/mA
vs Time			$\pm[10 + (100/G_1)] \cdot$ (1 + log khrs.)		µV
AMPLIFIER PARAMETERS, Apply to A_1 and A_2					
Bias Current(7)					
Initial				100	nA
vs Temperature			0.5		nA/°C
vs Supply			0.2		nA/V
Offset Current(7)			5	20	nA
Impedance	Common-Mode		100 ‖ 5		MΩ ‖ pF
Input Noise Voltage	f_B = 0.05Hz to 100Hz		5		µVp-p
	f_B = 10Hz to 10kHz		5		µVrms
Input Voltage Range(8)					
Linear Operation	Internal Supply			±5	V
	External Supply			Supply –5	V
Output Current	V_{OUT} = ±5V				
	±15V External Supply	±5			mA
	Internal Supply	±2.5			mA
	V_{OUT} = ±10V				
	±15V External Supply	±2.5			mA
	V_{OUT} = ±2V, $V_{P+,\,P-}$ = 8.5V				
	Internal Supply		±1		mA
Quiescent Current			150	450	µA

SPECIFICATIONS (CONT)

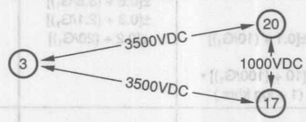
ELECTRICAL

At +25°C, V± = 15VDC and 15VDC between P+ and P–, unless otherwise specified.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE					
±3dB Response	Small Signal		30		kHz
Full Power			1.3		kHz
Slew Rate	Direction Measured at Output	+0.1, –0.04			V/µs
Settling Time	to 0.05%		500		µs
OUTPUT					
Noise Voltage (RTI)	f_B = 0.05Hz to 100Hz		$\sqrt{(5)^2 + (22/G_1)^2}$		µVp-p
	f_B = 10Hz to 10kHz		$\sqrt{(5)^2 + (11/G_1)^2}$		µVrms
Residual Ripple(9)			5		mVp-p
POWER SUPPLY IN, at P+, P–					
Rated Performance			15		VDC
Voltage Range(10)	Derated Performance	8.5		16	VDC
Ripple Current(9)			10	25	mAp-p
Quiescent Current(11)	Average		14	18	mA/DC
Current vs Load Current(12)	vs Current from +V, –V, V+, V–		0.7		mA/mA
ISOLATED POWER OUT, At +V, –V, V+, V– pins(13)					
Voltage, No Load	15V Between P+ and P–	8.5	9	9.5	V
Voltage, Full Load	±15mA (10mA sum) Load(12)	7	8	9	V
Voltage vs Power Supply	vs Supply Between P+ and P–		0.66		V/V
Ripple Voltage(9)					
No Load			40		mVp-p
Full Load	±5mA Load		80	200	mVp-p
TEMPERATURE RANGE					
Specification 3656AG, BG		–25		+85	°C
3656HG, JG, KG		0		+70	°C
Operation(10)		–55		+100	°C
Storage(14)		–65		+125	°C

NOTES: (1) Ratings in parenthesis are between P- (pin 20) and O/P Com (pin 17). Other isolation ratings are between I/P Com and O/P Com or I/P Com and P–. (2) See Performance Curves. (3) May be trimmed to zero. (4) If output swing is unipolar, or if the output is not loaded, specification same as if external supply were used. (5) Includes effects of A_1 and A_2 offset voltages and bias currents if recommended resistors used. (6) Versus the sum of all external currents drawn from V+, V–, +V, –V (= ISO). (7) Effects of A_1 and A_2 bias currents and offset currents are included in Offset Voltage specifications. (8) With respect to I/P Com (pin 3) for A_1 and with respect to O/P Com (pin 17) for A_2. CMR for A_1 and A_2 is 100dB, typical. (9) In configuration of Figure 3. Ripple frequency approximately 750kHz. Measurement bandwidth is 30kHz. (10) Decreases linearly from 16VDC at 85°C to 12VDC at 100°C. (11) Instantaneous peak current required from pins 19 and 20 at turn-on is 100mA for slow rising voltages (50ms) and 300mA for fast rises (50µs). (12) Load current is sum drawn form +V, –V, V+, V– (= I_{ISO}). (13) Maximum voltage rating at pins 1 and 4 is ±18VDC; maximum voltage rating at pins 12 and 16 is ±18VDC. (14) Isolation ratings may degrade if exposed to 125°C for more than 1000 hours or 90°C for more than 50,000 hours.

Example of the ratings for 3-port continuous isolation.



PIN DESIGNATIONS

NO.	DESCRIPTION	NO.	DESCRIPTION
1	+V	11	Output DEMOD
2	MOD Input	12	V–
3	Input DEMOD COM	13	A_2 Noninverting Input
4	–V	14	A_2 Inverting Input
5	Balance	15	A_2 Output
6	A_1 Inverting Input	16	V+
7	A_1 Noninverting Input	17	Output DEMOD COM
8	Balance	18	No Pin
9	A_1 Output	19	P+
10	Input DEMOD	20	P–

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
3656	20-Lead ISO Omni	102A

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

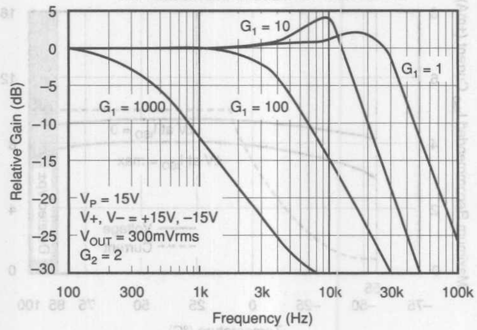
Supply Without Damage 16V
Input Voltage Range Using Internal Supply .... ±8V
Input Voltage Range Using External Supply .... Supply
Continuous Isolation Voltage(1) .... 3500, (1000) VDC
Storage Temperature .... –65°C to +125°C
Lead Temperature, (soldering, 10s) .... +300°C

NOTE: (1) Ratings in parenthesis are between P– (pin 20) and O/P Com (pin 17). Other isolation ratings are between I/P Com and O/P Com or I/P Com and P–.

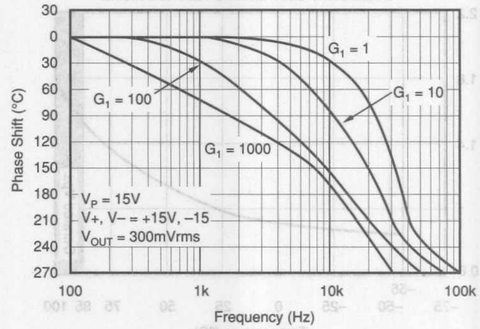
TYPICAL PERFORMANCE CURVES

All specifications typical at +25°C, unless otherwise specified.

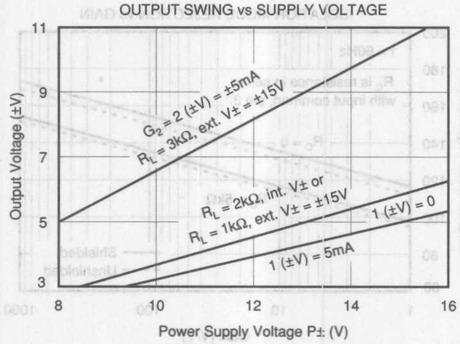
SMALL SIGNAL FREQUENCY RESPONSE



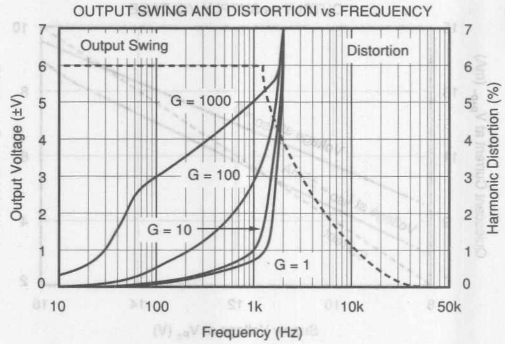
PHASE RESPONSE



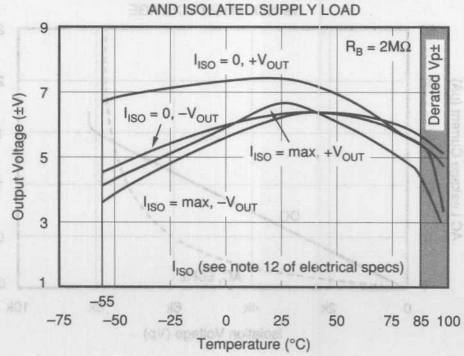
OUTPUT SWING vs SUPPLY VOLTAGE



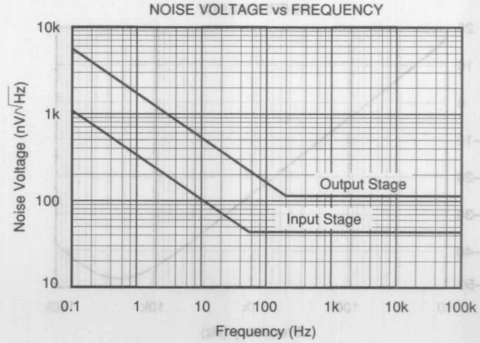
OUTPUT SWING AND DISTORTION vs FREQUENCY



OUTPUT VOLTAGE SWING vs TEMPERATURE
AND ISOLATED SUPPLY LOAD



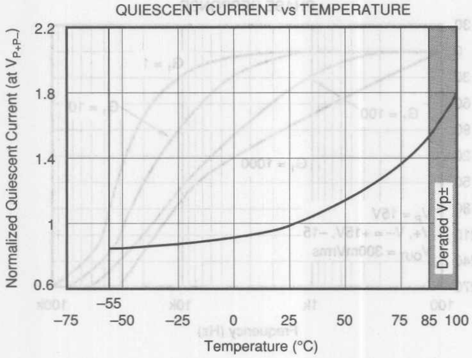
NOISE VOLTAGE vs FREQUENCY



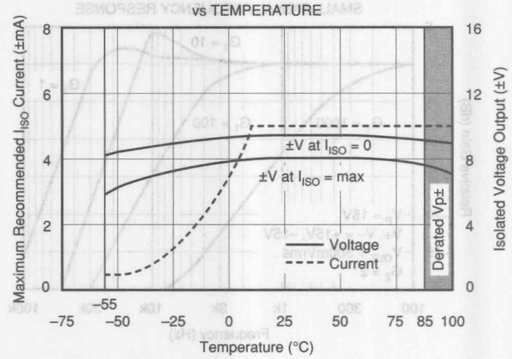
TYPICAL PERFORMANCE CURVES (CONT)

All specifications typical at +25°C, unless otherwise specified.

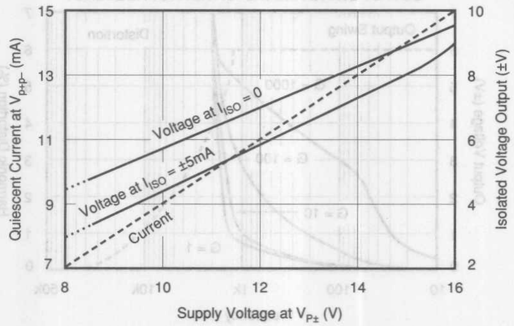
QUIESCENT CURRENT vs TEMPERATURE



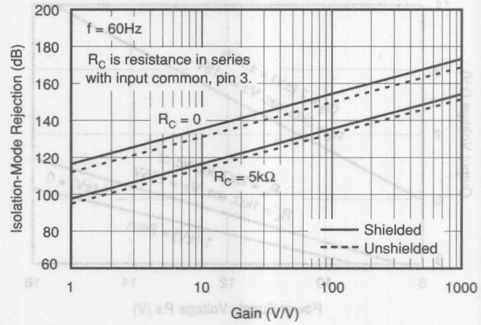
ISOLATED OUTPUT VOLTAGE AND CURRENT vs TEMPERATURE



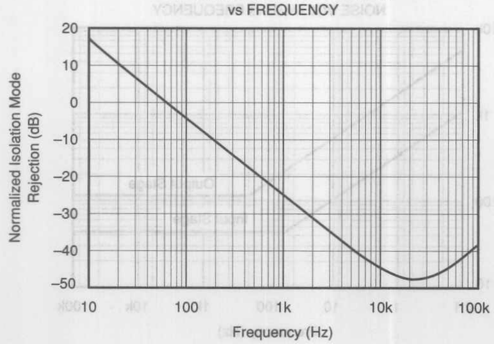
QUIESCENT CURRENT AND ISOLATED VOLTAGE OUTPUT vs SUPPLY VOLTAGE



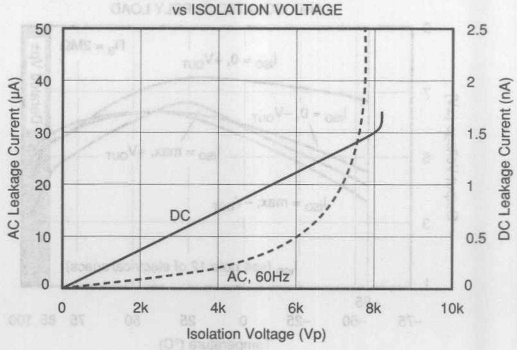
ISOLATION-MODE REJECTION vs GAIN



ISOLATION MODE REJECTION vs FREQUENCY



AC AND DC LEAKAGE CURRENT vs ISOLATION VOLTAGE



BURR-BROWN®

THEORY OF OPERATION

Details of the 3656 are shown in Figure 1. The external connections shown, place it in its simplest gain configuration —unity gain, noninverting. Several other amplifier gain configurations and power isolation configurations are possible. See Installation and Operating Instructions and Applications sections for details.

Isolation of both signal and power is accomplished with a single miniature toroid transformer with multiple windings. A pulse generator operating at approximately 750kHz provides a two-part voltage waveform to transformer, T_1. One part of the waveform is rectified by diodes D_1 through D_4 to provide the isolated power to the input and output stages (+V, –V and V+, V–). The other part of the waveform is modulated with input signal information by the modulator operating into the V_2 winding of the transformer.

The modulated signal is coupled by windings W_6 and W_7 to two matched demodulators—one in the input stage and one in the output stage—which generate identical voltages at their outputs, pins 10 and 11 (Voltages identical with respect to their respective commons, pins 3 and 17). In the input stage the input amplifier, A_1, the modulator and the input demodulator are connected in a negative feedback loop. This forces the voltage at pin 6 (connect as shown in Figure 1) to equal the input signal voltage applied at pin 7. Since the input and the output demodulators are matched and produce identical output voltages, the voltage at pin 11 (referenced to pin 17, the output common) is equal to the voltage at pin 10 (referenced to pin 3, the input common). In the output stage, output amplifier A_2 is connected as a unity gain buffer, thus the output voltage at pin 15 equals the output demodulator voltage at pin 11. The end result is an isolated output voltage at pin 15 equal to the input voltage at pin 7 with no galvanic connection between them.

Several amplifier and power connection variations are possible:

1. The input stage may be connected in various operational amplifier gain configurations.
2. The output stage may be operated at gains above unity.
3. The internally generated isolated voltages which provide power to A_1 and A_2 may be overridden and external supply voltages used instead.

Versatility and its three independent isolated grounds allow simple solutions to demanding analog signal conditioning problems. See the Installation and Operating Instructions and Applications sections for details.

INSTALLATION AND OPERATING INSTRUCTIONS

The 3656 is a very versatile device capable of being used in a variety of isolation and amplification configurations. There are several fundamental considerations that determine configuration and component value constraints:

1. Consideration must be given to the load placed on the resistance (pin 10 and pin 11) by external circuitry. Their output resistance is 100kΩ and a load resistor of 2MΩ or greater is recommended to prevent a voltage divider loading effect in excess of 5%.

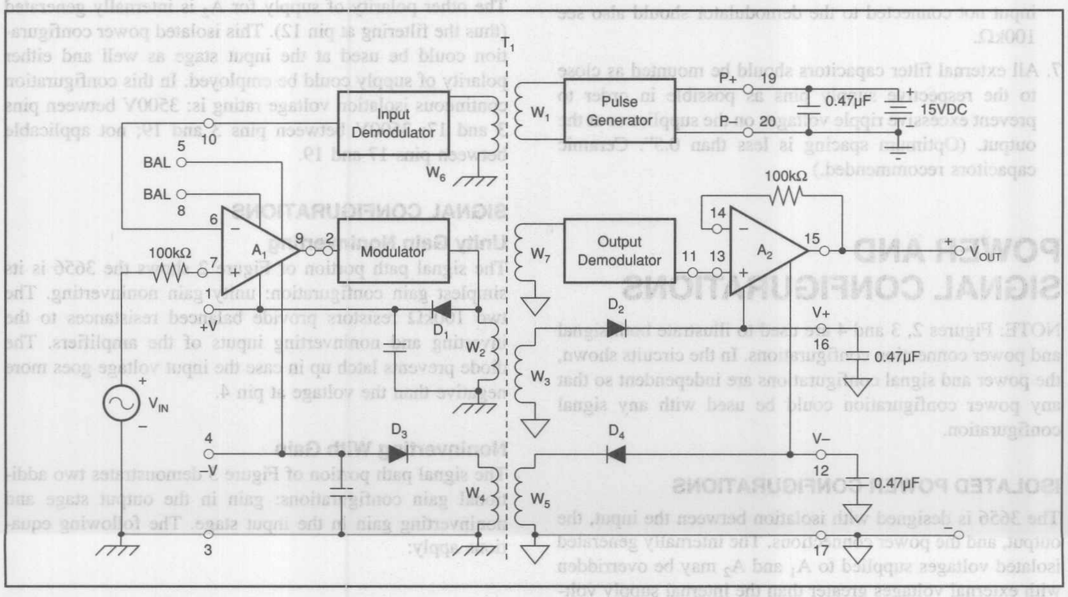


FIGURE 1. Block Diagram.

2. Demodulator loadings should be closely matched so their output voltages will be equal. (Unequal demodulator output voltages will produce a gain error.) At the 2MΩ level, a matching error of 5% will cause an additional gain error of 0.25%.
3. Voltage swings at demodulator outputs should be limited to 5V. The output may be distorted if this limit is exceeded. This constrains the maximum allowed gains of the input and output stages. Note that the voltage swings at demodulator outputs are tested with 2MΩ load for a minimum of 5V.
4. Total current drawn from the internal isolated supplies must be limited to less than ±5mA per supply and limited to a total of 10mA. In other words, the combination of external and internal current drawn from the internal circuitry which feeds the +V, –V, V+ and V– pins should be limited to 5mA per supply (total current to +V, –V, V+ and V– limited to 10mA). The internal filter capacitors for ±V are 0.01µF. If more than 0.1mA is drawn to provide isolated power for external circuitry (see Figure 12), additional capacitors are required to provide adequate filtering. A minimum of 0.1µF/mA is recommended.
5. The input voltage at pin 7 (noninverting input to A_1) must not exceed the voltage at pin 4 (negative supply voltage for A_1) in order to prevent a possible lockup condition. A low leakage diode connected between pins 7 and 4, as shown in Figure 2, can be used to limit this input voltage swing.
6. Impedances seen by each amplifier's + and – input terminals should be matched to minimize offset voltages caused by amplifier input bias currents. Since the demodulators have a 100kΩ output resistance, the amplifier input not connected to the demodulator should also see 100kΩ.
7. All external filter capacitors should be mounted as close to the respective supply pins as possible in order to prevent excessive ripple voltages on the supplies or at the output. (Optimum spacing is less than 0.5". Ceramic capacitors recommended.)

POWER AND SIGNAL CONFIGURATIONS

NOTE: Figures 2, 3 and 4 are used to illustrate both signal and power connection configurations. In the circuits shown, the power and signal configurations are independent so that any power configuration could be used with any signal configuration.

ISOLATED POWER CONFIGURATIONS

The 3656 is designed with isolation between the input, the output, and the power connections. The internally generated isolated voltages supplied to A_1 and A_2 may be overridden with external voltages greater than the internal supply voltages. These two features of 3656 provide a great deal of versatility in possible isolation and power supply hook-ups. When external supplies are applied, the rectifying diodes (D_1 through D_4) are reverse biased and the internal voltage sources are decoupled from the amplifiers (see Figure 1). Note that when external supplies are used, they must never be lower than the internal supply voltage.

Three-Port

The power supply connections in Figure 2 show the full three-port isolation configuration. The system has three separate grounds with no galvanic connections between them. The two external 0.47µF capacitors at pins 12 and 16 filter the rectified isolated voltage at the output stage. Filtering on the input stage is provided by internal capacitors. In this configuration continuous isolation voltage ratings are: 3500V between pins 3 and 17; 3500V between pins 3 and 19; 1000V between pins 17 and 19.

Two-Port Bipolar Supply

Figure 3 shows two-port isolation which uses an external bipolar supply with its common connected to the output stage ground (pin 17). One of the supplies (either + or – could be used) provides power to the pulse generator (pins 19 and 20). The same sort of configuration is possible with the external supplies connected to the input stage. With the connection shown, filtering at pins 12 and 16 is not required. In this configuration continuous isolation voltage rating is: 3500VDC between pins 3 and 17; not applicable between pins 17 and 19; 3500VDC between pins 3 and 19.

Two-Port Single Supply

Figure 4 demonstrates two-port isolation using a single polarity supply connected to the output common (pin 17). The other polarity of supply for A_2 is internally generated (thus the filtering at pin 12). This isolated power configuration could be used at the input stage as well and either polarity of supply could be employed. In this configuration continuous isolation voltage rating is: 3500V between pins 3 and 17; 3500V between pins 3 and 19; not applicable between pins 17 and 19.

SIGNAL CONFIGURATIONS

Unity Gain Noninverting

The signal path portion of Figure 2 shows the 3656 is its simplest gain configuration: unity gain noninverting. The two 100kΩ resistors provide balanced resistances to the inverting and noninverting inputs of the amplifiers. The diode prevents latch up in case the input voltage goes more negative than the voltage at pin 4.

Noninverting With Gain

The signal path portion of Figure 3 demonstrates two additional gain configurations: gain in the output stage and noninverting gain in the input stage. The following equations apply:

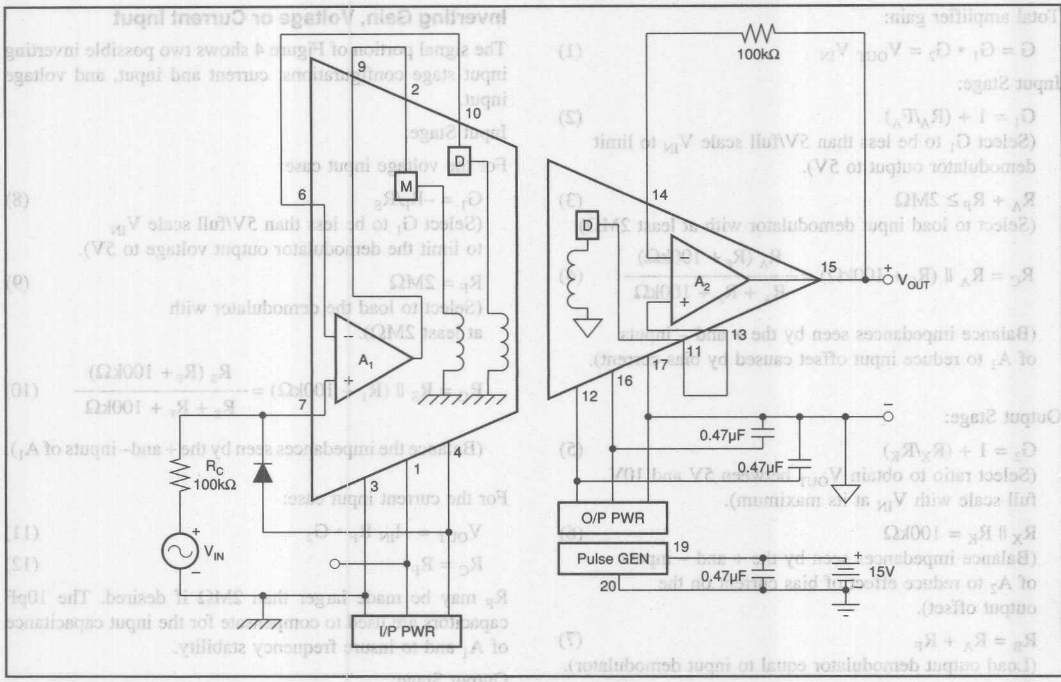


FIGURE 2. Power: Three-Port Isolation; Signal: Unity-Gain Noninverting.

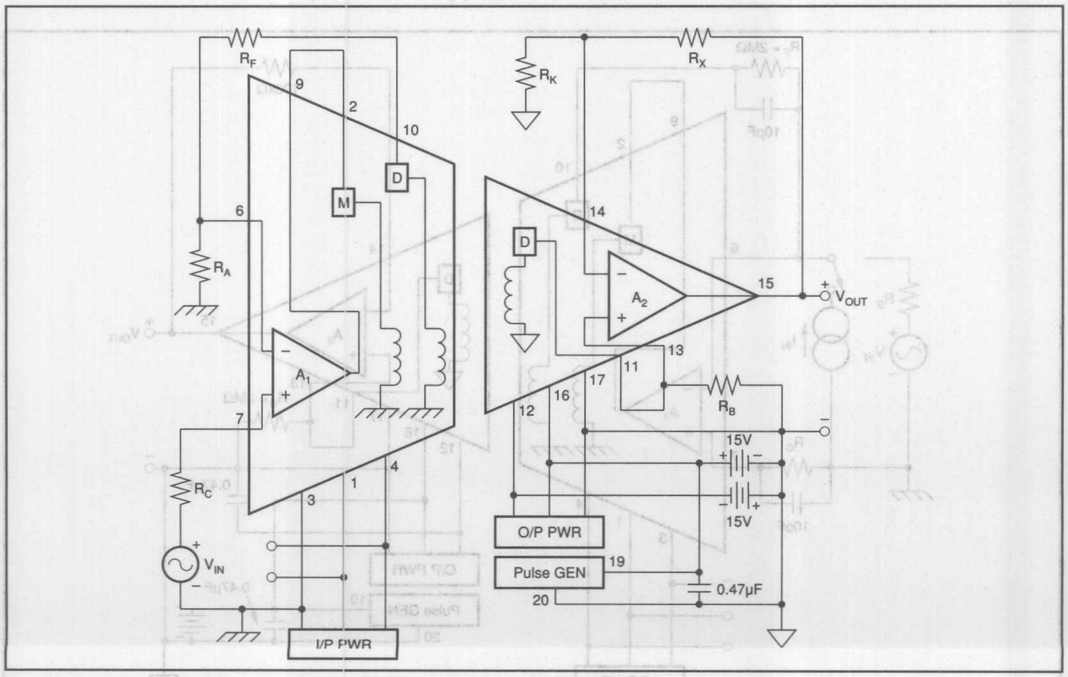


FIGURE 3. Power: Two-Port, Dual Supply; Signal: Noninverting Gain.

Total amplifier gain:

$$G = G_1 \bullet G_2 = V_{OUT}\ V_{IN} \quad (1)$$

Input Stage:

$$G_1 = 1 + (R_A/F_A) \quad (2)$$

(Select G_1 to be less than 5V/full scale V_{IN} to limit demodulator output to 5V).

$$R_A + R_F \geq 2M\Omega \quad (3)$$

(Select to load input demodulator with at least 2MΩ).

$$R_C = R_A \parallel (R_F + 100k\Omega) = \frac{R_A\,(R_F + 100k\Omega)}{R_A + R_F + 100k\Omega} \quad (4)$$

(Balance impedances seen by the + and – inputs of A_1 to reduce input offset caused by bias current).

Output Stage:

$$G_2 = 1 + (R_X/R_K) \quad (5)$$

(Select ratio to obtain V_{OUT} between 5V and 10V full scale with V_{IN} at its maximum).

$$R_X \parallel R_K = 100k\Omega \quad (6)$$

(Balance impedances seen by the + and – inputs of A_2 to reduce effect of bias current on the output offset).

$$R_B = R_A + R_F \quad (7)$$

(Load output demodulator equal to input demodulator).

Inverting Gain, Voltage or Current Input

The signal portion of Figure 4 shows two possible inverting input stage configurations: current and input, and voltage input.

Input Stage:

For the voltage input case:

$$G_1 = -R_F/R_S \quad (8)$$

(Select G_1 to be less than 5V/full scale V_{IN} to limit the demodulator output voltage to 5V).

$$R_F = 2M\Omega \quad (9)$$

(Select to load the demodulator with at least 2MΩ).

$$R_C = R_S \parallel (R_1 + 100k\Omega) = \frac{R_S\,(R_F + 100k\Omega)}{R_S + R_F + 100k\Omega} \quad (10)$$

(Balance the impedances seen by the + and– inputs of A_1).

For the current input case:

$$V_{OUT} = -I_{IN}\,R_F \bullet G_2 \quad (11)$$

$$R_C = R_F \quad (12)$$

R_F may be made larger than 2MΩ if desired. The 10pF capacitors are used to compensate for the input capacitance of A_1 and to insure frequency stability.

Output Stage:

The output stage is the same as shown in equations (5), (6), and (7).

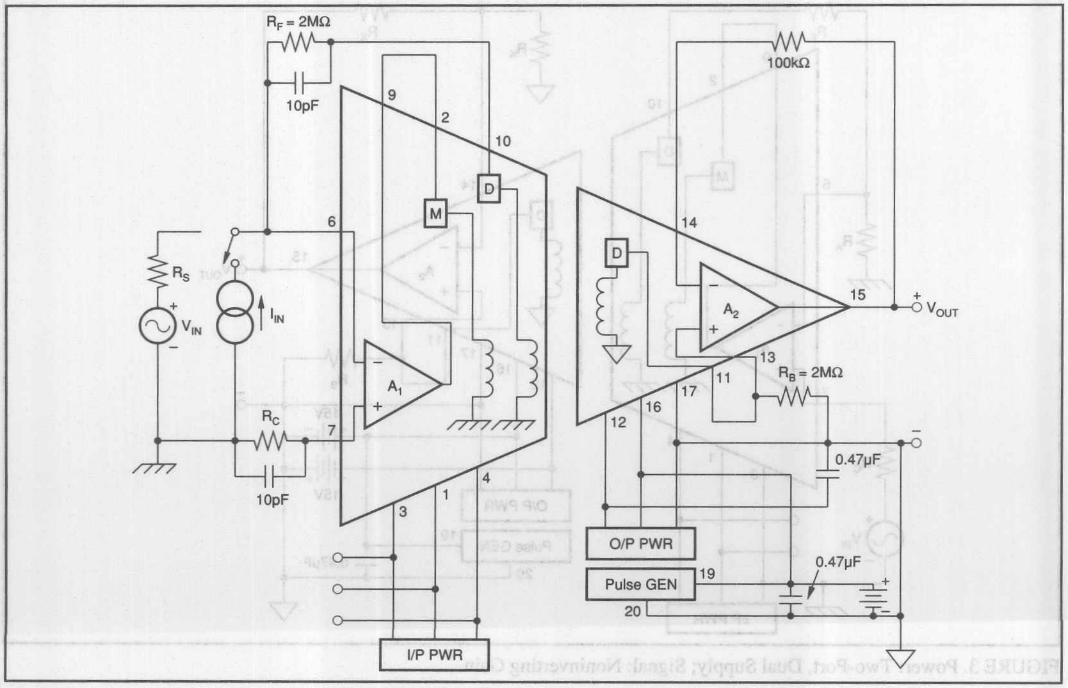


FIGURE 4. Power: Two-Port, Single Supply; Signal: Inverting Gains.

Illustrative Calculations:

The maximum input voltage is 100mV. It is desired to amplify the input signal for maximum accuracy. Noninverting output is desired.

Input Stage:

Step 1

G_1 max = 5V/max Input Signal = 5V 0.1V = 50V/V

With the above gain of 50V/V, if the input ever exceeds 100mV, it would drive the output to saturation. Therefore, it is good practice to allow reasonable input overrange.

So, to allow for 25% input overrange without saturation at the output, select:

$G_1 = 40V/V$

$G_1 = 1 + (R_F + R_A) = 40$

$\therefore\ R_F + R_A = 39$ (13)

Step 2

$R_A + R_F$ forms a voltage divider with the 100kΩ output resistance of the demodulator. To limit the voltage divider loading effect to no more than 5%, $R_A + R_F$ should be chosen to be at least 2MΩ. For most applications, the 2MΩ should be sufficiently large for $R_A + R_F$. Resistances greater than 2MΩ may help decrease the loading effect, but would increase the offset voltage drift.

The voltage divider with $R_A + R_F$ = 2MΩ is 2MΩ/(2MΩ + 100kΩ) = 2/(2 + 0.1) = 95.2%, i.e., the percent loading is 4.8%.

Choose $R_A + R_F = 2M\Omega$ (14)

Step 3

Solving equations (13) and (14)

$R_A = 50k\Omega$ and $R_F = 1.95M\Omega$

Step 4

The resistances seen by the + and – input terminals of the input amplifier A_1 should be closely matched in order to minimize offset voltage due to bias currents.

$\therefore R_C = R_A \parallel (R_F + 100k\Omega)$

$= 50k\Omega \parallel (1.95M\Omega + 100k\Omega)$

$\approx 49k\Omega$

Output Stage:

Step 5

$V_{OUT} = V_{IN\,MAX} \bullet G_1 \bullet G_2$

As discussed in Step 1, it is good practice to provide 25% input overrange.

So we will calculate G_2 for 10V output and 125% of the maximum input voltage.

$\therefore V_{OUT} = (1.25 \bullet 0.1)(G_1)(G_2)$

i.e., $10V = 0.125 \bullet 40 \bullet G_2$

$\therefore G_2 = 10V/5V = 2V/V$

Step 6

$G_2 = 1 + (R_X/R_K) = 2.0$

$\therefore R_X/R_K = 1.0$

$\therefore R_X = R_K$ (15)

Step 7

The resistance seen by the + input terminal of the output stage amplifier A_2 (pin 13) is the output resistance 100kΩ of the output demodulator. The resistance seen by the (–) input terminal of A_2 (pin 14) should be matched to the resistance seen by the + input terminal.

The resistance seen by pin 14 is the parallel combination of R_X and R_K.

$\therefore R_X \parallel R_K = 100k\Omega$

$(R_X \bullet R_K/(R_X + R_K) = 100k\Omega$

$R_K/[1 + (R_K/R_X)] = 100k\Omega$ (16)

Step 8

Solving equations (15) and (16) $R_K = 20k\Omega$ and $R_X = 200k\Omega$.

Step 9

The output demodulator must be loaded equal to the input demodulator.

$\therefore R_B = R_A + R_F = 2M\Omega$

(See equation (14) above in Step 2).

Use the resistor values obtained in Steps 3, 4, 8 and 9, and connect the 3656 as shown in Figure 3.

OFFSET TRIMMING

Figure 5 shows an optional offset voltage trim circuit. It is important that $R_A + R_F = R_B$.

CASE 1: Input and output stages in low gain, use output potentiometer (R_2) only. Input potentiometer (R_1) may be disconnected. For example, unity gain could be obtained by setting $R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_F = 0$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 2: Input stage in high gain and output stage in low gain, use input potentiometer (R_1) only. Output potentiometer (R_2) may be disconnected. For example, $G_T = 100$ could be obtained by setting $R_F = 2M\Omega$, $R_B = 2M\Omega$ returned to pin 17, $R_A = 20k\Omega$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 3: When it is necessary to perform a two-stage precision trim (to maintain a very small offset change under conditions of changing temperature and changing gain in A_1 and A_2), use step 1 to adjust the input stage and step 2 for the output stage. Carbon composition resistors are acceptable, but potentiometers should be stable.

Step 1: Input stage trim ($R_A = R_C = 20k\Omega$, $R_I = R_B = 20M\Omega$. $R_X = 100k\Omega$, $R_K = \infty$, R_2 disconnected); A_1 high, A_2 low gain. Adjust R_1 for 0V ±5mV or desired setting at V_{OUT}, pin 15.

3656

5

ISOLATION PRODUCTS

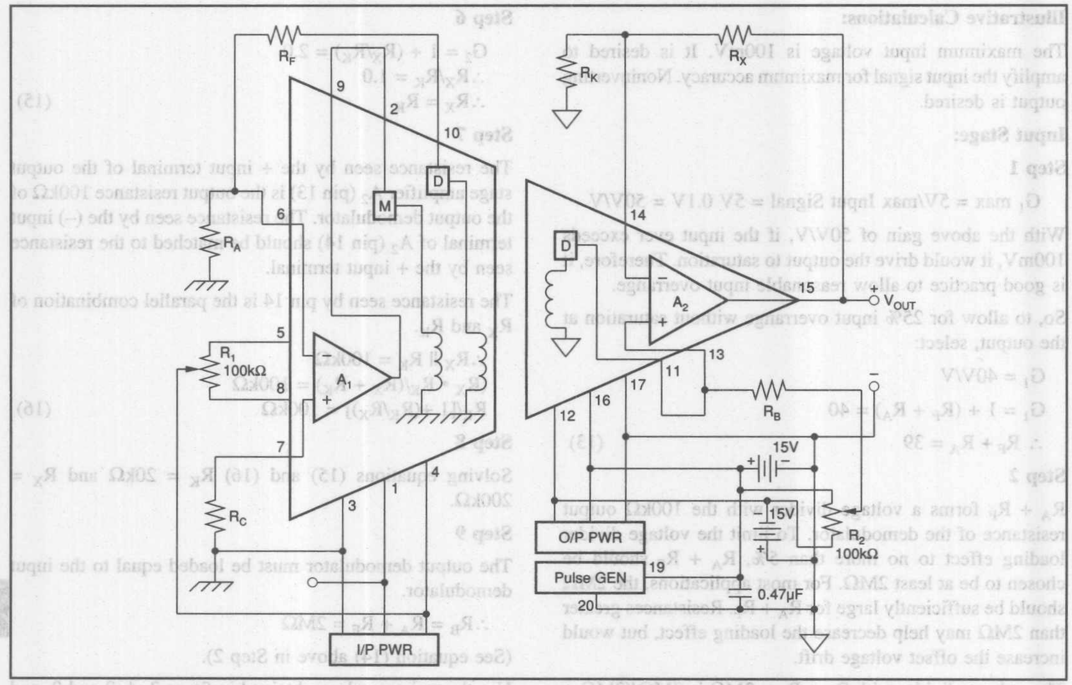


FIGURE 5. Optional Offset Voltage Trim.

Step 2: Output stage trim ($R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_F = 0$, $R_X = 100k\Omega$, $R_K = \infty$, R_1 and R_2 connected); A_1 low, A_2 low gain. Adjust R_2 for 0V ±1mV or desired setting at V_{OUT}, pin 15 (±110mV approximate total range).

NOTE: Other circuit component values can be used with valid results.

APPLICATIONS

ECG AMPLIFIER

Although the features of the circuit shown in Figure 6 are important in patient monitoring applications, they may also be useful in other applications. The input circuitry uses an external, low quiescent current op amp (OPA177 type) powered by the isolated power of the input stage to form a high impedance instrumentation amplifier input (true three-wire input). R_3 and R_4 give the input stage amplifier of the 3656 a noninverting gain of 10 and an inverting gain of –9. R_1 and R_2 give the external amplifier a noninverting gain of 1 + 1/9. The inputs are applied to the noninverting inputs of the two amplifiers and the composite input stage amplifier has a gain of 10.

The 330kΩ, 1W, carbon resistors and diodes D_1 - D_4 provide protection for the input amplifiers from defibrillation pulses.

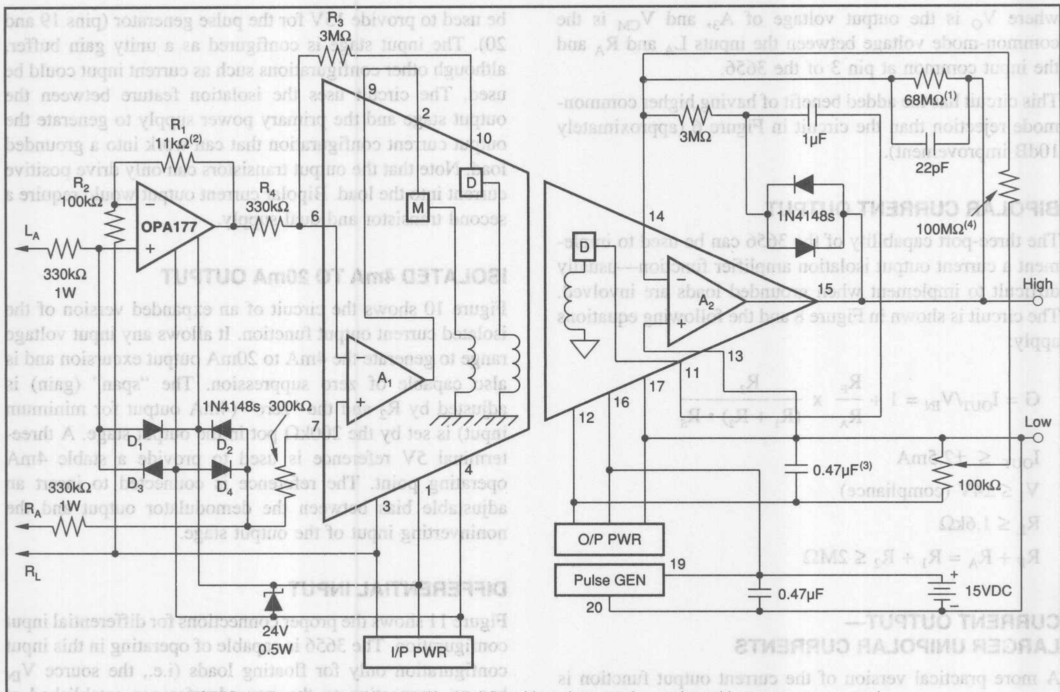
The output stage in Figure 6 is configured to provide a bandpass filter with a gain of 22.7 (68MΩ/3MΩ). The high-pass section (0.05Hz cutoff) is formed by the 1µF capacitor and 3MΩ resistor which are connected in series between the output demodulator and the inverting input of the output stage amplifier. The low-pass section (100Hz cutoff) is formed by the 68MΩ resistor and 22pF capacitor located in the feedback loop of the output stage. The diodes provide for quick recovery of the high-pass filter to overvoltages at the input. The 100kΩ pot and the 100MΩ resistor allow the output voltage to be trimmed to compensate for increased offset voltage caused by unbalanced impedances seen by the inputs of the output stage amplifier.

In many modern electrocardiographic systems, the patient is not grounded. Instead, the right-leg electrode is connected to the output of an auxiliary operational amplifier as shown in Figure 7. In this circuit, the common-mode voltage on the body is sensed by the two averaging resistors, R_1 and R_2, inverted, amplified, and fed back to the right-leg through resistor R_4. This negative feedback drives the common-mode voltage to a low value. The body's displacement current i_d does not flow to ground, but rather to the output circuit of A_3. This reduces the pickup as far as the ECG amplifier is concerned and effectively grounds the patient.

The value of R_4 should be as large as practical to isolate the patient from ground. The resistors R_3 and R_4 may be selected by these equations:

$R_3 = (R_1/2)(V_O/V_{CM})$ and $R_4 = (V_{CM} - V_O)/i_d$

$(-10V \leq V_O \leq +10V$ and $-10V \leq V_{CM} \leq +10V)$



NOTES: (1) Bandpass 0.05Hz to 100Hz. (2) Adjustable resistor may be used to achieve max common-mode rejection between L_A /R_A and RL.(3) Negative 15V supply may be connected in place of 0.47μF capacitor if available. (4) See offset trimming section.

FIGURE 6. ECG Amplifier.

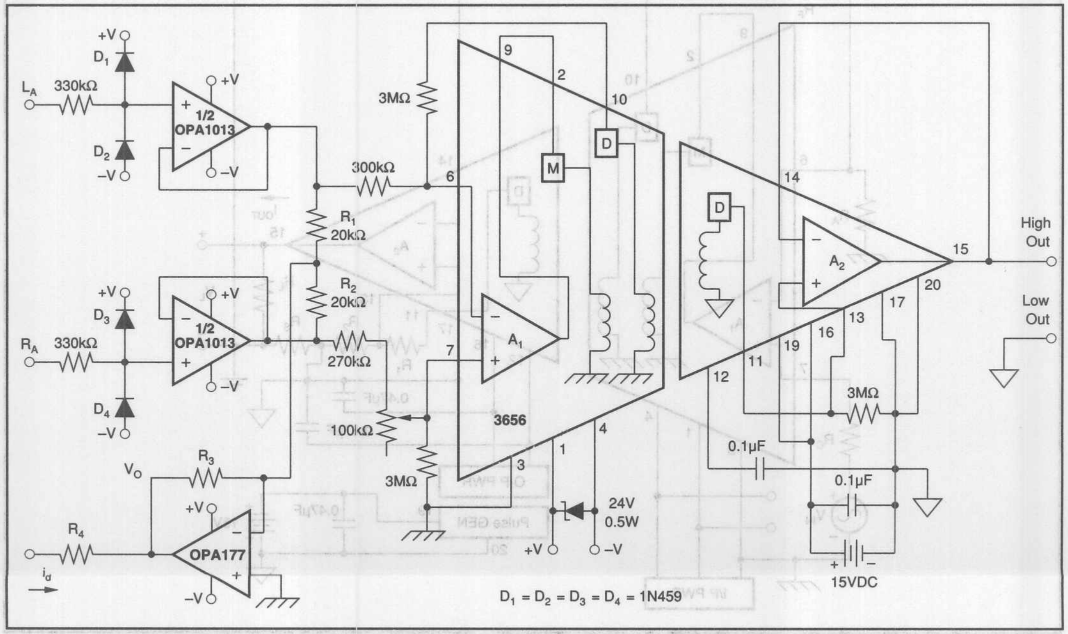


FIGURE 7. Driven Right-Leg Amplifier.

3656

5

ISOLATION PRODUCTS

where V_O is the output voltage of A_3, and V_{CM} is the common-mode voltage between the inputs L_A and R_A and the input common at pin 3 of the 3656.

This circuit has the added benefit of having higher common-mode rejection than the circuit in Figure 6 (approximately 10dB improvement).

BIPOLAR CURRENT OUTPUT

The three-port capability of the 3656 can be used to implement a current output isolation amplifier function—usually difficult to implement when grounded loads are involved. The circuit is shown in Figure 8 and the following equations apply:

$$G = I_{OUT}/V_{IN} = 1 + \frac{R_F}{R_A} \times \frac{R_2}{(R_1 + R_2) \cdot R_S}$$

$I_{OUT} \leq \pm 2.5\text{mA}$

$V_1 \leq \pm 4\text{V}$ (compliance)

$R_L \leq 1.6\text{k}\Omega$

$R_F + R_A = R_1 + R_2 \leq 2\text{M}\Omega$

CURRENT OUTPUT—LARGER UNIPOLAR CURRENTS

A more practical version of the current output function is shown in Figure 9. If the circuit is powered from a source greater than 15V as shown, a three-terminal regulator should be used to provide 15V for the pulse generator (pins 19 and 20). The input stage is configured as a unity gain buffer, although other configurations such as current input could be used. The circuit uses the isolation feature between the output stage and the primary power supply to generate the output current configuration that can work into a grounded load. Note that the output transistors can only drive positive current into the load. Bipolar current output would require a second transistor and dual supply.

ISOLATED 4mA TO 20mA OUTPUT

Figure 10 shows the circuit of an expanded version of the isolated current output function. It allows any input voltage range to generate the 4mA to 20mA output excursion and is also capable of zero suppression. The "span" (gain) is adjusted by R_2 and the "zero" (4mA output for minimum input) is set by the 200kΩ pot in the output stage. A three-terminal 5V reference is used to provide a stable 4mA operating point. The reference is connected to insert an adjustable bias between the demodulator output and the noninverting input of the output stage.

DIFFERENTIAL INPUT

Figure 11 shows the proper connections for differential input configuration. The 3656 is capable of operating in this input configuration only for floating loads (i.e., the source V_{IN} has no connection to the ground reference established at pin 3). For this configuration the usual 2MΩ resistor used in

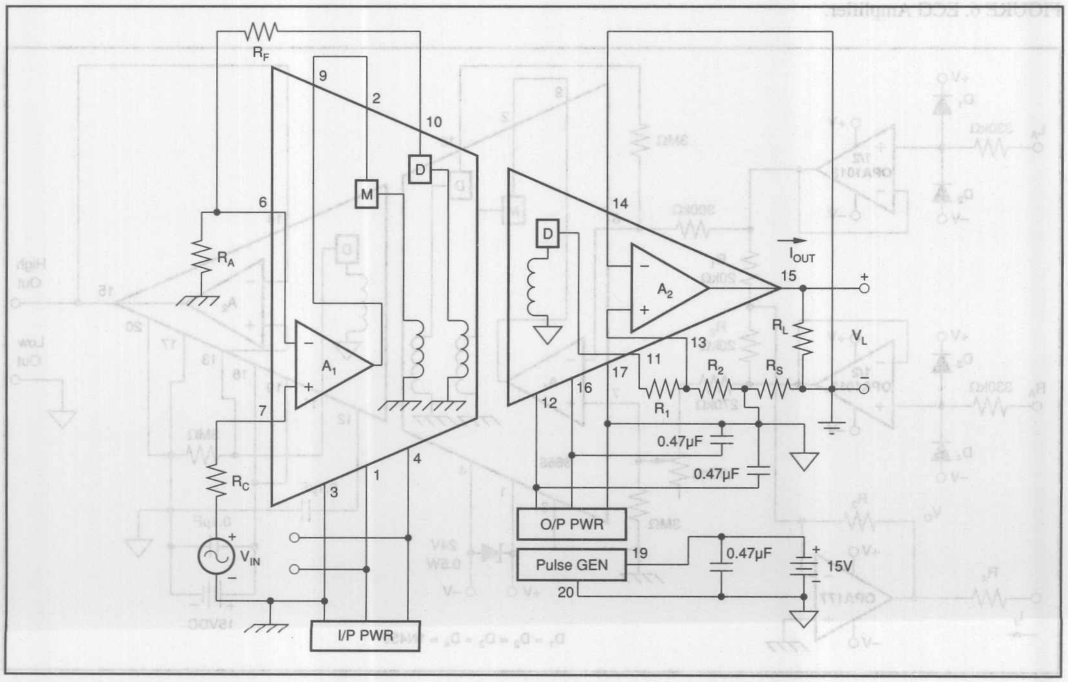


FIGURE 8. Bipolar Current Output.

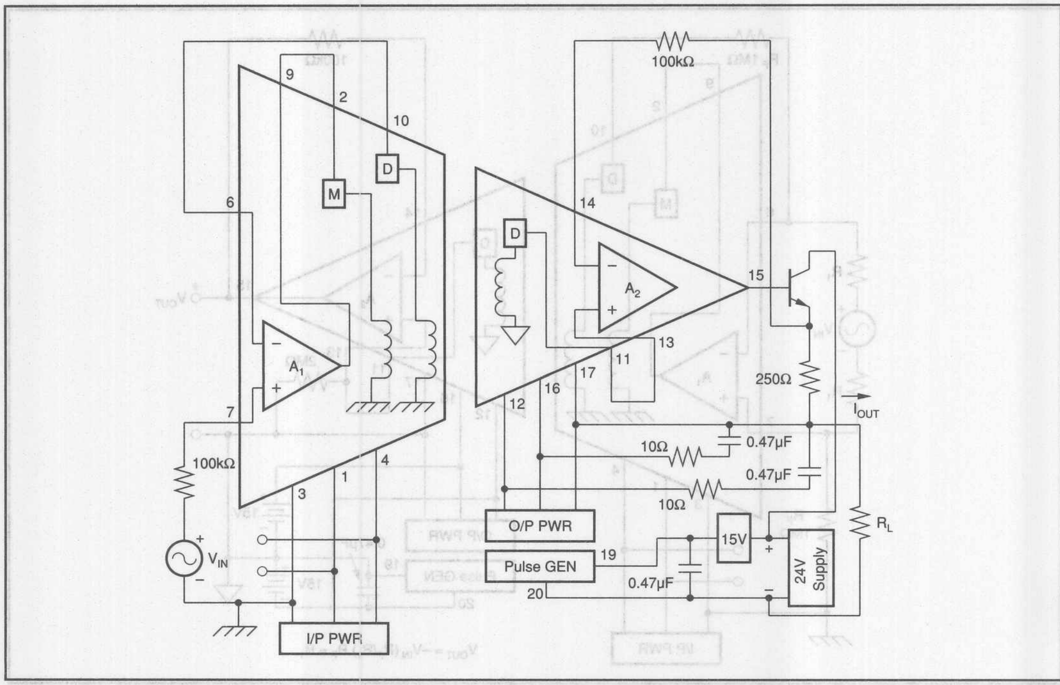


FIGURE 9. Isolated 1 to $5V_{IN}$/ 4mA to 20mA I_{OUT}.

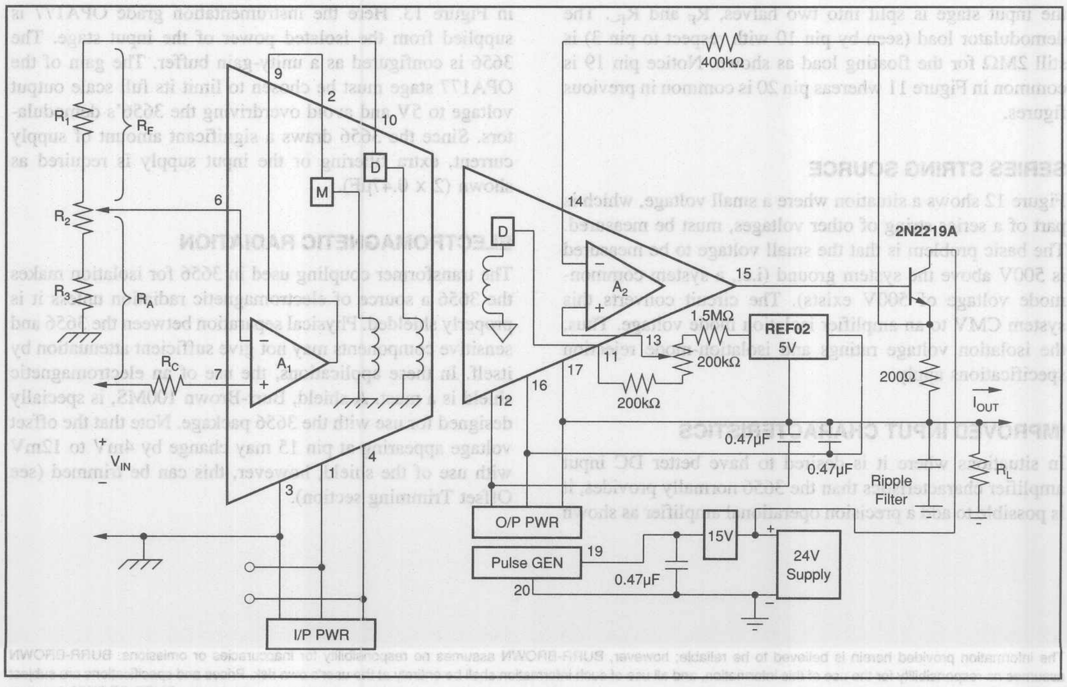


FIGURE 10. Isolated 4mA to 20mA I_{OUT}.

3656

5

ISOLATION PRODUCTS

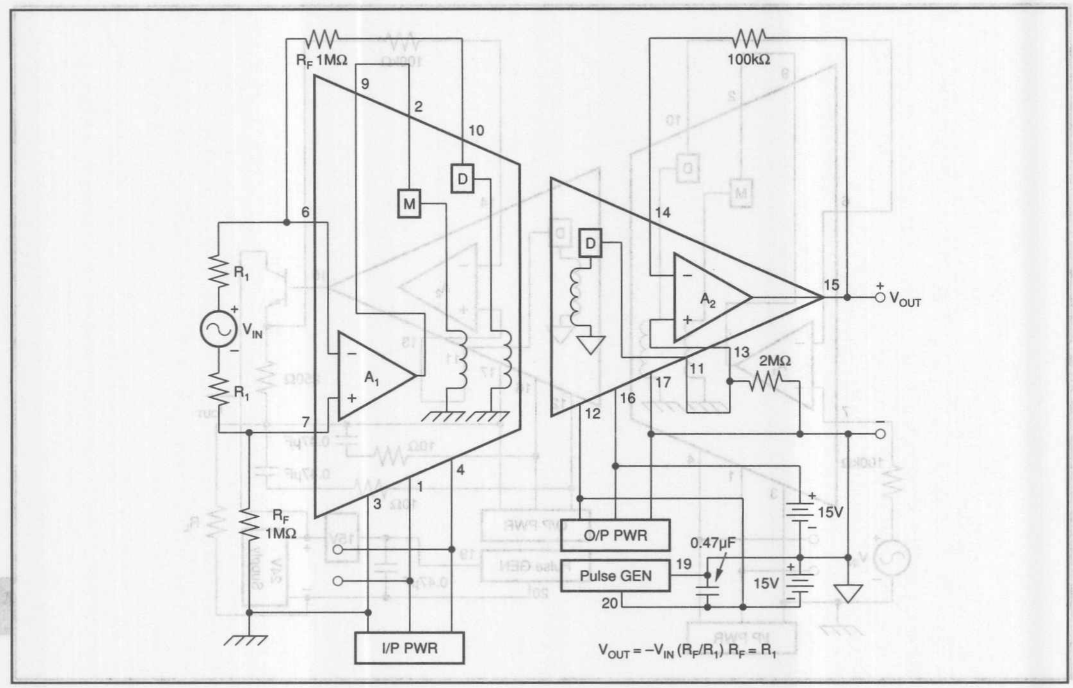


FIGURE 11. Differential Input, Floating Source.

the input stage is split into two halves, R_F and R_{F-}. The demodulator load (seen by pin 10 with respect to pin 3) is still 2MΩ for the floating load as shown. Notice pin 19 is common in Figure 11 whereas pin 20 is common in previous figures.

SERIES STRING SOURCE

Figure 12 shows a situation where a small voltage, which is part of a series string of other voltages, must be measured. The basic problem is that the small voltage to be measured is 500V above the system ground (i.e., a system common-mode voltage of 500V exists). The circuit converts this system CMV to an amplifier isolation mode voltage. Thus, the isolation voltage ratings and isolation-mode rejection specifications apply.

IMPROVED INPUT CHARACTERISTICS

In situations where it is desired to have better DC input amplifier characteristics than the 3656 normally provides, it is possible to add a precision operational amplifier as shown in Figure 13. Here the instrumentation grade OPA177 is supplied from the isolated power of the input stage. The 3656 is configured as a unity-gain buffer. The gain of the OPA177 stage must be chosen to limit its full scale output voltage to 5V and avoid overdriving the 3656's demodulators. Since the 3656 draws a significant amount of supply current, extra filtering or the input supply is required as shown (2 x 0.47μF).

ELECTROMAGNETIC RADIATION

The transformer coupling used in 3656 for isolation makes the 3656 a source of electromagnetic radiation unless it is properly shielded. Physical separation between the 3656 and sensitive components may not give sufficient attenuation by itself. In these applications, the use of an electromagnetic shield is a must. A shield, Burr-Brown 100MS, is specially designed for use with the 3656 package. Note that the offset voltage appearing at pin 15 may change by 4mV to 12mV with use of the shield; however, this can be trimmed (see Offset Trimming section).

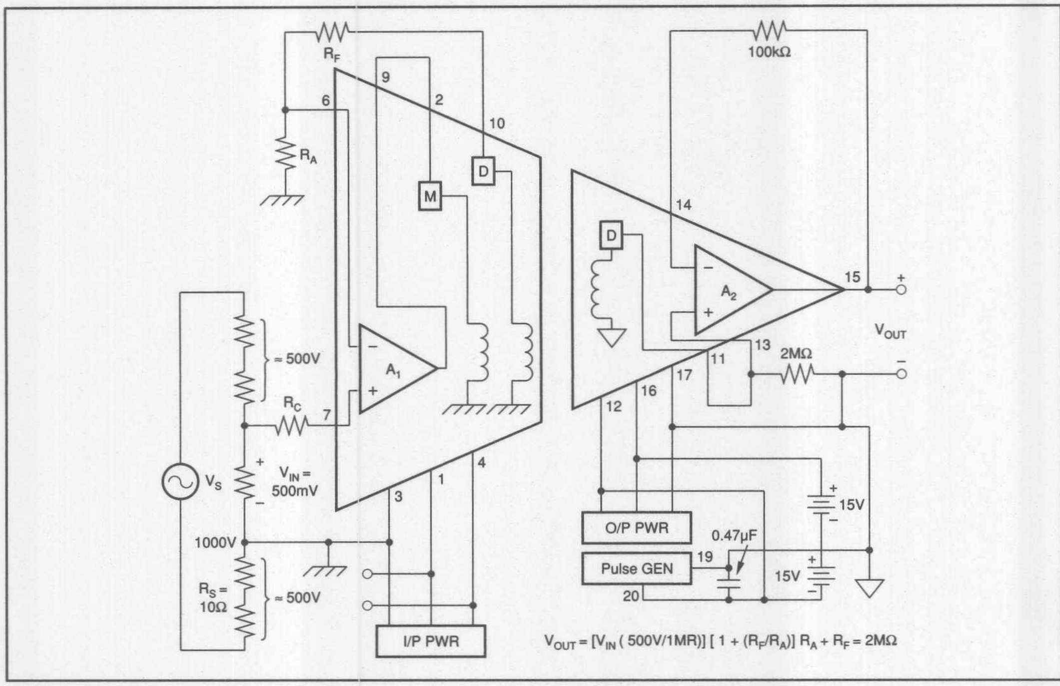


FIGURE 12. Series Source.

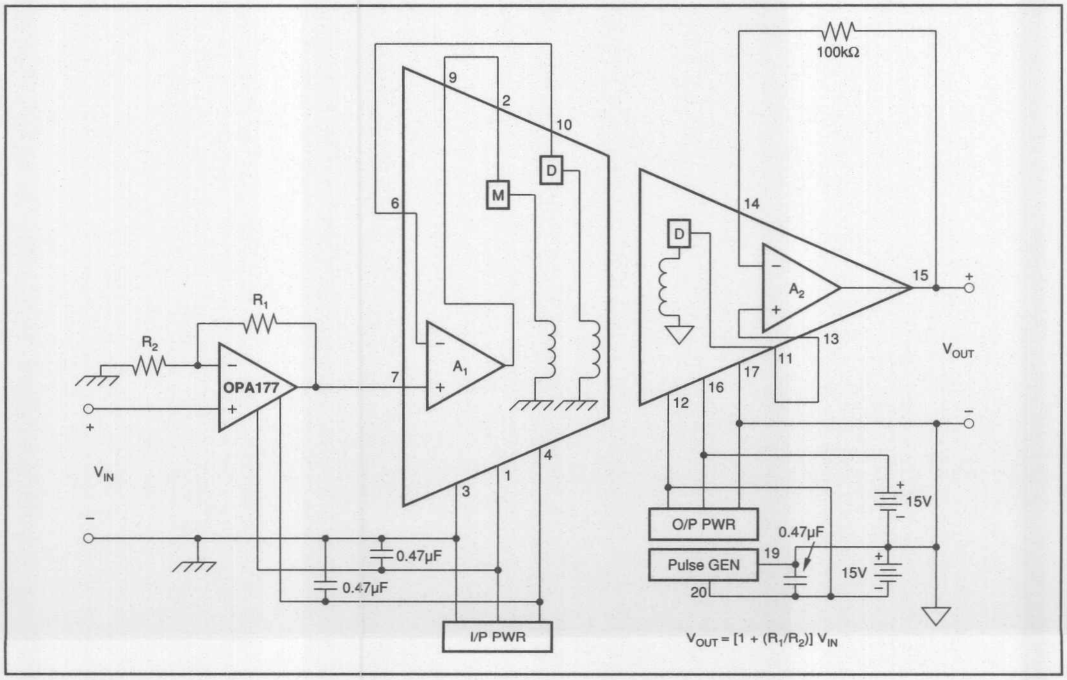


FIGURE 13. Isolator for Low-Level Signals.

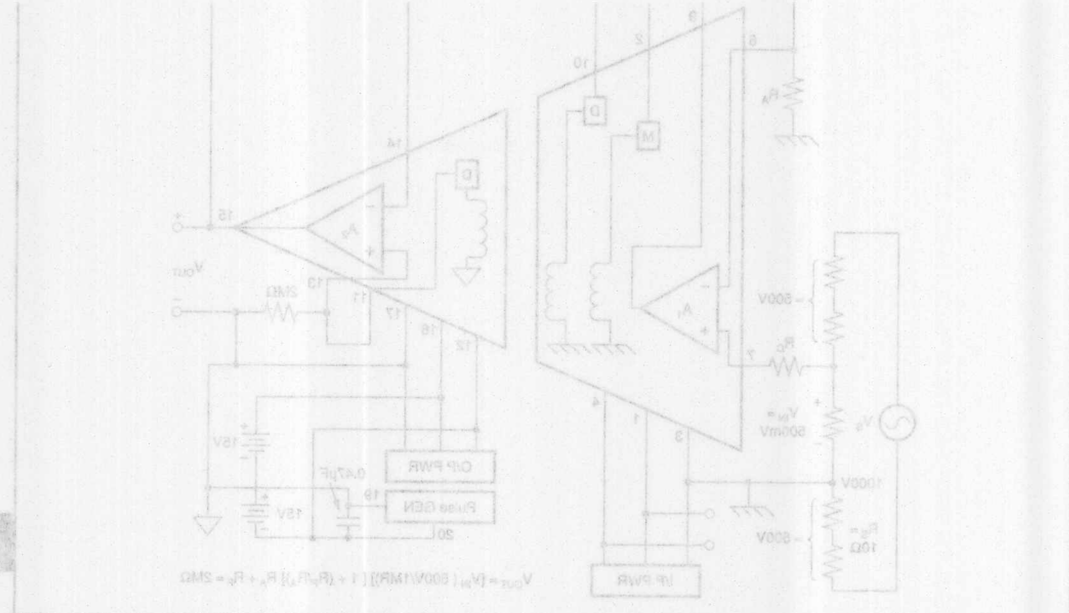


FIGURE 12. Series Source.

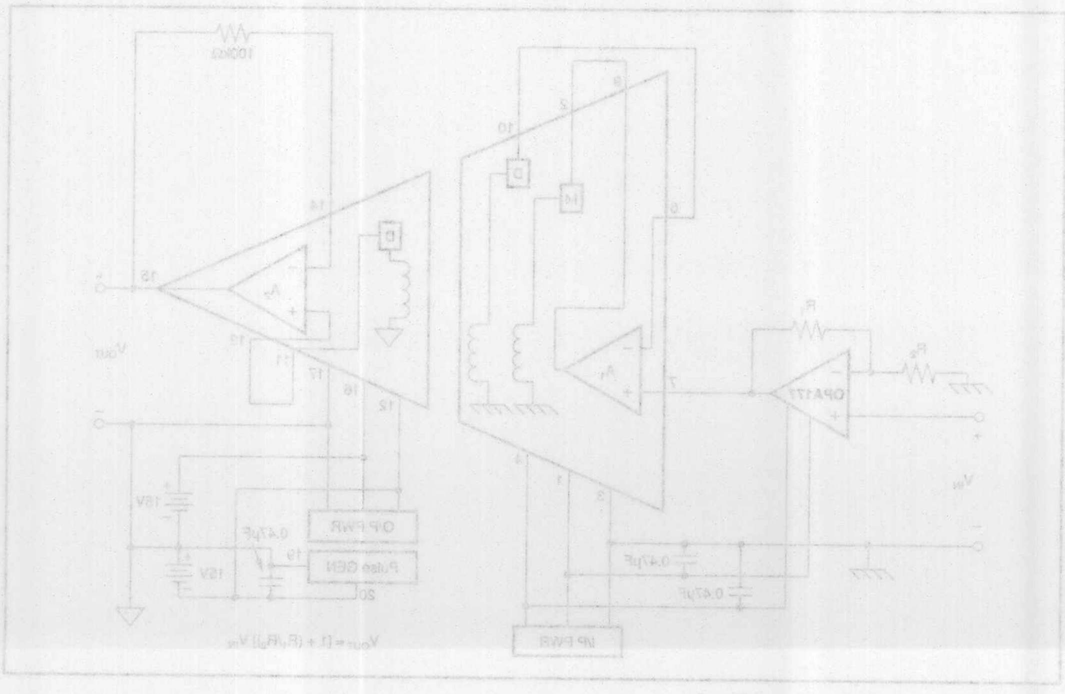


FIGURE 13. Isolator for Low-Level Signals.

6 Optical Sensors

Optical Electronic Integrated Sensors (OEICs) combine the building blocks traditionally used in a transimpedance amplifier on a single monolithic die. The photodiode; low noise, low bias current FET-input operational amplifier, and feedback network are matched to optimize performance.

Our monolithic sensor/amplifier combinations free designers from the tedious design rules necessary to optimize responsivity and speed while maintaining stability and minimal gain peaking in discrete solutions. Other errors that are reduced by a monolithic solution are leakage current errors and noise.

Light falling on the photodiode section of the die is converted to a current. The op amp is connected as a transimpedance amplifier, converting the photodiode current into an output voltage which is proportional to the intensity and wavelength of the light.

Several products and package options are available to allow flexibility in configuring light measurement systems. An external resistor can be placed in series with the internal 1MΩ to increase responsivity in all packages, or placed in parallel to reduce the overall responsivity (in all packages except the SIP).

OPT101—This device was designed to operate on a single power supply of +2.7V to +36V, with a quiescent current of only 120µA at dark. Response peaks at 850nm with a response of 0.6A/W.

OPT101-R—A new innovation in package design, this product is available in red molded plastic to provide optical filtering. The red package provides selective response to wavelengths greater than 570nm, making them ideal for applications using red or infrared illumination.

OPT202—Another innovation in package design—a 5-pin SIP that allows light to originate from the "side" of system boards rather than from perpendicular sources. Also available in a clear plastic DIP as well as a hermetic ceramic DIP.

OPT209—This device is available in plastic DIP, and will help to improve your signal-to-noise ratio in systems not needing the full 50kHz bandwidth of the OPT202.

OPT210—A new high performance silicon photodiode and precision FET-input transimpedance amplifier integrated on a single monolithic chip achieves low noise and 300kHz bandwidth at R_F = 1MΩ.

OPT301—This OEIC is packaged in a hermetic TO-99 package with a glass window, and is specified over the extended industrial temperature range of –40°C to +85°C. Offering a hermetic package and enhanced UV performance, the OPT301 has a 4kHz signal bandwidth.

OPTICAL SENSORS

WIDEBAND (BW, typ)	SPECIAL FEATURES (Basic Function)	GENERAL PURPOSE (I_Q, max)
OPT211 (150kHz)	OPT301 (UV, Hermetic Pkg)	**OPT101 (240µA, Red Filter Option)**
OPT202 (50kHz)	OPT101 (Single Supply)	OPT209 (500µA)
OPT210 (300kHz)	OPT202G (Hermetic DIP)	OPT202 (500µA)

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Product	Small Signal Bandwidth typ (kHz)	Photodiode Dimensions	Feedback Resistor typ	Dark Error max (mV)	Power Supply Range (mV)	Quiescent Current max (μA)	Description
OPT101(1)	**14**	**0.09" x 0.09"**	**1MΩ or external**	**+5 to +10 (offset for single single supply)**	**+2.7V to +36V**	**240**	**Low cost, general purpose. Single supply operation with nominal 7.5mV output offset pedestal.**
OPT202(2)	50	0.09" x 0.09"	1MΩ internal or external	±2	±2.25V to ±18V	500	Wide bandwidth, general purpose photodiode/amplifier.
OPT209	16	0.09" x 0.09"	1MΩ internal	±2	±2.25V to ±18V	500	General purpose photodiode/amplifier.
OPT210	**(900 with external bootstrap buffer)**	**0.09" x 0.09"**	**1MΩ internal or external**	**±10**	**±2.25V to ±18V**	**4000**	**Wide bandwidth with infrared response and extended bandwidth using bootstrap buffer.**
OPT211	50 (150 with external bootstrap buffer)	0.09" x 0.09"	External 330kΩ to 100GΩ	±2	±2.25V to ±18V	500	Wide bandwidth with very high transimpedance gain allows use of external photodiode buffer circuit for widest bandwidth.
OPT301(3)	4	0.09" x 0.09"	1MΩ or external	±2	±2.25V to ±18V	500	Hermetic, general purpose. Extended ultraviolet response.

NOTES: (1) Available with red plastic optical filter. (2) Available in hermetic ceramic DIP with glass window operating over Mil temperature range (–55°C to 125°C). (3) Hermetic, TO-99 package with glass window operating over Mil temperature range (–55°C to 125°C).

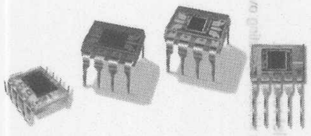
Or, Call Customer Service at 1-800-548-6132 (USA Only)

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.



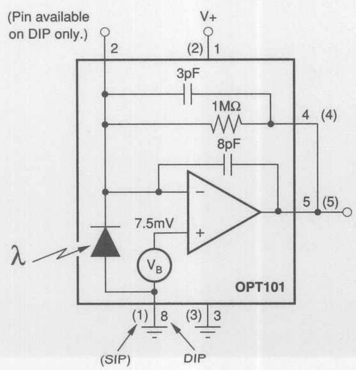
MONOLITHIC PHOTODIODE AND SINGLE-SUPPLY TRANSIMPEDANCE AMPLIFIER

FEATURES

- SINGLE SUPPLY: +2.7 to +36V
- PHOTODIODE SIZE: 0.090 x 0.090 inch
- INTERNAL 1MΩ FEEDBACK RESISTOR
- HIGH RESPONSIVITY: 0.45A/W (650nm)
- BANDWIDTH: 14kHz at R_F = 1MΩ
- LOW QUIESCENT CURRENT: 120µA
- AVAILABLE IN 8-PIN DIP, 5-PIN SIP, AND 8-LEAD SURFACE MOUNT PACKAGES
- CLEAR OR RED PLASTIC VERSIONS

APPLICATIONS

- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- BARCODE SCANNERS
- SMOKE DETECTORS
- CURRENCY CHANGERS

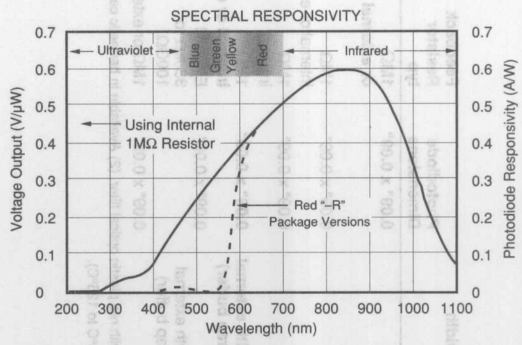


DESCRIPTION

The OPT101 is a monolithic photodiode with on-chip transimpedance amplifier. Output voltage increases linearly with light intensity. The amplifier is designed for single or dual power supply operation, making it ideal for battery operated equipment.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance. The 0.09 x 0.09 inch photodiode is operated in the photoconductive mode for excellent linearity and low dark current.

The OPT101 operates from +2.7V to +36V supplies and quiescent current is only 120µA. It is available in clear plastic 8-pin DIP, 5-pin SIP and J-formed DIP for surface mounting. Red plastic versions are also available with optical filter properties, providing selective response to wavelengths greater than 580nm. Temperature range is 0°C to 70°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

T_A = +25°C, V_S = +2.7V to +36V, λ = 650nm, internal 1MΩ feedback resistor, and R_L = 10kΩ unless otherwise noted.

PARAMETER	CONDITIONS	OPT101P, W MIN	TYP	MAX	UNITS
RESPONSIVITY					
Photodiode Current	650nm		0.45		A/W
Voltage Output	650nm		0.45		V/µW
vs Temperature			100		ppm/°C
Unit to Unit Variation	650nm		±5		%
Nonlinearity(1)	FS Output = 24V		±0.01		% of FS
Photodiode Area	(0.090 x 0.090in)		0.008		in^2
	(2.29 x 2.29mm)		5.2		mm^2
DARK ERRORS, RTO(2)					
Offset Voltage, Output		+5	+7.5	+10	mV
vs Temperature			±2.5		µV/°C
vs Power Supply	V_S = +2.7V to +36V		10	100	µV/V
Voltage Noise, Dark, f_B = 0.1Hz to 20kHz	V_S = +15V, V_{PIN3} = –15V		300		µVrms
TRANSIMPEDANCE GAIN					
Resistor			1		MΩ
Tolerance, P			±0.5	±2	%
W			±0.5		%
vs Temperature			±50		ppm/°C
FREQUENCY RESPONSE					
Bandwidth	V_{OUT} = 10Vp-p		14		kHz
Rise Fall Time, 10% to 90%	V_{OUT} = 10V Step		28		µs
Settling Time, 0.05%	V_{OUT} = 10V Step		160		µs
0.1%			80		µs
1%			70		µs
Overload Recovery	100%, Return to Linear Operation		50		µs
OUTPUT					
Voltage Output, High		(V_S) – 1.3	(V_S) – 1.15		V
Capacitive Load, Stable Operation			10		nF
Short-Circuit Current	V_S = 36V		15		mA
POWER SUPPLY					
Operating Voltage Range		+2.7		+36	V
Quiescent Current	Dark, V_{PIN3} = 0V		120	240	µA
	R_L = ∞, V_{OUT} = 10V		220		µA
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		0		+70	°C
Storage		–25		+85	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

PHOTODIODE SPECIFICATIONS

T_A = +25°C, V_S = +2.7V to +36V unless otherwise noted.

PARAMETER	CONDITIONS	Photodiode of OPT101P MIN	TYP	MAX	UNITS
Photodiode Area	(0.090 x 0.090in)		0.008		in^2
	(2.29 x 2.29mm)		5.2		mm^2
Current Responsivity	650nm		0.45		A/W
	650nm		865		$µA/W/cm^2$
Dark Current	V_{DIODE} = 7.5mV		2.5		pA
vs Temperature			doubles every 7°C		
Capacitance			1200		pF

OP AMP SPECIFICATIONS

T_A = +25°C, V_S = +2.7V to +36V, λ = 650nm, internal 1MΩ feedback resistor, and R_L = 10kΩ unless otherwise noted.

PARAMETER	CONDITIONS	OPT101 Op Amp(1) MIN	TYP	MAX	UNITS
INPUT					
Offset Voltage			±0.5		mV
vs Temperature			±2.5		µV/°C
vs Power Supply			10		µV/V
Input Bias Current	(–) Input		165		pA
vs Temperature	(–) Input		1		pA/°C
Input Impedance					
Differential			400 $\|$ 5		MΩ $\|$ pF
Common-Mode			250 $\|$ 35		GΩ $\|$ pF
Common-Mode Input Voltage Range	Linear Operation		0 to [(V_S) – 1]		V
Common-Mode Rejection			90		dB
OPEN-LOOP GAIN					
Open-loop Voltage Gain			90		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product(2)			2		MHz
Slew Rate			1		V/µs
Settling Time 1%			5.8		µs
0.1%			7.7		µs
0.05%			8.0		µs
OUTPUT					
Voltage Output, High		(V_S) – 1.3	(V_S) – 1.15		V
Short-Circuit Current	V_S = +36V		15		mA
POWER SUPPLY					
Operating Voltage Range		+2.7		+36	V
Quiescent Current	Dark, V_{PIN3} = 0V		120	240	µA
	R_L ∞, V_{OUT} = 10V		220		µA

NOTES: (1) Op amp specifications provided for information and comparison only. (2) Stable gains ≥ 10V/V.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

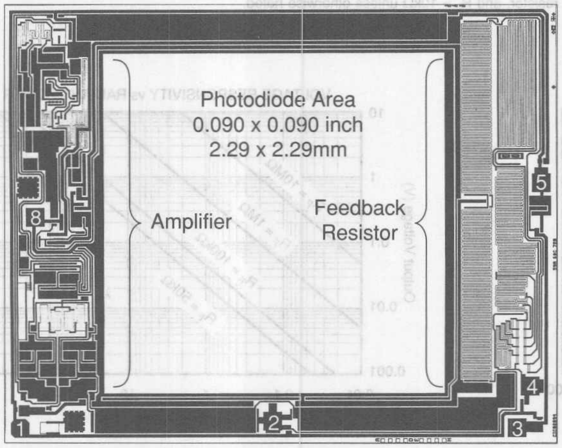
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

MOISTURE SENSITIVITY AND SOLDERING

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that plastic devices be baked-out at +85°C for 24 hours.

The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT101 plastic packages cannot meet flammability test, UL-94.

DICE INFORMATION



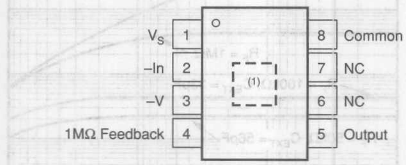
NOTE: Pad numbers correspond to pin numbers on DIP package.

PAD	FUNCTION
1	V_S
2	–In
3	–V
4	1MΩ Feedback
5	Output
8	Common

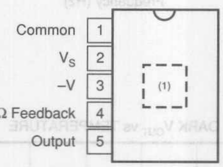
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	150 x 120	3.81 x 3.05
Die Thickness	18	0.51
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	None	

PIN CONFIGURATIONS



NOTE: (1) Photodiode location.



ABSOLUTE MAXIMUM RATINGS

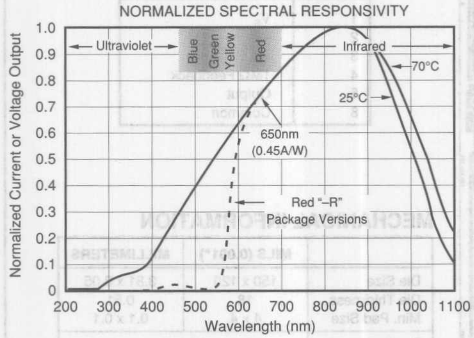
Supply Voltage (V_S to *"Common"* or pin 3) .... 0 to +36V
Output Short-Circuit (to ground) .... Continuous
Operating Temperature .... –25°C to +85°C
Storage Temperature .... –25°C to +85°C
Junction Temperature .... +85°C
Lead Temperature (soldering, 10s) .... +300°C
(Vapor-Phase Soldering Not Recommended)

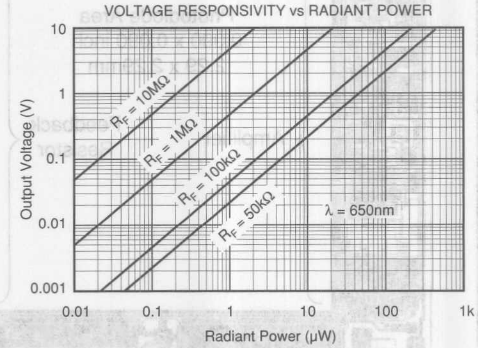
PACKAGE INFORMATION

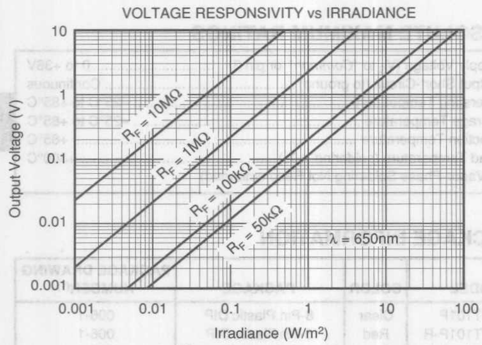
MODEL	COLOR	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPT101P	Clear	8-Pin Plastic DIP	006-1
OPT101P-R	Red	8-Pin Plastic DIP	006-1
OPT101P-J	Clear	8-Lead Surface Mount(2)	006-4
OPT101P-R-J	Red	8-Lead Surface Mount(2)	006-4
OPT101W	Clear	5-Pin Plastic SIP	321
OPT101W-R	Red	5-Pin Plastic SIP	321

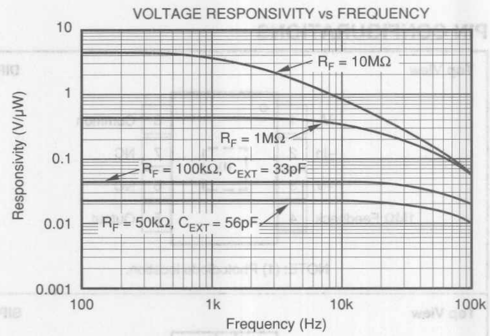
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) 8-pin DIP with J-formed leads for surface mounting.

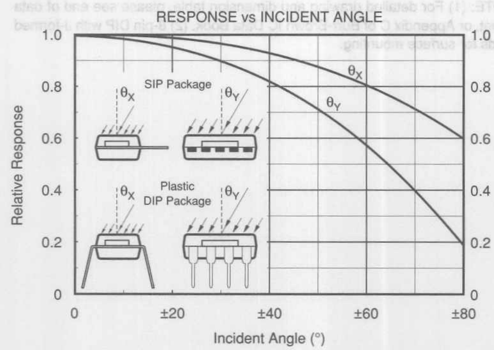
λ = 650nm, internal 1MΩ feedback resistor, and R_L = 10kΩ unless otherwise noted.

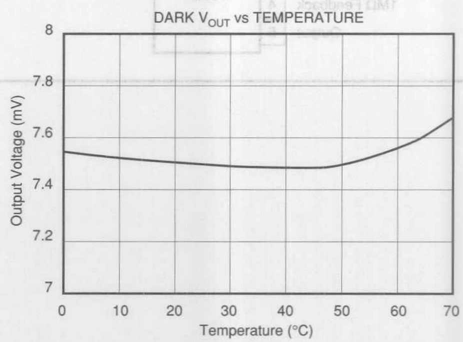








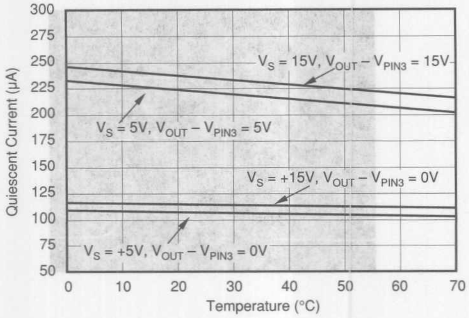




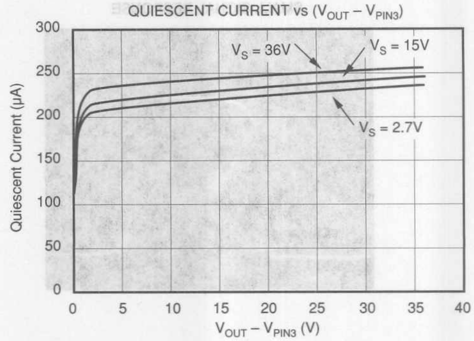
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = +2.7V$ to $+36V$, $\lambda = 650nm$, internal $1M\Omega$ feedback resistor, and $R_L = 10k\Omega$ unless otherwise noted.

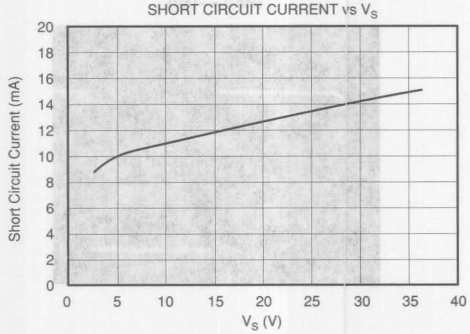
QUIESCENT CURRENT vs TEMPERATURE



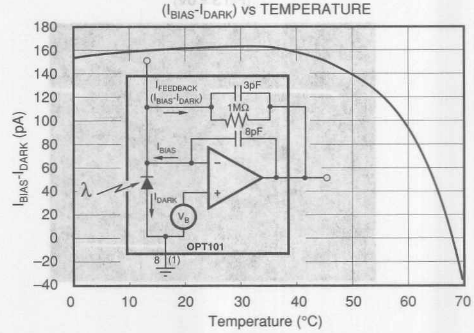
QUIESCENT CURRENT vs ($V_{OUT} - V_{PIN3}$)



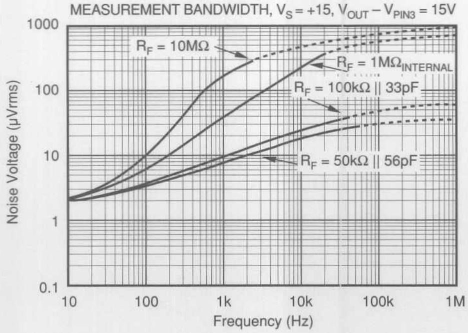
SHORT CIRCUIT CURRENT vs V_S



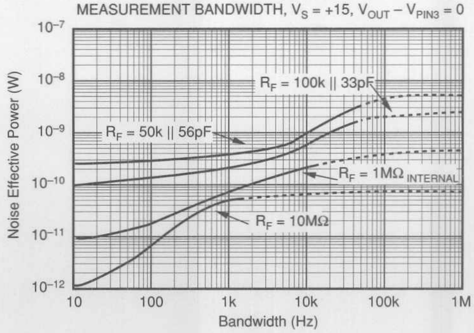
(I_{BIAS}-I_{DARK}) vs TEMPERATURE



OUTPUT NOISE VOLTAGE vs MEASUREMENT BANDWIDTH, $V_S = +15$, $V_{OUT} - V_{PIN3} = 15V$



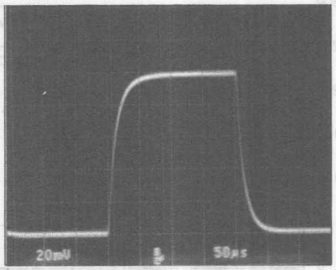
NOISE EFFECTIVE POWER vs MEASUREMENT BANDWIDTH, $V_S = +15$, $V_{OUT} - V_{PIN3} = 0$



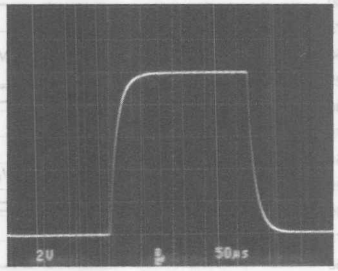
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = +2.7V$ to $+36V$, $\lambda = 650nm$, internal $1M\Omega$ feedback resistor, and $R_L = 10k\Omega$ unless otherwise noted.

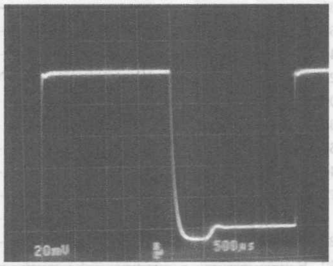
SMALL SIGNAL RESPONSE



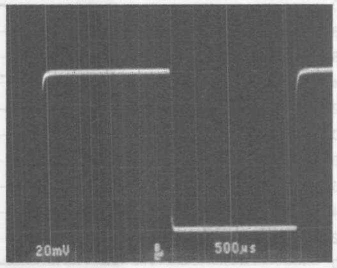
LARGE SIGNAL RESPONSE



SMALL SIGNAL RESPONSE (C_{LOAD} = 10,000 pF)
(Pin 3 = 0V)



SMALL SIGNAL RESPONSE (C_{LOAD} = 10,000 pF)
(Pin 3 = –15V)



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required to operate the OPT101. Applications with high-impedance power supplies may require decoupling capacitors located close to the device pins as shown. Output is 7.5mV dc with no light and increases with increasing illumination.

Photodiode current, I_D, is proportional to the radiant power, or flux, (in watts) falling on the photodiode. At a wavelength of 650nm (visible red) the photodiode Responsivity, R_I, is approximately 0.45A/W. Responsivity at other wavelengths is shown in the typical performance curve "Responsivity vs Wavelength."

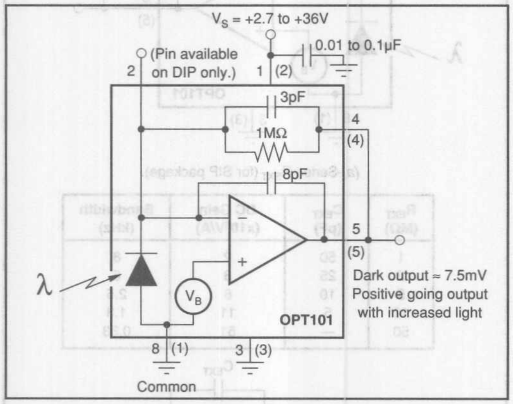


FIGURE 1. Basic Circuit Connections.

The typical performance curve "Output Voltage vs Radiant Power" shows the response throughout a wide range of radiant power. The response curve "Output Voltage vs Irradiance" is based on the photodiode area of $5.2mm^2$.

The OPT101's voltage output is the product of the photodiode current times the feedback resistor, (I_DR_F), plus a pedestal voltage, V_B, of approximately 7.5mV introduced for single supply operation. The internal feedback resistor is laser trimmed to 1MΩ. Using this resistor, the output voltage responsivity, R_V, is approximately 0.45V/µW at 650nm wavelength. Figure 1 shows the basic circuit connections for the OPT101 operating with a single power supply and using the internal 1MΩ feedback resistor for a response of 0.45V/µW at 650nm. Pin 3 is connected to common in this configuration.

CAPACITIVE LOADING

The OPT101 is capable of driving load capacitances of 10nF without instability. However, dynamic performance with capacitive loads can be improved by applying a negative bias voltage to Pin 3 (shown in Figure 2). This negative power supply voltage allows the output to go negative in response to the reactive effect of a capacitive load. An internal JFET connected between pin 5 (output) and pin 3 allows the output to sink current. This current sink capability can also be useful when driving the capacitive inputs of some analog-to-digital converters which require the signal source to sink currents up to approximately 100µA. The benefits of this current sink are shown in the typical performance curves "Small Signal Response (C_{LOAD} = 10,000pF)" which compare operation with pin 3 grounded and connected to −15V.

Due to the architecture of this output stage current sink, there is a slight increase in operating current when there is a voltage between pin 3 and the output. Depending on the magnitude of this voltage, the quiescent current will increase by approximately 100µA as shown in the typical performance curve "Quiescent Current vs ($V_{OUT} - V_{PIN3}$)".

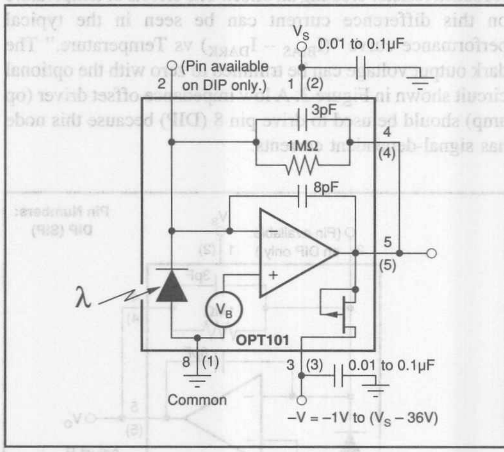


FIGURE 2. Bipolar Power Supply Circuit Connections.

NOISE PERFORMANCE

Noise performance of the OPT101 is determined by the op amp characteristics, feedback components and photodiode capacitance. The typical performance curve "Output Noise Voltage vs Measurement Bandwidth" shows how the noise varies with R_F and measured bandwidth (0.1Hz to the indicated frequency), when the output voltage minus the voltage on pin 3 is greater than approximately 50mV. Below this level, the output stage is powered down, and the effective bandwidth is decreased. This reduces the noise to approximately 1/3 the nominal noise value of 300µVrms, or 100µVrms. This enables a low level signal to be resolved.

Noise can be reduced by filtering the output with a cutoff frequency equal to the signal bandwidth. This will improve signal-to-noise ratio. Also, output noise increases in proportion to the square root of the feedback resistance, while responsivity increases linearly with feedback resistance. Best signal-to-noise ratio is achieved with large feedback resistance. This comes with the trade-off of decreased bandwidth.

The noise performance of the photodetector is sometimes characterized by *Noise Effective Power* (NEP). This is the radiant power that would produce an output signal equal to the noise level. NEP has the units of radiant power (watts), or Watts/$\sqrt{Hz}$ to convey spectral information about the noise. The typical performance curve "Noise Effective Power" vs Measurement Bandwidth" illustrates the NEP for the OPT101.

DARK ERRORS

The dark errors in the specification table include all sources. The dominant source of dark output voltage is the "pedestal" voltage applied to the non-inverting input of the op amp. This voltage is introduced to provide linear operation in the absence of light falling on the photodiode. Photodiode dark current is approximately 2.5pA and contributes virtually no offset error at room temperature. The bias current of the op amp's summing junction (– input) is approximately 165pA. The dark current will be subtracted from the amplifier's bias current, and this residual current will flow through the feedback resistor creating an offset. The effects of temperature on this difference current can be seen in the typical performance curve "(I_{BIAS} – I_{DARK}) vs Temperature." The dark output voltage can be trimmed to zero with the optional circuit shown in Figure 3. A low impedance offset driver (op amp) should be used to drive pin 8 (DIP) because this node has signal-dependent currents.

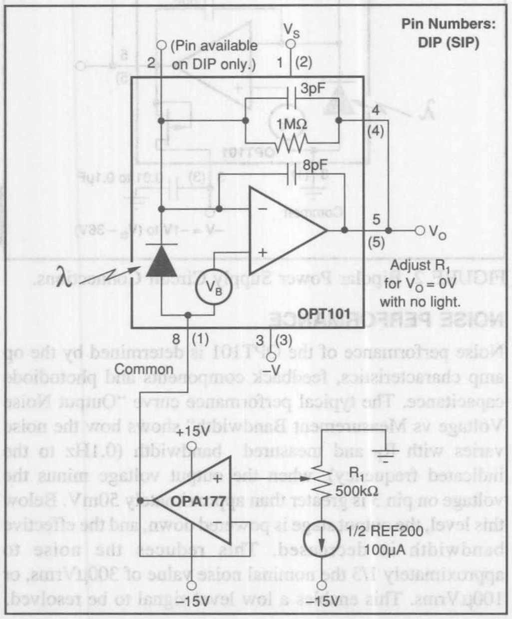
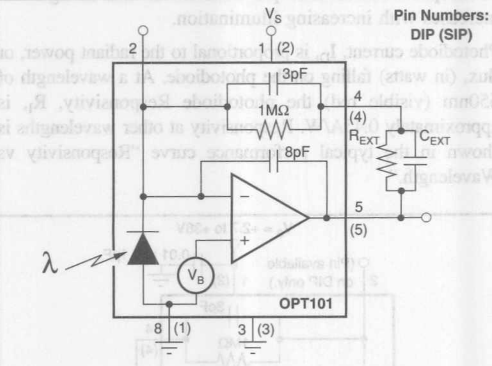


FIGURE 3. Dark Error (Offset) Adjustment Circuit.

CHANGING RESPONSIVITY

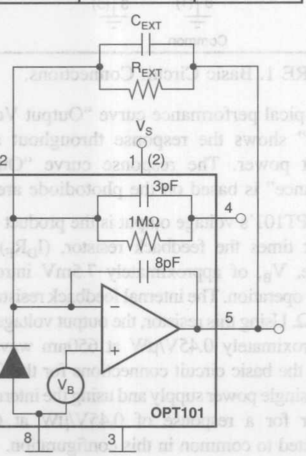
An external resistor, R_{EXT}, can be connected to set a different voltage responsivity. To increase the responsivity, this resistor can be placed in series with the internal 1MΩ (Figure 4a), or with the DIP package, the external resistor can replace the internal resistor by not connecting pin 4 (Figure 4b). The second configuration also allows the circuit gain to be reduced below 10^6V/A by using external resistors of less than 1MΩ.

Figure 4 includes tables showing the responsivity and bandwidth. For values of R_F less than 1MΩ, an external capacitor, C_{EXT} should be connected in parallel with R_F. This capacitor eliminates gain peaking and prevents instability. The value of C_{EXT} can be determined from the table in Figure 4. Values of R_F, other than shown in the table, can be interpolated.



(a)-Series R_{EXT} (for SIP package).

R_{EXT} (MΩ)	C_{EXT} (pF)	DC Gain ($\times10^6$V/A)	Bandwidth (kHz)
1	50	2	8
2	25	3	6
5	10	6	2.5
10	5	11	1.3
50	—	51	0.33



(b)-External Feedback (for DIP package).

R_{EXT} (MΩ)	C_{EXT} (pF)	DC Gain ($\times10^6$V/A)	Bandwidth (kHz)
0.05(1)	56	0.05	58
0.1(1)	33	0.1	44
1	—	1	23
2	—	2	9.4
5	—	5	3.6
10	—	10	1.8
50	—	50	0.34

Note: (1) May require 1kΩ in series with pin 5 when driving large capacitances.

FIGURE 4. Changing Responsivity with External Resistor.

LIGHT SOURCE POSITIONING

The OPT101 is tested with a light source that uniformly illuminates the full area of the integrated circuit, including the op amp. Although IC amplifiers are light-sensitive to some degree, the OPT101 op amp circuitry is designed to minimize this effect. Sensitive junctions are shielded with metal, and the photodiode area is very large relative to the op amp input circuitry.

If your light source is focused to a small area, be sure that it is properly aimed to fall on the photodiode. A narrowly focused beam falling on only the photodiode will provide improved settling times compared to a source that uniformly illuminates the full area of the die. If a narrowly focused light source were to miss the photodiode area and fall only on the op amp circuitry, the OPT101 would not perform properly. The large 0.09" x 0.09" (2.29mm x 2.29mm) photodiode area allows easy positioning of narrowly focused light sources. The photodiode area is easily visible, as it appears very dark compared to the surrounding active circuitry.

The incident angle of the light source also effects the apparent sensitivity in uniform irradiance. For small incident angles, the loss in sensitivity is simply due to the smaller effective light gathering area of the photodiode (proportional to the cosine of the angle). At a greater incident angle, light is diffracted and scattered by the package. These effects are shown in the typical performance curve "Responsivity vs Incident Angle."

DYNAMIC RESPONSE

Using the internal 1MΩ resistor, the dynamic response of the photodiode/op amp combination can be modeled as a simple R • C circuit with a –3dB cutoff frequency of approximately 14kHz. The R and C values are 1MΩ and 11pF respectively. By using external resistors, with less than 3pF parasitic capacitance, the frequency response can be improved. An external 1MΩ resistor used in the configuration shown in Figure 4b will create a 23kHz bandwidth with the same 10^6V/A dc transimpedance gain. This yields a rise time of approximately 15µs (10% to 90%). Dynamic response is not limited by op amp slew rate. This is demonstrated by the dynamic response oscilloscope photographs showing virtually identical large-signal and small-signal response.

Dynamic response will vary with feedback resistor value as shown in the typical performance curve "Responsivity vs Frequency." Rise time (10% to 90%) will vary according to the –3dB bandwidth produced by a given feedback resistor value:

$$t_r = \frac{0.35}{f_C}$$

where:

t_r is the rise time (10% to 90%)
f_C is the –3dB bandwidth

LINEARITY PERFORMANCE

The photodiode is operated in the photoconductive mode so the current output of the photodiode is very linear with radiant power throughout a wide range. Nonlinearity remains below approximately 0.05% up to 100µA photodiode current. The photodiode can produce output currents of 1mA or greater with high radiant power, but nonlinearity increases to several percent in this region.

This very linear performance at high radiant power assumes that the full photodiode area is uniformly illuminated. If the light source is focused to a small area of the photodiode, nonlinearity will occur at lower radiant power.

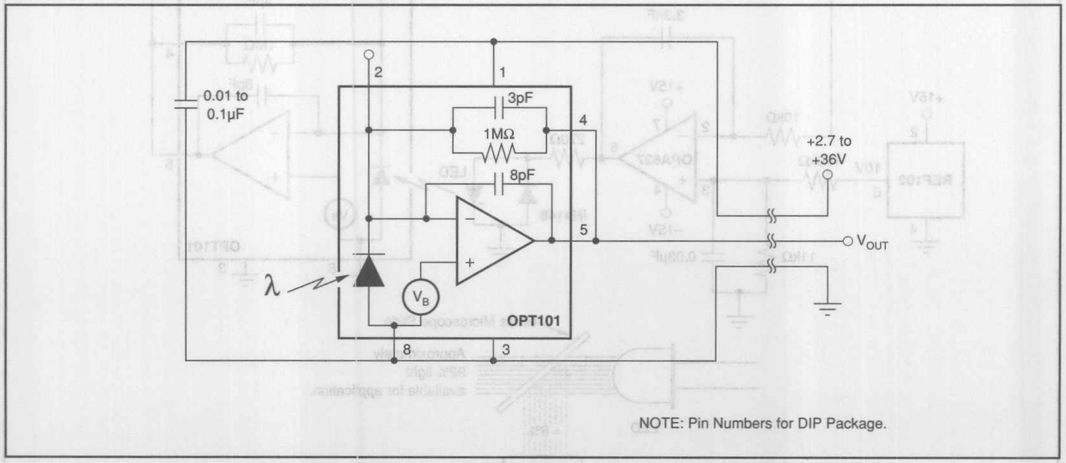


FIGURE 5. Three-Wire Remote Light Measurement.

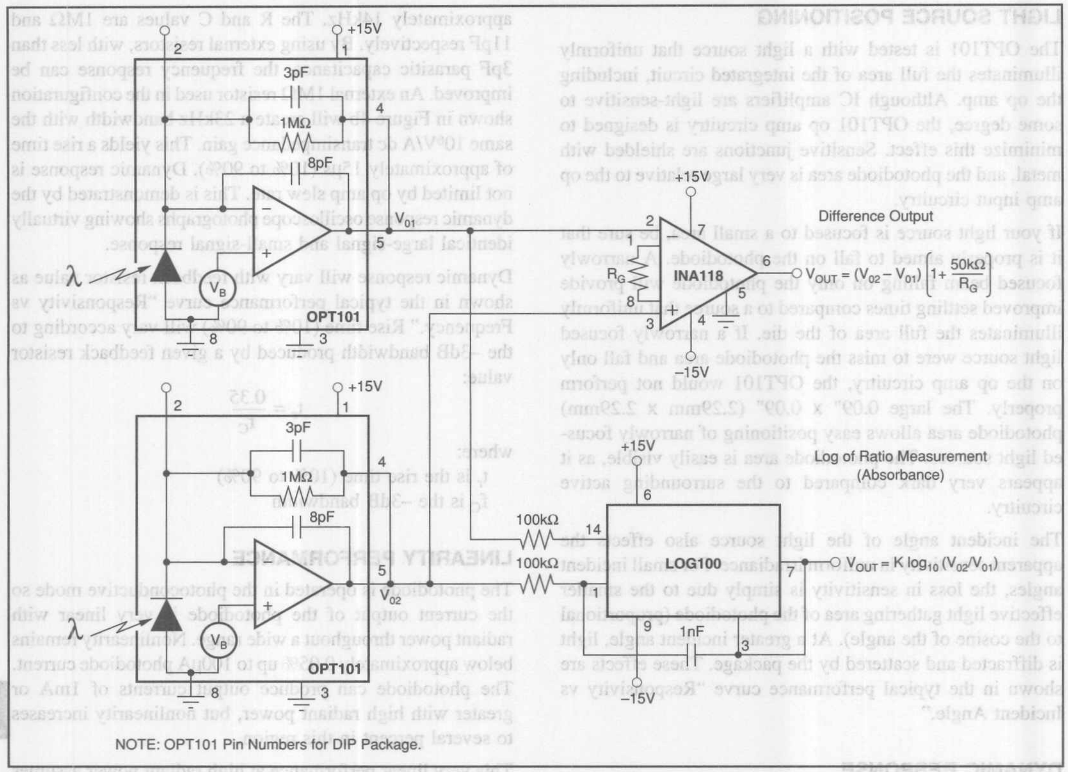


FIGURE 6. Differential Light Measurement.

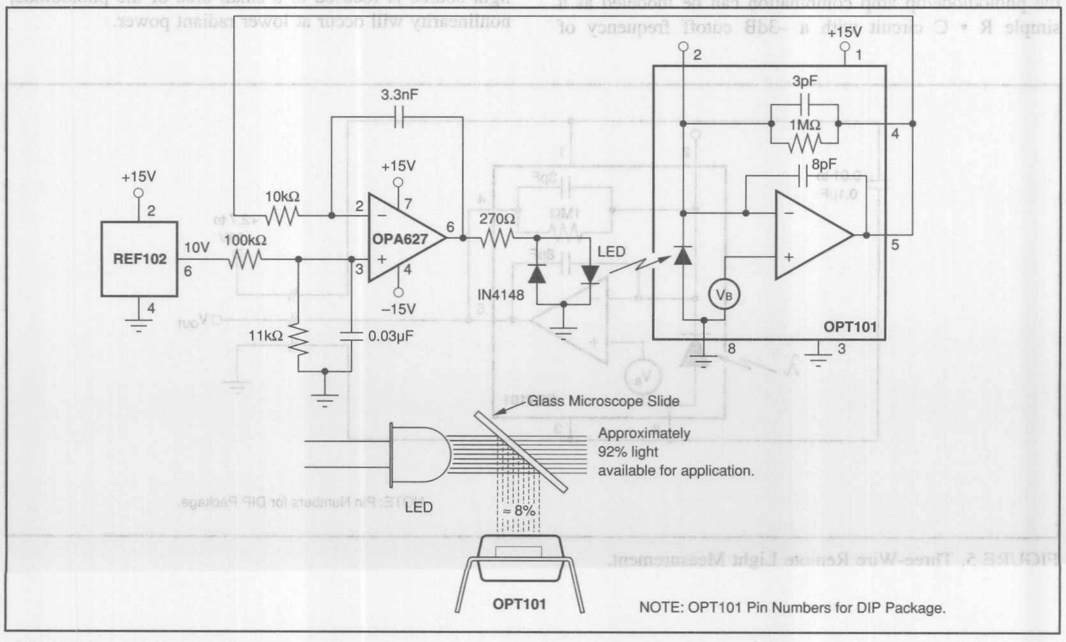
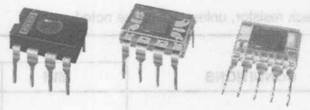


FIGURE 7. LED Output Regulation Circuit.

BURR - BROWN®



OPT202

PHOTODIODE WITH ON-CHIP AMPLIFIER

FEATURES

- BANDWIDTH: 50kHz
- PHOTODIODE SIZE: 0.090 x 0.090 inch (2.29 x 2.29mm)
- 1MΩ FEEDBACK RESISTOR
- HIGH RESPONSIVITY: 0.45A/W (650nm)
- LOW DARK ERRORS: 2mV
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 400μA
- TRANSPARENT 8-PIN DIP AND 5-PIN SIP
- HERMETIC 8-PIN CERAMIC DIP

APPLICATIONS

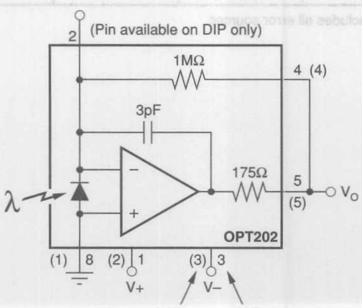
- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- SMOKE DETECTORS

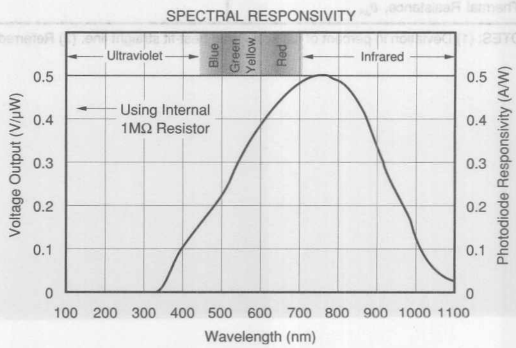
DESCRIPTION

The OPT202 is an opto-electronic integrated circuit containing a photodiode and transimpedance amplifier on a single dielectrically isolated chip. The transimpedance amplifier consists of a precision FET-input op amp and an on-chip metal film resistor. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT202 operates over a wide supply range (±2.25 to ±18V) and supply current is only 400μA. It is packaged in a transparent plastic 8-pin DIP or 5-pin SIP, specified for the 0°C to +70°C temperature range as well as a hermetic ceramic 8-pin DIP with a glass window, specified for the –40°C to +85°C temperature range.





International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

ELECTRICAL

T_A = +25°C, V_S = ±15V, λ = 650nm, internal 1MΩ feedback resistor, unless otherwise noted.

PARAMETER	CONDITIONS	OPT202P, W, G MIN	TYP	MAX	UNITS
RESPONSIVITY					
Photodiode Current	650nm		0.45		A/W
Voltage Output	650nm		0.45		V/μW
vs Temperature			100		ppm/°C
Unit-to-Unit Variation	650nm		±5		%
Nonlinearity[1]	FS Output = 10V		0.01		% of FS
Photodiode Area	(0.090 x 0.090in)		0.008		in^2
	(2.29 x 2.29mm)		5.2		mm^2
DARK ERRORS, RTO[2]					
Offset Voltage, Output: P, W Packages			±0.5	±2	mV
G Package			±0.5	±3	mV
vs Temperature			±10		μV/°C
vs Power Supply	V_S = ±2.25V to ±18V		10	100	μV/V
Voltage Noise	Measured BW = 0.1Hz to 100kHz		1		mVrms
RESISTOR—1MΩ Internal					
Resistance			1		MΩ
Tolerance: P, G Packages			±0.5	±2	%
W Package			±0.5		%
vs Temperature			50		ppm/°C
FREQUENCY RESPONSE					
Bandwidth, Large or Small-Signal, –3dB			50		kHz
Rise Time, 10% to 90%			10		μs
Settling Time, 1%	FS to Dark		10		μs
0.1%	FS to Dark		20		μs
0.01%	FS to Dark		40		μs
Overload Recovery Time (to 1%)	100% Overdrive, V_S = ±15V		44		μs
	100% Overdrive, V_S = ±5V		100		μs
	100% Overdrive, V_S = ±2.25V		240		μs
OUTPUT					
Voltage Output	R_L = 10kΩ	(V+) – 1.25	(V+) – 1		V
	R_L = 5kΩ	(V+) – 2	(V+) – 1.5		V
Capacitive Load, Stable Operation			10		nF
Short-Circuit Current			±18		mA
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±2.25		±18	V
Quiescent Current	V_O = 0		±400	±500	μA
TEMPERATURE RANGE					
Specification; P, W Packages		0		+70	°C
G Package		–40		+85	°C
Operating, P, W Packages		0		+70	°C
G Package		–55		+125	°C
Storage P, W Packages		–25		+85	°C
G Package		–55		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

SPECIFICATIONS (CONT)

ELECTRICAL

Op Amp Section of OPT202(1)

T_A = +25°C, V_S = ±15V, unless otherwise noted.

PARAMETER	CONDITIONS	OPT202 Op Amp MIN	TYP	MAX	UNITS
INPUT					
Offset Voltage			±0.5		mV
vs Temperature			±5		µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		10		µV/V
Input Bias Current			1		pA
vs Temperature			doubles every 10°C		
NOISE					
Input Voltage Noise					
Voltage Noise Density, f = 10Hz			30		nV/√Hz
f = 100Hz			25		nV/√Hz
f = 1kHz			15		nV/√Hz
Current Noise Density, f = 1kHz			0.8		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range			±14.4		V
Common-Mode Rejection			106		dB
INPUT IMPEDANCE					
Differential			10^{12}‖3		Ω ‖ pF
Common-Mode			10^{12}‖3		Ω ‖ pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain			120		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			16		MHz
Slew Rate			6		V/µs
Settling Time 0.1%			4		µs
0.01%			5		µs
OUTPUT					
Voltage Output	R_L = 10kΩ	(V+) – 1.25	(V+) – 1		V
	R_L = 5kΩ	(V+) – 2	(V+) – 1.5		V
Short-Circuit Current			±18		mA
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±2.25		±18	V
Quiescent Current	I_O = 0		±400	±500	µA

NOTE: (1) Op amp specifications provided for information and comparison only.

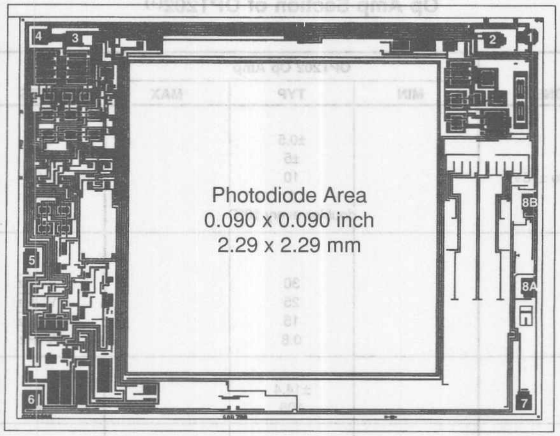
PHOTODIODE SPECIFICATIONS

T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	Photodiode of OPT202 MIN	TYP	MAX	UNITS
Photodiode Area	(0.090 x 0.090in)		0.008		in²
	(2.29 x 2.29mm)		5.2		mm²
Current Responsivity	650nm		0.45		A/W
Dark Current	V_D = 0V(1)		500		fA
vs Temperature			doubles every 10°C		
Capacitance	V_D = 0V(1)		600		pF

NOTE: (1) Voltage Across Photodiode.

DICE INFORMATION



OPT202 DIE TOPOGRAPHY

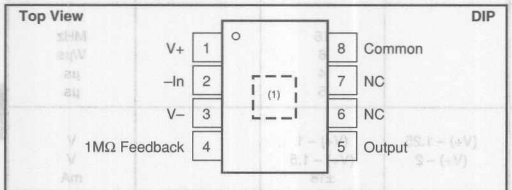
PAD	FUNCTION
1	V+
2	–In
3	V–
4	1MΩ Feedback
5	Output
6	NC
7	NC
8A, 8B	Common

NC: No Connection. Pads 8A and 8B must both be connected to common. Substrate Bias: The substrate is electrically connected to internal circuitry. Do not make electrical connection to the substrate.

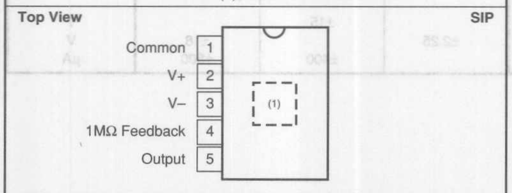
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	154 x 120 ±5	3.91 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATIONS



NOTE: (1) Photodiode location.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±18V
Input Voltage Range (Common Pin)		$\pm V_S$
Output Short-Circuit (to ground)		Continuous
Operating Temperature:	P, W	–25°C to +85°C
	G	–55°C to +125°C
Storage Temperature:	P, W	–25°C to +85°C
	G	–55°C to +125°C
Junction Temperature:	P, W	+85°C
	G	+150°C
Lead Temperature (soldering, 10s)		+300°C
(Vapor-Phase Soldering Not Recommended on Plastic Packages)		

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPT202P	8-Pin Plastic DIP	006-1
OPT202W	5-Pin Plastic SIP	321
OPT202G	8-Pin Ceramic DIP	161-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

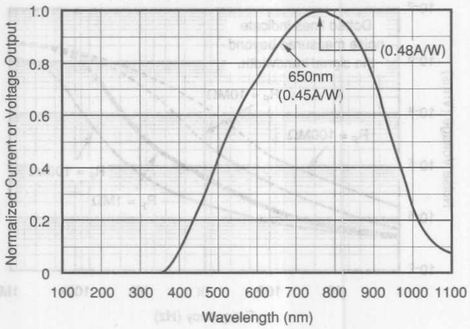
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

MOISTURE SENSITIVITY AND SOLDERING

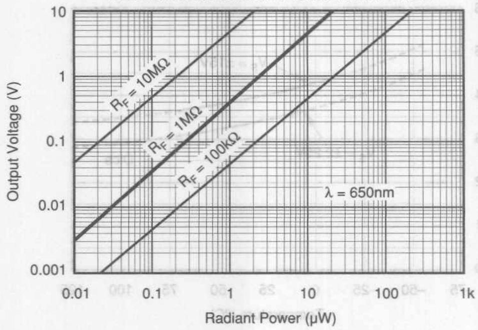
Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that plastic devices be baked-out at 85°C for 24 hours.

The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT202 plastic packages cannot meet flammability test, UL-94.

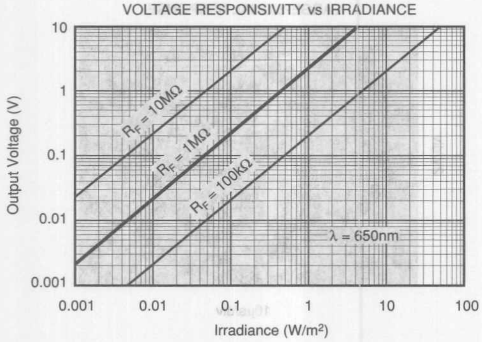
NORMALIZED SPECTRAL RESPONSIVITY



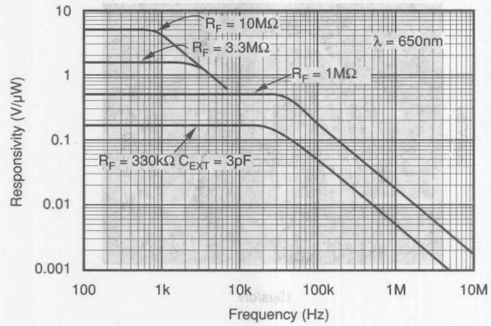
VOLTAGE RESPONSIVITY vs RADIANT POWER



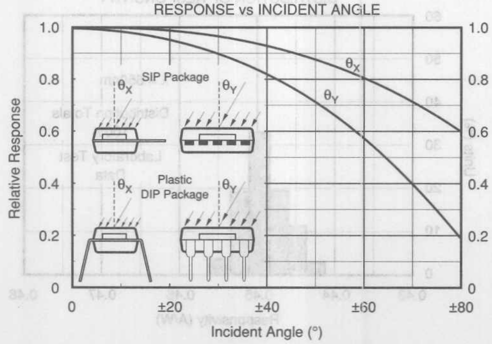
VOLTAGE RESPONSIVITY vs IRRADIANCE



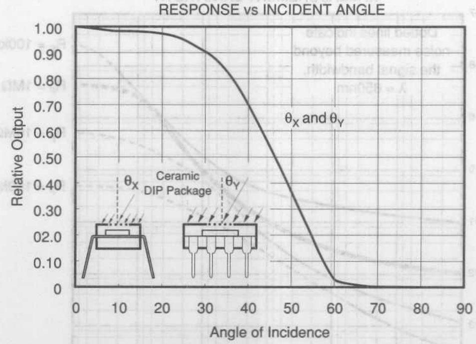
VOLTAGE OUTPUT RESPONSIVITY vs FREQUENCY



RESPONSE vs INCIDENT ANGLE

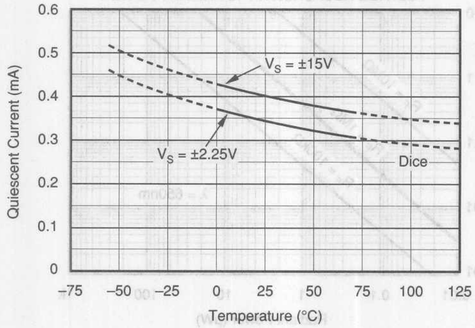


RESPONSE vs INCIDENT ANGLE

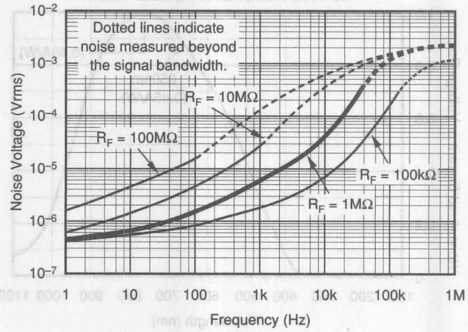


At $T_A = +25°C$, $V_S = \pm15V$, $\lambda = 650nm$, unless otherwise noted.

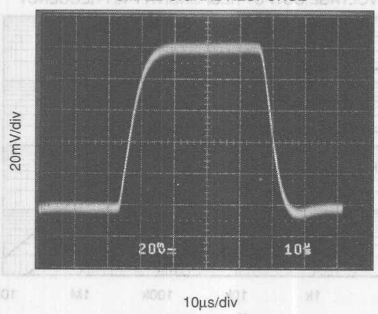
QUIESCENT CURRENT vs TEMPERATURE



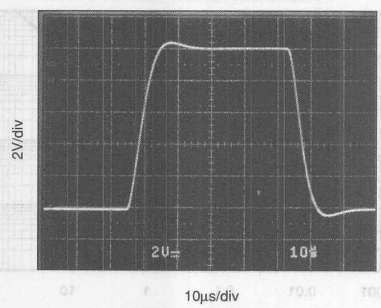
OUTPUT NOISE VOLTAGE vs MEASUREMENT BANDWIDTH



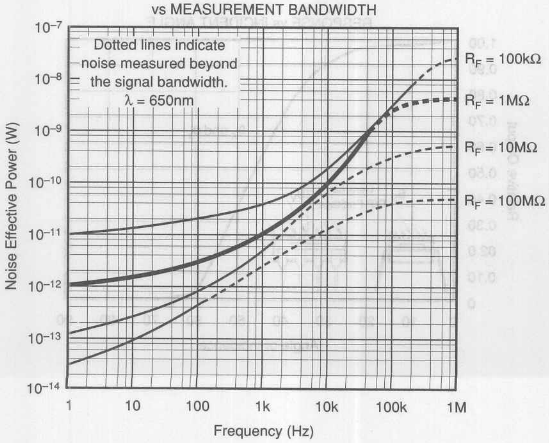
SMALL-SIGNAL RESPONSE



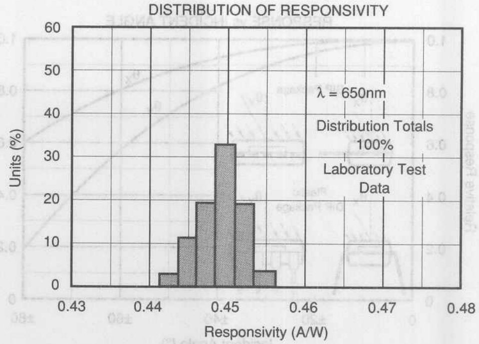
LARGE-SIGNAL RESPONSE



NOISE EFFECTIVE POWER vs MEASUREMENT BANDWIDTH



DISTRIBUTION OF RESPONSIVITY



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required to operate the OPT202. Applications with high-impedance power supplies may require decoupling capacitors located close to the device pins as shown. Output is zero volts with no light and increases with increasing illumination.

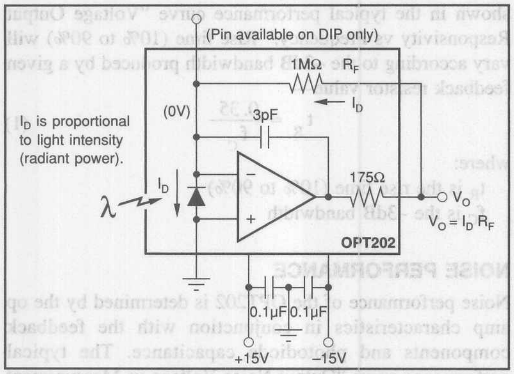


FIGURE 1. Basic Circuit Connections.

Photodiode current, I_D, is proportional to the radiant power or flux (in watts) falling on the photodiode. At a wavelength of 650nm (visible red) the photodiode Responsivity, R_I, is approximately 0.45A/W. Responsivity at other wavelengths is shown in the typical performance curve "Responsivity vs Wavelength."

The typical performance curve "Output Voltage vs Radiant Power" shows the response throughout a wide range of radiant power. The response curve "Output Voltage vs Irradiance" is based on the photodiode area of $5.23 \times 10^{-6}m^2$.

The OPT202's voltage output is the product of the photodiode current times the feedback resistor, (I_DR_F). The internal feedback resistor is laser trimmed to 1MΩ ±2%. Using this resistor, the output voltage responsivity, R_V, is approximately 0.45V/µW at 650nm wavelength.

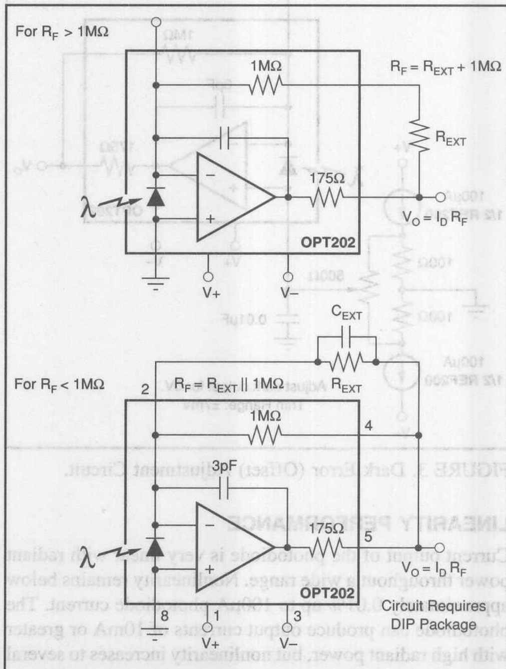
An external resistor can be connected to set a different voltage responsivity. Best dynamic performance is achieved by connecting R_{EXT} in series (for R_F > 1MΩ), or in parallel (for R_F < 1MΩ), with the internal resistor as shown in Figure 2. Placing the external resistor in parallel with the internal resistor requires the DIP package. These connections take advantage of on-chip capacitive guarding of the internal resistor, which improves dynamic performance. For values of R_F less than 1MΩ, an external capacitor, C_{EXT}, should be connected in parallel with R_F (see Figure 2). This capacitor eliminates gain peaking and prevents instability. The value of C_{EXT} can be read from the table in Figure 2.

LIGHT SOURCE POSITIONING

The OPT202 is 100% tested with a light source that uniformly illuminates the full area of the integrated circuit, including the op amp. Although all IC amplifiers are light-sensitive to some degree, the OPT202 op amp circuitry is designed to minimize this effect. Sensitive junctions are shielded with metal, and differential stages are cross-coupled. Furthermore, the photodiode area is very large relative to the op amp input circuitry making these effects negligible.

If your light source is focused to a small area, be sure that it is properly aimed to fall on the photodiode. If a narrowly focused light source were to miss the photodiode area and fall only on the op amp circuitry, the OPT202 would not perform properly. The large (0.090 x 0.090 inch) photodiode area allows easy positioning of narrowly focused light sources. The photodiode area is easily visible—it appears very dark compared to the surrounding active circuitry.

The incident angle of the light source also affects the apparent sensitivity in uniform irradiance. For small incident angles, the loss in sensitivity is simply due to the smaller effective light gathering area of the photodiode (proportional to the cosine of the angle). At a greater incident angle, light is diffused by the side of the package. These effects are shown in the typical performance curve "Response vs Incident Angle."



EQUIVALENT R_F	C_{EXT}
100MΩ	(1)
10MΩ	(1)
1MΩ	(1)
330kΩ	2pF
≤100kΩ	(2)

NOTES: (1) No C_{EXT} required. (2) Not recommended due to possible op amp instability.

FIGURE 2. Using External Feedback Resistor.

DARK ERRORS

The dark errors in the specification table include all sources. The dominant error source is the input offset voltage of the op amp. Photodiode dark current and input bias current of the op amp are in the 2pA range and contribute virtually no offset error at room temperature. Dark current and input bias current double for each 10°C above 25°C. At 70°C, the error current can be approximately 100pA. This would produce a 1mV offset with R_F = 10MΩ. The OPT202 is useful with feedback resistors of 100MΩ or greater at room temperature. The dark output voltage can be trimmed to zero with the optional circuit shown in Figure 3.

When used with very large feedback resistors, tiny leakage currents on the circuit board can degrade the performance of the OPT202. Careful circuit board design and clean assembly procedures will help achieve best performance. A "guard ring" on the circuit board can help minimize leakage to the critical non-inverting input (pin 2). This guard ring should encircle pin 2 and connect to Common, pin 8.

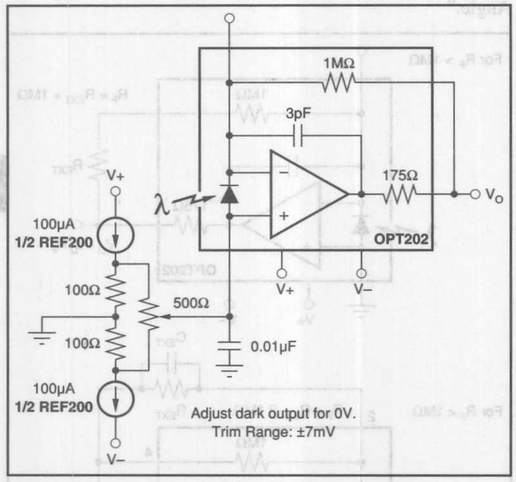


FIGURE 3. Dark Error (Offset) Adjustment Circuit.

LINEARITY PERFORMANCE

Current output of the photodiode is very linear with radiant power throughout a wide range. Nonlinearity remains below approximately 0.01% up to 100µA photodiode current. The photodiode can produce output currents of 10mA or greater with high radiant power, but nonlinearity increases to several percent in this region.

This very linear performance at high radiant power assumes that the full photodiode area is uniformly illuminated. If the light source is focused to a small area of the photodiode, nonlinearity will occur at lower radiant power.

DYNAMIC RESPONSE

Using the internal 1MΩ resistor, the dynamic response of the photodiode/op amp combination can be modeled as a simple R/C circuit with a –3dB cutoff frequency of 50kHz. This yields a rise time of approximately 10µs (10% to 90%). Dynamic response is not limited by op amp slew rate. This is demonstrated by the dynamic response oscilloscope photographs showing virtually identical large-signal and small-signal response.

Dynamic response will vary with feedback resistor value as shown in the typical performance curve "Voltage Output Responsivity vs Frequency." Rise time (10% to 90%) will vary according to the –3dB bandwidth produced by a given feedback resistor value—

$$t_R \approx \frac{0.35}{f_C} \quad (1)$$

where:

t_R is the rise time (10% to 90%)
f_C is the –3dB bandwidth

NOISE PERFORMANCE

Noise performance of the OPT202 is determined by the op amp characteristics in conjunction with the feedback components and photodiode capacitance. The typical performance curve "Output Noise Voltage vs Measurement Bandwidth" shows how the noise varies with R_F and measured bandwidth (1Hz to the indicated frequency). The signal bandwidth of the OPT202 is indicated on the curves. Noise can be reduced by filtering the output with a cutoff frequency equal to the signal bandwidth.

Output noise increases in proportion to the square-root of the feedback resistance, while responsivity increases linearly with feedback resistance. So best signal-to-noise ratio is achieved with large feedback resistance. This comes with the trade-off of decreased bandwidth.

The noise performance of a photodetector is sometimes characterized by Noise Effective Power (NEP). This is the radiant power which would produce an output signal equal to the noise level. NEP has the units of radiant power (watts). The typical performance curve "Noise Effective Power vs Measurement Bandwidth" shows how NEP varies with R_F and measurement bandwidth.

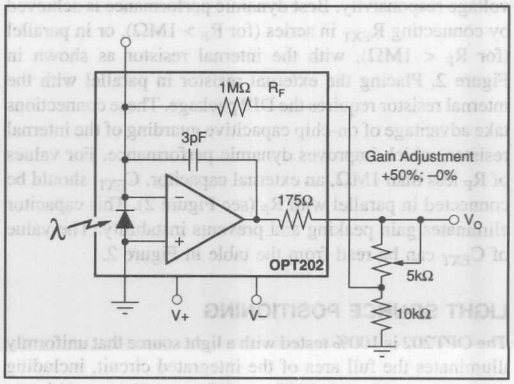


FIGURE 4. Responsivity (Gain) Adjustment Circuit.

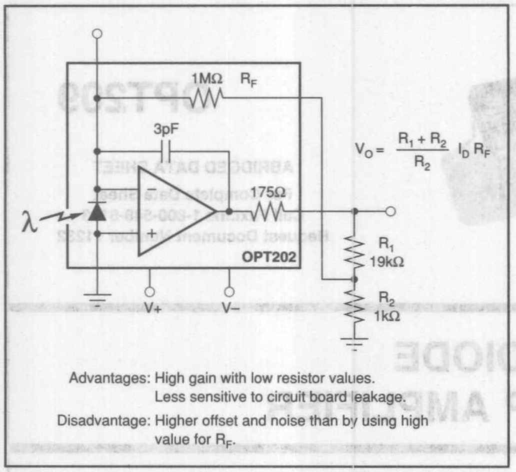


FIGURE 5. "T" Feedback Network.

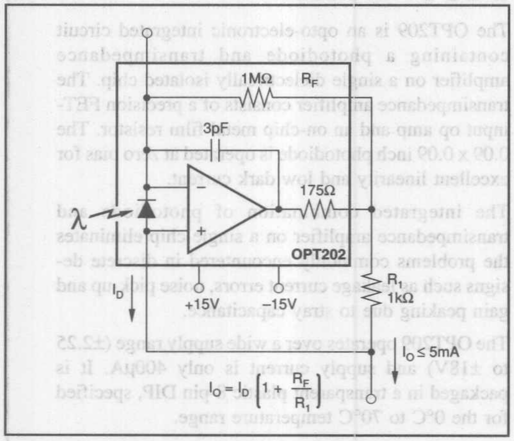


FIGURE 6. Current Output Circuit.

Other application circuits can be seen in the OPT209 data sheet.

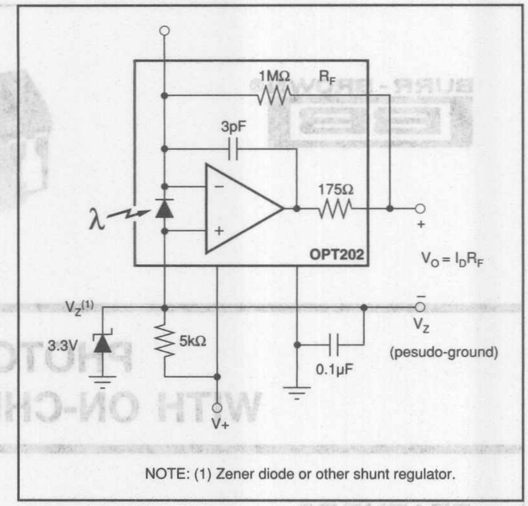


FIGURE 7. Single Power Supply Operation.

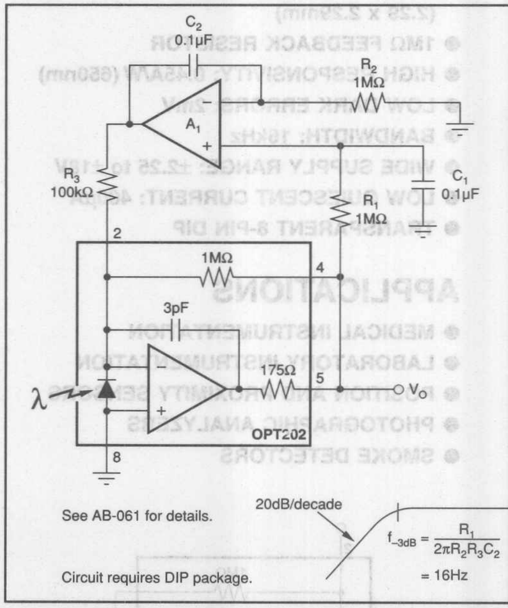
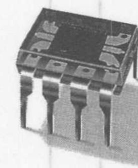


FIGURE 8. DC Restoration Rejects Unwanted Steady-State Background Light.

BURR - BROWN®

OPT209



ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11232

PHOTODIODE WITH ON-CHIP AMPLIFIER

FEATURES

- PHOTODIODE SIZE: 0.090 x 0.090 inch (2.29 x 2.29mm)
- 1MΩ FEEDBACK RESISTOR
- HIGH RESPONSIVITY: 0.45A/W (650nm)
- LOW DARK ERRORS: 2mV
- BANDWIDTH: 16kHz
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 400µA
- TRANSPARENT 8-PIN DIP

APPLICATIONS

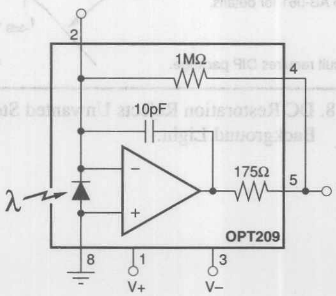
- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- SMOKE DETECTORS

DESCRIPTION

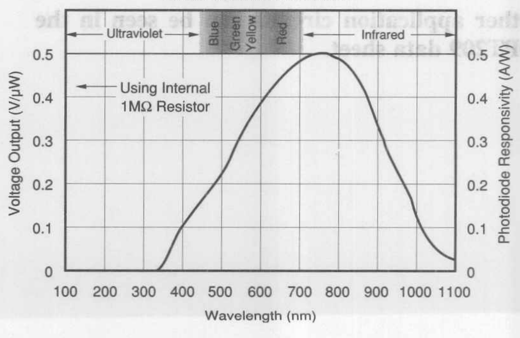
The OPT209 is an opto-electronic integrated circuit containing a photodiode and transimpedance amplifier on a single dielectrically isolated chip. The transimpedance amplifier consists of a precision FET-input op amp and an on-chip metal film resistor. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT209 operates over a wide supply range (±2.25 to ±18V) and supply current is only 400µA. It is packaged in a transparent plastic 8-pin DIP, specified for the 0°C to 70°C temperature range.



SPECTRAL RESPONSIVITY



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

T_A = +25°C, V_S = ±15V, λ = 650nm, internal 1MΩ feedback resistor, unless otherwise noted.

PARAMETER	CONDITIONS	OPT209P MIN	TYP	MAX	UNITS
RESPONSIVITY					
Photodiode Current	650nm		0.45		A/W
Voltage Output	650nm		0.45		V/µW
vs Temperature			100		ppm/°C
Unit-to-Unit Variation	650nm		±5		%
Nonlinearity[1]	FS Output = 10V		0.01		% of FS
Photodiode Area	(0.090 x 0.090in)		0.008		in^2
	(2.29 x 2.29mm)		5.2		mm^2
DARK ERRORS, RTO[2]					
Offset Voltage, Output			±0.5	±2	mV
vs Temperature			±10		µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		10	100	µV/V
Voltage Noise	Measured BW = 0.1 to 100kHz		350		µVrms
RESISTOR—1MΩ Internal					
Resistance			1		MΩ
Tolerance			±0.5	±2	%
vs Temperature			50		ppm/°C
FREQUENCY RESPONSE					
Bandwidth, Large or Small-Signal, –3dB			16		kHz
Rise Time, 10% to 90%			22		µs
Settling Time, 1%	FS to Dark		60		µs
0.1%	FS to Dark		85		µs
0.01%	FS to Dark		100		µs
Overload Recovery Time (to 1%)	100% 0verdrive, V_S = ±15V		44		µs
	100% 0verdrive, V_S = ±5V		100		µs
	100% 0verdrive, V_S = ±2.25V		240		µs
OUTPUT					
Voltage Output	R_L = 10kΩ	(V+) – 1.25	(V+) – 1		V
	R_L = 5kΩ	(V+) – 2	(V+) – 1.5		V
Capacitive Load, Stable Operation			1		nF
Short-Circuit Current			±18		mA
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±2.25		±18	V
Quiescent Current	V_O = 0		±400	±500	µA
TEMPERATURE RANGE					
Specification, Operating		0		+70	°C
Storage		–25		+85	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

PHOTODIODE SPECIFICATIONS

T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	Photodiode of OPT209 MIN	TYP	MAX	UNITS
Photodiode Area	(0.090 x 0.090in)		0.008		in^2
	(2.29 x 2.29mm)		5.1		mm^2
Current Responsivity	650nm		0.45		A/W
Dark Current	V_D = 0V[1]		500		fA
vs Temperature			doubles every 10°C		
Capacitance	V_D = 0V[1]		600		pF

NOTE: (1) Voltage Across Photodiode.

SPECIFICATIONS (CONT)

ELECTRICAL

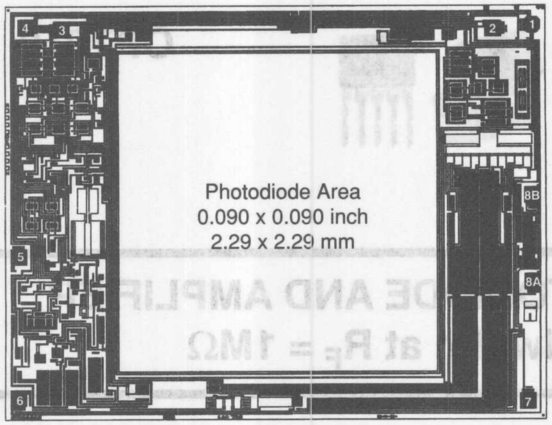
Op Amp Section of OPT209(1)

T_A = +25°C, V_S = ±15V, unless otherwise noted.

PARAMETER	CONDITIONS	OPT209 Op Amp MIN	TYP	MAX	UNITS
INPUT					
Offset Voltage			±0.5		mV
vs Temperature			±5		µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		10		µV/V
Input Bias Current			1		pA
vs Temperature			doubles every 10°C		
NOISE					
Input Voltage Noise					
Voltage Noise Density, f=10Hz			30		nV/√Hz
f=100Hz			25		nV/√Hz
f=1kHz			15		nV/√Hz
Current Noise Density, f=1kHz			0.8		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range			±14.4		V
Common-Mode Rejection			106		dB
INPUT IMPEDANCE					
Differential			10^{12}‖3		Ω‖pF
Common-Mode			10^{12}‖3		Ω‖pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain			120		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			4		MHz
Slew Rate			6		V/µs
Settling Time 0.1%			4		µs
0.01%			5		µs
OUTPUT					
Voltage Output	R_L = 10kΩ	(V+) – 1.25	(V+) – 1		V
	R_L = 5kΩ	(V+) – 2	(V+) – 1.5		V
Short-Circuit Current			±18		mA
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±2.25		±18	V
Quiescent Current	I_O = 0		±400	±500	µA

NOTE: (1) Op amp specifications provided for information and comparison only.

DICE INFORMATION



OPT209 DIE TOPOGRAPHY

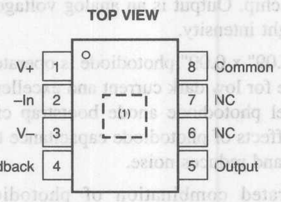
PAD	FUNCTION
1	V+
2	–In
3	V–
4	1MΩ Feedback
5	Output
6	NC
7	NC
8A, 8B	Common

NC: No Connection. Pads 8A and 8B must both be connected to common. Substrate Bias: The substrate is electrically connected to internal circuitry. Do not make electrical connection to the substrate.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	154 x 120 ±5	3.91 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATION



NOTE: (1) Photodiode location.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range (Common Pin)	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–25°C to +85°C
Storage Temperature	–25°C to +85°C
Junction Temperature	+85°C
Lead Temperature (soldering, 10s) (Vapor-Phase Soldering Not Recommended)	+300°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPT209P	8-Pin DIP	006-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

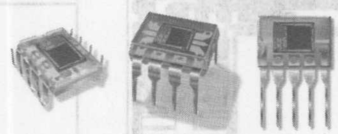
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

MOISTURE SENSITIVITY AND SOLDERING

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that devices be baked-out at 85°C for 24 hours.

The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT209 cannot meet flammability test, UL-94.

BURR - BROWN®



OPT210

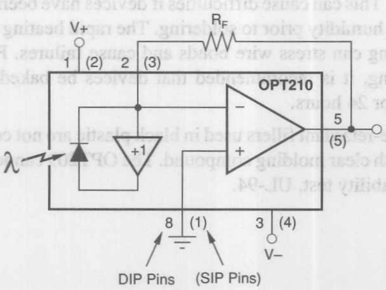
MONOLITHIC PHOTODIODE AND AMPLIFIER
300kHz Bandwidth at $R_F = 1M\Omega$

FEATURES

- BOOTSTRAP ANODE DRIVE:
  Extends Bandwidth: 900kHz ($R_F = 100K\Omega$)
  Reduces Noise
- LARGE PHOTODIODE: 0.09" x 0.09"
- HIGH RESPONSIVITY: 0.45A/W (650nm)
- EXCELLENT SPECTRAL RESPONSE
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- TRANSPARENT DIP, SIP AND SURFACE-MOUNT PACKAGES

APPLICATIONS

- BARCODE SCANNERS
- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY DETECTORS
- PARTICLE DETECTORS



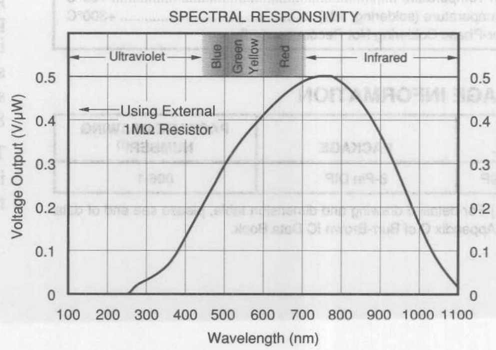
DESCRIPTION

The OPT210 is a photodetector consisting of a high performance silicon photodiode and precision FET-input transimpedance amplifier integrated on a single monolithic chip. Output is an analog voltage proportional to light intensity.

The large 0.09" x 0.09" photodiode is operated at low bias voltage for low dark current and excellent linearity. A novel photodiode anode bootstrap circuit reduces the effects of photodiode capacitance to extend bandwidth and reduces noise.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered with discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT210 operates from ±2.25 to ±18V supplies and quiescent current is only 2mA. Available in a transparent 8-pin DIP, 8-lead surface-mount and 5-pin SIP, it is specified for 0° to 70°C operation.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25°C$, $V_S = \pm15V$, $\lambda = 650nm$, External $R_F = 1M\Omega$, $R_L = 10k\Omega$, unless otherwise noted.

PARAMETER	CONDITIONS	OPT210P OPT210W MIN	TYP	MAX	UNITS
RESPONSIVITY					
Photodiode Current	$\lambda = 650nm$		0.45		A/W
Unit-to-Unit Variation			±5		%
Voltage Output	$\lambda = 650nm$, External $R_F = 1M\Omega$		0.45		V/µW
Nonlinearity			0.01		% of FS
Photodiode Area	(0.09 x 0.09in)		0.008		in²
	(2.29 x 2.29mm)		5.2		mm²
DARK ERROR, RTO					
Offset Voltage			±2	±10	mV
vs Temperature			±35		µV/°C
vs Power Supply	$V_S = \pm2.25V$ to $\pm18V$		100	1000	µV/V
Voltage Noise	BW = 0.01Hz to 100kHz		160		µVrms
FREQUENCY RESPONSE					
Bandwidth	External $R_F = 1M\Omega$		300		kHz
Rise Time	10% to 90%		1.2		µs
Settling Time, 1%	FS to Dark step		3		µs
0.1%			8		µs
0.01%			20		µs
Overload Recovery	100% Overdrive		7		µs
OUTPUT					
Voltage Output, Positive	$R_L = 10k\Omega$	(V+)–1.25	(V+)–0.75		V
Positive	$R_L = 5k\Omega$		(V+)–1		
Negative(1)	$R_L = 10k\Omega$	–0.4	–0.5		V
Capacitive Load, Stable Operation			500		pF
Short-Circuit Current(2)			+50		mA
POWER SUPPLY					
Operating Range		±2.25		±18	V
Quiescent Current			+2.0/–1.7	±4	mA
TEMPERATURE RANGE					
Specification		0		70	°C
Operating		0		70	°C
Storage		–25		85	°C
θ_{JA}			100		°C/W

NOTES: (1) Output typically swings to 0.5V below the voltage applied to the non-inverting input terminal, which is normally connected to ground. (2) Positive current (sourcing) is limited. Negative current (sinking) is not limited.

PHOTODIODE SPECIFICATIONS

PARAMETER	CONDITIONS	PHOTODIODE MIN	TYP	MAX	UNITS
Photodiode Area	(0.09 x 0.09in)		0.008		in²
	(2.29 x 2.29mm)		5.2		mm²
Current Responsivity	$\lambda = 650nm$		0.45		A/W
			865		µA/W/cm²
Dark Current	$V_D = -1.2V$		70		pA
vs Temperature			Doubles every 10°C		
Capacitance	$V_D = -1.2V$		550		pF
Effective Capacitance(1)	$V_D = -1.2V$		10		pF

NOTES: (1) Effect of photodiode capacitance is reduced by internal buffer bootstrap drive. See text

OP AMP SPECIFICATIONS

Op amp specifications provided for comparative information only.

PARAMETER	CONDITIONS	OP AMP MIN	OP AMP TYP	OP AMP MAX	UNITS
INPUT					
Offset Voltage			±2		mV
vs Temperature			±35		µV/°C
vs Power Supply			100		µV/V
Input Bias Current					
Inverting Input			15		pA
vs Temperature			Doubles every 10°C		
Non-inverting Input			300		µA
NOISE					
Voltage Noise					
f = 10Hz			20		nV/√Hz
f = 100Hz			9		nV/√Hz
f = 1kHz			6		nV/√Hz
Current Noise Density, Inverting Input	BW = 0.01Hz to 100kHz		0.8		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range(1)			V_S±2.25		V
Common-Mode Rejection			65		dB
INPUT IMPEDANCE					
Inverting Input Impedance			3×10^{10}‖3		Ω ‖ pF
Non-Inverting Input Impedance			250		kΩ
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = 0V to +13.75V		70		dB
FREQUENCY RESPONSE					
Bandwidth, Small Signal			35		MHz
Rise Time, Large Signal	10% to 90%		25		ns
Settling Time, 1%	10V step		240		ns
0.1%			390		ns
0.01%			800		ns
Overload Recovery	100% Overdrive		7		µs
OUTPUT					
Voltage Output, Positive	R_L = 10kΩ	(V+)–1.25	(V+)–0.75		V
Positive	R_L = 5kΩ		(V+)–1		
Negative(1)	R_L = 10kΩ	–0.4	–0.5		V
Capacitive Load, Stable Operation			500		pF
Short-Circuit Current(2)			+50		mA
POWER SUPPLY					
Operating Voltage		±2.25		±18	V
Quiescent Current			+1.7/–1.4	±4	mA

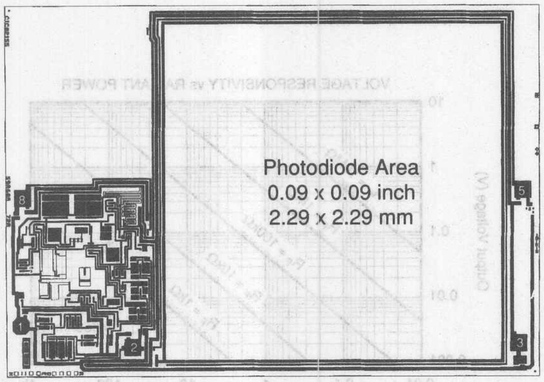
NOTES: (1) Output typically swings to 0.5V below the voltage applied to the non-inverting input terminal, which is normally connected to ground. (2) Positive current (sourcing) is limited. Negative current (sinking) is not limited.

BUFFER SPECIFICATIONS

Buffer specifications provided for comparative information only.

PARAMETER	CONDITIONS	BUFFER MIN	BUFFER TYP	BUFFER MAX	UNITS
INPUT					
Offset Voltage(1)			–1.2		V
Input Bias Current			15		pA
vs Temperature			Doubles every 10°C		
Input Impedance			10^{11}‖3		Ω ‖ pF
FREQUENCY RESPONSE					
Bandwidth, Small Signal			500		MHz
OUTPUT					
Current			±200		µA
Voltage Gain			0.99		V/V
POWER SUPPLY					
Operating Range		±2.25		±18	V
Quiescent Current			±0.3		mA

NOTE: (1) Intentional voltage offset to reverse bias photodiode.



OPT210 DIE TOPOGRAPHY

PAD	FUNCTION
1	V+
2	–In
3	V–
5	Output
8	Common

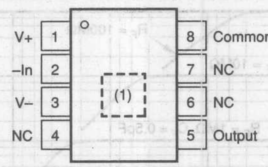
Substrate Bias: The substrate is electrically connected to internal circuitry. Do not make electrical connection to the substrate.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	148 x 104 ±5	3.76 x 2.64 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

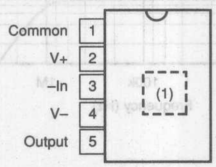
PIN CONFIGURATIONS

Top View — DIP



NOTE: (1) Photodiode location.

Top View — SIP



NOTE: (1) Photodiode location.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range (Common Pin)	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature: P, W	–25°C to +85°C
Storage Temperature: P, W	–25°C to +85°C
Junction Temperature: P, W	+85°C
Lead Temperature (soldering, 10s)	+300°C
(Vapor-Phase Soldering Not Recommended on Plastic Packages)	

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPT210P	8-Pin Plastic DIP	006-5
OPT210P-J	8-Lead Surface Mount(2)	006-6
OPT210W	5-Pin Plastic SIP	321-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) 8-pin DIP with leads formed for surface mounting.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

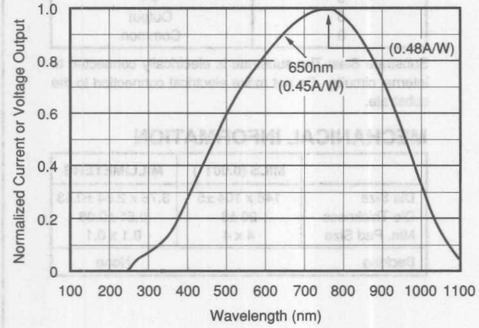
MOISTURE SENSITIVITY AND SOLDERING

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that plastic devices be baked-out at 85°C for 24 hours.

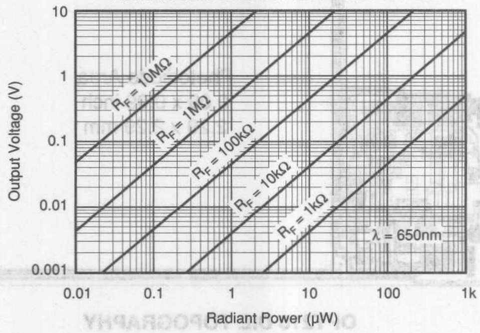
The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT210 plastic packages cannot meet flammability test, UL-94.

At T_A = +25°C, V_S = ±15V, λ = 650nm, unless otherwise noted.

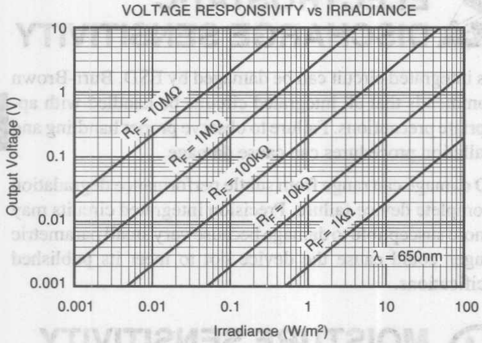
NORMALIZED SPECTRAL RESPONSIVITY



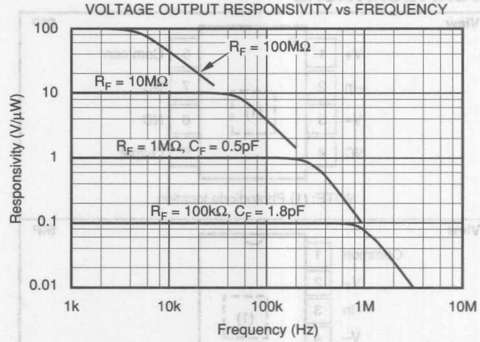
VOLTAGE RESPONSIVITY vs RADIANT POWER



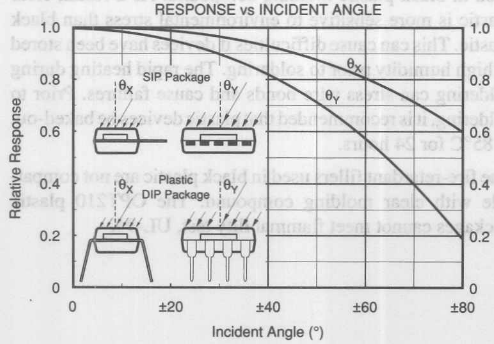
VOLTAGE RESPONSIVITY vs IRRADIANCE



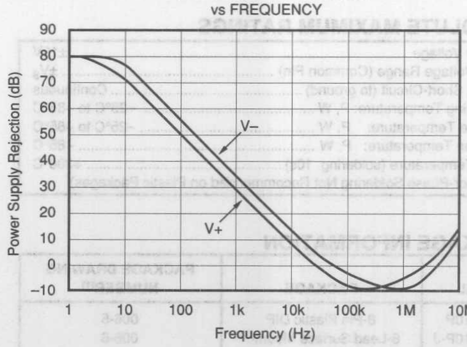
VOLTAGE OUTPUT RESPONSIVITY vs FREQUENCY



RESPONSE vs INCIDENT ANGLE

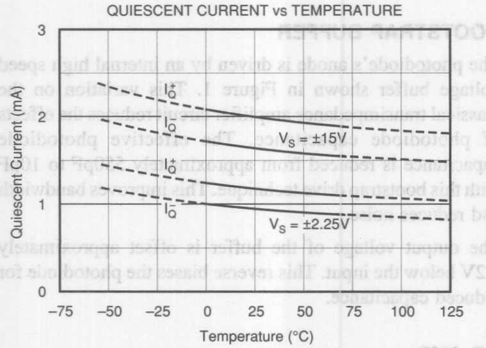


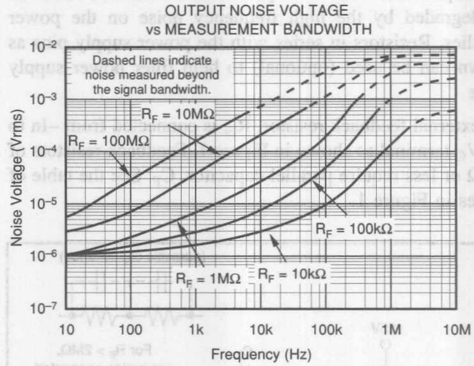
POWER SUPPLY REJECTION vs FREQUENCY

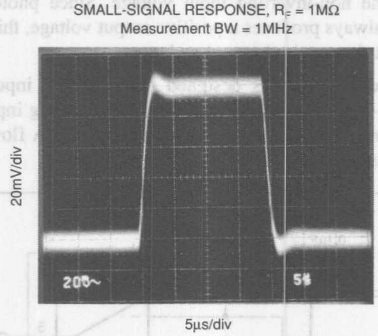


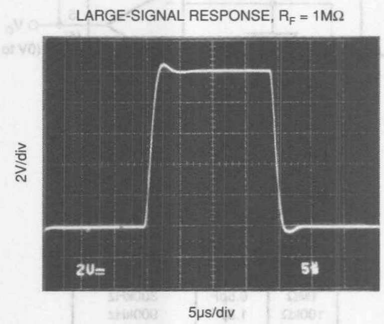
TYPICAL PERFORMANCE CURVES (CONT)

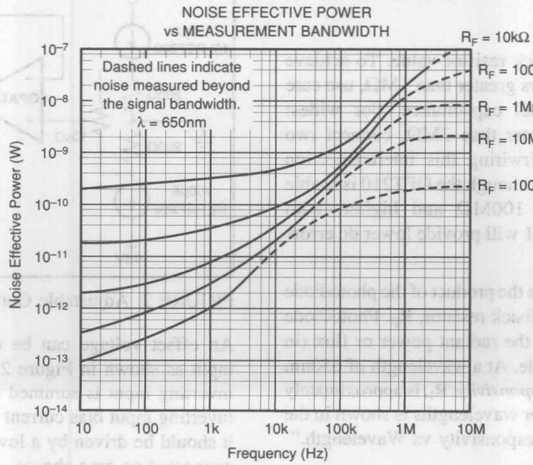
At T_A = +25°C, V_S = ±15V, λ = 650nm, unless otherwise noted.







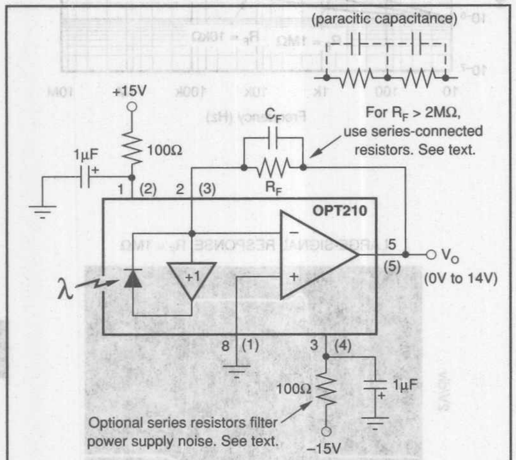




APPLICATIONS INFORMATION

Basic operation of the OPT210 is shown in Figure 1. Power supply bypass capacitors should be connected near the device pins as shown. Noise performance of the OPT210 can be degraded by the high frequency noise on the power supplies. Resistors in series with the power supply pins as shown can be used (optional) to help filter power supply noise

An external feedback resistor, R_F, is connected from –In to the V_O terminal as shown in Figure 1. Feedback resistors of 1MΩ or less require parallel capacitor, C_F. See the table of values in Figure 1.



R_F	C_F (min)	BANDWIDTH
10MΩ	(1)	70kHz
1MΩ	0.5pF	300kHz
100kΩ	1.8pF	900kHz
10kΩ	10pF	1.6MHz
1kΩ	20pF	1.6MHz

NOTE: (1) Two series-connected resistors of $R_F/2$ for low capacitance. See text.

FIGURE 1. Basic Operation.

Bandwidth varies with feedback resistor value. To achieve widest bandwidth with resistors greater than 1MΩ, use care to minimize parasitic parallel capacitance. For widest bandwidth with resistors greater than 2MΩ, connect two resistors ($R_F/2$) in series. Airwiring this interconnection provides lowest capacitance. Although the OPT210 is usable with feedback resistors of 100MΩ and higher, with $R_F \geq 10M\Omega$ the model OPT211 will provide lower dc errors and reduced noise.

The OPT210's output voltage is the product of the photodiode current times the external feedback resistor, R_F. Photodiode current, I_D, is proportional to the radiant power or flux (in watts) falling on the photodiode. At a wavelength of 650nm (visible red) the photodiode *Responsivity*, R_I, is approximately 0.45A/W. Responsivity at other wavelengths is shown in the typical performance curve "Responsivity vs Wavelength."

The typical performance curve "Output Voltage vs Radiant Power" shows the response throughout a wide range of radiant power and feedback resistor values. The response curve "Output Voltage vs Irradiance" is based on the photodiode area of $5.23x10^{-6}m^2$.

BOOTSTRAP BUFFER

The photodiode's anode is driven by an internal high speed voltage buffer shown in Figure 1. This variation on the classical transimpedance amplifier circuit reduces the effects of photodiode capacitance. The effective photodiode capacitance is reduced from approximately 550pF to 10pF with this bootstrap drive technique. This improves bandwidth and reduces noise.

The output voltage of the buffer is offset approximately 1.2V below the input. This reverse biases the photodiode for reduced capacitance.

OP AMP

A special op amp design is used to achieve wide bandwidth. The op amp output voltage cannot swing lower than 0.5V below the non-inverting input voltage. Since photodiode current always produces a positive output voltage, this does not limit the required output swing.

The inverting input is designed for very low input bias current—approximately 15pA. The non-inverting input has much larger bias current—approximately 300µA flows out of this terminal.

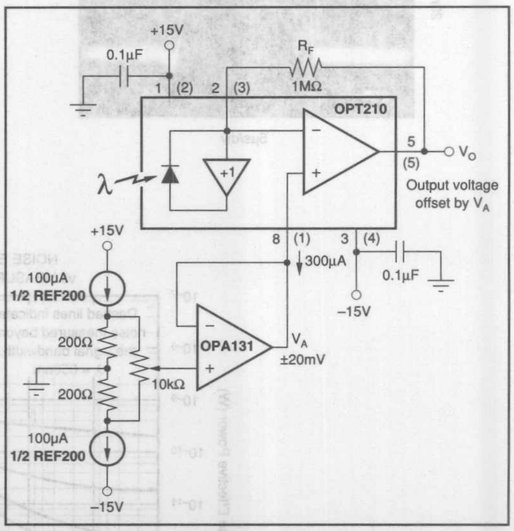


FIGURE 2. Adjustable Output Offset.

An offset voltage can be connected to the non-inverting input as shown in Figure 2. A voltage applied to the non-inverting input is summed at the output. Because the non-inverting input bias current is high (approximately 300µA), it should be driven by a low impedance such as the buffer-connected op amp shown.

The OPT210 can be connected to operate from a single power supply as shown in Figure 3. The non-inverting input bias current flows through a zener diode to provide a bias voltage. The output voltage is referenced to this bias point.

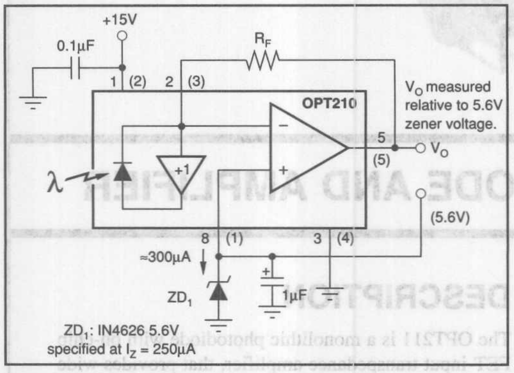


FIGURE 3. Single Power Supply Operation.

DARK ERRORS

The dark errors in the specification table include all sources with R_F = 1MΩ. The dominant error source is the input offset voltage of the op amp. Photodiode dark current is approximately 70pA and the combined input bias current of the op amp and buffer is approximately 30pA. Photodiode dark current and input bias current total approximately 100pA at 25°C and double for each 10°C above 25°C. At 70°C, the total error current is approximately 2nA. With R_F = 1MΩ, this would produce a 2mV offset voltage in addition to the initial amplifier offset voltage (10mV max) at 25°C. The dark output voltage can be trimmed to zero with the optional circuit shown in Figure 2.

LIGHT SOURCE POSITIONING

The OPT210 is tested with a light source that uniformly illuminates the full integrated circuit area, including the op amp. Although all IC amplifiers are light sensitive to some degree, the OPT210 op amp circuitry is designed to minimize this effect. Sensitive junctions are shielded with metal where possible. Furthermore, the photodiode area is very large compared to the op amp circuitry making these effects negligible.

If your light source is focused to a small area, be sure that it is properly aimed to fall on the photodiode. If a narrowly focused light source were to miss the photodiode and fall on the op amp circuitry, the OPT210 would not perform properly. The large photodiode area is clearly visible as a very dark area slightly offset from the center of the IC.

The incident angle of the light source also affects the apparent sensitivity in uniform irradiance. For small incident angles, the loss in sensitivity is due to the smaller effective light gathering area of the photodiode (proportional to the cosine of the incident angle). At a greater incident angle, light is diffused by the side of the package. These effects are shown in the typical performance curve, "Response vs Incident Angle."

LINEARITY PERFORMANCE

Photodiode current is very linear with radiant power throughout its range. Nonlinearity remains below approximately 0.01% up to 200μA. The anode buffer drive, however, is limited to approximately 200μA. This produces an abrupt limit to photodiode output current when radiant power reaches approximately 450μW.

Best linearity is achieved with the photodiode uniformly illuminated. A light source focused to a very small beam, illuminating only a small percentage of the photodiode area, may produce a higher nonlinearity.

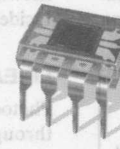
NOISE PERFORMANCE

Noise performance of the OPT210 is determined by the op amp characteristics in conjunction with the feedback components, photodiode capacitance, and buffer performance. The typical performance curve "Output Noise Voltage vs Measurement Bandwidth" shows how the noise varies with R_F and measured bandwidth (0.1Hz to the indicated frequency). The signal bandwidth of the OPT210 is indicated on the curves. Noise can be reduced by filtering the output with a cutoff frequency equal to the signal bandwidth.

Output noise increases in proportion to the square-root of the feedback resistance, while responsivity increases linearly with feedback resistance. So best signal-to-noise ratio is achieved with large feedback resistance. This comes with the trade-off of decreased bandwidth.

The noise performance of a photodetector is sometimes characterized by *Noise Effective Power* (NEP). This is the radiant power which would produce an output signal equal to the noise level. NEP has the units of radiant power (watts), or Watts/$\sqrt{\text{Hz}}$ to convey spectral information about the noise. The typical performance curve "Output Noise Voltage vs Measurement Bandwidth" is also scaled for NEP on the right-hand side.

BURR - BROWN®



OPT211

MONOLITHIC PHOTODIODE AND AMPLIFIER

FEATURES

- **WIDE BANDWIDTH, HIGH RESPONSIVITY:**

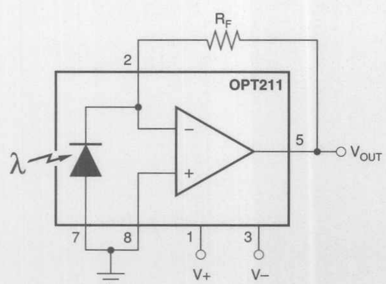
R_F	BANDWIDTH	
1MΩ	50kHz	*150kHz
100MΩ	5kHz	*13kHz

*with bootstrap buffer

- **PHOTODIODE SIZE: 0.090 x 0.090 inch (2.29 x 2.29mm)**
- **HIGH RESPONSIVITY: 0.45A/W (650nm)**
- **LOW DARK ERRORS: 2mV max**
- **EXCELLENT SPECTRAL RESPONSE**
- **LOW QUIESCENT CURRENT: 400µA**
- **TRANSPARENT 8-PIN DIP**

APPLICATIONS

- **MEDICAL INSTRUMENTATION**
- **LABORATORY INSTRUMENTATION**
- **POSITION AND PROXIMITY SENSORS**
- **PHOTOGRAPHIC ANALYZERS**
- **BARCODE SCANNERS**
- **SMOKE DETECTORS**

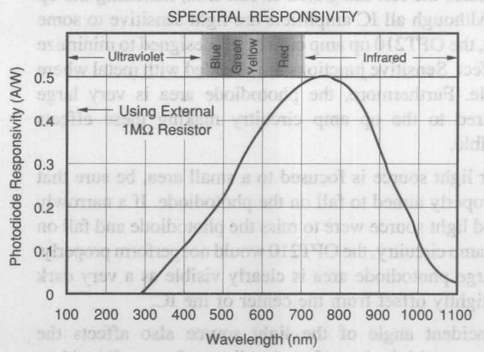


DESCRIPTION

The OPT211 is a monolithic photodiode with on-chip FET-input transpedance amplifier, that provides wide bandwidth at very high gains. Uncommitted input and feedback nodes allow a variety of feedback options for maximum versatility. Trade-offs in responsivity (gain), bandwidth and SNR can easily be made.

The monolithic combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pickup and gain peaking due to stray capacitance. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current. Direct access to the detector's anode allows photodiode bootstrapping, which increases speed performance.

The OPT211 operates over a wide supply range (±2.25V to ±18V) and supply current is only 400µA. It is packaged in a transparent plastic 8-pin DIP specified for the 0°C to 70°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

T_A = +25°C, V_S = ±15V, λ = 650nm, external 1MΩ feedback resistor, circuit shown in Figure 1, unless otherwise noted.

PARAMETER	CONDITIONS	OPT211P MIN	TYP	MAX	UNITS
RESPONSIVITY					
Photodiode Current	650nm		0.45		A/W
Unit-to-Unit Variation	650nm		±5		%
Voltage Output	λ = 650nm, R_F = 1MΩ		0.45		V/μW
Nonlinearity			0.01		% of FS
Photodiode Area	(0.090 x 0.090 inches)		0.008		in²
	(2.29 x 2.29mm)		5.2		mm²
DARK ERRORS, RTO(1)					
Offset Voltage, Output			±0.5	±2	mV
vs Temperature			±10		μV/°C
vs Power Supply	V_S = ±2.25V to ±18V		10	100	μV/V
Voltage Noise, Dark	Dark, f_B = 0.1Hz to 100kHz		1		mVrms
FREQUENCY RESPONSE					
Bandwidth	Anode Grounded(2)		50		kHz
	Anode Bootstrapped(3)		150		kHz
Rise Time, 10% to 90%, R_F = 1MΩ	Anode Grounded(2)		5		μs
	Anode Bootstrapped(3)		2		μs
Settling Time, FS to Dark	Anode Grounded(2)				
1%			10		μs
0.1%			25		μs
0.01%			30		μs
100% Overload Recovery Time	FS to Dark (to 1%)		44		μs
	V_S = ±5V		100		μs
	V_S = ±2.25V		240		μs
OUTPUT					
Voltage Output	R_L = 10kΩ	(V+) – 1.25	(V+) – 1		V
	R_L = 5kΩ	(V+) – 2	(V+) – 1.5		V
Capacitive Load, Stable Operation(4)			250		pF
Short-Circuit Current			±18		mA
POWER SUPPLY					
Operating Voltage Range		±2.25	±15	±18	V
Quiescent Current	V_{OUT} = 0V		±400	±500	μA
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		0		+70	°C
Storage		–25		+85	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTES: (1) Referred to Output. Includes all error sources. (2) See Figure 1. (3) See Figure 3. (4) See Figure 2.

PHOTODIODE SPECIFICATIONS

T_A = +25°C, λ = 650nm, unless otherwise noted.

PARAMETER	CONDITIONS	Photodiode of OPT211 MIN	TYP	MAX	UNITS
Photodiode Area	(0.090 x 0.090 inches)		0.008		in²
	(2.29 x 2.29mm)		5.2		mm²
Current Responsivity	λ = 650nm		0.45		A/W
			865		μA/W/cm²
Dark Current	V_D = 0V		500		fA
vs Temperature			doubles every 10°C		
Capacitance	V_D = 0V		600		pF

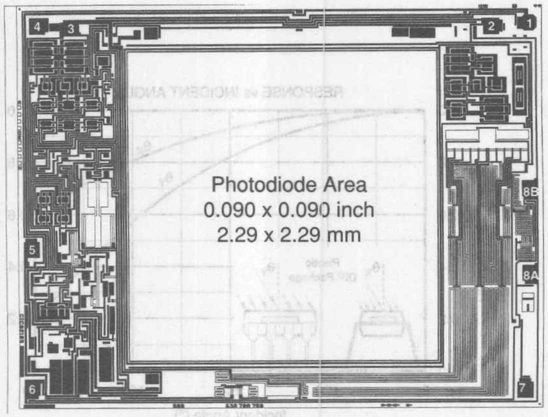
OP AMP SPECIFICATIONS

T_A = +25°C, V_S = ±15V, R_L = 10kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	OPT211 Op Amp(1) MIN	TYP	MAX	UNITS
INPUT					
Offset Voltage			±0.5		mV
vs Temperature			±5		µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		10		µV/V
Input Bias Current			±1		pA
vs Temperature			doubles every 10°C		
Input Impedance					
Differential			10^{12} ‖ 3		Ω ‖ pF
Common-Mode			10^{12} ‖ 3		Ω ‖ pF
Common-Mode Input Voltage Range	Linear Operation		±14.4		V
Common-Mode Rejection			106		dB
NOISE					
Voltage Noise Density	f = 10Hz		30		nV/√Hz
	f = 100Hz		25		nV/√Hz
	f = 1kHz		15		nV/√Hz
Current Noise Density	f = 1kHz		0.8		fA/√Hz
OPEN-LOOP GAIN					
Open-Loop Voltage Gain			120		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product(2)			16		MHz
Slew Rate			6		V/µs
Settling Time 0.1%			4		µs
0.01%			5		µs
OUTPUT					
Voltage Output	R_L = 10kΩ	(V+) – 1.25	(V+) – 1		V
	R_L = 5kΩ	(V+) – 2	(V+) – 1.5		V
Short-Circuit Current			±18		mA
POWER SUPPLY					
Operating Voltage Range		±2.25	±15	±18	V
Quiescent Current	I_O = 0mA		±400	±500	µA

NOTES: (1) Op amp specifications provided for information and comparison only. (2) Stable in gains ≥ 20V/V.

DICE INFORMATION



OPT211 DIE TOPOGRAPHY

PAD	FUNCTION
1	V+
2	–In
3	V–
4	NC
5	V_{OUT}
6	NC
7	PD Anode
8A, 8B	Common

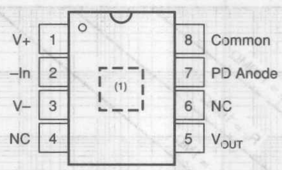
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	154 x 120	3.91 x 3.05
Die Thickness	18	0.46
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATIONS

Top View DIP



NOTE: (1) Photodiode location.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–25°C to +85°C
Storage Temperature	–25°C to +85°C
Junction Temperature	+85°C
Lead Temperature (soldering, 10s)	+300°C
(Vapor-Phase Soldering Not Recommended)	

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPT211P	8-Pin DIP	006-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

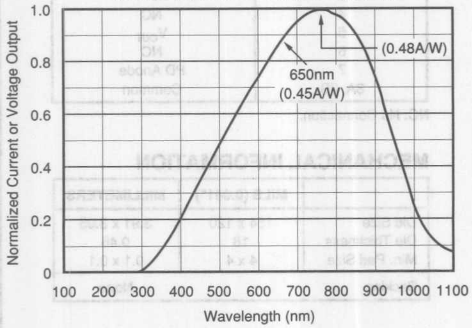
MOISTURE SENSITIVITY AND SOLDERING

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that plastic devices be baked-out at +85°C for 24 hours.

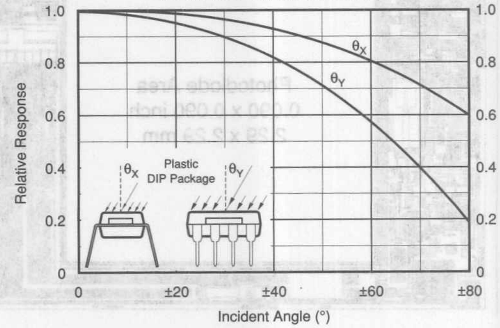
The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT211 plastic packages cannot meet flammability test, UL-94.

... external 1MΩ feedback resistor, circuit shown in Figure 1, unless otherwise noted.

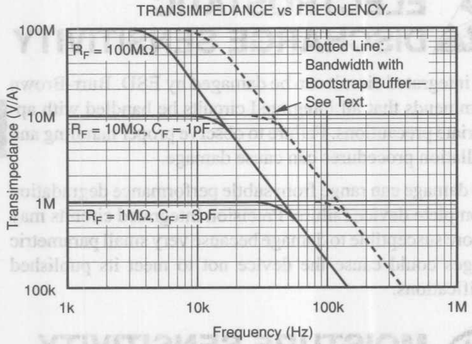
NORMALIZED SPECTRAL RESPONSIVITY



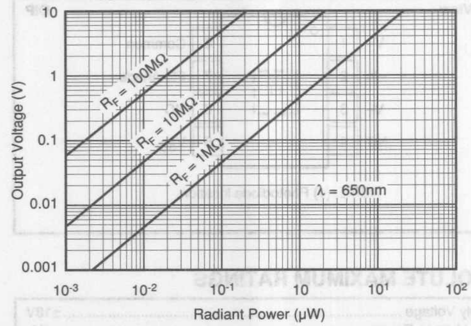
RESPONSE vs INCIDENT ANGLE



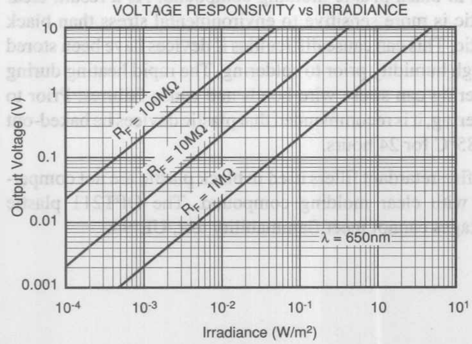
TRANSIMPEDANCE vs FREQUENCY



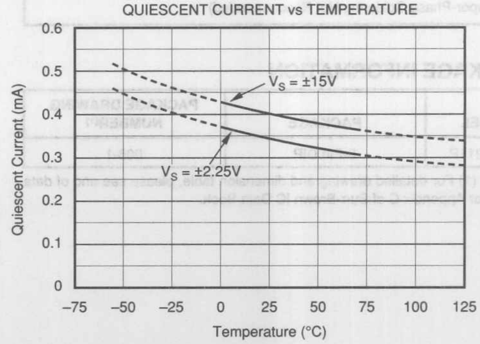
VOLTAGE RESPONSIVITY vs RADIANT POWER



VOLTAGE RESPONSIVITY vs IRRADIANCE



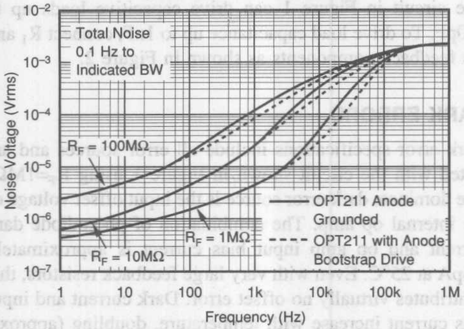
QUIESCENT CURRENT vs TEMPERATURE



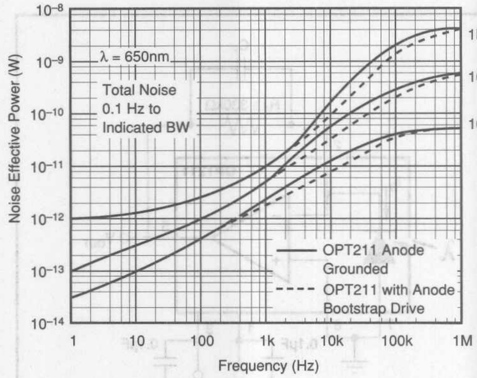
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm15V$, λ = 650nm, external 1MΩ feedback resistor, circuit shown in Figure 1, unless otherwise noted.

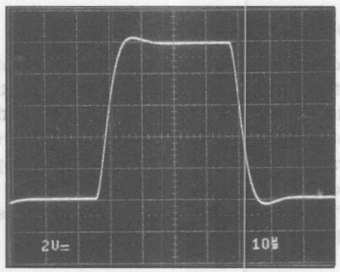
OUTPUT NOISE VOLTAGE vs MEASUREMENT BANDWIDTH



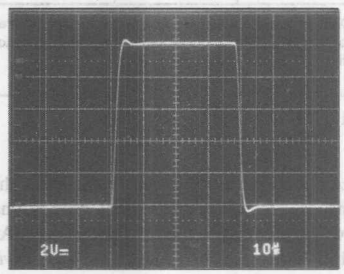
NOISE EFFECTIVE POWER vs MEASUREMENT BANDWIDTH



STEP RESPONSE
R_F = 1MΩ, Anode Grounded

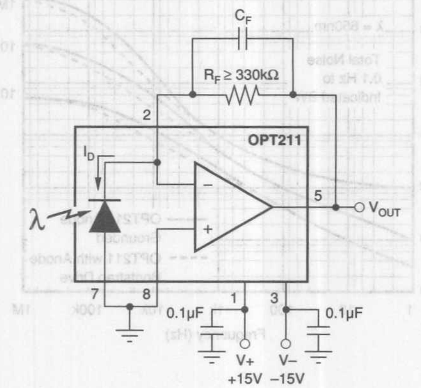


STEP RESPONSE
R_F = 1MΩ, Bootstrap Buffer



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required to operate the OPT211. Applications with high impedance power supplies may require decoupling capacitors located close to the device pins as shown in Figure 1.



R_F (Ω)	C_F (pF)	BANDWIDTH (kHz)
330k	5.6	86
1M	3	50
10M	1(1)	16
100M	0.3(1)	5

NOTE: (1) Feedback resistor has approximately 1pF stray capacitance. C_F<1pF requires series-connected feedback resistors. See text.

FIGURE 1. Basic Circuit Connections.

Output is zero volts with no light and increases with increasing illumination. Photodiode current is proportional to the radiant power (watts) falling in the photodiode. At 650nm wavelength (visible red) the photodiode *responsivity* is approximately 0.45A/W. Responsivity at other wavelengths is shown in the typical performance curve "Responsivity vs Wavelength."

The OPT211's output voltage is the product of the photodiode current and feedback resistor, (I_DR_F). The feedback resistor must be greater than 330kΩ for proper stability. A feedback capacitor, C_F, must be connected as shown. Recommended values are shown in Figure 1. Capacitor values for other feedback resistances can be interpolated.

The OPT211 provides excellent performance with very high feedback resistor values. To achieve maximum bandwidth with $R_F \geq 10M\Omega$, good circuit layout is required. With careful circuit board layout and a 10MΩ feedback resistor, stray capacitance will provide approximately the correct parallel capacitance for stable operation and widest bandwidth. For larger feedback resistor values, two resistors connected in series and laid-out end-to-end will reduce the stray capacitance to a few tenths of a picofarad. With experimentation, circuit board traces can be used to produce the necessary stray capacitance for proper compensation and widest possible bandwidth.

The circuit in Figure 1 can drive capacitive loads up to 250pF. To drive load capacitance up to 1nF, connect R_1 and the feedback components as shown in Figure 2.

DARK ERRORS

Dark error specifications include all error sources and are tested with the circuit shown in Figure 1 using R_F=1MΩ. The dominate dark error source is the input offset voltage of the internal op amp. The combination of photodiode dark current and op amp input bias current is approximately 1.5pA at 25°C. Even with very large feedback resistors, this contributes virtually no offset error. Dark current and input bias current increase with temperature, doubling (approximately) for each 10°C increase. At 70°C, dark current is approximately 35pA. This would produce 3.5mV offset with a 100MΩ feedback resistor.

Circuit board leakage currents can increase dark error. Use clean assembly procedures to avoid contamination, particularly around the sensitive inverting input node (pin 2). Errors due to leakage current from the V+ supply (pin 1) can be eliminated by encircling the trace connecting to pin 2 with a guard trace connected to ground.

IMPROVING BANDWIDTH

Bandwidth of the OPT211 can be increased with the feedback buffer circuits shown in Figure 3. Driving the anode of the photodiode (pin 7) in this manner reduces the effect of the photodiode's capacitance on signal bandwidth. This "bootstrap drive" circuit boosts bandwidth by approximately 3x. Bandwidth achieved with various R_F values is shown in Figure 2. When using a bootstrap buffer, R_F must be greater or equal to 1MΩ for stable operation.

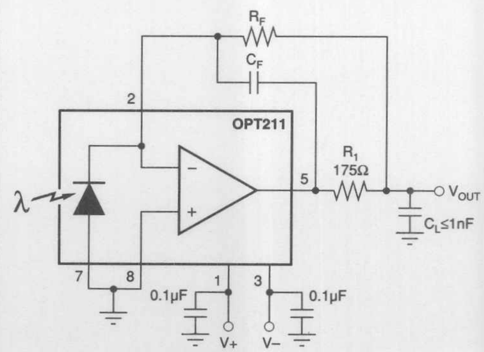
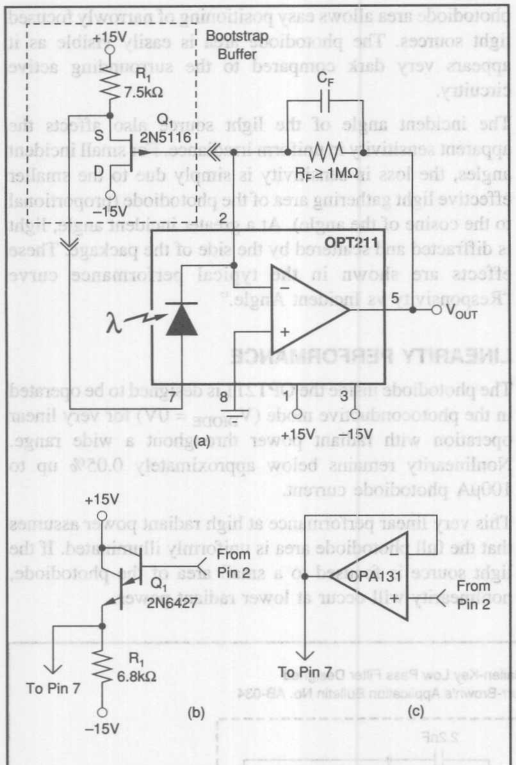


FIGURE 2. Increasing C-Load Drive.



R_F (Ω)	C_F (pF)	Bandwidth (kHz)
330k	Not Recommended	
1M	1(1)	150
10M	<0.2(1)	42
100M	<0.2(1)	13

NOTE: (1) Most resistors have approximately 1pF stray capacitance. C_F<1pF requires series-connected feedback resistors. See text.

FIGURE 3. Increasing Bandwidth with Bootstrap Buffer.

Gate or base current of the buffer transistor flows through the feedback resistor, increasing the dark offset voltage. If dark errors are important, use a FET transistor with picoamp gate current. A P-channel FET is used to assure that the anode is at ground potential or slightly negative.

If dark errors are not critical, an NPN Darlington transistor can be used for a buffer as shown in Figure 3b. A FET-input op amp connected as a buffer can be used as shown in Figure 3c, but its noise may degrade circuit performance slightly. Bandwidth of the buffer should be 4MHz, minimum.

AC COUPLING

Some applications are concerned only with sensing variation in light intensity. Simple capacitive coupling at the OPT211's output may be adequate. With large feedback resistors or bright ambient light, however, the OPT211's output may saturate. The circuit in Figure 4 can reject very bright ambient light, yet provide high AC gain for best signal-to-noise ratio. The output voltage is integrated and fed back to the inverting input through R_3. This drives the average (dc) voltage at the output to zero. Application Bulletin AB-061 provides more details on this technique.

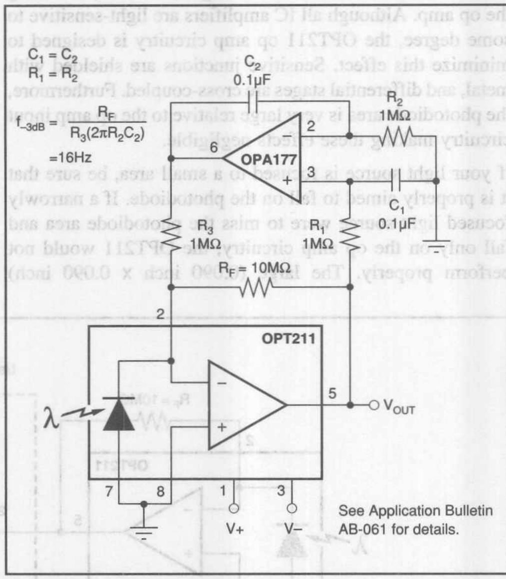


FIGURE 4. Rejecting Ambient Light.

This circuit also corrects output offset produced by input bias current of a buffer used to extend bandwidth. A Darlington transistor can be used for a bandwidth-enhancing bootstrap buffer in this circuit without creating offset error.

NOISE PERFORMANCE

Noise performance of the OPT211 is shown in typical curves for various feedback resistor values. This curve specifies the total noise measured from 0.1Hz to the indicated bandwidth. High frequency noise is reduced with the bootstrap transistor buffer circuits shown in Figure 1. This effect is shown on the typical curve.

Output noise of the OPT211 extends beyond the signal bandwidth, especially for high feedback resistor values. Signal-to-noise ratio can be improved by filtering the OPT211's output to a bandwidth equal to the signal bandwidth—see Figure 5.

decreased bandwidth.

The noise performance of a photodetector is sometimes characterized by its *noise effective power* (NEP). This is the radiant power which would produce an output signal equal to the output noise level. NEP has the units of radiant power (W). A NEP curve is provided.

LIGHT SOURCE POSITIONING

The OPT211 is 100% tested with a light source that uniformly illuminates the full area of the integrated circuit, including the op amp. Although all IC amplifiers are light-sensitive to some degree, the OPT211 op amp circuitry is designed to minimize this effect. Sensitive junctions are shielded with metal, and differential stages are cross-coupled. Furthermore, the photodiode area is very large relative to the op amp input circuitry making these effects negligible.

If your light source is focused to a small area, be sure that it is properly aimed to fall on the photodiode. If a narrowly focused light source were to miss the photodiode area and fall only on the op amp circuitry, the OPT211 would not perform properly. The large (0.090 inch x 0.090 inch) light sources. The photodiode area is easily visible as it appears very dark compared to the surrounding active circuitry.

The incident angle of the light source also affects the apparent sensitivity in uniform irradiance. For small incident angles, the loss in sensitivity is simply due to the smaller effective light gathering area of the photodiode (proportional to the cosine of the angle). At a greater incident angle, light is diffracted and scattered by the side of the package. These effects are shown in the typical performance curve "Responsivity vs Incident Angle."

LINEARITY PERFORMANCE

The photodiode inside the OPT211 is designed to be operated in the photoconductive mode (V_{DIODE} = 0V) for very linear operation with radiant power throughout a wide range. Nonlinearity remains below approximately 0.05% up to 100μA photodiode current.

This very linear performance at high radiant power assumes that the full photodiode area is uniformly illuminated. If the light source is focused to a small area of the photodiode, nonlinearity will occur at lower radiant power.

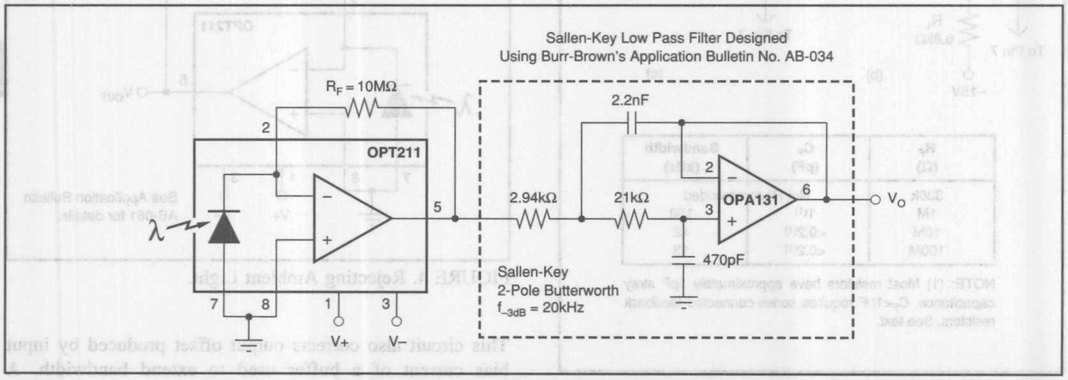


FIGURE 5. Low Pass Filter for Improved Signal-to-Noise Ratio.

OPT301

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11228

INTEGRATED PHOTODIODE AND AMPLIFIER

FEATURES

- PHOTODIODE SIZE: 0.090 x 0.090 inch (2.29 x 2.29mm)
- 1MΩ FEEDBACK RESISTOR
- HIGH RESPONSIVITY: 0.47A/W (650nm)
- IMPROVED UV RESPONSE
- LOW DARK ERRORS: 2mV
- BANDWIDTH: 4kHz
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 400µA
- HERMETIC TO-99

APPLICATIONS

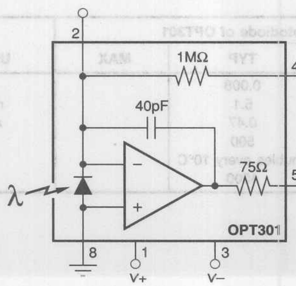
- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- SMOKE DETECTORS

DESCRIPTION

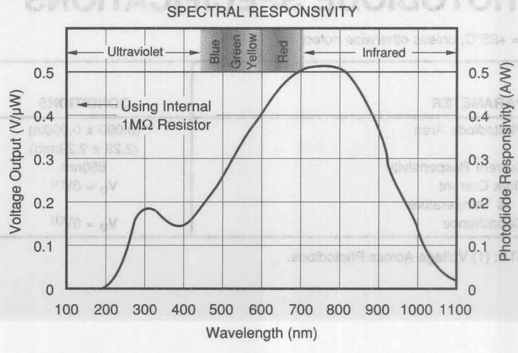
The OPT301 is an opto-electronic integrated circuit containing a photodiode and transimpedance amplifier on a single dielectrically isolated chip. The transimpedance amplifier consists of a precision FET-input op amp and an on-chip metal film resistor. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT301 operates over a wide supply range (±2.25 to ±18V) and supply current is only 400µA. It is packaged in a hermetic TO-99 metal package with a glass window, and is specified for the –40°C to 85°C temperature range.



SPECTRAL RESPONSIVITY



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V, λ = 650nm, internal 1MΩ feedback resistor, unless otherwise noted.

PARAMETER	CONDITIONS	OPT301M MIN	OPT301M TYP	OPT301M MAX	UNITS
RESPONSIVITY					
Photodiode Current	650nm		0.47		A/W
Voltage Output	650nm		0.47		V/μW
vs Temperature			200		ppm/°C
Unit-to-Unit Variation	650nm		±5		%
Nonlinearity(1)	FS Output = 10V		0.01		% of FS
Photodiode Area	(0.090 x 0.090in)		0.008		in²
	(2.29 x 2.29mm)		5.2		mm²
DARK ERRORS, RTO(2)					
Offset Voltage, Output			±0.5	±2	mV
vs Temperature			±10		μV/°C
vs Power Supply	V_S = ±2.25V to ±18V		10	100	μV/V
Voltage Noise	Measured BW = 0.1 to 100kHz		160		μVrms
RESISTOR—1MΩ Internal					
Resistance			1		MΩ
Tolerance			±0.5	±2	%
vs Temperature			50		ppm/°C
FREQUENCY RESPONSE					
Bandwidth, Large or Small-Signal, –3dB			4		kHz
Rise Time, 10% to 90%			90		μs
Settling Time, 1%	FS to Dark		240		μs
0.1%	FS to Dark		350		μs
0.01%	FS to Dark		900		μs
Overload Recovery Time	100% overdrive, V_S = ±15V		240		μs
	100% overdrive, V_S = ±5V		500		μs
	100% overdrive, V_S = ±2.25V		1000		μs
OUTPUT					
Voltage Output	R_L = 10kΩ	(V+) – 1.25	(V+) – 0.65		V
	R_L = 5kΩ	(V+) – 2	(V+) – 1		V
Capacitive Load, Stable Operation			10		nF
Short-Circuit Current			±18		mA
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±2.25		±18	V
Quiescent Current	I_O = 0		±0.4	±0.5	mA
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operating/Storage		–55		+125	°C
Thermal Resistance, θ_{JA}			200		°C/W

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

PHOTODIODE SPECIFICATIONS

T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	Photodiode of OPT301 MIN	Photodiode of OPT301 TYP	Photodiode of OPT301 MAX	UNITS
Photodiode Area	(0.090 x 0.090in)		0.008		in²
	(2.29 x 2.29mm)		5.1		mm²
Current Responsivity	650nm		0.47		A/W
Dark Current	V_D = 0V(1)		500		fA
vs Temperature			doubles every 10°C		
Capacitance	V_D = 0V(1)		4000		pF

NOTE: (1) Voltage Across Photodiode.

SPECIFICATIONS (CONT)

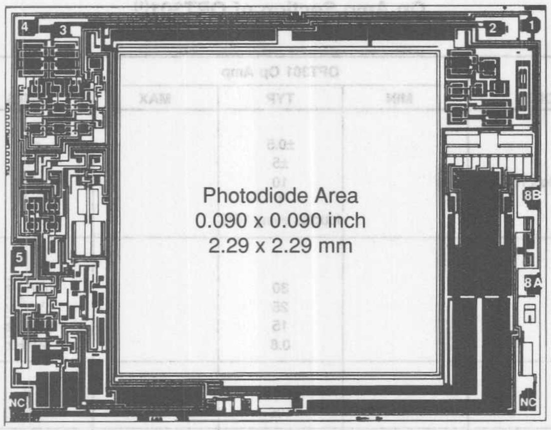
ELECTRICAL

Op Amp Section of OPT301(1)

T_A = +25°C, V_S = ±15V, unless otherwise noted.

		OPT301 Op Amp			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT					
Offset Voltage			±0.5		mV
vs Temperature			±5		µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		10		µV/V
Input Bias Current			1		pA
vs Temperature			doubles every 10°C		
NOISE					
Input Voltage Noise					
Voltage Noise Density, f=10Hz			30		$nV/\sqrt{Hz}$
f=100Hz			25		$nV/\sqrt{Hz}$
f=1kHz			15		$nV/\sqrt{Hz}$
Current Noise Density, f=1kHz			0.8		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE					
Common-Mode Input Range			±14.4		V
Common-Mode Rejection			106		dB
INPUT IMPEDANCE					
Differential			$10^{12}\|\|3$		Ω||pF
Common-Mode			$10^{12}\|\|3$		Ω||pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain			120		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			380		kHz
Slew Rate			0.5		V/µs
Settling Time 0.1%			4		µs
0.01%			5		µs
OUTPUT					
Voltage Output	R_L = 10kΩ	(V+) – 1.25	(V+) – 0.65		V
	R_L = 5kΩ	(V+) – 2	(V+) – 1		V
Short-Circuit Current			±18		mA
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±2.25		±18	V
Quiescent Current	I_O = 0		±0.4	±0.5	mA

NOTE: (1) Op amp specifications provided for information and comparison only.



OPT301 DIE TOPOGRAPHY

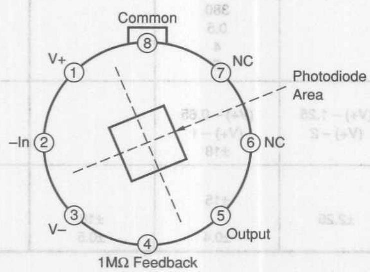
PAD	FUNCTION
1	V+
2	–In
3	V–
4	1MΩ Feedback
5	Output
6	NC
7	NC
8A, 8B	Common

NC: No Connection. Pads 8A and 8B must both be connected to common. Substrate Bias: The substrate is electrically connected to internal circuitry. Do not make electrical connection to the substrate.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	154 x 120 ±5	3.91 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATION



NOTE: Metal package is internally connected to common (Pin 8).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range (Common Pin)	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+125°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPT301M	8-Pin TO-99	001-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

7 Special Functions

Some analog circuit functions defy classification. In this section you will find a diverse assortment of circuit functions—at least one is bound to be your hidden treasure! Consider some of the possibilities:

IVC102—A new, precision FET-input integrating amplifier with on-chip integration capacitors, and low leakage analog switches that convert low-level input current to an output voltage. A lower noise alternative to op amp/resistor transimpedance amplifiers.

UAF42—Universal Analog Filter. Add only external resistors and make a wide range of low-pass, high-pass, band-pass and notch filters.

ACF2101—Dual Integrating Transimpedance Amplifier. Integrates input signal currents for a user-determined period of time. Measures tiny currents without using high value resistors.

MPY634—Analog Multiplier. Output is equal to the product of two input voltages. Useful in communications (modulation and mixing), power measurement, computation and linearization.

LOG100—Logarithmic Amplifier. Output is proportional to the logarithm of the ratio of two input currents. Useful as computational element—calculating decibels, for instance.

SPECIAL FUNCTIONS

MULTIPLIERS

MPY100 (550kHz)
MPY534 (3MHz)
MPY634 (10MHz)
MPY600 (30MHz)

OTHER
(Basic Function)

ACF2101 (Switched Integrator)
DIV100 (Divider)
IVC102 (Switched Integrator)
LOG100 (Log Ratio Amplifier)
SHC615 (Video DC Restoration)
UAF42 (Univ. Active Filter)
4127 (Logrithmic Amplifier)
4341 (RMS-to-DC Converter)
4302 (Multi-Function)

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

OTHER

Product	Function	Temp Range(1)	Pkg	Description	Comments
ACF2101	Switched Integrator	Ind	DIP, SOIC	This is a dual, integrating, transimpedance amplifier that converts an input current to an output voltage by integrating the current for a user determined period of time. Eliminates large feedback resistor of traditional I to V converters.	Includes HOLD and RESET switches and output multiplexer. $V_{OUT} = -\frac{1}{C}\int i_{IN}dt$
ALD1000	**Current/Voltage Transmitter**	**Ind**	**SOIC**	**Programmable voltage-to-current or voltage-to-voltage analog driver circuit.**	**Includes current and voltage sensing capability with error flag for open-circuit. Also has disable function.**
DIV100	10 x N/D	Com	DIP	Two-quadrant analog divider. V_O = 10N/D.	Input Range = 250mV to 10V, accuracy = 0.25% (max), rated output = ±10V, ±5mA (min), 0.5%, BW = 15kHz, and temp coeff = 0.2%/°C.
IVC102	**Switched Integrator**	**Ind**	**DIP, SOIC**	**Single, integrating amplifier with integrating capacitors and low leakage FET switches.**	**Ideal for amplifying low level sensors such as photodiodes and ionization chambers.**
LOG100	Logarithmic Amplifier	Com	DIP	K Log (I_1/I_2)	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.
SHC615	DC Restoration	XInd	14-Pin DIP, SOIC	Wide Bandwidth, fast, DC-Restoration circuit for sampling or hum suppression	Bandwidth - OTA: 750kHz Comparator: 280MHz Switching Transients: +1/–7mV Feedthrough Rejection: 100dB
UAF42	Universal Active Filter	Ind	DIP, SOIC	Universal Active Filter which can be configured for a wide range of low-pass, high-pass, and band-pass filters.	Uses classical state variable analog architecture.
4127	Logarithmic Amplifier	Com	DIP	K Log (I_1/I_{REF})	A more versatile part that contains an internal reference and a current inverter. 1% and 0.5% accuracy.
4302	Multifunction Converter	Ind	DIP	Y $(Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	Plastic Package.
4341	$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)dt}$	Ind	DIP	True RMS-to-DC conversion based on a log-antilog proportional approach.	Some external trimming required. Lower cost in plastic package.

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

MULTIPLIERS/DIVIDERS

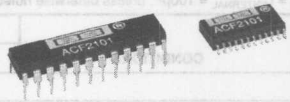
Product	Transfer Function	Error at +25°C max (%)	Temp Coeff (%/°C)	Feed-through (mV)	1% BW (MHz)	Temp Range(1)	Pkg
MPY100	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$	±0.5	0.008	30	0.07	Ind	TO-100
MPY534	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$	±0.25	0.008	0.05%	3	Com	TO-100
MPY600	$[(X_1 - X_2)(Y_1 - Y_2)/2] + Z_2$	±0.025	0.02	2	30	Ind	DIP
MPY634	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$	±0.5	0.015	0.15%	10	Ind	TO-100, DIP, SOIC

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C.

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

BURR - BROWN®



ACF2101

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11078

Low Noise, Dual
SWITCHED INTEGRATOR

FEATURES

- INCLUDES INTEGRATION CAPACITOR, RESET AND HOLD SWITCHES, AND OUTPUT MULTIPLEXER
- LOW NOISE: 10μVrms
- LOW CHARGE TRANSFER: 0.1pC
- WIDE DYNAMIC RANGE: 120dB
- LOW BIAS CURRENT: 100fA

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- PHOTODIODE INTEGRATOR
- CURRENT MEASUREMENT
- CHARGE MEASUREMENT
- CT SCANNER FRONT END
- MEDICAL, SCIENTIFIC, AND INDUSTRIAL INSTRUMENTATION

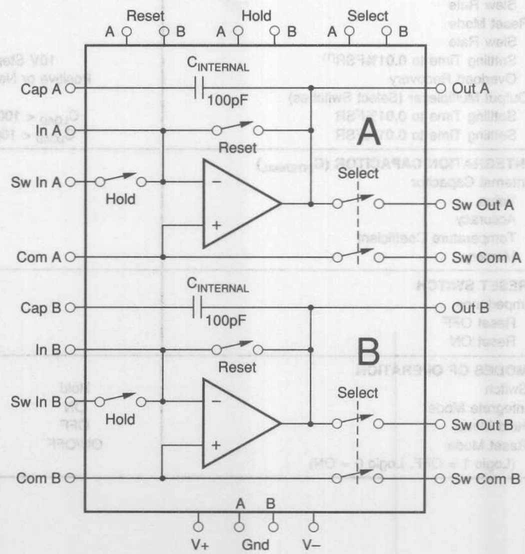
DESCRIPTION

The ACF2101 is a dual switched integrator for precision applications. Each channel can convert an input current to an output voltage by integration, using either an internal or external capacitor. Included on the chip are precision 100pF integration capacitors, hold and reset switches, and output multiplexers.

As a complete circuit on a single chip, the ACF2101 eliminates many of the problems commonly encountered in discrete designs, such as leakage current errors and noise pickup. The integrating approach can provide lower noise than conventional transimpedance amplifier designs and also eliminates the need for high performance, high value feedback resistors.

The extremely low bias current and low noise of the ACF2101's ***Difet®*** amplifiers, along with active laser trimming of both offset and drift, assure precision current to voltage conversion.

Although designed for +5V, –15V supplies, the ACF2101 can be operated on supplies up to ±18VDC. It is available in both 24-pin plastic DIP and SOIC packages.



Difet® Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At $T_A = +25°C$, $V+ = +5V$, $V- = -15V$, Internal $C_{INTEGRATION} = C_{INTERNAL} = 100pF$, unless otherwise noted.

PARAMETER	CONDITIONS	ACF2101BP, BU MIN	TYP	MAX	UNITS
ANALOG INPUT					
INPUT RANGE					
Input Current Range					
Switched Input (Sw In A, Sw In B)				±100	µA
Direct Input (In A, In B)				±100	µA
INPUT IMPEDANCE					
Switched Input					
Hold Switch OFF			1000		GΩ
Hold Switch ON			1.5		kΩ
Direct Input			Virtual Ground		
HOLD SWITCH VOLTAGE					
Hold Switch Withstand Voltage	Hold Switch OFF	−10		+0.5	V
OFFSET VOLTAGE					
Input Offset Voltage			±0.5	±2	mV
Average Drift			±1	±5	µV/°C
DIGITAL INPUTS					
Logic Family	TTL Compatible				
V_{IH} (Logic 1 = Switch OFF)		2		5.5	V
V_{IL} (Logic 0 = Switch ON)		−0.5		0.8	V
I_{IH}	$V_{IH} = +5V$		2		µA
I_{IL}	$V_{IL} = 0V$		0		µA
Switching Speed (All Switches)					
Switch ON			200		ns
Switch OFF			200		ns
TRANSFER CHARACTERISTICS					
TRANSFER FUNCTION			$V_{OUT} = -\frac{1}{C_{INTEGRATION}}\int I_{IN}dt$		V
DYNAMIC CHARACTERISTICS					
Integrate Mode					
Slew Rate		1	3		V/µs
Reset Mode					
Slew Rate			3		V/µs
Settling Time to 0.01%FSR(1)	10V Step		5	10	µs
Overload Recovery	Positive or Negative		5		µs
Output Multiplexer (Select Switches)					
Settling Time to 0.01%FSR	$C_{LOAD} < 1000pF$		6.5		µs
Settling Time to 0.01%FSR	$C_{LOAD} < 100pF$		2		µs
INTEGRATION CAPACITOR ($C_{INTERNAL}$)					
Internal Capacitor					
Value			100		pF
Accuracy			0.5	2	%
Temperature Coefficient		−50	−25	0	ppm/°C
Memory			30	100	ppm of FSR
RESET SWITCH					
Impedance					
Reset OFF			1000		GΩ
Reset ON			1.5		kΩ
MODES OF OPERATION					
Switch	Hold / Reset				
Integrate Mode	ON / OFF				
Hold Mode	OFF / OFF				
Reset Mode	ON/OFF / ON				
(Logic 1 = OFF, Logic 0 = ON)					

SPECIFICATIONS (CONT)

At T_A = +25°C, V+ = +5V, V− = −15V, Internal $C_{INTEGRATION}$ = $C_{INTERNAL}$ = 100pF, unless otherwise noted.

PARAMETER	CONDITIONS	ACF2101BP, BU MIN	TYP	MAX	UNITS
OUTPUT					
Voltage Output Range (All Outputs)		−10	−13.5, +1.0	+0.5	V
Current Output, Direct Output (Out A, Out B)		±5			mA
Short Circuit Current					
Direct Output			±25		mA
Switched Output (Sw Out A, Sw Out B)		±2	±8		mA
Select Switch Withstand Voltage					
Switched Output		−10		+0.5	V
Switched Common (Sw Com A, Sw Com B)		−0.5		+0.5	V
Output Impedance					
Direct Output			0.1		Ω
Switched Output					
Select Switch ON			250 || 5		Ω || pF
Select Switch OFF			1000 || 4		GΩ || pF
Leakage Current	Select Switch OFF		10	100	pA
Load Capacitance Stability					
Direct Output			500		pF
Switched Output			Any		pF
OUTPUT ACCURACY					
Nonlinearity			±0.005	±0.01	%FSR
Channel Separation			−80		dB
Op Amp Bias Current					
Value			100	1000	fA
Temperature Coefficient			Doubles Each +10°C		
Hold Mode Droop			1	10	nV/µs
Integrate Mode Droop			1	10	nV/µs
Voltage Offset(2)					
Value			3		mV
Temperature Coefficient			5		µV/°C
Power Supply Rejection	V_S = +4.5V to +18V, −10V to −18V	80	100		dB
OUTPUT NOISE					
Total Output Noise(3)	BW = 0.1Hz to 10Hz		2		µVrms
Integrate Mode(4)	BW = 0.1Hz to 250kHz		$10(1 + C_{IN}/C_{INTEGRATION})$		µVrms
Hold Mode	BW = 0.1Hz to 250kHz		10		µVrms
Reset Mode	BW = 0.1Hz to 250kHz		10		µVrms
CHARGE TRANSFER ERRORS(5)					
Reset to Integrate Mode(6)					
Charge Transfer			0.1	0.5	pC
Charge Transfer TC			0.2		fC/°C
Charge Offset Error			1	5	mV
Charge Offset TC			2		µV/°C
Integrate to Hold Mode	C_{IN} > 50pF				
Charge Transfer			0.2	1	pC
Charge Transfer TC			0.4		fC/°C
Charge Offset Error			2	10	mV
Charge Offset TC			4		µV/°C
Hold to Integrate Mode	C_{IN} > 50pF				
Charge Transfer			0.2	1	pC
Charge Transfer TC			0.4		fC/°C
Charge Offset Error			2	10	mV
Charge Offset TC			4		µV/°C
POWER SUPPLY					
Specified Operating Voltage			+5, −15		V
Operating Voltage Range					
Positive Supply		+4.5		+18	V
Negative Supply		−10		−18	V
Current					
Positive Supply	For Dual		12	15	mA
Negative Supply	For Dual		3.5	5.2	mA
TEMPERATURE RANGE					
Specification		−40		+85	°C
Operation		−40		+125	°C
Storage		−40		+125	°C
Thermal Resistance (both packages)	Junction to Ambient		100		°C/W

NOTES: (1) FSR is Full Scale Range = 10V (0 to −10V). (2) Includes offset errors from all modes of operation. (3) Total noise is rms total of noise for the modes of operation used. (4) C_{IN} = capacitance of sensor connected to ACF2101 input; $C_{INTERGRATION}$ = integration capacitance = $C_{INTERNAL}$ + $C_{EXTERNAL}$. (5) Errors created when the internal switches are driven from one mode to another. (6) The charge transfer is 0.1pC; for an integration capacitance of 100pF, the resultant charge offset voltage error is 1mV.

Supply	±18V
Input Current	±5mA
Output Short Circuit Duration	Continuous to Ground
Power Dissipation	500mW
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
ACF2101BP	24-Pin Plastic DIP	–40°C to +85°C
ACF2101BU	24-Pin Plastic SOIC	–40°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ACF2101BP	24-Pin Plastic DIP	243
ACF2101BU	24-Pin Plastic SOIC	239

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

BASIC CIRCUIT CONNECTION

Basic Layout

As with any precision circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the analog and digital input pins.

Figures 1a and 1b illustrate the basic connections needed for operation. Figures 1c and 1d illustrate the addition of external integration capacitors and input guards.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the ACF2101. A circuit board "guard" pattern reduces leakage effects by surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential. Leakage will flow harmlessly to the low impedance node. Figure 2a and 2b show printed circuit patterns that can be used to guard critical pins. Note that traces leading to these pins should also be guarded.

Improper handling or cleaning may increase droop. Contamination from handling parts and circuit boards can be removed with cleaning solvents and de-ionized water.

NOTE: DIP and SOIC package have different pin outs.

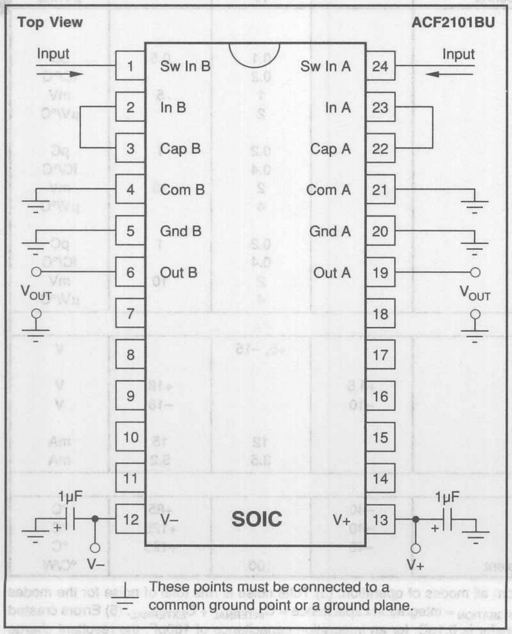


FIGURE 1a. Basic Circuit Connections, **SOIC package**.

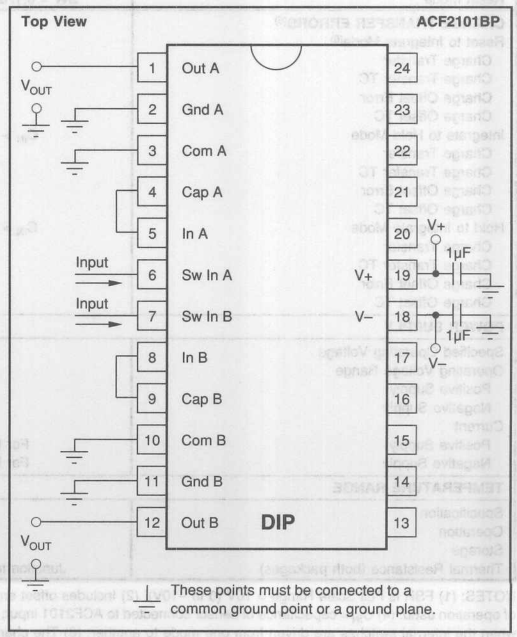
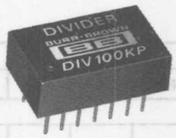


FIGURE 1b. Basic Circuit Connections, **DIP**.

BURR - BROWN®



DIV100

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10427

ANALOG DIVIDER

FEATURES

- **HIGH ACCURACY: 0.25% Maximum Error, 40:1 Denominator Range**
- **TWO-QUADRANT OPERATION**
  Dedicated Log-Antilog Technique
- **EASY TO USE**
  Laser-trimmed to Specified Accuracy
  No External Resistors Needed
- **LOW COST**
- **DIP PACKAGE**

APPLICATIONS

- **DIVISION**
- **SQUARE ROOT**
- **RATIOMETRIC MEASUREMENT**
- **PERCENTAGE COMPUTATION**
- **TRANSDUCER AND BRIDGE LINEARIZATION**
- **AUTOMATIC LEVEL AND GAIN CONTROL**
- **VOLTAGE CONTROLLED AMPLIFIERS**
- **ANALOG SIMULATION**

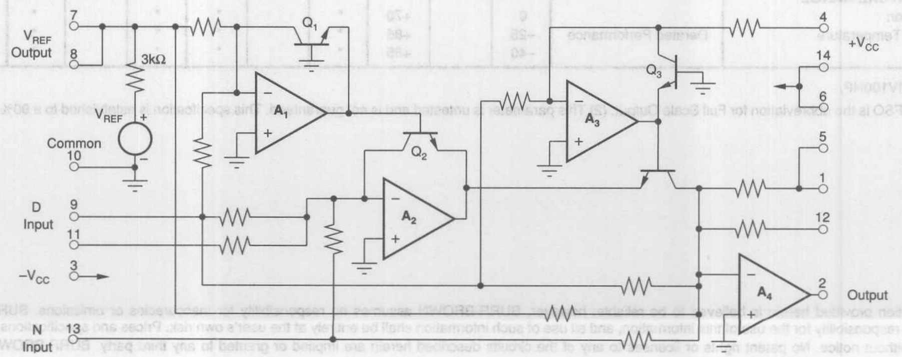
DESCRIPTION

The DIV100 is a precision two-quadrant analog divider offering superior performance over a wide range of denominator input. Its accuracy is nearly two orders of magnitude better than multipliers used for division. It consists of four operational amplifiers and logging transistors integrated into a single monolithic circuit and a laser-trimmed, thin-film resistor network. The electrical characteristics of these devices offer the user guaranteed accuracy without the need for external adjustment — the DIV100 is a complete, single package analog divider.

For those applications requiring higher accuracy than the DIV100 specifies, the capability for optional adjustment is provided. These adjustments allow the user to set scale factor, feedthrough, and output-referred offsets for the lowest total divider error.

The DIV100 also gives the user a precision, temperature-compensated reference voltage for external use.

Designers of industrial process control systems, analytical instruments, or biomedical instrumentation will find the DIV100 easy to use and also a low cost, but highly accurate solution to their analog divider applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC} = ±15VDC, unless otherwise specified.

PARAMETER	CONDITIONS	DIV100HP MIN	DIV100HP TYP	DIV100HP MAX	DIV100JP MIN	DIV100JP TYP	DIV100JP MAX	DIV100KP MIN	DIV100KP TYP	DIV100KP MAX	UNITS
TRANSFER FUNCTION		V_O = 10N/D									
ACCURACY	$R_L \geq 10k\Omega$										
Total Error											
Initial	0.25V ≤ D ≤ 10V, N ≤ |D|		0.7	1.0		0.3	0.5		0.2	0.25	% FSO[1]
vs Temperature	1V ≤ D ≤ 10V, N ≤ |D|		0.02	0.05[2]		*	*		*	*	% FSO/°C
	0.25V ≤ D ≤ 1V, N ≤ |D|		0.06	0.2[2]		*	*		*	*	% FSO/°C
vs Supply	0.25V ≤ D ≤ 10V, N ≤ |D|		0.15			*			*		% FSO/%
Warm-up TIme to Rated Performace			5			*			*		Minutes
AC PERFORMANCE	D = +10V										
Small-Signal Bandwidth	–3dB		350			*			*		kHz
0.5% Amplitude Error	Small-Signal		15			*			*		kHz
0.57° Vector Error	Small-Signal		1000			*			*		Hz
Full-Power Bandwidth	V_O = ±10V, I_O = ±5mA		30			*			*		kHz
Slew Rate	V_D = ±10V, I_O = ±5mA		2			*			*		V/µs
Settling Time	ε = 1%, ΔV_O = 20V		15			*			*		µs
Overload Recovery	50% Output Overload		4			*			*		µs
INPUT CHARACTERISTICS											
Input Voltage Range											
Numerator	N ≤ |D|	±10			*			*			V
Denominatior	D ≥ +250mV	±10			*			*			V
Input Resistance	Either Input		25			*			*		kΩ
OUTPUT CHARACTERISTICS											
Full-Scale Output		±10			*			*			V
Rated Output											
Voltage	I_O = ±5mA	±10			*			*			V
Current	V_O = ±10V	±5			*			*			mA
Current Limit											
Positive			15	20[2]		*			*		mA
Negative			19	23[2]		*			*		mA
OUTPUT NOISE VOLTAGE	N = 0V										
f_B = 10Hz to 10kHz											
D = +10V			370			*			*		µVrms
D = +250mV			1			*			*		mVrms
REFERENCE VOLTAGE CHARACTERISTICS, $R_L \geq 10M\Omega$											
Output Voltage											
Initial	At 25°C	6.5[2]	6.8	7.1[2]	*	*	*	*	*	*	V
vs Supply			±25			*			*		µV/V
Temperature Coefficient			±50			*			*		ppm/°C
Output Resistance			3			*			*		kΩ
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*			*		VDC
Operating Range	Derated Performance	±12		±20	*		*	*		*	VDC
Quiescent Current											
Postive Supply			5	7[2]		*	*		*	*	mA
Negative Supply			8	10[2]		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		0		+70	*		*	*		*	°C
Operating Temperature	Derated Performance	–25		+85	*		*	*		*	°C
Storage		–40		+85	*		*	*		*	°C

*Same as DIV100HP.

NOTES: (1) FSO is the abbreviation for Full Scale Output. (2) This parameter is untested and is not guaranteed. This specifcation is established to a 90% confidence level.

PIN CONFIGURATION

Bottom View — DIP

Left Function	Pin	Pin	Right Function
$+V_{CC}$	14	1	Gain Error Adjust
Numerator (N) Input	13	2	Output
Output Offset Adjust	12	3	$-V_{CC}$
N Input Offset Adjust	11	4	D Input Offset Adjust
Common	10	5	Internally Connected to Pin 1
Denominator (D) Input	9	6	Internally Connected to Pin 14
Refererence Voltage	8	7	Internally Connected to Pin 8

ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	600mW
Input Voltage Range(2)	±20VDC
Storage Temperature Range	–40°C to +85°C
Operating Temperature Range	–25°C to 85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit Duration(1, 3)	Continuous
Junction Temperature	+175°C

NOTES: (1) See General Information section for discussion. (2) For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage. (3) Short-circuit may be to ground only. Rating applies to an ambient temperature of +38°C at rated supply voltage.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DIV100HP	14-Pin DIP	105
DIV100JP	14-Pin DIP	105
DIV100KP	14-Pin DIP	105

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

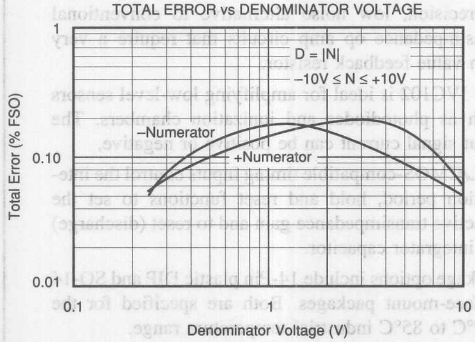
ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	TOTAL INITIAL ERROR (% FSO)
DIV100HP	0°C to +70°C	1.0
DIV100JP	0°C to +70°C	0.5
DIV100KP	0°C to +70°C	0.25

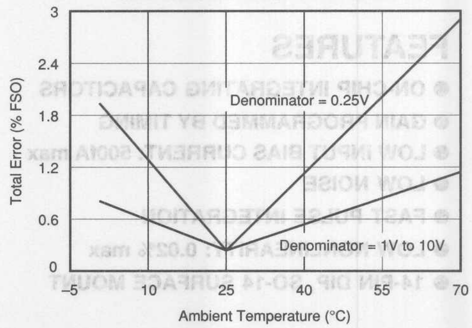
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = ±15VDC$, unless otherwise specified.

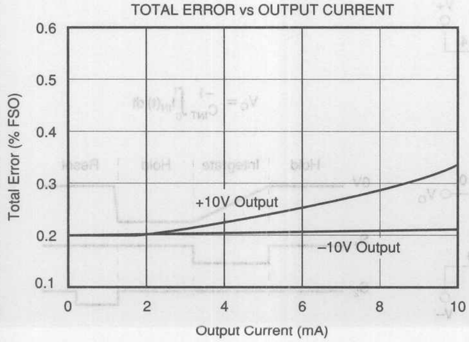
TOTAL ERROR vs DENOMINATOR VOLTAGE



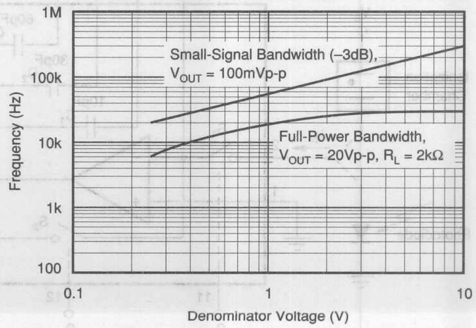
TOTAL ERROR vs AMBIENT TEMPERATURE



TOTAL ERROR vs OUTPUT CURRENT



FREQUENCY RESPONSE vs DENOMINATOR VOLTAGE



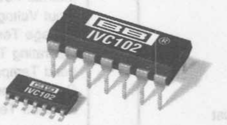
DIV100

7

SPECIAL FUNCTIONS

BURR - BROWN®

IVC102



PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

PRECISION SWITCHED INTEGRATOR TRANSIMPEDANCE AMPLIFIER

APPLICATIONS

- PRECISION LOW CURRENT MEASUREMENT
- PHOTODIODE MEASUREMENTS
- IONIZATION CHAMBER MEASUREMENTS
- CURRENT-OUTPUT SENSORS
- LEAKAGE CURRENT MEASUREMENT

FEATURES

- ON-CHIP INTEGRATING CAPACITORS
- GAIN PROGRAMMED BY TIMING
- LOW INPUT BIAS CURRENT: 500fA max
- LOW NOISE
- FAST PULSE INTEGRATION
- LOW NONLINEARITY: 0.02% max
- 14-PIN DIP, SO-14 SURFACE MOUNT

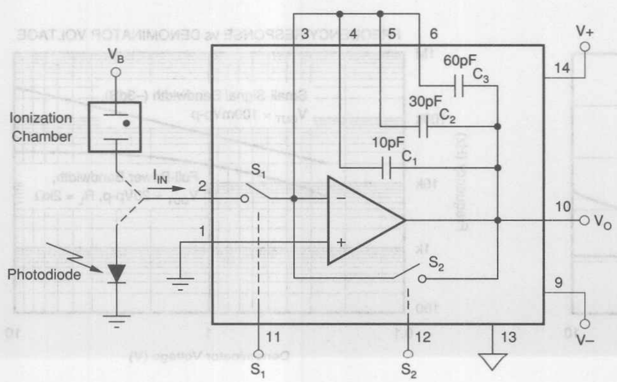
DESCRIPTION

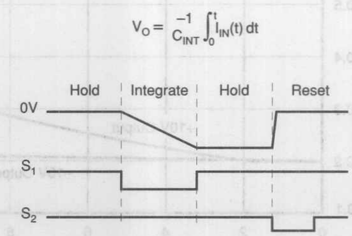
The IVC102 is a precision integrating amplifier with FET op amp, integrating capacitors, and low leakage FET switches. It integrates low-level input current for a user-determined period, storing the resulting voltage on the integrating capacitor. The output voltage can be held for accurate measurement. The IVC102 provides a precision, low noise alternative to conventional transimpedance op amp circuits that require a very high value feedback resistor.

The IVC102 is ideal for amplifying low-level sensors such as photodiodes and ionization chambers. The input signal current can be positive or negative.

TTL/CMOS-compatible timing inputs control the integration period, hold and reset functions to set the effective transimpedance gain and to reset (discharge) the integrator capacitor.

Package options include 14-Pin plastic DIP and SO-14 surface-mount packages. Both are specified for the –40°C to 85°C industrial temperature range.





International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1329

BURR - BROWN®

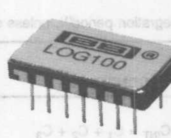
SPECIFICATIONS

At $T_A = +25°C$, $V_S = ±15V$, $R_L = 2kΩ$, $C_{INT} = C_1 + C_2 + C_3$, 1ms integration period(1), unless otherwise specified.

PARAMETER	CONDITIONS	IVC102 MIN	TYP	MAX	UNITS
TRANSFER FUNCTION			$V_O = -(T_{INT})(I_{IN})/C_{INT}$		
Gain Error	$C_{INT} = C_1 + C_2 + C_3$		±5	+25/–17	%
vs Temperature			+30/+60		ppm/°C
Nonlinearity	$V_O = ±10V$		±0.005	±0.02	%
Input Current Range			±100		µA
Offset Voltage(2)	$I_{IN} = 0$, $C_{SOURCE} = 50pF$		–1/–3	±10	mV
vs Temperature			±10		µV/°C
vs Power Supply	$V_S = +4.75/–10$ to $+18/–18V$		150	500	µV/V
Droop Rate, Hold Mode			1		nV/µs
INPUT					
Input Bias Current	S_1, S_2 Open		100	500	fA
Offset Voltage (Op Amp V_{OS})			±0.5	±5	mV
vs Temperature			±5		µV/°C
vs Power Supply	$V_S = +4.75/–10$ to $+18/–18V$		10	100	µV/V
Noise Voltage	f = 1kHz		10		nV/√Hz
INTEGRATION CAPACITORS					
$C_1 + C_2 + C_3$		80	100	120	pF
vs Temperature			–25		ppm/°C
Voltage Coefficient			2		ppm/V
C_1			10		pF
C_2			30		pF
C_3			60		pF
OUTPUT					
Voltage Range		(V_S) ±3	(V_S) ±2.5		V
Short-Circuit Current			±20		mA
Capacitive Load Drive			500		pF
DYNAMIC CHARACTERISTIC					
Op Amp Gain-Bandwidth			2		MHz
Op Amp Slew Rate			3		V/µs
Reset					
Slew Rate			3		V/µs
Settling Time, 0.01%	10V Step		6		µs
DIGITAL INPUTS	(TTL/CMOS Compatible)				
V_{IH} (referred to digital ground)		2		5.5	V
V_{IL} (referred to digital ground)		–0.5		0.8	V
$V_{DIGITAL\ GROUND}$ (referred to analog ground)				±200	mV
I_{IH}	$V_{IH} = 5V$		2		µA
I_{IL}	$V_{IL} = 0V$		0		µA
Switching Time			100		ns
POWER SUPPLY					
Voltage Range: Positive		4.75	15	18	V
Negative		–10	–15	–18	V
Current: Positive			3.8	4.5	mA
Negative			–1.6	–2	mA
Analog Ground			–220		µA
Digital Ground			–1.9		mA
TEMPERATURE RANGE					
Operating Range		–40		85	°C
Storage		–40		125	°C
Thermal Resistance, θ_{JA}					
DIP			100		°C/W
SO-14			150		°C/W

NOTES: (1) Standard test timing: 1ms integration, 200µs hold, 100µs reset. (2) Hold mode output voltage after 1ms integration of zero input current. Includes op amp offset voltage, integration of input error current and switch charge injection effects.

BURR - BROWN®



LOG100

Precision LOGARITHMIC AND LOG RATIO AMPLIFIER

FEATURES

- **ACCURACY**
  0.37% FSO max Total Error Over 5 Decades
- **LINEARITY**
  0.1% max Log Conformity Over 5 Decades
- **EASY TO USE**
  Pin-selectable Gains
  Internal Laser-trimmed Resistors
- **WIDE INPUT DYNAMIC RANGE**
  6 Decades, 1nA to 1mA
- **HERMETIC CERAMIC DIP**

APPLICATIONS

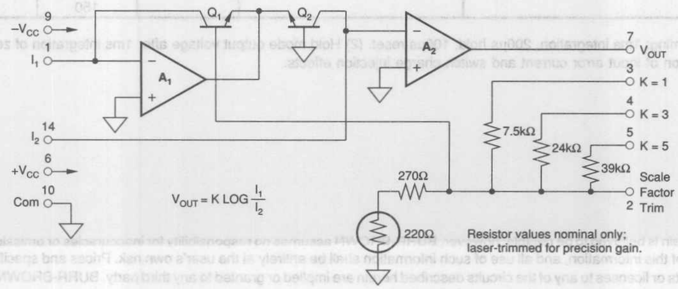
- **LOG, LOG RATIO AND ANTILOG COMPUTATIONS**
- **ABSORBANCE MEASUREMENTS**
- **DATA COMPRESSION**
- **OPTICAL DENSITY MEASUREMENTS**
- **DATA LINEARIZATION**
- **CURRENT AND VOLTAGE INPUTS**

DESCRIPTION

The LOG100 uses advanced integrated circuit technologies to achieve high accuracy, ease of use, low cost, and small size. It is the logical choice for your logarithmic-type computations. The amplifier has guaranteed maximum error specifications over the full six-decade input range (1nA to 1mA) and for all possible combinations of I_1 and I_2. Total error is guaranteed so that involved error computations are not necessary.

The circuit uses a specially designed compatible thin-film monolithic integrated circuit which contains amplifiers, logging transistors, and low drift thin-film resistors. The resistors are laser-trimmed for maximum precision. FET input transistors are used for the amplifiers whose low bias currents (1pA typical) permit signal currents as low as 1nA while maintaining guaranteed total errors of 0.37% FSO maximum.

Because scaling resistors are self-contained, scale factors of 1V, 3V or 5V per decade are obtained simply by pin selections. No other resistors are required for log ratio applications. The LOG100 will meet its guaranteed accuracy with no user trimming. Provisions are made for simple adjustments of scale factor, offset voltage, and bias current if enhanced performance is desired.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C and $\pm V_{CC}$ = ±15V, after 15 minute warm-up, unless otherwise specified.

PARAMETER	CONDITIONS	LOG100JP MIN	LOG100JP TYP	LOG100JP MAX	UNITS
TRANSFER FUNCTION			$V_{OUT} = K \text{ Log } (I_1/I_2)$		
Log Conformity Error[1]	Either I_1 or I_2				
Initial	1nA to 100µA (5 decades)		0.04	0.1	%
	1nA to 1mA (6 decades)		0.15	0.25	%
Over Temperature	1nA to 100µA (5 decades)		0.002		%/°C
	1nA to 1mA (6 decades)		0.001		%/°C
K Range[2]			1, 3, 5		V/decade
Accuracy			0.3		%
Temperature Coefficient			0.03		%/°C
ACCURACY					
Total Error[3]	K = 1,[4] Current Input Operation				
Initial	I_1, I_2 = 1mA			±55	mV
	I_1, I_2 = 100µA			±30	mV
	I_1, I_2 = 10µA			±25	mV
	I_1, I_2 = 1µA			±20	mV
	I_1, I_2 = 100nA			±25	mV
	I_1, I_2 = 10nA			±30	mV
	I_1, I_2 = 1nA			±37	mV
vs Temperature	I_1, I_2 = 1mA		±0.20		mV/°C
	I_1, I_2 = 100µA		±0.37		mV/°C
	I_1, I_2 = 10µA		±0.28		mV/°C
	I_1, I_2 = 1µA		±0.033		mV/°C
	I_1, I_2 = 100nA		±0.28		mV/°C
	I_1, I_2 = 10nA		±0.51		mV/°C
	I_1, I_2 = 1nA		±1.26		mV/°C
vs Supply	I_1, I_2 = 1mA		±4.3		mV/V
	I_1, I_2 = 100µA		±1.5		mV/V
	I_1, I_2 = 10µA		±0.37		mV/V
	I_1, I_2 = 1µA		±0.11		mV/V
	I_1, I_2 = 100nA		±0.61		mV/V
	I_1, I_2 = 10nA		±0.91		mV/V
	I_1, I_2 = 1nA		±2.6		mV/V
INPUT CHARACTERISTICS (of Amplifiers A_1 and A_2)					
Offset Voltage					
Initial			±0.7	±5	mV
vs Temperature			±80		µV/°C
Bias Current					
Initial			1	5[5]	pA
vs Temperature			Doubles Every 10°C		
Voltage Noise	10Hz to 10kHz, RTI		3		µVrms
Current Noise	10Hz to 10kHz, RTI		0.5		pArms
AC PERFORMANCE					
3dB Response[6], I_2 = 10µA					
1nA	C_C = 4500pF		0.11		kHz
1µA	C_C = 150pF		38		kHz
10µA	C_C = 150pF		27		kHz
1mA	C_C = 50pF		45		kHz
Step Response[6]					
Increasing	C_C = 150pF				
1µA to 1mA			11		µs
100nA to 1µA			7		µs
10nA to 100nA			110		µs
Decreasing	C_C = 150pF				
1mA to 1µA			45		µs
1µA to 100nA			20		µs
100nA to 10nA			550		µs
OUTPUT CHARACTERISTICS					
Full Scale Output (FSO)		±10			V
Rated Output					
Voltage	I_{OUT} = ±5mA	±10			V
Current	V_{OUT} = ±10V	±5			mA
Current Limit					
Positive			12.5		mA
Negative			15		mA
Impedance			0.05		Ω

ELECTRICAL

T_A = +25°C and $\pm V_{CC}$ = ±15V, after 15 minute warm-up, unless otherwise specified.

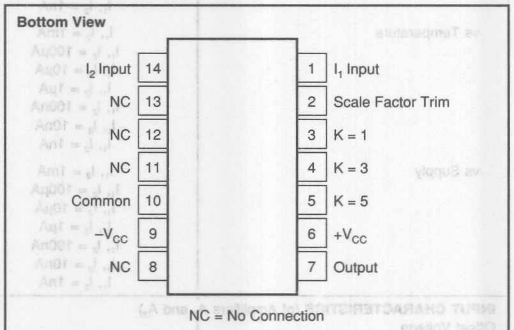
PARAMETER	CONDITIONS	LOG100JP MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS					
Rated Voltage			±15		VDC
Operating Range	Derated Performance	±12		±18	VDC
Quiescent Current			±7	±9	mA
AMBIENT TEMPERATURE RANGE					
Specification		0		+70	°C
Operating Range	Derated Performance	–25		+85	°C
Storage		–40		+85	°C

NOTES: (1) Log Conformity Error is the peak deviation from the best-fit straight line of the V_{OUT} vs Log I_{IN} curve expressed as a percent of peak-to-peak full scale output. (2) May be trimmed to other values. See Applications section. (3) The worst-case Total Error for any ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately. (4) Total Error at other values of K is K times Total Error for K = 1. (5) Guaranteed by design. Not directly measurable due to amplifier's committed configuration. (6) 3dB and transient response are a function of both the compensation capacitor and the level of input current. See Typical Performance Curves.

ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Internal Power Dissipation	600mV
Input Current	10mA
Input Voltage Range	±18V
Storage Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

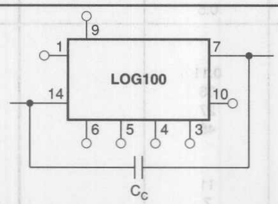
PIN CONFIGURATION



SCALE FACTOR PIN CONNECTIONS

K, V/DECADE	CONNECTIONS
5	5 to 7
3	4 to 7
1.9	4 and 5 to 7
1	3 to 7
0.85	3 and 5 to 7
0.77	3 and 4 to 7
0.68	3 and 4 and 5 to 7

FREQUENCY COMPENSATION



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ORDERING INFORMATION

MODEL	PACKAGE	SPECIFIED TEMPERATURE RANGE
LOG100JP	14-Pin Hermetic Ceramic DIP	0°C to +70°C

PACKAGE INFORMATION

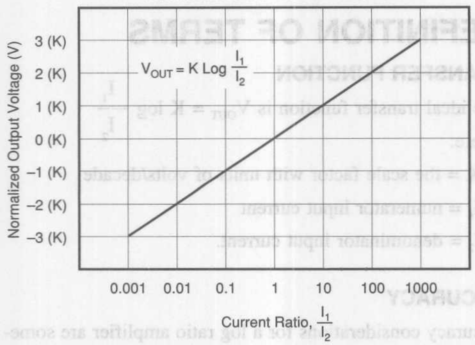
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
LOG100JP	14-Pin Hermetic Ceramic DIP	148[2]

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) During 1994, the package was changed from plastic to hermetic ceramic. Pinout, model number, and specifications remained unchanged. The metal lid of the new package is internally connected to common, pin 10.

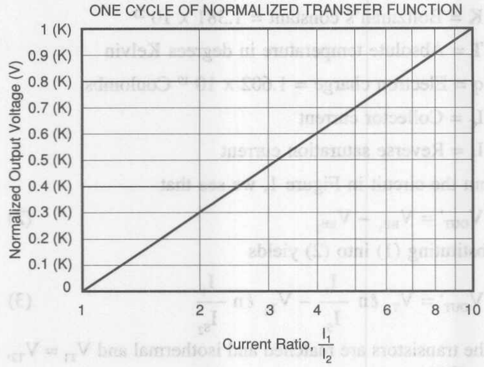
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = \pm15VDC$, unless otherwise noted.

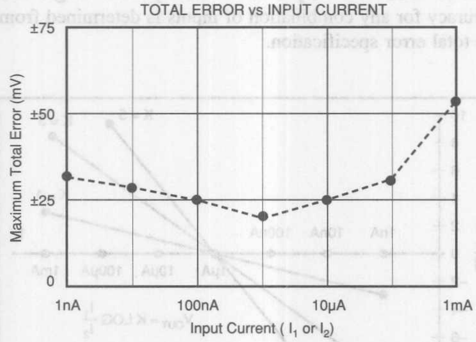
NORMALIZED TRANSFER FUNCTION



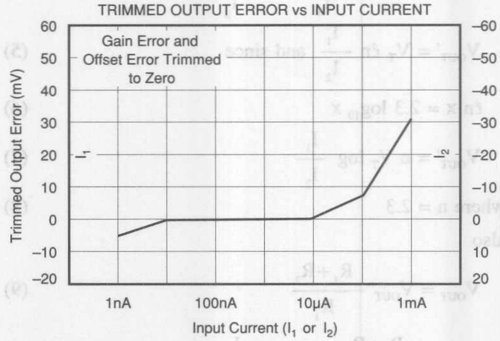
ONE CYCLE OF NORMALIZED TRANSFER FUNCTION



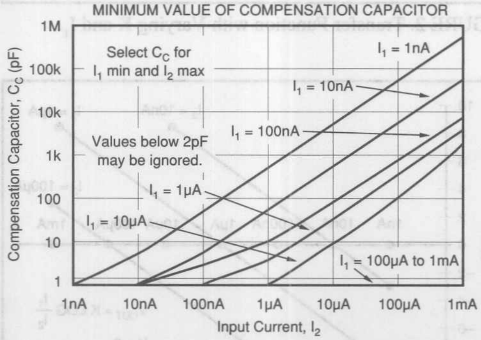
TOTAL ERROR vs INPUT CURRENT



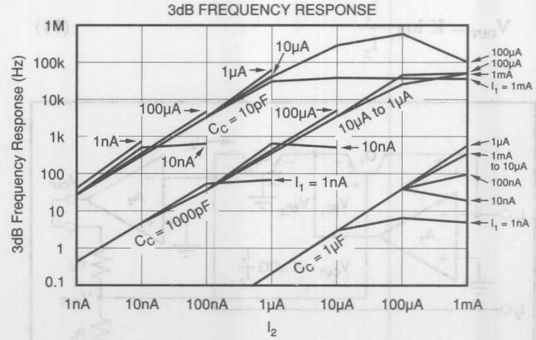
TRIMMED OUTPUT ERROR vs INPUT CURRENT



MINIMUM VALUE OF COMPENSATION CAPACITOR



3dB FREQUENCY RESPONSE



THEORY OF OPERATION

The base-emitter voltage of a bipolar transistor is

$$V_{BE} = V_T \,\ell n \frac{I_C}{I_S} \quad \text{where: } V_T = \frac{KT}{q} \tag{1}$$

K = Boltzman's constant = 1.381×10^{-23}

T = Absolute temperature in degrees Kelvin

q = Electron charge = 1.602×10^{-19} Coulombs

I_C = Collector current

I_S = Reverse saturation current

From the circuit in Figure 1, we see that

$$V_{OUT}' = V_{BE_1} - V_{BE_2} \tag{2}$$

Substituting (1) into (2) yields

$$V_{OUT}' = V_{T_1} \,\ell n \frac{I_1}{I_{S_1}} - V_{T_2} \,\ell n \frac{I_1}{I_{S_2}} \tag{3}$$

If the transistors are matched and isothermal and $V_{T1} = V_{T2}$, then (3) becomes:

$$V_{OUT}' = V_T \left[\ell n \frac{I_1}{I_S} - \ell n \frac{I_2}{I_S}\right] \tag{4}$$

$$V_{OUT}' = V_T \,\ell n \frac{I_1}{I_2} \quad \text{and since} \tag{5}$$

$$\ell n\, x = 2.3 \log_{10} x \tag{6}$$

$$V_{OUT}' = n\, V_T \log \frac{I_1}{I_2} \tag{7}$$

where n = 2.3 (8)

also

$$V_{OUT} = V_{OUT}' \frac{R_1 + R_2}{R_1} \tag{9}$$

$$= \frac{R_1 + R_2}{R_1}\, n\, V_T \log \frac{I_1}{I_2} \tag{10}$$

or

$$V_{OUT} = K \log \frac{I_1}{I_2} \tag{11}$$

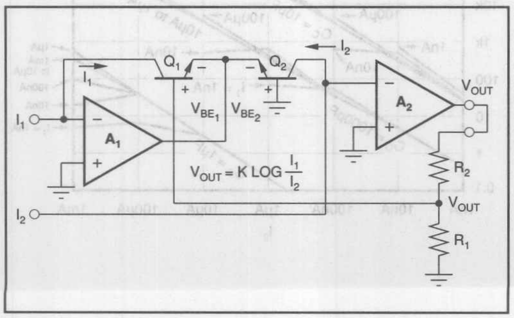


FIGURE 1. Simplified Model of Log Amplifier.

It should be noted that the temperature dependance associated with $V_T = KT/q$ is compensated by making R_1 a temperature sensitive resistor with the required positive temperature coefficient.

DEFINITION OF TERMS

TRANSFER FUNCTION

The ideal transfer function is $V_{OUT} = K \log \frac{I_1}{I_2}$

where:

K = the scale factor with units of volts/decade

I_1 = numerator input current

I_2 = denominator input current.

ACCURACY

Accuracy considerations for a log ratio amplifier are somewhat more complicated than for other amplifiers. The reason is that the transfer function is nonlinear and has two inputs, each of which can vary over a wide dynamic range. The accuracy for any combination of inputs is determined from the total error specification.

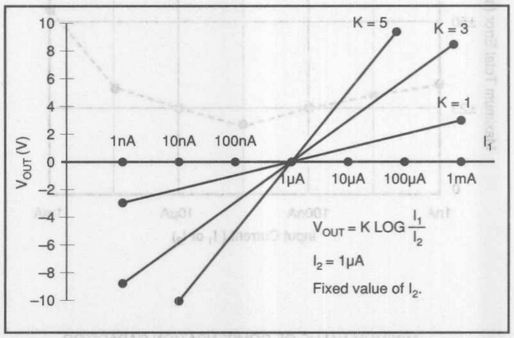


FIGURE 2. Transfer Function with Varying K and I_1.

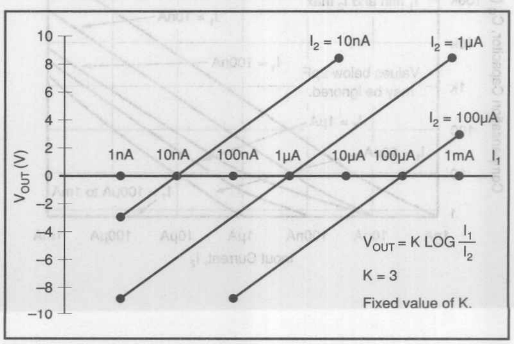


FIGURE 3. Transfer Function with Varying I_2 and I_1.

TOTAL ERROR

The total error is the deviation (expressed in mV) of the actual output from the ideal output of $V_{OUT} = K \log (I_1/I_2)$. Thus,

$$V_{OUT\,(ACTUAL)} = V_{OUT\,(IDEAL)} \pm \text{Total Error.}$$

It represents the sum of all the individual components of error normally associated with the log amp when operated in the current input mode. The worst-case error for any given ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately.

Example:

I_1 varies over a range of 10nA to 1µA and I_2 varies from 100nA to 10µA. What is the maximum error?

Table I shows the maximum errors for each decade combination of I_1 and I_2.

I_2 (maximum error)(1) \ I_1 (maximum error)(1)	10nA (30mV)	100nA (25mV)	1µA (20mV)
100nA (25mV)	0.1 (30mV)	1 (25mV)	10 (25mV)
1µA (20mV)	0.01 (30mV)	0.1 (25mV)	1 (20mV)
10µA (25mV)	0.001 (30mV)	0.01 (25mV)	0.1 (25mV)

NOTE: (1) Maximum errors are in parenthesis.

TABLE I. I_1/I_2 and Maximum Errors.

Since the largest value of I_1/I_2 is 10 and the smallest is 0.001, K is set at 3V per decade so the output will range from +3V to –9V. The maximum total error occurs when I_1 = 10nA and is equal to K x 30mV. This represents a 0.75% of peak-to-peak FSO error 3 x 0.030/12 x 100% = 0.75% where the full scale output is 12V (from +3V to –9V).

ERRORS RTO AND RTI

As with any transfer function, errors generated by the function itself may be Referred-to-Output (RTO) or Referred-to-Input (RTI). In this respect, log amps have a unique property:

> Given some error voltage at the log amp's output, that error corresponds to a constant percent of the input regardless of the actual input level.

Refer to: Yu Jen Wong and William E. Ott, "Function Circuits: Design & Applications", McGraw-Hill Book, 1976.

LOG CONFORMITY

Log conformity corresponds to linearity when V_{OUT} is plotted versus I_1/I_2 on a semilog scale. In many applications, log conformity is the most important specification. This is true because bias current errors are negligible (1pA compared to input currents of 1nA and above) and the scale factor and offset errors may be trimmed to zero or removed by system calibration. This leaves log conformity as the major source of error.

Log conformity is defined as the peak deviation from the best-fit straight line of the V_{OUT} versus $\log (I_1/I_2)$ curve. This is expressed as a percent of peak-to-peak full scale output. Thus, the nonlinearity error expressed in volts over m decades is

$$V_{OUT\,(NONLIN)} = K\ 2Nm\ V \qquad (12)$$

where N is the log conformity error, in percent.

INDIVIDUAL ERROR COMPONENTS

The ideal transfer function with current input is

$$V_{OUT} = K \log \frac{I_1}{I_2} \qquad (13)$$

The actual transfer function with the major components of error is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{I_1 - I_{B1}}{I_2 - I_{B2}} \pm K\ 2Nm \pm V_{OS\,OUT} \qquad (14)$$

The individual component of error is

- ΔK = scale factor error (0.3%, typ)
- I_{B1} = bias current of A_1 (1pA, typ)
- I_{B2} = bias current of A_2 (1pA, typ)
- N = log conformity error (0.05%, 0.1%, typ)
- $V_{OS\,OUT}$ = output offset voltage (1mV, typ)
- m = number of decades over which N is specified: 0.05% for m = 5, 0.1% for m = 6

Example: what is the error with K = 3 when I_1 = 1µA and I_2 = 100nA

$$V_{OUT} = 3(1 \pm 0.003) \log \frac{10^{-6} - 10^{-12}}{10^{-7} - 10^{-12}} \pm 3(2)(0.0005)5 \pm 1\text{mV} \qquad (15)$$

$$\approx 3.009 \log \frac{10^{-6}}{10^{-7}} + 0.015 + 0.001 \qquad (16)$$

$$= 3.009\,(1) + 0.015 + 0.001 \qquad (17)$$

$$= 3.025\text{V} \qquad (18)$$

Since the ideal output is 3.000V, the error as a percent of reading is

$$\%\ \text{error} = \frac{0.025}{3} \times 100\% = 0.83\% \qquad (19)$$

For the case of voltage inputs, the actual transfer function is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{\dfrac{V_1}{R_1} - I_{B_1} \pm \dfrac{E_{OS_1}}{R_1}}{\dfrac{V_2}{R_2} - I_{B_2} \pm \dfrac{E_{OS_2}}{R_2}} \pm K\ 2Nm \pm V_{OS\,OUT} \qquad (20)$$

FREQUENCY RESPONSE

The 3dB frequency response of the LOG100 is a function of the magnitude of the input current levels and of the value of the frequency compensation capacitor. See Typical Performance Curves for details.

and I_2 with a small signal AC current on one of them.

The transient response of the LOG100 is different for increasing and decreasing signals. This is due to the fact that a log amp is a nonlinear gain element and has different gains at different levels of input signals. Frequency response decreases as the gain increases.

GENERAL INFORMATION

INPUT CURRENT RANGE

The stated input range of 1nA to 1mA is the range for specified accuracy. Smaller or larger input currents may be applied with decreased accuracy. Currents larger than 1mA result in increased nonlinearity. The 10mA absolute maximum is a conservative value to limit the power dissipation in the output stage of A_1 and the logging transistor. Currents below 1nA will result in increased errors due to the input bias currents of A_1 and A_2 (1pA typical). These errors may be nulled. See Optional Adjustments section.

FREQUENCY COMPENSATION

Frequency compensation for the LOG100 is obtained by connecting a capacitor between pins 7 and 14. The size of the capacitor is a function of the input currents as shown in the Typical Performance Curves. For any given application, the smallest value of the capacitor which may be used is determined by the maximum value at I_2 and the minimum value of I_1. Larger values of C_C will make the LOG100 more stable, but will reduce the frequency response.

SETTING THE REFERENCE CURRENT

When the LOG100 is used as a straight log amplifier I_2 is constant and becomes the reference current in the expression

$$V_{OUT} = K \log \frac{I_1}{I_{REF}} \tag{21}$$

I_{REF} can be derived from an external current source (such as shown in Figure 4), or it may be derived from a voltage source with one or more resistors.

When a single resistor is used, the value may be quite large when I_{REF} is small. If I_{REF} is 10nA and +15V is used

$$R_{REF} = \frac{15V}{10nA} = 1500M\Omega.$$

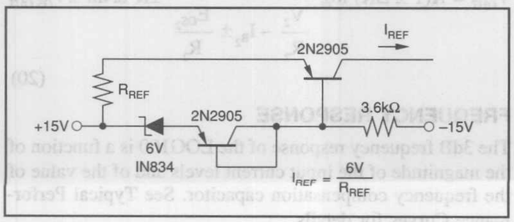


FIGURE 4. Temperature-Compensated Current Reference.

resistor. When this is done, one must be aware of possible errors caused by the amplifier's input offset voltage. This is shown in Figure 5.

In this case the voltage at pin 14 is not exactly zero, but is equal to the value of the input offset voltage of A_1, which ranges from zero to ±5mV. V_T must be kept much larger than 5mV in order to make this effect negligible. This concept also applies to pin 1.

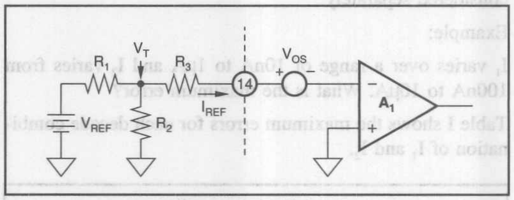


FIGURE 5. "T" Network for Reference Current.

OPTIONAL ADJUSTMENTS

The LOG100 will meet its specified accuracy with no user adjustments. If improved performance is desired, the following optional adjustments may be made.

INPUT BIAS CURRENT

The circuit in Figure 6 may be used to compensate for the input bias currents of A_1 and A_2. Since the amplifiers have FET inputs with the characteristic bias current doubling every 10°C, this nulling technique is practical only where the temperature is fairly stable.

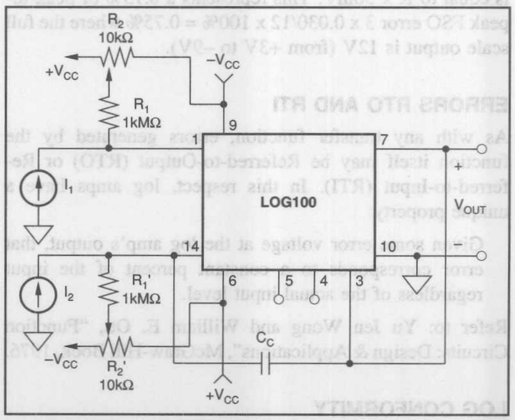


FIGURE 6. Bias Current Nulling.

OUTPUT OFFSET

The output offset may be nulled with the circuit in Figure 7. I_1 and I_2 are set equal at some convenient value in the range of 100nA to 100µA. R_1 is then adjusted for zero output voltage.

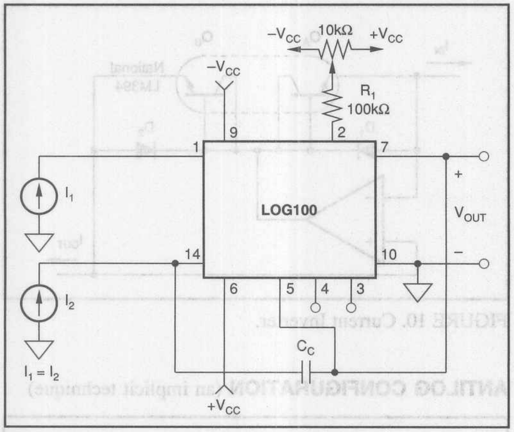


FIGURE 7. Output Offset Nulling.

ADJUSTMENTS OF SCALE FACTOR K

The value of K may be changed by increasing or decreasing the voltage divider resistor normally connected to the output, pin 7. To increase K put resistance in series between pin 7 and the appropriate scaling resistor pin (3, 4 or 5). To decrease K place a parallel resistor between pin 2 and either pin 3, 4 or 5.

APPLICATION INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the LOG100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 100pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the LOG100's output. This resistor will, of course, form a voltage divider with other resistive loads.

CIRCUIT PROTECTION

The LOG100 can be protected against accidental power supply reversal by putting a diode (1N4001 type) in series with each power supply line as shown in Figure 8. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off. If this protection circuit is used, the accuracy of the LOG100 will be degraded slightly by the voltage drops across the diodes as determined by the power supply sensitivity specification.

The LOG100 uses small geometry FET transistors to achieve the low input bias currents. Normal FET handling

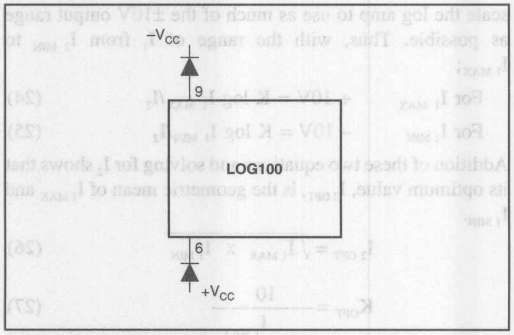


FIGURE 8. Reverse Polarity Protection.

techniques should be used to avoid damage caused by low energy electrostatic discharge (ESD).

LOG RATIO

One of the more common uses of log ratio amplifiers is to measure absorbance. A typical application is shown in Figure 9.

Absorbance of the sample is $A = \log \frac{\lambda_1}{\lambda_1}$ (22)

If $\lambda_2 = \lambda_1$ and D_1 and D_2 are matched $A \propto K \log \frac{I_1}{I_2}$. (23)

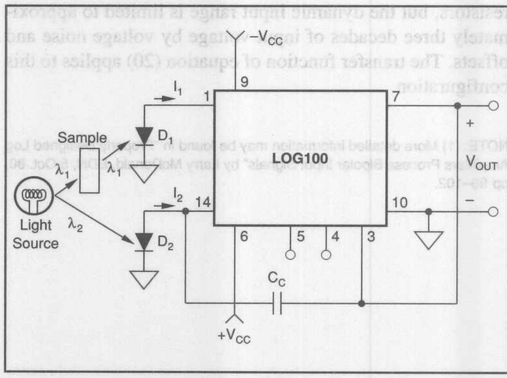


FIGURE 9. Absorbance Measurement.

DATA COMPRESSION

In many applications the compressive effects of the logarithmic transfer function is useful. For example, a LOG100 preceding an 8-bit analog-to-digital converter can produce equivalent 20-bit converter operation.

SELECTING OPTIMUM VALUES OF I_2 AND K

In straight log applications (as opposed to log ratio), both K and I_2 are selected by the designer. In order to minimize errors due to output offset and noise, it is normally best to

scale the log amp to use as much of the ±10V output range as possible. Thus, with the range of I_1 from $I_{1\ MIN}$ to $I_{1\ MAX}$;

For $I_{1\ MAX}$ $\qquad + 10V = K \log I_{1\ MAX}/I_2 \qquad (24)$

For $I_{1\ MIN}$ $\qquad - 10V = K \log I_{1\ MIN}/I_2 \qquad (25)$

Addition of these two equations and solving for I_2 shows that its optimum value, $I_{2\ OPT}$, is the geometric mean of $I_{1\ MAX}$ and $I_{1\ MIN}$.

$$I_{2\ OPT} = \sqrt{I_{1\ MAX} \times I_{1\ MIN}} \qquad (26)$$

$$K_{OPT} = \frac{10}{\log \dfrac{I_{1\ MAX}}{I_{2\ OPT}}} \qquad (27)$$

Since K is selectable in discrete steps, use the largest value of K available which does not exceed K_{OPT}.

NEGATIVE INPUT CURRENTS

The LOG100 will function only with positive input currents (conventional current flow into pins 1 and 14). Some current sources (such as photomultiplier tubes) provide negative input currents. In such situations, the circuit in Figure 10 may be used.[1]

VOLTAGE INPUTS

The LOG100 gives the best performance with current inputs. Voltage inputs may be handled directly with series resistors, but the dynamic input range is limited to approximately three decades of input voltage by voltage noise and offsets. The transfer function of equation (20) applies to this configuration.

NOTE: (1) More detailed information may be found in "Properly Designed Log Amplifiers Process Bipolar Input Signals" by Larry McDonald, EDN, 5 Oct. 80, pp 99–102.

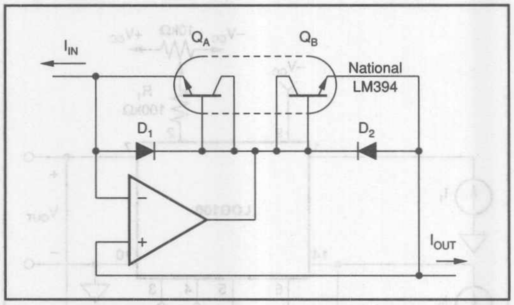


FIGURE 10. Current Inverter.

ANTILOG CONFIGURATION (an implicit technique)

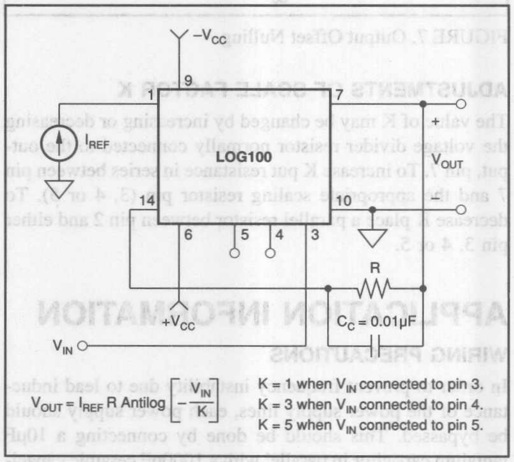
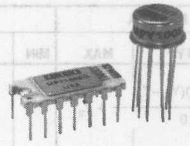


FIGURE 11. Connections for Antilog Function.

BURR - BROWN®



MPY100

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10412

MULTIPLIER-DIVIDER

FEATURES

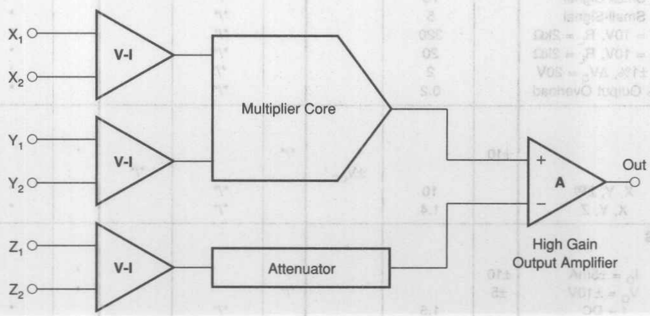
- LOW COST
- DIFFERENTIAL INPUT
- ACCURACY 100% TESTED AND GUARANTEED
- NO EXTERNAL TRIMMING REQUIRED
- LOW NOISE: 90μVrms, 10Hz to 10kHz
- HIGHLY RELIABLE ONE-CHIP DESIGN
- DIP OR TO-100 TYPE PACKAGE
- WIDE TEMPERATURE OPERATION

APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOT
- LINEARIZATION
- POWER COMPUTATION
- ANALOG SIGNAL PROCESSING
- ALGEBRAIC COMPUTATION
- TRUE RMS-TO-DC CONVERSION

DESCRIPTION

The MPY100 multiplier-divider is a low cost precision device designed for general purpose application. In addition to four-quadrant multiplication, it also performs analog square root and division without the bother of external amplifiers or potentiometers. Laser-trimmed one-chip design offers the most in highly reliable operation with guaranteed accuracies. Because of the internal reference and pretrimmed accuracies the MPY100 does not have the restrictions of other low cost multipliers. It is available in both TO-100 and DIP ceramic packages.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C and $\pm V_S$ = 15VDC, unless otherwise specified.

		MPY100A			MPY100B/C			MPY100S			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$			*/*			*		
Total Error	$-10V \le X, Y \le 10V$										
Initial	T_A = +25°C			±2.0			±1.0/0.5			±0.5	% FSR
vs Temperature	$-25°C \le T_A \le +85°C$		±0.017	±0.05		±0.008/0.008	±0.02/0.02				% FSR/°C
vs Temperature	$-55°C \le T_A \le +125°C$								±0.025	±0.05	% FSR/°C
vs Supply(1)			±0.05			*/*			*		% FSR/%
Individual Errors											
Output Offset											
Initial	T_A = +25°C		±50	±100		±10/7	±50/25		±7	±50	mV
vs Temperature	$-25°C \le T_A \le +85°C$		±0.7	±2.0		±0.7/0.3	±2.0/±0.7				mV/°C
vs Temperature	$-55°C \le T_A \le +125°C$								±0.3	±0.7	mV/°C
vs Supply(1)			±0.25			*/*			*		mV/%
Scale Factor Error											
Initial	T_A = +25°C		±0.12			*/*			*		% FSR
vs Temperature	$-25°C \le T_A \le +85°C$		±0.008			*/*					% FSR/°C
vs Temperature	$-55°C \le T_A \le +125°C$								±0.008		% FSR/°C
vs Supply(1)			±0.05			*/*			*		% FSR %
Nonlinearity											
X Input	X = 20Vp-p; Y = ±10VDC		±0.08			*/*			*		% FSR
Y Input	Y = 20Vp-p: X = ±10VDC		±0.08			*/*			*		% FSR
Feedthrough	f = 50Hz										
X Input	X = 20Vp-p; Y = 0		100			30/30			30		mVp-p
Y Input	Y = 20Vp-p; X = 0		6			*/*					mVp-p
vs Temperature	$-25°C \le T_A \le +85°C$		0.1			*/*					mVp-p/°C
vs Temperature	$-55°C \le T_A \le 125°C$								0.1		mVp-p/°C
vs Supply(1)			0.15						*		mVp-p/%
DIVIDER PERFORMANCE											
Transfer Function	$X_1 > X_2$		$\frac{10(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			*/*			*		
Total Error (with external adjustments)	X = 10V $-10V \le Z \le +10V$		±1.5			±0.75/0.35			±0.35		% FSR
	X = 1V $-1V \le Z \le +1V$		±4.0			±2.0/1.0			±1.0		% FSR
	$+0.2V \le X \le +10V$ $-10V \le Z \le +10V$		±5.0			±2.5/1.0			±1.0		% FSR
SQUARER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)^2}{10} + Z_2$			*/*			*		
Total Error	$-10V \le X \le +10V$		±1.2			±0.6/0.3			±0.3		% FSR
SQUARE ROOTER PERFORMANCE											
Transfer Function	$Z_1 < Z_2$		$+\sqrt{10(Z_2 - Z_1)} + X_2$			*/*			*		
Total Error	$1V \le Z \le 10V$		±2			±1/0.5			±0.5		% FSR
AC PERFORMANCE											
Small-Signal Bandwidth			550			*/*			*		kHz
% Amplitude Error	Small-Signal		70			*/*			*		kHz
% (0.57°) Vector Error	Small-Signal		5			*/*			*		kHz
Full Power Bandwidth	$\lvert V_O\rvert$ = 10V, R_L = 2kΩ		320			*/*			*		kHz
Slew Rate	$\lvert V_O\rvert$ = 10V, R_L = 2kΩ		20			*/*			*		V/µs
Settling Time	$\varepsilon = \pm 1\%$, ΔV_O = 20V		2			*/*			*		µs
Overload Recovery	50% Output Overload		0.2			*/*			*		µs
INPUT CHARACTERISTICS											
Input Voltage Range											
Rated Operation		±10			*/*			*			V
Absolute Maximum				$\pm V_{CC}$			*/*			*	V
Input Resistance	X, Y, Z(2)		10			*/*			*		MΩ
Input Bias Current	X, Y, Z		1.4			*/*			*		µA
OUTPUT CHARACTERISTICS											
Rated Output											
Voltage	I_O = ±5mA	±10			*/*			*			V
Current	V_O = ±10V	±5			*/*			*			mA
Output Resistance	f = DC		1.5			*/*			*		Ω

SPECIFICATIONS (CONT)

At T_A = +25°C and $\pm V_S$ = 15VDC, unless otherwise specified.

		MPY100A			MPY100B/C			MPY100S			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OUTPUT NOISE VOLTAGE	X = Y = 0										
f_O = 1Hz			6.2			*/*			*		µV/√Hz
f_O = 1kHz			0.6			*/*			*		µV/√Hz
l/f Corner Frequency			110			*/*			*		Hz
f_B = 5Hz to 10kHz			60			*/*			*		µVrms
f_B = 5Hz to 5MHz			1.3			*/*			*		mVrms
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*/*			*		VDC
Operating Range	Derated Performance	±8.5		±20	*/*		*/*	*		*	VDC
Quiescent Current			±5.5			*/*			*		mA
TEMPERATURE RANGE (Ambient)											
Specification		–25		+85	*/*		*/*	–55		+125	°C
Operating Range	Derated Performance	–55		+125	*/*		*/*	*		*	°C
Storage		–65		+150	*/*		*/*	*		*	°C

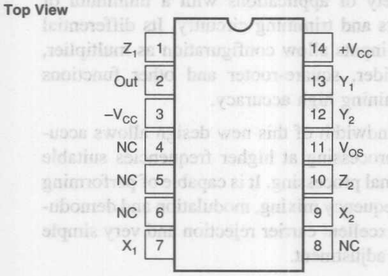
* Same as MPY100A specification.

/ B/C grades same as MPY100A specification.

NOTES: (1) Includes effects of recommended null pots. (2) Z_2 input resistance is 10MΩ, typical, with V_{OS} pin open. If V_{OS} pin is grounded or used for optional offset adjustment, the Z_2 input resistance may be as low as 25kΩ

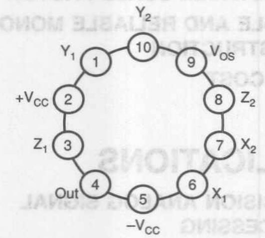
PIN CONFIGURATIONS

Top View DIP



NOTES: (1) V_{OS} adjustment optional not normally recommended. V_{OS} pin may be left open or grounded. (2) All unused input pins should be grounded.

Top View TO-100



NOTES: (1) V_{OS} adjustment optional not normally recommended. V_{OS} pin may be left open or grounded. (2) All unused input pins should be grounded.

ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-circuit Duration(3)	Continuous
Junction Temperature	+150°C

NOTES: (1) Package must be derated on θ_{JC} = 15°C/W and θ_{JA} = 165°C/W for the metal package and θ_{JC} = 35°C/W and θ_{JA} = 220°C/W for the ceramic package. (2) For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage. (3) Short-circuit may be to ground only. Rating applies to +85°C ambient for the metal package and +65°C for the ceramic package.

ORDERING INFORMATION

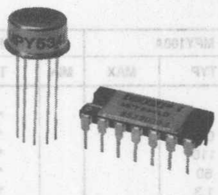
MODEL	PACKAGE	TEMPERATURE RANGE
MPY100AG	14-Pin Ceramic DIP	–25°C to +85°C
MPY100AM	Metal TO-100	–25°C to +85°C
MPY100BG	14-Pin Ceramic DIP	–25°C to +85°C
MPY100BM	Metal TO-100	–25°C to +85°C
MPY100CG	14-Pin Ceramic DIP	–25°C to +85°C
MPY100CM	Metal TO-100	–25°C to +85°C
MPY100SG	14-Pin Ceramic DIP	–55°C to +125°C
MPY100SM	Metal TO-100	–55°C to +125°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPY100AG	14-Pin Ceramic DIP	169
MPY100AM	Metal TO-100	007
MPY100BG	14-Pin Ceramic DIP	169
MPY100BM	Metal TO-100	007
MPY100CG	14-Pin Ceramic DIP	169
MPY100CM	Metal TO-100	007
MPY100SG	14-Pin Ceramic DIP	169
MPY100SM	Metal TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®



MPY534

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10614

Precision ANALOG MULTIPLIER

FEATURES

- ±0.25% max 4-QUADRANT ACCURACY
- WIDE BANDWIDTH: 1MHz min, 3MHz typ
- ADJUSTABLE SCALE FACTOR
- STABLE AND RELIABLE MONOLITHIC CONSTRUCTION
- LOW COST

APPLICATIONS

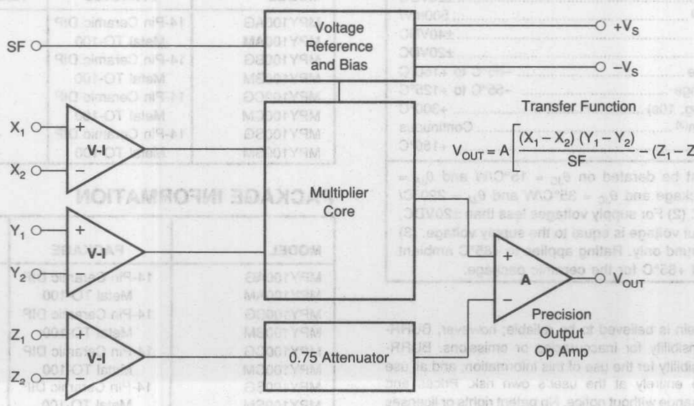
- PRECISION ANALOG SIGNAL PROCESSING
- VIDEO SIGNAL PROCESSING
- VOLTAGE CONTROLLED FILTERS AND OSCILLATORS
- MODULATION AND DEMODULATION
- RATIO AND PERCENTAGE COMPUTATION

DESCRIPTION

The MPY534 is a high accuracy, general purpose four-quadrant analog multiplier. Its accurately laser trimmed transfer characteristics make it easy to use in a wide variety of applications with a minimum of external parts and trimming circuitry. Its differential X, Y and Z inputs allow configuration as multiplier, squarer, divider, square-rooter and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows accurate signal processing at higher frequencies suitable for video signal processing. It is capable of performing IF and RF frequency mixing, modulation and demodulation with excellent carrier rejection and very simple feedthrough adjustment.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user selected scale factors from 0.1 to 10 using external feedback resistors.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C and V_S = ±15VDC, unless otherwise specified.

	MPY534J			MPY534K			MPY534L			MPY534S			MPY534T			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE																
Transfer Function		*		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$				*			*			*		
Total Error(1) (–10V ≤ X, Y ≤ +10V)			±1.0			±0.5			±0.25			±1.0			*	%
T_A = min to max		±1.5			±1.0			±0.5				±2.0			±1.0	%
Total Error vs Temperature		±0.022			±0.015			±0.008				±0.02			±0.01	%/°C
Scale Factor Error (SF = 10.000V Nominal)(2)		±0.25			±0.1			*			±0.25			*		%
Temperature Coefficient of Scaling Voltage		±0.02			±0.01			±0.005			±0.02			±0.005		%/°C
Supply Rejection (±15V ±1V)		*			±0.01			*			*			*		%
Nonlinearity:																
X (X = 20Vp-p, Y = 10V)		±0.4			±0.2	±0.3		±0.10	±0.12		±0.4			*	*	%
Y (Y = 20Vp-p, X = 10V)		*			±0.01	±0.1		±0.005	*		*			*	*	%
Feedthrough(3)																
X (Y Nulled, Y = 20Vp-p 50Hz)		±0.3			±0.15	±0.3		±0.05	±0.12		±0.3			*	*	%
Y (X Nulled, Y = 20Vp-p 50Hz)		*			±0.01	±0.1		±0.003	*		*			*	*	%
Output Offset Voltage		±5	±30		±2	±15		*	±10		±5	±30		*	*	mV
Output Offset Voltage Drift		200			100			*				500			300	μV/°C
DYNAMICS																
Small Signal BW, (V_{OUT} = 0.1Vrms)	*	*		1	3		*			*	*		*	*		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		*			50			*			*			*		kHz
Slew Rate (V_{OUT} = 20Vp-p)		*			20			*			*			*		V/μs
Settling Time (to 1%, ΔV_{OUT} = 20V)		*			2			*			*			*		μs
NOISE																
Noise Spectral Density: SF = 10V		*			0.8			*			*			*		$\mu V/\sqrt{Hz}$
Wideband Noise: f = 10Hz to 5MHz		*			1			*			*			*		mVrms
f = 10Hz to 10kHz		*			90			*			*			*		μVrms
OUTPUT																
Output Voltage Swing	*			±11			*			*			*			V
Output Impedance (f ≤ 1kHz)		*			0.1			*			*			*		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		*			30			*			*			*		mA
Amplifier Open Loop Gain (f = 50Hz)		*			70			*			*			*		dB
INPUT AMPLIFIERS (X, Y and Z)																
Input Voltage Range																
Differential V_{IN} (V_{CM} = 0)		*			±12			*			*			*		V
Common-Mode V_{IN} (V_{DIFF} = 0) (see Typical Performance Curves)		*			±10			*			*			*		V
Offset Voltage X, Y		±5	±20		±2	±10		*	*		±5	±20		*	*	mV
Offset Voltage Drift X, Y		100			50			*			100			*		μV/°C
Offset Voltage Z		±5	±30		±2	±15		*	±10		±5	±30		*	*	mV
Offset Voltage Drift Z		200			100			*				500			300	μV/°C
CMRR	60	80		70	90		*	*		60	80		*	*		dB
Bias Current		*	*		0.8	2.0		*	*		*	*		*	*	μA
Offset Current		*			0.1			0.05	0.2		*	2.0		*	2.0	μA
Differential Resistance		*			10			*			*			*		MΩ
DIVIDER PERFORMANCE																
Transfer Function ($X_1 > X_2$)		*		$10V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$												
Total Error(1) (X = 10V, –10V ≤ Z ≤ +10V)		±0.75			±0.35			±0.2			±0.75			*		%
(X – 1V, –1V ≤ Z ≤+1V)		±2.0			±1.0			±0.8			±2.0			*		%
(0.1V ≤ X ≤ 10V, –10V ≤ Z ≤ 10V)		±2.5			±1.0			±0.8			±2.5					%

MPY534

7

SPECIAL FUNCTIONS

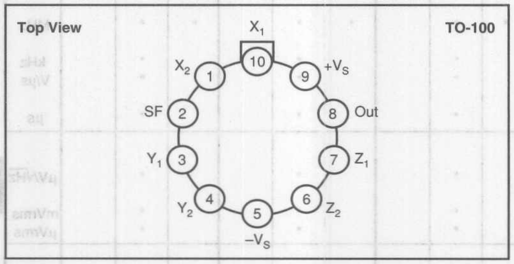
$T_A = +25°C$ and $V_S = ±15VDC$, unless otherwise specified.

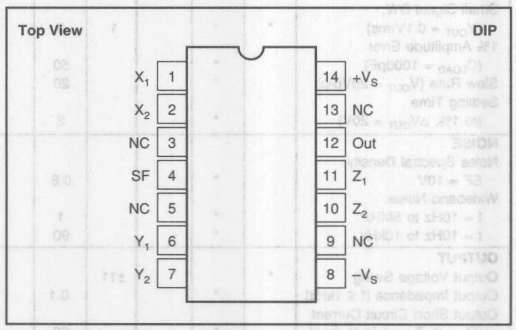
	MPY534J			MPY534K			MPY534L			MPY534S			MPY534T			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
SQUARE PERFORMANCE																
Transfer Function		*			$\frac{(X_1 - X_2)^2}{10V} + Z_2$			*			*			*		
Total Error ($-10V \le X \le 10V$)		0.6			±0.3			±0.2			±0.6			*		%
SQUARE-ROOTER PERFORMANCE																
Transfer Function ($Z_1 \le Z_2$)		*			$\sqrt{10V(Z_2 - Z_1)} + X_2$			*			*			*		
Total Error(1) ($1V \le Z \le 10V$)		±1.0			±0.5			±0.25			±1.0			±0.5		%
POWER SUPPLY																
Supply Voltage:																
Rated Performance		*			±15			*			*			*		VDC
Operating	*		*	±8		±18	*		*	*		±20	*		±20	VDC
Supply Current, Quiescent		*	*		4	6		*	*		*	*		*	*	mA
TEMPERATURE RANGE																
Operating	*		*	0		+70	*		*	−55		+125	−55		+125	°C
Storage	*		*	−65		+150	*		*	*		*	*		*	°C

*Specifications same as for MPY534K.

NOTES: (1) Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV). (2) May be reduced to 3V using external resistor between −Vs and SF. (3) Irreducible component due to nonlinearity; excludes effect of offsets.

PIN CONFIGURATIONS





ABSOLUTE MAXIMUM RATINGS

PARAMETER	MPY534J, K, L	MPY534S, T
Power Supply Voltage	±18	±20
Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltage (all X, Y and Z)	$±V_S$	*
Operating Temperature Range	0°C to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature (soldering, 10s)	+300°C	*

*Specification same as for MPY534K.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPY534JD	Ceramic DIP	169
MPY534JH	Metal TO-100	007
MPY534KD	Ceramic DIP	169
MPY534KH	Metal TO-100	007
MPY534LD	Ceramic DIP	169
MPY534LH	Metal TO-100	007
MPY534SD	Ceramic DIP	169
MPY534SH	Metal TO-100	007
MPY534TD	Ceramic DIP	169
MPY534TH	Metal TO-100	007

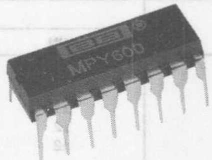
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
MPY534JD	Ceramic DIP	0°C to +70°C
MPY534JH	Metal TO-100	0°C to +70°C
MPY534KD	Ceramic DIP	0°C to +70°C
MPY534KH	Metal TO-100	0°C to +70°C
MPY534LD	Ceramic DIP	0°C to +70°C
MPY534LH	Metal TO-100	0°C to +70°C
MPY534SD	Ceramic DIP	−55°C to +125°C
MPY534SH	Metal TO-100	−55°C to +125°C
MPY534TD	Ceramic DIP	−55°C to +125°C
MPY534TH	Metal TO-100	−55°C to +125°C

BURR - BROWN®

MPY600



ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11019

Wide Bandwidth SIGNAL MULTIPLIER

FEATURES

- **WIDE BANDWIDTH:**
  75MHz — Current Output
  30MHz — Voltage Output
- **LOW NOISE**
- **LOW FEEDTHROUGH: –60dB (5MHz)**
- **GROUND-REFERRED OUTPUT**
- **LOW OFFSET VOLTAGE**

APPLICATIONS

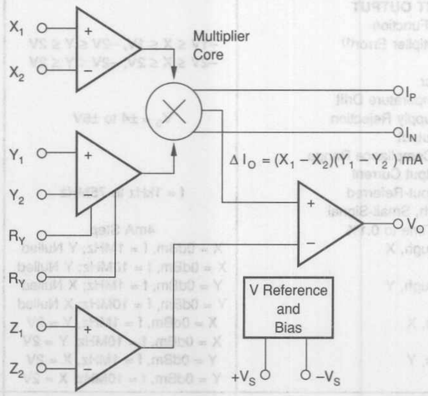
- **MODULATOR/DEMODULATOR**
- **VIDEO SIGNAL PROCESSING**
- **CRT GEOMETRY CORRECTION**
- **CRT FOCUS CORRECTION**
- **VOLTAGE-CONTROLLED CIRCUITS**

DESCRIPTION

The MPY600 is a wide-bandwidth four-quadrant signal multiplier. Its output voltage is equal to the algebraic product of the X and Y input voltages. For signals up to 30MHz, the on-board output op amp provides the complete multiplication function with a low-impedance voltage output. Differential current outputs extend multiplier bandwidth to 75MHz.

The MPY600 offers improved performance compared to common semiconductor modulator or multiplier circuits. It can be used for both two-quadrant (voltage-controlled amplifier) and four-quadrant (double-balanced) applications. While previous devices required cumbersome circuitry for trimming, balance and level-shifting, the MPY600 requires no external components. A single external resistor can be used to program the conversion gain for optimum spurious-free dynamic range. When used as a modulator, carrier feedthrough measures –60dB at 5MHz.

Differential X, Y and Z inputs can be connected in a variety of useful configurations, including squarer, divider, and square-rooter circuits. The MPY600 is available in 16-pin plastic DIP, specified for the industrial temperature range.



$$V_O = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{2V} + Z_2 - Z_1\right]$$

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $V_S = \pm5V$, $T_A = +25°C$, unless otherwise noted.

SPECIFICATION	CONDITIONS	MPY600AP MIN	TYP	MAX	UNITS
INPUTS (X, Y, Z)					
Full-Scale Differential Input					
X_1-X_2		±1			V
Y_1-Y_2		±2			V
Z_1-Z_2		±2			V
Input Voltage Range			±2.2		V
Differential Input Range			±2.5		V
Input Impedance			100 || 1.5		kΩ || pF
Input Offset Voltage			±0.5	±5	mV
Drift			25		µV/°C
CMRR	$V_{CM} = \pm2V$		70		dB
PSRR			70		dB
Input Bias Current (X, Y)			+15		µA
Z Input			–15		µA
VOLTAGE OUTPUT					
Transfer Function			$V_O = \frac{(X_1-X_2)(Y_1-Y_2)}{2} + Z_2$		V
Total Multiplier Error(1)	–1V ≤ X ≤ 1V, –2V ≤ Y ≤ 2V		±15	±25	mV
	–2V ≤ X ≤ 2V, –2V ≤ Y ≤ 2V		±25		mV
Gain Error			±1		%
Gain Temperature Drift			±200		ppm/°C
Power Supply Rejection	V_S = ±4 to ±6V		70		dB
Noise	f = 1kHz to 30MHz		120		nV/ Hz
Output Voltage Swing	$R_L = 100\Omega$	±2.2	±3		V
Output Current		±22	±30		mA
Short-Circuit Limit			50		mA
Bandwidth	Small Signal		30		MHz
Slew Rate			150		V/µs
Settling Time to 0.1%	4V Step		150		ns
Differential Gain Error	3.58MHz, 0 to 0.7V		0.2		%
Differential Phase Error	3.58MHz, 0 to 0.7V		0.2		Degrees
Capacitive Load, Max	Stable Operation		100		pF
Feedthrough, X	X = 0dBm, f = 500kHz; Y Nulled		–65		dB
	X = 0dBm, f = 5MHz; Y Nulled		–60		dB
Feedthrough, Y	Y = 0dBm, f = 500kHz; X Nulled		–70		dB
	Y = 0dBm, f = 5MHz; X Nulled		–50		dB
Distortion, X	X = 0dBm, f = 500kHz, Y = 2V		–60		dB
	X = 0dBm, f = 5MHz, Y = 2V		–55		dB
Distortion, Y	Y = 0dBm, f = 500kHz, X = 2V		–65		dB
	Y = 0dBm, f = 5MHz, X = 2V		–55		dB
CURRENT OUTPUT					
Transfer Function			$\Delta I_O = (X_1 - X_2)(Y_1 - Y_2)/1000$		A
Total Multiplier Error(1)	–1V ≤ X ≤ 1V, –2V ≤ Y ≤ 2V		±20	±80	µA
	–2V ≤ X ≤ 2V, –2V ≤ Y ≤ 2V		±80		µA
Gain Error			±1		%
Gain Temperature Drift			±200		ppm/°C
Power Supply Rejection	V_S = ±4 to ±6V		50		dB
Noise, Output			100		pA/√Hz
Voltage Compliance Range			±2.5		V
Peak Output Current			5		mA
Noise, Input-Referred	f = 1kHz to 75MHz		50		nV/√Hz
Bandwidth, Small-Signal			75		MHz
Settling Time to 0.1%	4mA Step		150		ns
Feedthrough, X	X = 0dBm, f = 1MHz; Y Nulled		–65		dB
	X = 0dBm, f = 10MHz; Y Nulled		–45		dB
Feedthrough, Y	Y = 0dBm, f = 1MHz; X Nulled		–75		dB
	Y = 0dBm, f = 10MHz; X Nulled		–55		dB
Distortion, X	X = 0dBm, f = 1MHz, Y = 2V		–55		dB
	X = 0dBm, f = 10MHz, Y = 2V		–50		dB
Distortion, Y	Y = 0dBm, f = 1MHz, X = 2V		–65		dB
	Y = 0dBm, f = 10MHz, X = 2V		–50		dB
POWER SUPPLY					
Rated Performance			±5		V
Operating		±4.75		±8	V
Current			±30	±35	mA
TEMPERATURE RANGE					
Specified Temperature Range		–25		+85	°C
Storage Temperature Range		–40		+125	°C
Thermal Resistance, $\theta_{J\text{-}A}$			50		°C/W

NOTE: (1) Deviation from ideal transfer function referred to full scale output. Includes gain, nonlinearity and offset errors.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$\pm V_S$
Op Amp Output Current	100mA
Operating Temperature	+125°C
Storage Temperature	+150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	SPECIFIED TEMPERATURE RANGE
MPY600AP	16-Pin Plastic DIP	–25°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPY600AP	16-Pin Plastic DIP	180

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATION

Top View — DIP

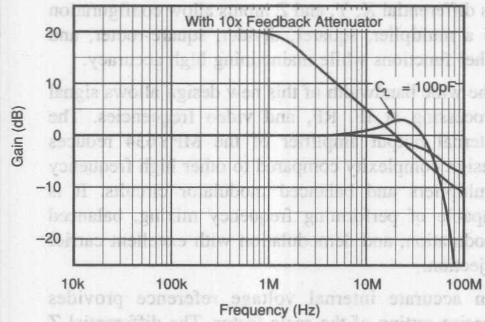
Function	Pin	Name	Name	Pin	Function
Voltage Output	1	V_O	I_P	16	+Current Output
Z_1 Input	2	Z_1	I_N	15	–Current Output
Z_2 Input	3	Z_2	NC	14	NC
Y_1 Input	4	Y_1	X_1	13	X_1 Input
Y-Gain Adj.	5	R_Y	NC	12	NC
Y-Gain Adj.	6	R_Y	NC	11	NC
Y_2 Input	7	Y_2	X_2	10	X_2 Input
$+V_S$ Power	8	$+V_S$	$-V_S$	9	$-V_S$ Power

NC: No internal connection.

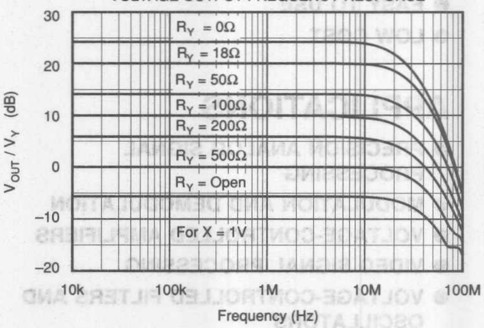
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±5V, unless otherwise noted.

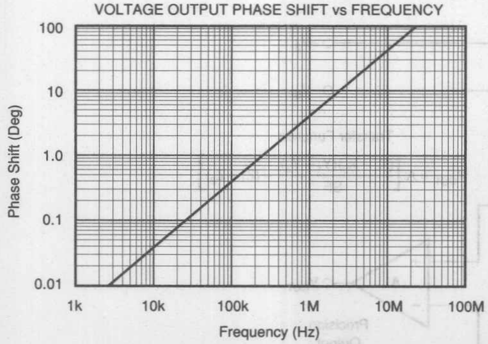
MULTIPLIER GAIN vs FREQUENCY



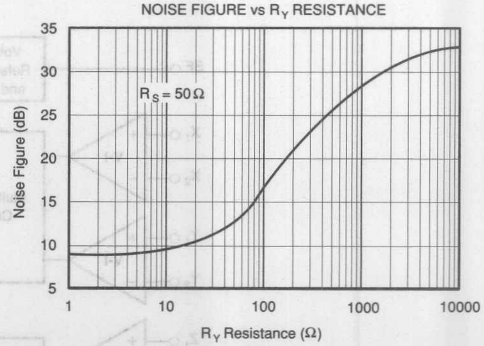
VOLTAGE OUTPUT FREQUENCY RESPONSE



VOLTAGE OUTPUT PHASE SHIFT vs FREQUENCY

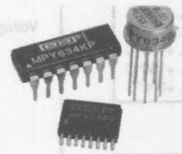


NOISE FIGURE vs R_Y RESISTANCE



BURR - BROWN®

MPY634



ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10636

Wide Bandwidth
PRECISION ANALOG MULTIPLIER

FEATURES

- WIDE BANDWIDTH: 10MHz typ
- ±0.5% MAX FOUR-QUADRANT ACCURACY
- INTERNAL WIDE-BANDWIDTH OP AMP
- EASY TO USE
- LOW COST

APPLICATIONS

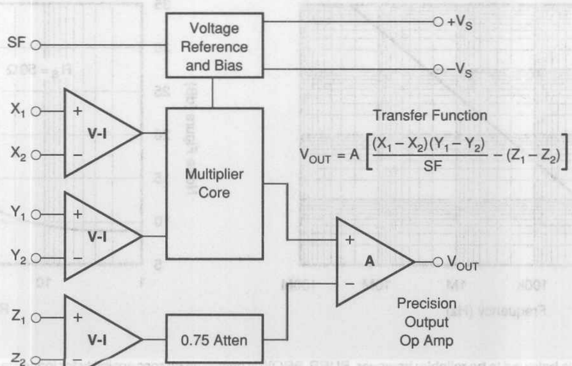
- PRECISION ANALOG SIGNAL PROCESSING
- MODULATION AND DEMODULATION
- VOLTAGE-CONTROLLED AMPLIFIERS
- VIDEO SIGNAL PROCESSING
- VOLTAGE-CONTROLLED FILTERS AND OSCILLATORS

DESCRIPTION

The MPY634 is a wide bandwidth, high accuracy, four-quadrant analog multiplier. Its accurately laser-trimmed multiplier characteristics make it easy to use in a wide variety of applications with a minimum of external parts, often eliminating all external trimming. Its differential X, Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows signal processing at IF, RF, and video frequencies. The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency multipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modulation, and demodulation with excellent carrier rejection.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = ±15VDC, unless otherwise noted.

	MPY634KP/KU			MPY634AM			MPY634BM			MPY634SM			
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE													
Transfer Function		*			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$			*					
Total Error[1]													
(−10V ≤ X, Y ≤ +10V)			±2.0			±1.0			±0.5			*	%
T_A = min to max		±2.5			±1.5			±1.0				±2.0	%
Total Error vs Temperature		±0.03			±0.022			±0.015				±0.02	%/°C
Scale Factor Error													
(SF = 10.000V Nominal)[2]		±0.25			±0.1			*			*		%
Temperature Coefficient of													
Scaling Voltage		±0.02			±0.01			±0.01			*		%/°C
Supply Rejection (±15V ±1V)		*			±0.01			*			*		%
Nonlinearity													
X (X = 20Vp-p, Y = 10V)		*			±0.4			0.2	±0.3		*		%
Y (Y = 20Vp-p, X = 10V)		*			±0.01			*	±0.1		*		%
Feedthrough[3]													
X (Y Nulled, X = 20Vp-p, 50Hz)		*			±0.3			±0.15	±0.3		*		%
Y (X Nulled, Y = 20Vp-p, 50Hz)		*			±0.01			*	±0.1		*		%
Both Inputs (500kHz, 1Vrms)													
Unnulled	40[4]	50		45	55		*	60		*	*		dB
Nulled	55[4]	60		55	65		60	70		*	*		dB
Output Offset Voltage		±50	±100		±5	±30		*	±15		*	*	mV
Output Offset Voltage Drift		*			±200			±100			*	±500	µV/°C
DYNAMICS													
Small Signal BW,													
(V_{OUT} = 0.1Vrms)	6[4]	*		8	10		*	*		6	*		MHz
1% Amplitude Error													
(C_{LOAD} = 1000pF)		*			100			*			*		kHz
Slew Rate (V_{OUT} = 20Vp-p)		*			20			*			*		V/µs
Settling Time													
(to 1%, ΔV_{OUT} = 20V)		*			2			*			*		µs
NOISE													
Noise Spectral Density:													
SF = 10V		*			0.8			*			*		µV/√Hz
Wideband Noise:													
f = 10Hz to 5MHz		*			1			*			*		mVrms
f = 10Hz to 10kHz		*			90			*			*		µVrms
OUTPUT													
Output Voltage Swing	*			±11			*			*			V
Output Impedance (f ≤ 1kHz)		*			0.1			*					Ω
Output Short Circuit Current													
(R_L = 0, T_A = min to max)		*			30			*			*		mA
Amplifier Open Loop Gain													
(f = 50Hz)		*			85			*			*		dB
INPUT AMPLIFIERS (X, Y and Z)													
Input Voltage Range													
Differential V_{IN} (V_{CM} = 0)		*			±12			*			*		V
Common-Mode V_{IN} (V_{DIFF} = 0)		*			±10			*			*		V
(see Typical Performance Curves)													
Offset Voltage X, Y		±25	±100		±5	±20		±2	±10		*	*	mV
Offset Voltage Drift X, Y		200			100			50			*		µV/°C
Offset Voltage Z		±25	±100		±5	±30		±2	±15		*	*	mV
Offset Voltage Drift Z		*			200			100				500	µV/°C
CMRR	*	*		60	80		70	90		*	*		dB
Bias Current		*	*		0.8	2.0		*	*		*	*	µA
Offset Current		*			0.1			*			*	2.0	µA
Differential Resistance		*			10			*					MΩ
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)		*			$10V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			*					
Total Error[1] untrimmed													
(X = 10V, −10V ≤ Z ≤ +10V)		1.5			±0.75			±0.35			±0.75		%
(X = 1V, −1V ≤ Z ≤ +1V)		4.0			±2.0			±1.0			*		%
(0.1V≤ X ≤ 10V, −10V ≤ Z ≤ 10V)		5.0			±2.5			±1.0			*		%
SQUARE PERFORMANCE													
Transfer Function		*			$\frac{(X_1 - X_2)^2}{10V} + Z_2$			*					
Total Error (−10V ≤ X ≤ 10V)		±1.2			±0.6			±0.3			*		%

MPY634

7

SPECIAL FUNCTIONS

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C and V_S = ±15VDC, unless otherwise noted.

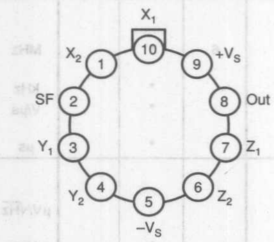
	MPY634KP/KU			MPY634AM			MPY634BM			MPY634SM			
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
SQUARE-ROOTER PERFORMANCE													
Transfer Function ($Z_1 \le Z_2$)		*			$\sqrt{10V\,(Z_2 - Z_1)} + X_2$			*			*		
Total Error(1) ($1V \le Z \le 10V$)		±2.0			±1.0			±0.5			*		%
POWER SUPPLY													
Supply Voltage:													
Rated Performance		*			±15			*			*		VDC
Operating	*		*	±8		±18	*		*	*		±20	VDC
Supply Current, Quiescent		*	*		4	6		*	*		*	*	mA
TEMPERATURE RANGE													
Specification	*(5)		*(5)	–25		+85	*		*	–55		+125	°C
Storage	–40		+85	–65		+150	*		*	*		*	°C

* Specification same as for MPY634AM.

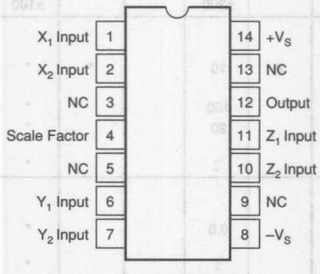
NOTES: (1) Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV). (2) May be reduced to 3V using external resistor between $-V_S$ and SF. (3) Irreducible component due to nonlinearity; excludes effect of offsets. (4) KP grade only. (5) KP grade only. 0°C to +70°C for KU grade.

PIN CONFIGURATIONS

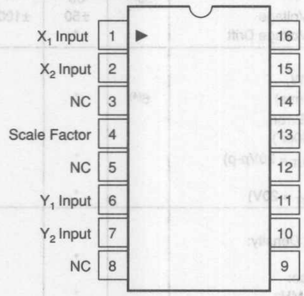
Top View



TO-100: MPY634AM/BM/SM



DIP: MPY634KP



SOIC: MPY634KU

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MPY634AM/BM	MPY634KP/KU	MPY634SM
Power Supply Voltage	±18	*	±20
Power Dissipation	500mW	*	*
Output Short-Circuit to Ground	Indefinite	*	*
Input Voltage (all X, Y and Z)	$\pm V_S$	*	*
Temperature Range:			
Operating	–25°C/+85°C	*	–55°C/+125°C
Storage	–65°C/+150°C	–40°C/+85°C	*
Lead Temperature (soldering, 10s)	+300°C	*	*
SOIC 'KU' Package		+260°C	

* Specification same as for MPY634AM/BM.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPY634KP	14-Pin PDIP	010
MPY634KU	16-Pin SOIC	211
MPY634AM	TO-100	007
MPY634BM	TO-100	007
MPY634SM	TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MPY634 ( ) ( )

Basic Model Number

Performance Grade(1)

K: –25°C to +85°C ('U' package 0°C to +70°C)

A: –25°C to +85°C

B: –25°C to +85°C

S: –55°C to +125°C

Package Code

M: TO-100 Metal

P: Plastic 14-pin DIP

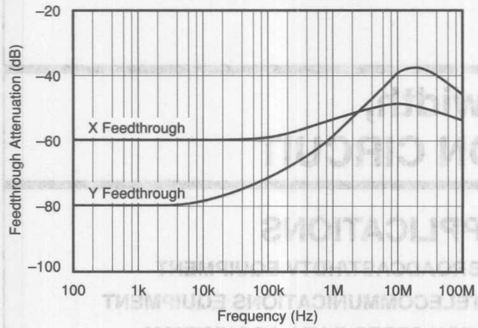
U: 16-pin SOIC

NOTE: (1) Performance grade identifier may not be marked on the SOIC package; a blank denotes "K" grade.

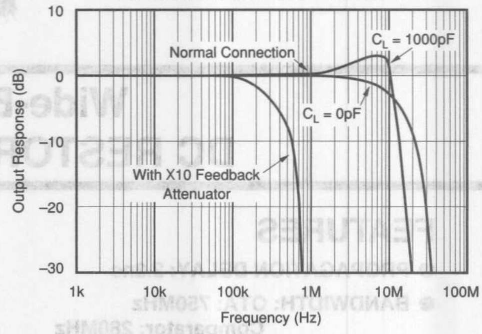
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = \pm15VDC$, unless otherwise noted.

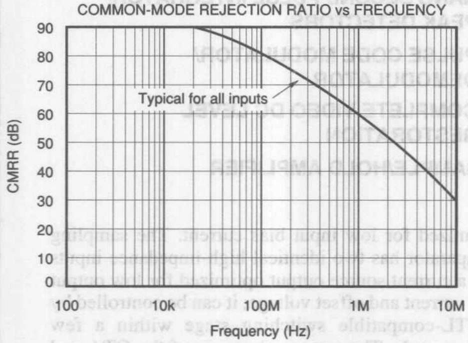
FEEDTHROUGH vs FREQUENCY



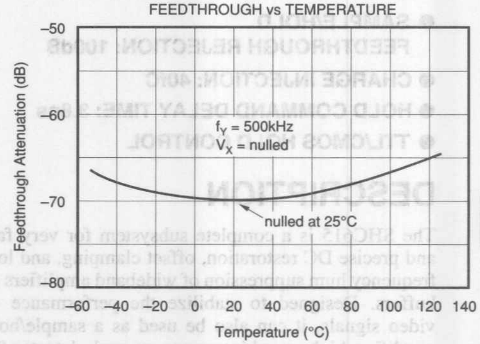
FREQUENCY RESPONSE AS A MULTIPLIER



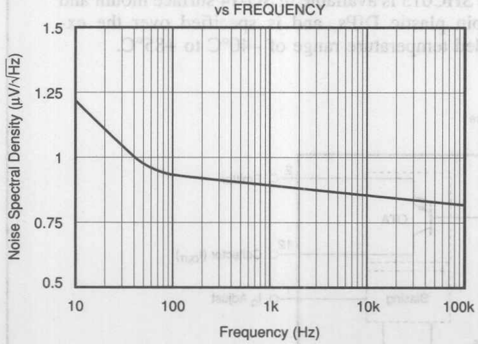
COMMON-MODE REJECTION RATIO vs FREQUENCY



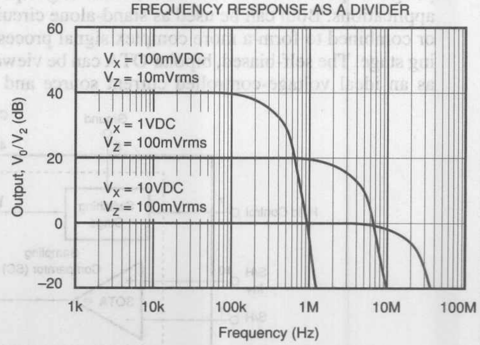
FEEDTHROUGH vs TEMPERATURE



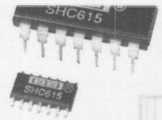
NOISE SPECTRAL DENSITY vs FREQUENCY



FREQUENCY RESPONSE AS A DIVIDER



BURR - BROWN®



SHC615

Wide-Bandwidth, DC RESTORATION CIRCUIT

FEATURES

- PROPAGATION DELAY: 2.2ns
- BANDWIDTH: OTA: 750MHz
  Comparator: 280MHz
- LOW INPUT BIAS CURRENT: –0.3μA
- SAMPLE/HOLD
  SWITCHING TRANSIENTS: +1/–7mV
- SAMPLE/HOLD
  FEEDTHROUGH REJECTION: 100dB
- CHARGE INJECTION: 40fC
- HOLD COMMAND DELAY TIME: 3.8ns
- TTL/CMOS HOLD CONTROL

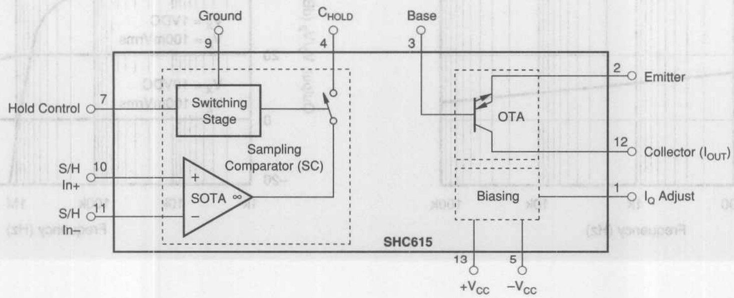
APPLICATIONS

- BROADCAST/HDTV EQUIPMENT
- TELECOMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION
- CAD MONITORS/CCD IMAGE PROCESSING
- NANO SECOND PULSE INTEGRATOR/ PEAK DETECTORS
- PULSE CODE MODULATOR/ DEMODULATOR
- COMPLETE VIDEO DC LEVEL RESTORATION
- SAMPLE/HOLD AMPLIFIER

DESCRIPTION

The SHC615 is a complete subsystem for very fast and precise DC restoration, offset clamping, and low frequency hum suppression of wideband amplifiers or buffers. Designed to stabilize the performance of video signals, it can also be used as a sample/hold amplifier, high-speed integrator, or peak detector for nanosecond pulses. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and fast sampling comparator set a new standard for high-speed applications. Both can be used as stand-alone circuits or combined to form a more complex signal processing stage. The self-biased, bipolar OTA can be viewed as an ideal voltage-controlled current source and is optimized for low input bias current. The sampling comparator has two identical high-impedance inputs and a current source output optimized for low output bias current and offset voltage; it can be controlled by a TTL-compatible switching stage within a few nanoseconds. The transconductance of the OTA and sampling comparator can be adjusted by an external resistor, allowing bandwidth, quiescent current, and gain tradeoffs to be optimized.

The SHC615 is available in SO-14 surface mount and 14-pin plastic DIPs, and is specified over the extended temperature range of –40°C to +85°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

DC SPECIFICATIONS

At V_{CC} = ±5V, R_{LOAD} = 100Ω, R_Q = 300Ω, R_{IN} = 150Ω and T_A = +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU MIN	TYP	MAX	UNITS
OFFSET VOLTAGE, V_E at V_B = 0					
Initial			8	±40	mV
vs Temperature			40		µV/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V	50	55		dB
B-INPUT BIAS CURRENT					
Initial			–0.3	±0.9	µA
vs Temperature			1		nA/°C
C-OUTPUT BIAS CURRENT, I_C at V_B = 0					
Initial		–200	–77	+100	µA
B-INPUT IMPEDANCE			4.4		MΩ
INPUT NOISE					
Voltage Noise Density, B-to-E	f_{OUT} = 100kHz to 100MHz		2.2		nV/√Hz
Voltage Noise Density, B-to-C	f_{OUT} = 100kHz to 100MHz		4.5		nV/√Hz
INPUT VOLTAGE RANGE			±3.4		V
OUTPUT					
Output Voltage Compliance			±3.2		V
C-Current Output		±18	±20		mA
E-Current Output		±18	±20		mA
C-Output Impedance			0.5		MΩ
E-Output Impedance			12		Ω
Open-Loop Gain			96		dB
TRANSCONDUCTANCE	Small Signal, <200mV		70		mA/V

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

DC SPECIFICATIONS (CONT)

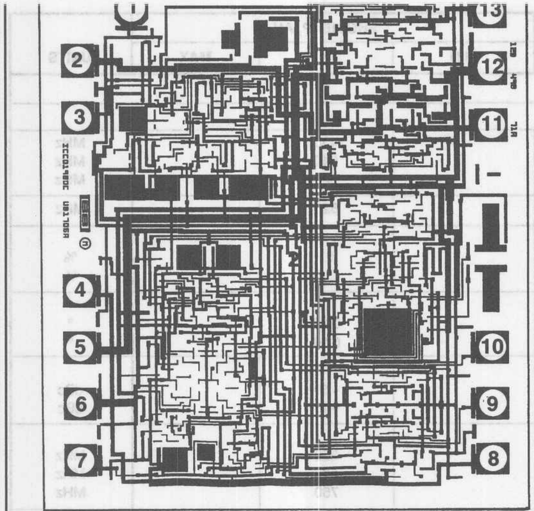
At $V_{CC} = \pm5V$, $R_{LOAD} = 1k\Omega$, $R_Q = 300\Omega$, and $T_A = +25°C$, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU MIN	TYP	MAX	UNITS
INPUT BIAS CURRENT					
Initial			1.0	±5	µA
vs Temperature			–2.3		nA/°C
C-OUTPUT BIAS CURRENT					
Initial			±10	±50	µA
vs Temperature			±13		nA/°C
INPUT IMPEDANCE					
Input Impedance			0.2		MΩ
INPUT NOISE					
Voltage Noise Density	f_{OUT} = 100kHz to 100MHz		5		$nV/\sqrt{Hz}$
INPUT VOLTAGE RANGE					
Input Voltage Range			±3.0		V
Common-Mode Input Range			±3.2		V
OUTPUT					
Output Voltage Compliance			±3.5		V
C-Current Output		±2.5	±3.2		mA
C-Output Impedance			620 || 2		kΩ || pF
Open-Loop Gain			83		dB
TRANSCONDUCTANCE					
Transconductance			22		mA/V
HOLD CONTROL					
Logic 1 Voltage		+2		$+V_{CC}$ +0.6	V
Logic 0 Voltage		0		0.8	V
Logic 1 Current	V Hold Control = 5.0V		1		µA
Logic 0 Current	V Hold Control = 0.8V		0.05		µA
TRANSFER CHARACTERISTICS					
Charge Injection	Track-To-Hold		40		fC
Feedthrough Rejection	Hold Mode		–100		dB
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	R_Q = 300Ω	±12	±15	±18	mA
Quiescent Current Range	Programmable (Useful Range)		±3 to ±36		mA
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–40		+125	°C

AC SPECIFICATIONS

At $V_{CC} = \pm5V$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_Q = 300\Omega$, and $T_A = +25°C$, unless otherwise specified.

		SHC615AP, AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
FREQUENCY DOMAIN					
OTA					
LARGE-SIGNAL BANDWIDTH (–3dB), (B-to-E)	$V_{OUT} = 5.0Vp\text{-}p$ $V_{OUT} = 2.8Vp\text{-}p$ $V_{OUT} = 1.4Vp\text{-}p$		430 540 620		MHz MHz MHz
SMALL-SIGNAL BANDWIDTH B-TO-E	$V_{OUT} = 0.2Vp\text{-}p$		520		MHz
DIFFERENTIAL GAIN (B-TO-E)	f = 4.43MHz, $V_{OUT} = 0.7Vp\text{-}p$, $R_L = 150\Omega$ $R_L = 500\Omega$		1.8 0.1		% %
DIFFERENTIAL PHASE (B-TO-E)	f = 4.43MHz, $V_{OUT} = 0.7Vp\text{-}p$, $R_L = 150\Omega$ $R_L = 500\Omega$		0.07 0.01		° °
HARMONIC DISTORTION (B-TO-E) Second Harmonic Third Harmonic	f = 30MHz, $V_{OUT} = 1.4Vp\text{-}p$		–50 –46		dBc dBc
LARGE SIGNAL BANDWIDTH (–3dB), (B-to-C)	$V_{OUT} = 5.0Vp\text{-}p$ $V_{OUT} = 2.8Vp\text{-}p$ $V_{OUT} = 1.4Vp\text{-}p$		250 580 750		MHz MHz MHz
SMALL SIGNAL BANDWIDTH B-to-C	$V_{OUT} = 0.2Vp\text{-}p$		680		MHz
COMPARATOR	Sample Mode				
BANDWIDTH (–3dB)	$I_{OUT} = 4mAp\text{-}p$ $I_{OUT} = 2mAp\text{-}p$ $I_{OUT} = 1mAp\text{-}p$		240 270 280		MHz MHz MHz
TIME DOMAIN					
OTA					
RISE TIME	2Vp-p Step, 10% to 90% B-to-E B-to-C		1.1 1.2		ns ns
SLEW RATE	2Vp-p,B-to-E B-to-C 5Vp-p,B-to-E B-to-C		1800 1700 3300 3000		V/µs V/µs V/µs V/µs
COMPARATOR					
RISE TIME (Sample Mode)	10% to 90%, $R_L = 50\Omega$, $I_{OUT} = \pm2mA$ $C_{LOAD} = 1pF$		2.5		ns
SLEW RATE (Sample Mode)	10% to 90%, $R_L = 50\Omega$, $I_{OUT} = \pm2mA$ $C_{LOAD} = 1pF$		0.95		mA/ns
DYNAMIC CHARACTERISTICS Propagation Delay Time Propagation Delay Time Delay Time	t_{PDH}, $V_{OD} = 200mV$ t_{PDL}, $V_{OD} = 200mV$ Sample-to-Hold Hold-to-Sample		2.2 2.15 3.8 3.0		ns ns ns ns



SHC615 DIE TOPOGRAPHY

1	I_Q Adjust
2	OTA-Emitter
3	OTA-Base
4	C_{HOLD}
5	–5V Supply, Analog
6	–5V Supply, Digital
7	Hold Control
8	Ground
9	S/H In+
10	S/H In–
11	I_{OUT}, OTA-Collector
12	+5V Supply, Analog
13	+5V Supply, Digital

Substrate Bias: Negative Supply.
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

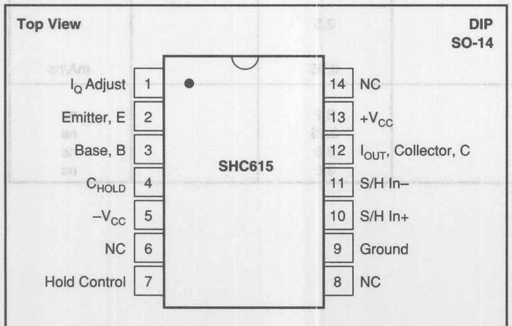
	MILS (0.001")	MILLIMETERS
Die Size	73 x 81, ±5	1.86 x 2.06, ±0.13
Die Thickness	14, ±1	0.55, ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, –0.0	0.0005, +0.0013, –0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (±V_{CC}) .... ±6V
Input Voltage[1] .... ±V_{CC} ±0.7V
Operating Temperature .... –40°C to +85°C
Storage Temperature .... –40°C to +125°C
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) .... +300°C
Hold Control .... –0.5V to +V_{CC} +0.7V

NOTE: (1) Inputs are internally diode-clamped to ±V_{CC}.

PIN CONFIGURATION



PACKAGE INFORMATION

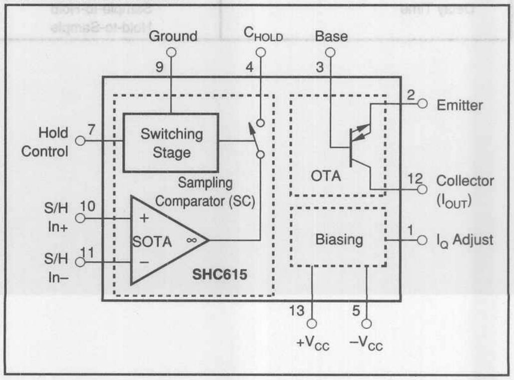
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
SHC615AP	Plastic 14-Pin DIP	010
SHC615AU	SO 14-Pin Surface Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

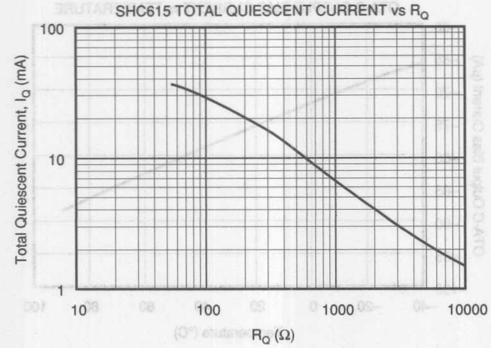
MODEL	PACKAGE	TEMPERATURE
SHC615AP	Plastic 14-Pin DIP	–40°C to +85°C
SHC615AU	SO 14-Pin Surface Mount	–40°C to +85°C

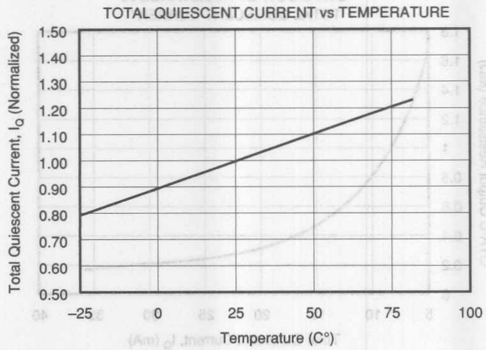
BLOCK DIAGRAM



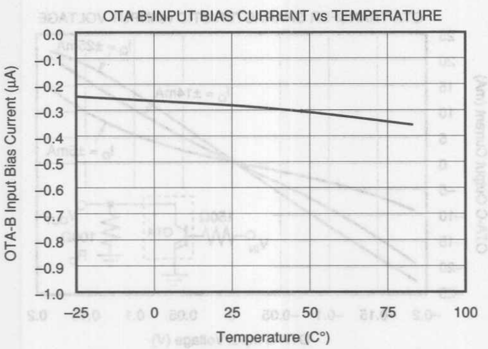
TYPICAL PERFORMANCE CURVES

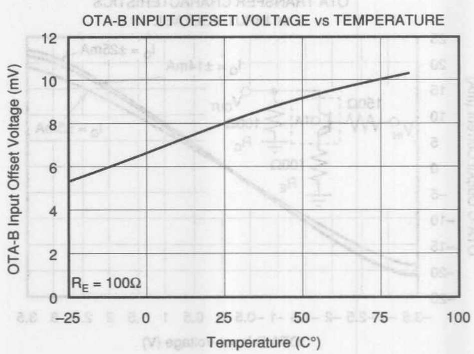
$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm 5V$ unless otherwise noted.

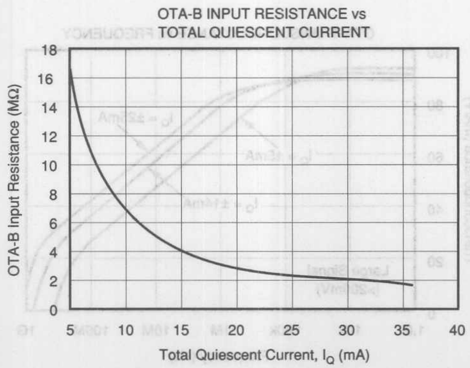


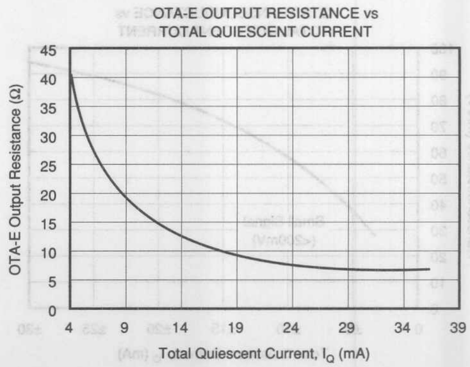


OPERATIONAL TRANSCONDUCTANCE AMPLIFIER





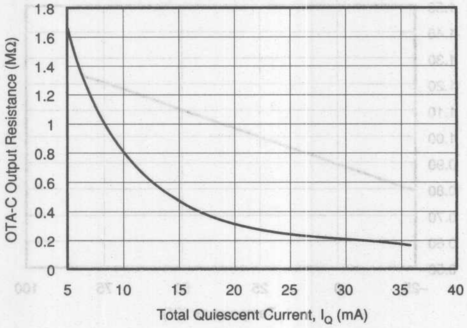




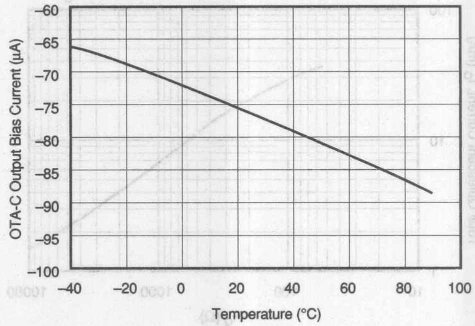
TYPICAL PERFORMANCE CURVES (CONT)

$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

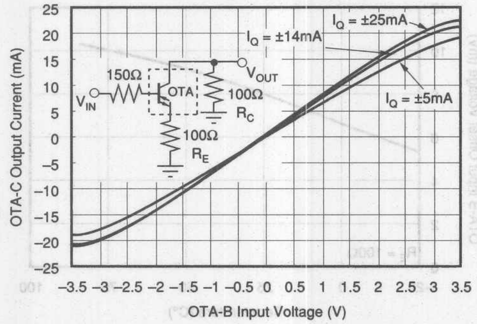
OTA-C OUTPUT RESISTANCE vs TOTAL QUIESCENT CURRENT



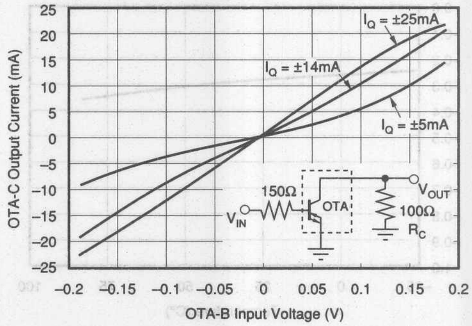
OTA-C OUTPUT BIAS CURRENT vs TEMPERATURE



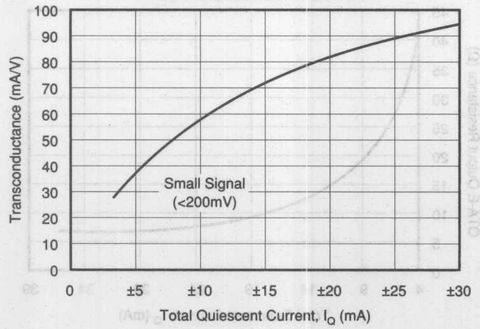
OTA TRANSFER CHARACTERISTICS vs INPUT VOLTAGE



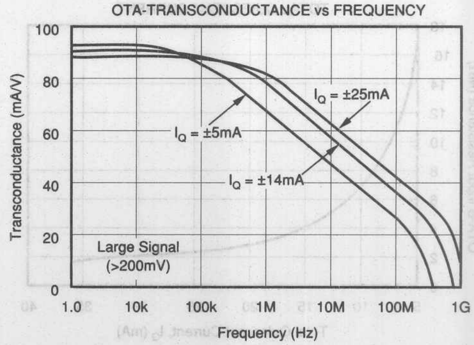
OTA TRANSFER CHARACTERISTIC vs INPUT VOLTAGE



OTA TRANSCONDUCTANCE vs TOTAL QUIESCENT CURRENT



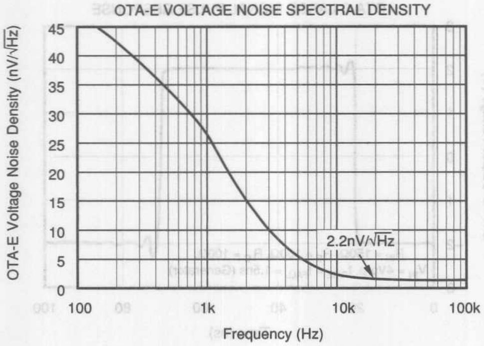
OTA-TRANSCONDUCTANCE vs FREQUENCY



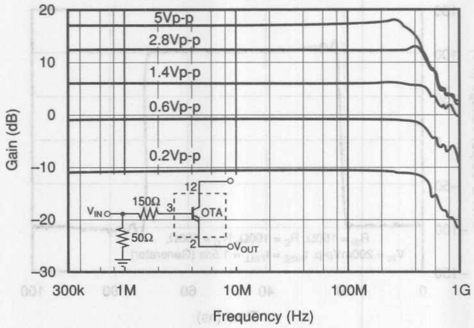
TYPICAL PERFORMANCE CURVES (CONT)

$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

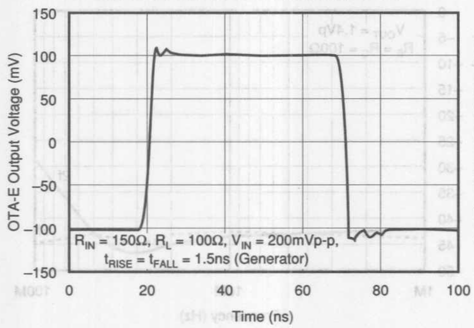
OTA-E VOLTAGE NOISE SPECTRAL DENSITY



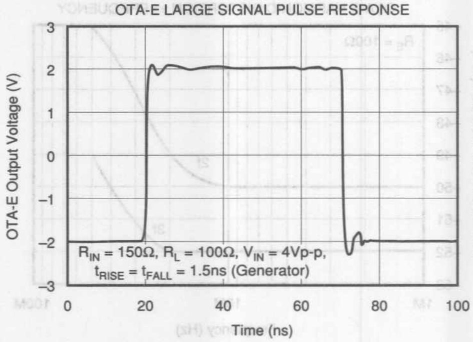
OTA-E FREQUENCY RESPONSE



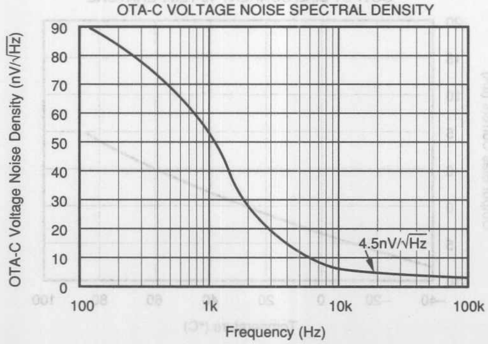
OTA-E SMALL SIGNAL PULSE RESPONSE



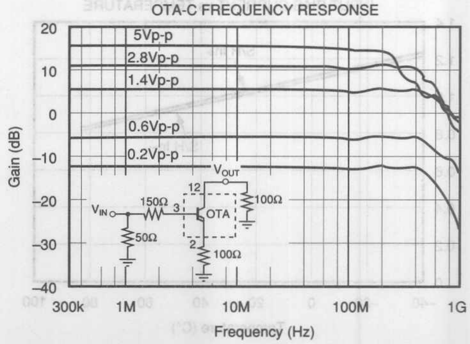
OTA-E LARGE SIGNAL PULSE RESPONSE



OTA-C VOLTAGE NOISE SPECTRAL DENSITY



OTA-C FREQUENCY RESPONSE

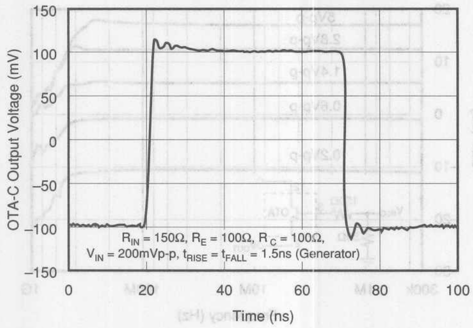


SHC615

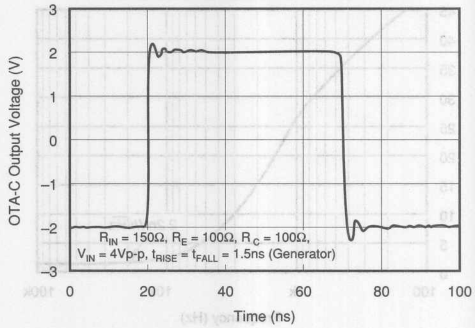
7

SPECIAL FUNCTIONS

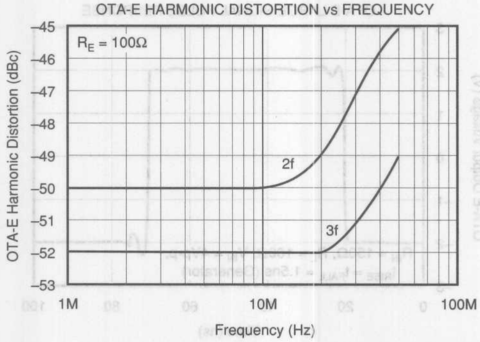
OTA-C SMALL SIGNAL PULSE RESPONSE



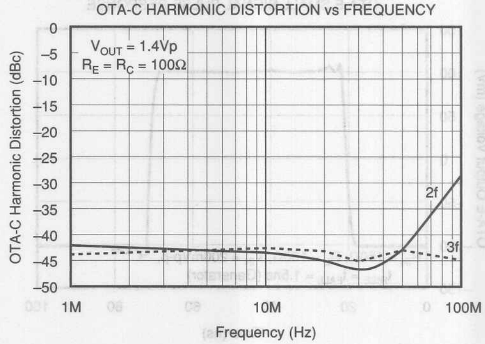
OTA-C LARGE SIGNAL PULSE RESPONSE



OTA-E HARMONIC DISTORTION vs FREQUENCY

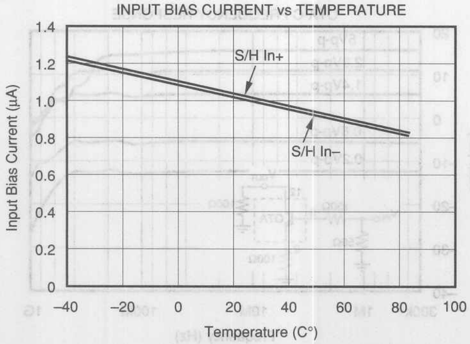


OTA-C HARMONIC DISTORTION vs FREQUENCY

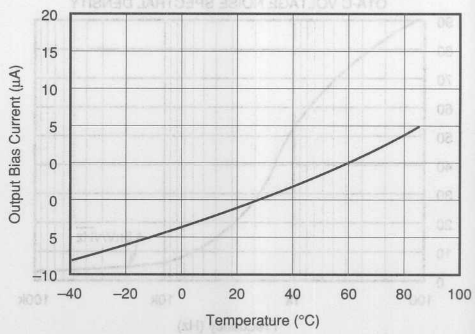


SAMPLING COMPARATOR

INPUT BIAS CURRENT vs TEMPERATURE

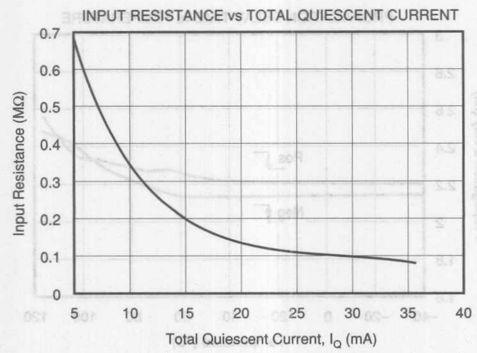


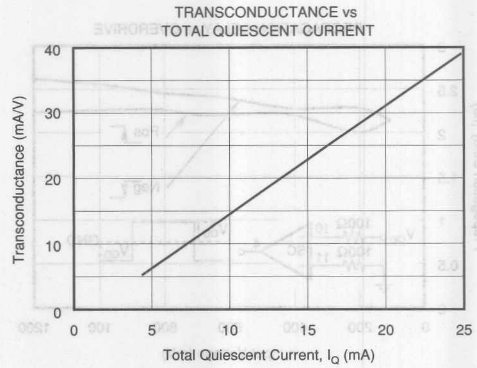
OUTPUT BIAS CURRENT vs TEMPERATURE

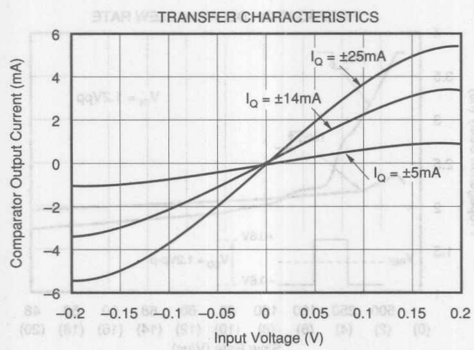


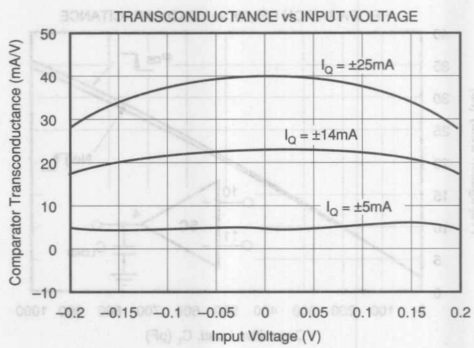
TYPICAL PERFORMANCE CURVES (CONT)

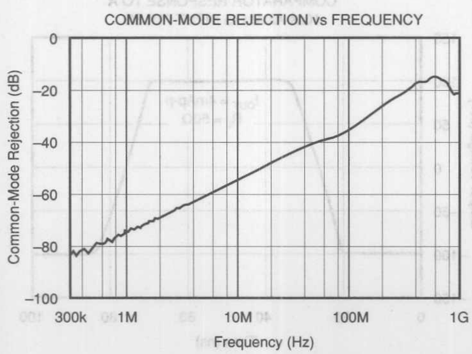
$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

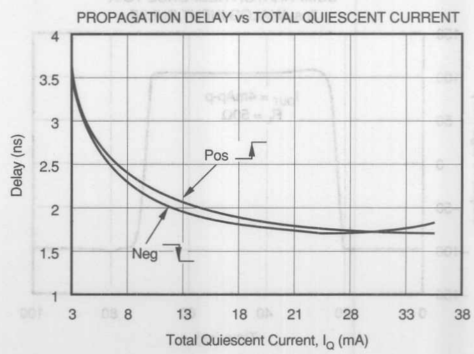












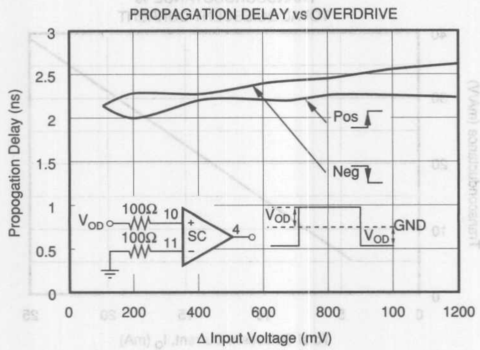
SHC615

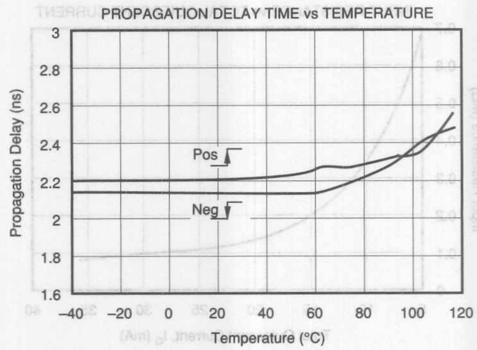
7

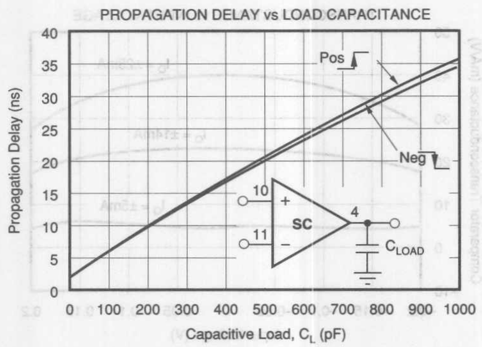
SPECIAL FUNCTIONS

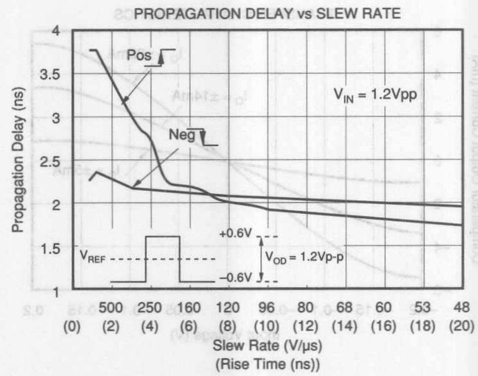
TYPICAL PERFORMANCE CURVES (CONT)

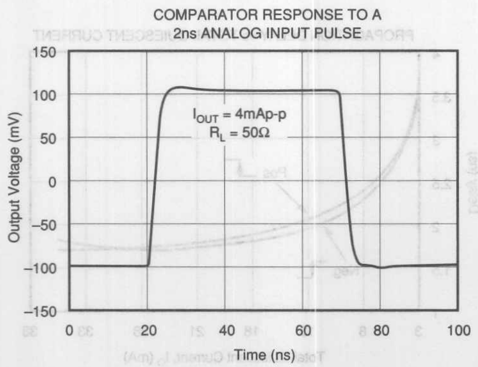
$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

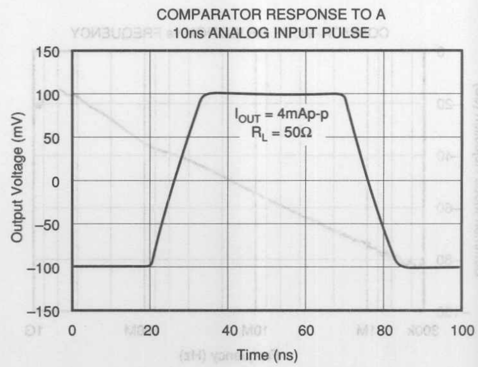








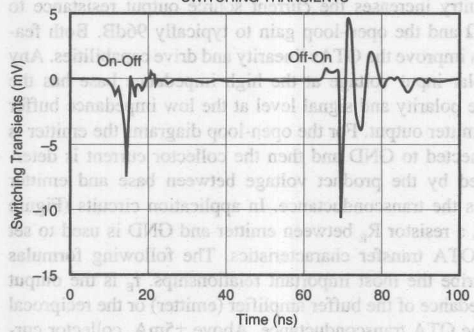




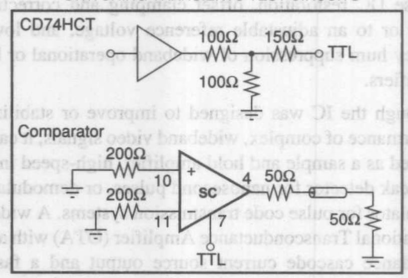
TYPICAL PERFORMANCE CURVES (CONT)

$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

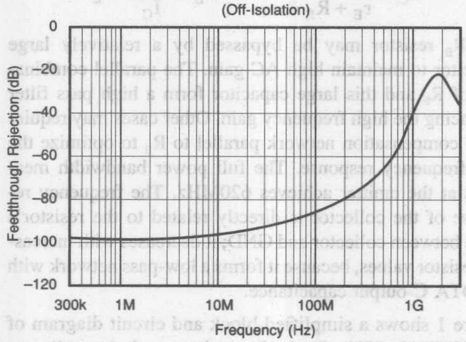
SWITCHING TRANSIENTS



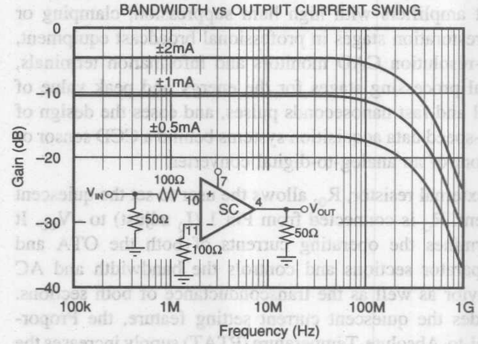
SWITCHING TRANSIENTS TEST CIRCUITS



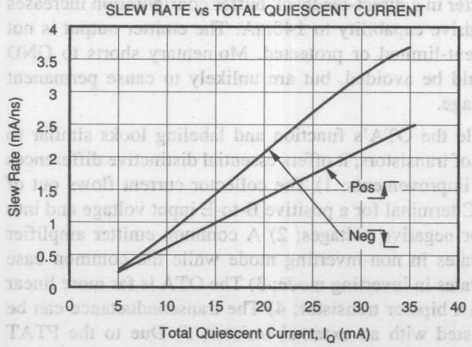
FEEDTHROUGH REJECTION vs FREQUENCY
(Off-Isolation)



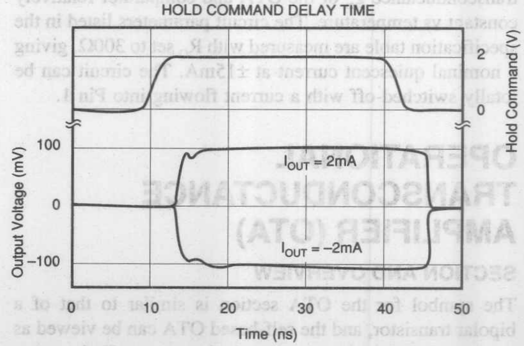
BANDWIDTH vs OUTPUT CURRENT SWING



SLEW RATE vs TOTAL QUIESCENT CURRENT



HOLD COMMAND DELAY TIME



PERFORMANCE

The SHC615, which contains a wideband Operational Transconductance Amplifier and a fast sampling comparator, represents a complete subsystem for very fast and precise DC restoration, offset clamping and correction to GND or to an adjustable reference voltage, and low frequency hum suppression of wideband operational or buffer amplifiers.

Although the IC was designed to improve or stabilize the performance of complex, wideband video signals, it can also be used as a sample and hold amplifier, high-speed integrator, peak detector for nanosecond pulses, or demodulator or modulator for pulse code transmission systems. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and a fast and precise sampling comparator set a new standard for high-speed sampling applications.

Both can be used as stand-alone circuits or combined to create more complex signal processing stages like sample and hold amplifiers. The SHC615 simplifies the design of input amplifiers with high hum suppression, clamping or DC-restoration stages in professional broadcast equipment, high-resolution CAD monitors and information terminals, signal processing stages for the energy and peak value of small and fast nanoseconds pulses, and eases the design of high-speed data acquisition systems behind a CCD sensor or in front of an analog-to-digital converter.

An external resistor, R_Q, allows the user to set the quiescent current. R_Q is connected from Pin 1 (I_Q adjust) to $-V_{CC}$. It determines the operating currents of both the OTA and comparator sections and controls the bandwidth and AC behavior as well as the transconductance of both sections. Besides the quiescent current setting feature, the Proportional-to-Absolute-Temperature (PTAT) supply increases the quiescent current vs temperature and keeps it constant over a wide range of input voltages. This variation holds the transconductance g_m of the OTA and comparator relatively constant vs temperature. The circuit parameters listed in the specification table are measured with R_Q set to 300Ω, giving a nominal quiescent current at ±15mA. The circuit can be totally switched-off with a current flowing into Pin 1.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

SECTION AND OVERVIEW

The symbol for the OTA section is similar to that of a bipolar transistor, and the self-based OTA can be viewed as a quasi-ideal transistor or as a voltage-controlled current source. Application circuits for the OTA look and operate much like transistor circuits—the bipolar transistor, also, is a voltage-controlled current source. Like a transistor, it has three terminals: a high-impedance input (base) optimized for a low input bias current of 0.3μA, a low-impedance input/

The OTA consists of a complementary buffer amplifier and a subsequent complementary current mirror. The buffer amplifier features a Darlington output stage and the current mirror has a cascoded output. The addition of this cascode circuitry increases the current source output resistance to 1MΩ and the open-loop gain to typically 96dB. Both features improve the OTAs linearity and drive capabilities. Any bipolar input voltage at the high impedance base has the same polarity and signal level at the low impedance buffer or emitter output. For the open-loop diagrams the emitter is connected to GND and then the collector current is determined by the product voltage between base and emitter times the transconductance. In application circuits (Figure 2b.), a resistor R_E between emitter and GND is used to set the OTA transfer characteristics. The following formulas describe the most important relationships. r_E is the output impedance of the buffer amplifier (emitter) or the reciprocal of the OTA transconductance. Above ±5mA, collector current, I_C, will be slightly less than indicated by the formula.

$$I_C = \frac{V_{IN}}{r_E + R_E} \qquad R_E = \frac{V_{IN}}{I_C} - r_E$$

The R_E resistor may be bypassed by a relatively large capacitor to maintain high AC gain. The parallel combination of R_E and this large capacitor form a high pass filter enhancing the high frequency gain. Other cases may require a RC compensation network parallel to R_E to optimize the high-frequency response. The full power bandwidth measured at the emitter achieves 620MHz. The frequency response of the collector is directly related to the resistor's value between collector and GND; it decreases with increasing resistor values, because it forms a low-pass network with the OTA C-output capacitance.

Figure 1 shows a simplified block and circuit diagram of the SHC615 OTA. Both the emitter and the collector outputs offer a drive capability of ±20mA for driving low impedance lines or inputs. Connecting the collector to the emitter in a direct-feedback buffer configuration increases the drive capability to ±40mA. The emitter output is not current-limited or protected. Momentary shorts to GND should be avoided, but are unlikely to cause permanent damage.

While the OTA's function and labeling looks similar to that of transistors, it offers essential distinctive differences and improvements: 1) The collector current flows out of the C terminal for a positive B-to-E input voltage and into it for negative voltages; 2) A common emitter amplifier operates in non-inverting mode while the common base operates in inverting mode; 3) The OTA is far more linear than a bipolar transistor; 4) The transconductance can be adjusted with an external resistor; 5) Due to the PTAT biasing characteristic the quiescent current increases as shown in the typical performance curve vs temperature and keeps the AC performance constant; 6) The OTA is self-biased and bipolar; and, 7) The output current is zero for zero differential input voltages. AC inputs centered at zero produce an output current centered at zero.

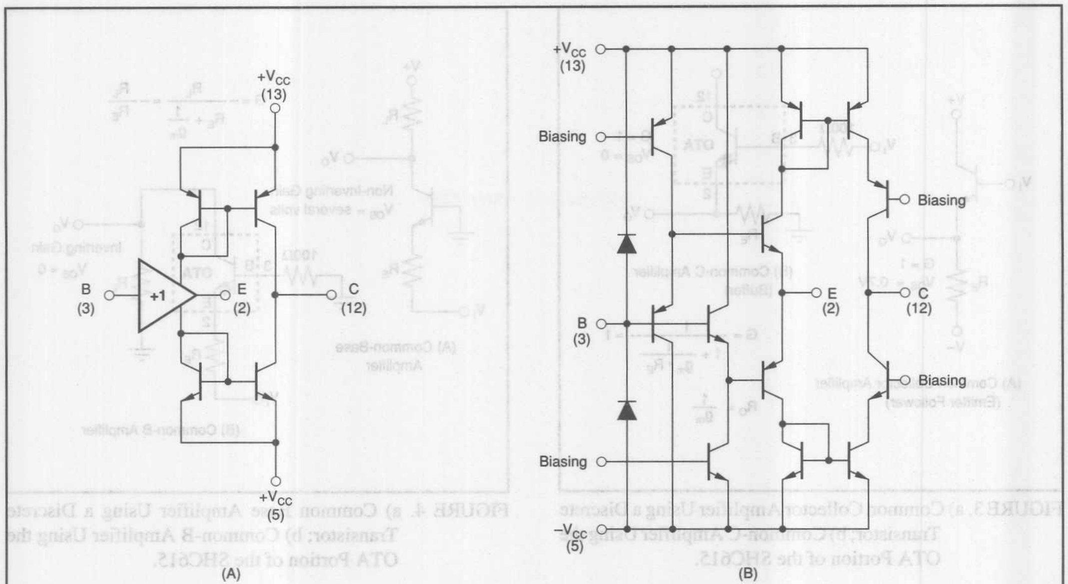


FIGURE 1. a) Simplified Block; and, b) Circuit Diagram of the OTA Section.

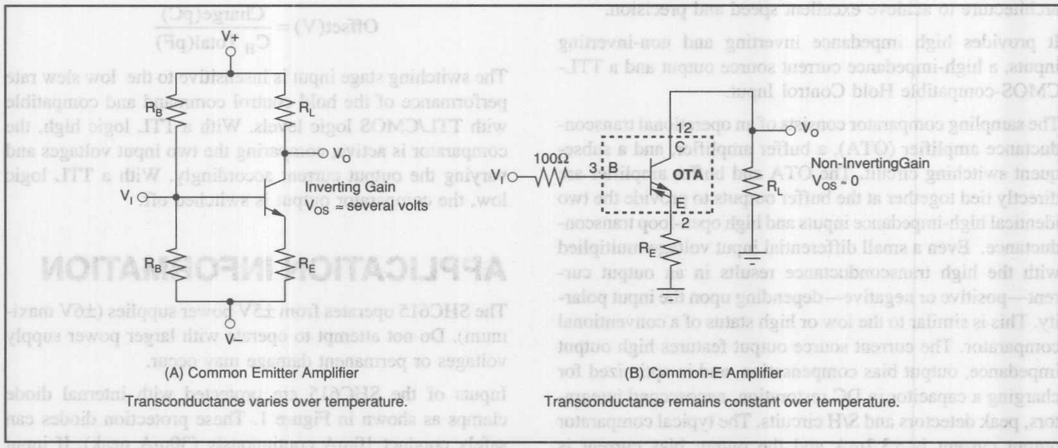


FIGURE 2. a) Common Emitter Amplifier Using a Discrete Transistor; b) Common-E Amplifier Using the OTA Portion of the SHC615.

BASIC APPLICATIONS CIRCUITS

Most application circuits for the OTA section consist of a few basic types which are best understood by analogy to discrete transistor circuits. Just as the transistor has three basic operating modes—common emitter, common base, and common collector—the OTA has three equivalent operating modes common-E, common-B, and common-C (See Figures 2, 3 and 4). Figure 2 shows the OTA connected as a Common-E amplifier which is equivalent to a common emitter transistor amplifier. Input and output can be ground referenced without any biasing. Due to the sense of the output current, the amplifier is non-inverting.

Figure 4 shows the common-B amplifier. This configuration produces an inverting gain, and the input is low-impedance. When a high impedance input is needed, it can be created by inserting a buffer amplifier like BUF600 in series.

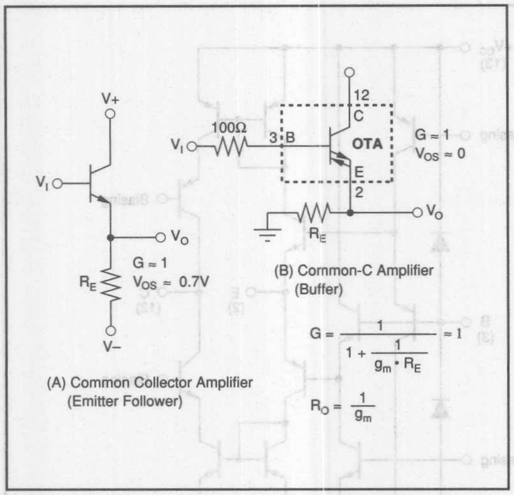


FIGURE 3. a) Common Collector Amplifier Using a Discrete Transistor; b) Common-C Amplifier Using the OTA Portion of the SHC615.

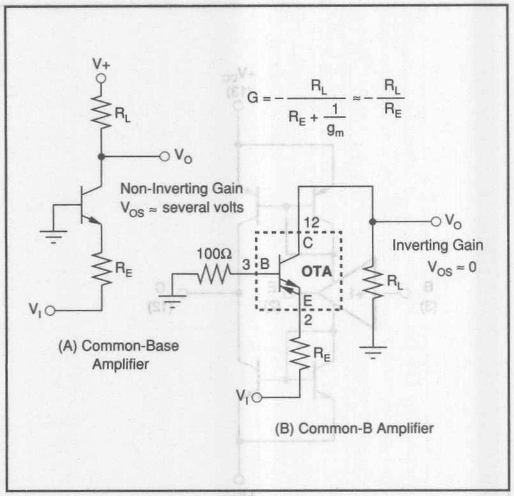


FIGURE 4. a) Common Base Amplifier Using a Discrete Transistor; b) Common-B Amplifier Using the OTA Portion of the SHC615.

SAMPLING COMPARATOR

The SHC615 sampling comparator features a very short 2.2ns propagation delay and utilizes a new switching circuit architecture to achieve excellent speed and precision.

It provides high impedance inverting and non-inverting inputs, a high-impedance current source output and a TTL-CMOS-compatible Hold Control Input.

The sampling comparator consists of an operational transconductance amplifier (OTA), a buffer amplifier, and a subsequent switching circuit. The OTA and buffer amplifier are directly tied together at the buffer outputs to provide the two identical high-impedance inputs and high open-loop transconductance. Even a small differential input voltage multiplied with the high transconductance results in an output current—positive or negative—depending upon the input polarity. This is similar to the low or high status of a conventional comparator. The current source output features high output impedance, output bias compensation, and is optimized for charging a capacitor in DC restoration, nanosecond integrators, peak detectors and S/H circuits. The typical comparator output current is ±3.2mA and the output bias current is minimized to typically ±10μA in the sampling mode.

This innovative circuit achieves the slew rate representatives of an open-loop design. In addition, the acquisition slew current for a hold or storage capacitor is higher than standard diode bridge and switch configurations, removing a main contributor to the limits of maximum sampling rate and input frequency.

The switching circuits in the SHC615 use current steering (versus voltage switching) to provide improved isolation between the switch and analog sections. This results in low aperture time sensitivity to the analog input signal, reduced power supply and analog switching noise. Sample-to-hold peak switching is 40fC.

The additional offset voltage or switching transient induced on a capacitor at the current source output by the switching charge can be determined by the following formula:

$$\text{Offset(V)} = \frac{\text{Charge(pC)}}{C_H \text{ Total(pF)}}$$

The switching stage input is insensitive to the low slew rate performance of the hold control command and compatible with TTL/CMOS logic levels. With a TTL logic high, the comparator is active, comparing the two input voltages and varying the output current accordingly. With a TTL logic low, the comparator output is switched off.

APPLICATION INFORMATION

The SHC615 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur.

Inputs of the SHC615 are protected with internal diode clamps as shown in Figure 1. These protection diodes can safely conduct 10mA continuously (30mA peak). If input voltages can exceed the power supply voltages by 0.7V, the input signal current must be limited.

BASIC CONNECTIONS

Figure 6 shows the basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best. See "Circuit Layout" at the end of the applications discussion for further suggestions on layout.

If the high speed TTL-hold command signal goes negative due to reflections for AC-coupling, the hold control input must be protected by an external reverse bias diode to ground as shown in Figure 6.

CIRCUIT LAYOUT

The high-frequency performance of the SHC615 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions, not as absolute requirements. Oscillations, ringing, poor bandwidth, poor settling, and peaking are all typical problems that plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2μF); parallel 470pF and/or 10nF ceramic chip capacitors may be added if desired. Surface mount types are recommended because of their low lead inductance. Supply bypassing is extremely critical at high frequencies and when driving high current loads.
- PC board traces for power lines should be wide to reduce impedance.

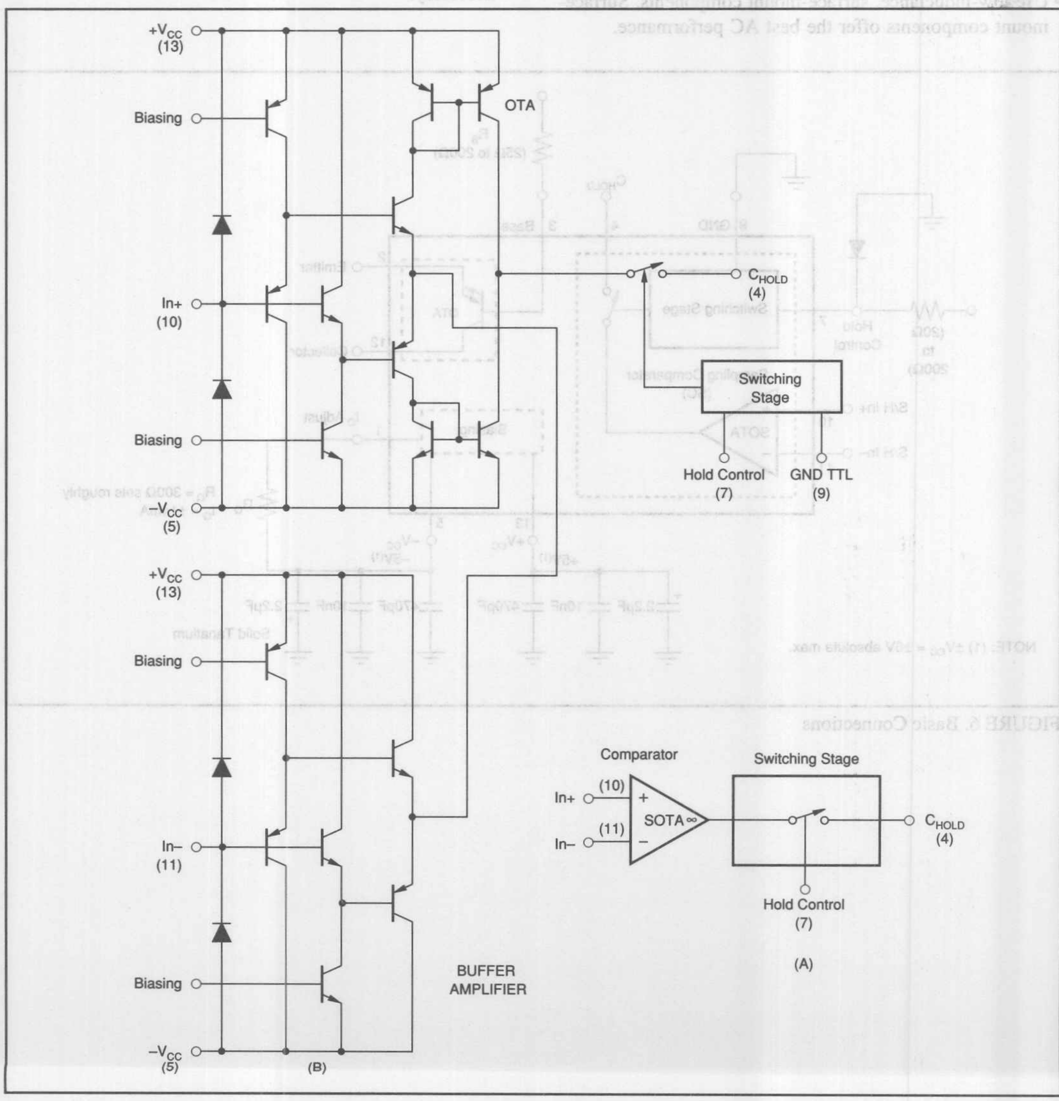


FIGURE 5. a) Simplified Block Diagram; and, b) Circuit Diagram of the Sampling Comparator which Includes the Sampling Operational Transconductance Amplifier (SOTA) and the Switching Stage.

- Use a low-impedance ground plane on the component side to ensure that a low-impedance ground is available throughout the layout.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances such as the amplifier's input terminals.
- Sockets are not recommended since they add significant inductance and parasitic capacitance. If sockets are required, use zero-profile sockets.
- Use low-inductance, surface-mount components. Surface-mount components offer the best AC performance.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.
- Terminate transmission line loads. Unterminated lines, such as box cables, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.
- Protect the hold control input with an external diode if necessary.

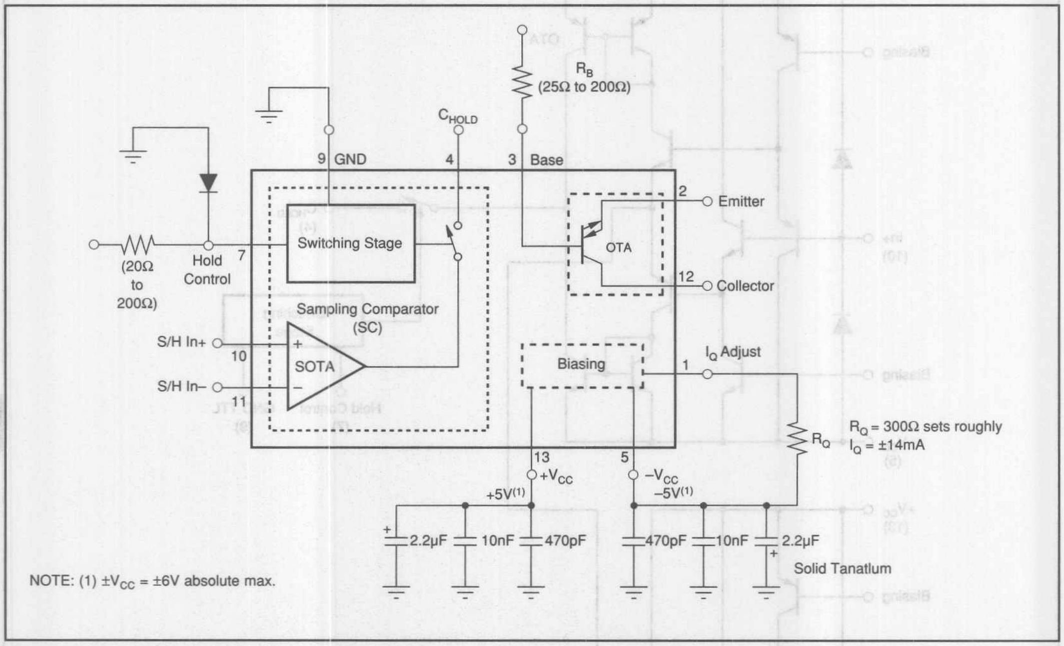


FIGURE 6. Basic Connections

TYPICAL APPLICATIONS

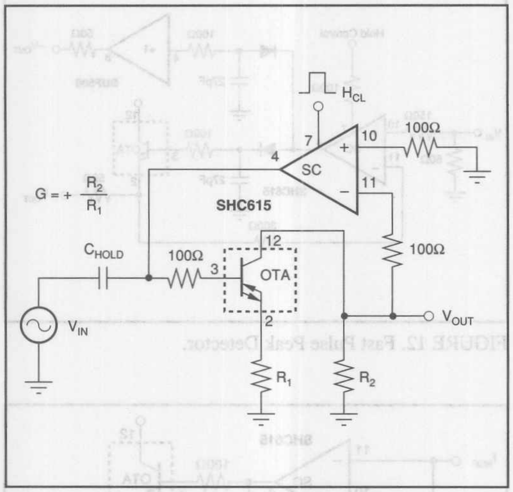


FIGURE 7. Complete DC Restoration System.

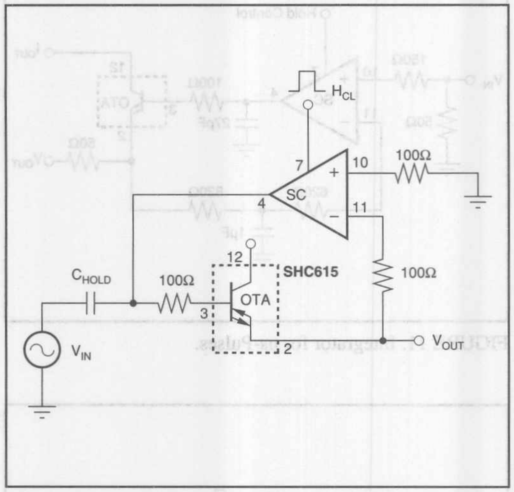


FIGURE 8. DC Restoration of a Buffer Amplifier.

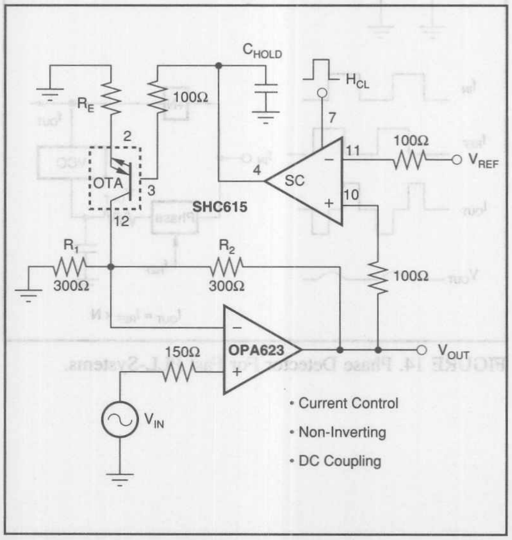


FIGURE 9. Clamped Video/RF Amplifier.

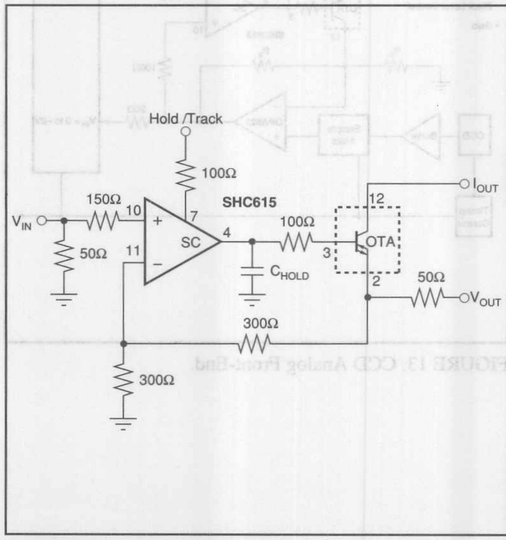


FIGURE 10. Sample/Hold Amplifier.

SHC615

7

SPECIAL FUNCTIONS

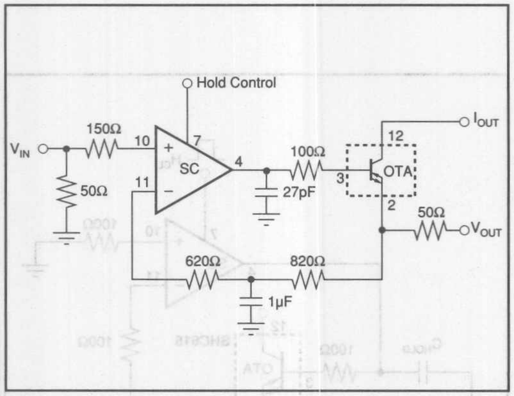


FIGURE 11. Integrator for ns-Pulses.

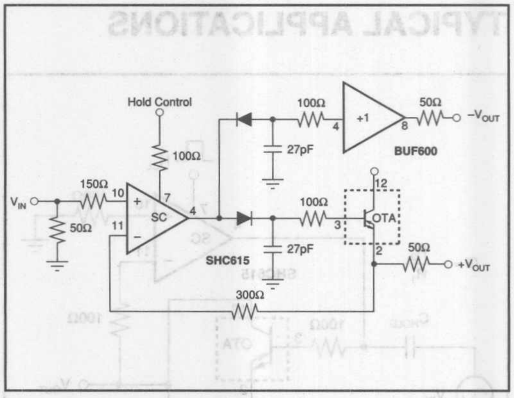


FIGURE 12. Fast Pulse Peak Detector.

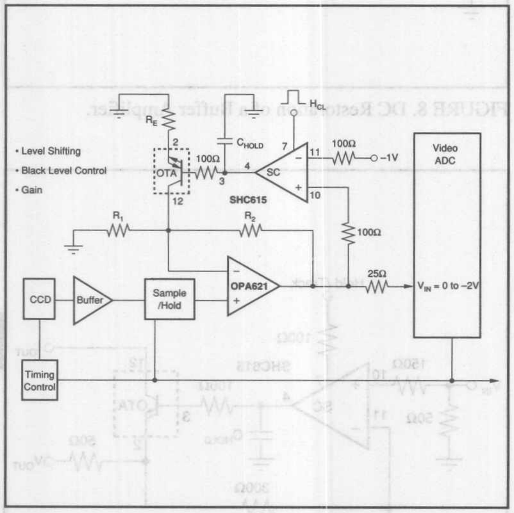


FIGURE 13. CCD Analog Front-End.

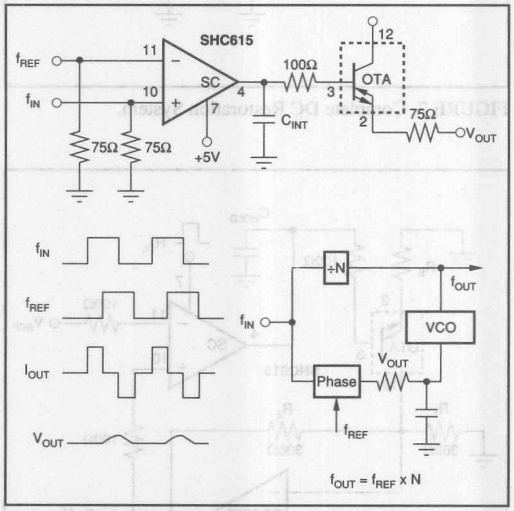
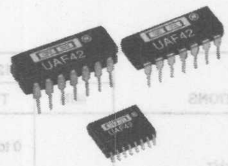


FIGURE 14. Phase Detector For Fast PLL-Systems.

BURR - BROWN®

BB



UAF42

UNIVERSAL ACTIVE FILTER

FEATURES

- VERSATILE— LOW-PASS, HIGH-PASS BAND-PASS, BAND-REJECT
- SIMPLE DESIGN PROCEDURE
- ACCURATE FREQUENCY AND Q — INCLUDES ON CHIP 1000pF ±0.5% CAPACITORS

APPLICATIONS

- TEST EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEMS
- MONOLITHIC REPLACEMENT FOR UAF41

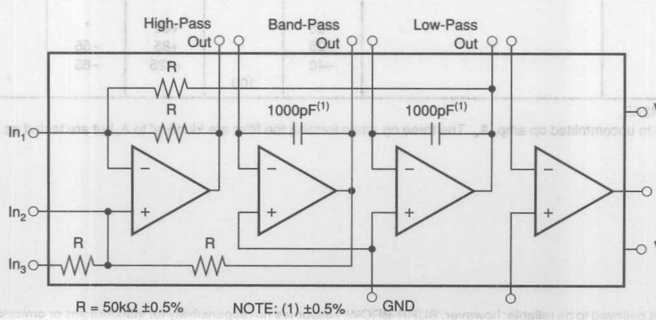
DESCRIPTION

The UAF42 is a universal active filter which can be configured for a wide range of low-pass, high-pass, and band-pass filters. It uses a classical state-variable analog architecture with an inverting amplifier and two integrators. The integrators include on-chip 1000pF capacitors trimmed to 0.5%. This solves one of the most difficult problems of active filter design—obtaining tight tolerance, low-loss capacitors.

A DOS-compatible filter design program allows easy implementation of many filter types such as Butterworth, Bessel, and Chebyshev. A fourth, uncommitted FET-input op amp (identical to the other three) can be used to form additional stages, or for special filters such as band-reject and Inverse Chebyshev.

The classical topology of the UAF42 forms a time-continuous filter, free from the anomalies and switching noise associated with switched-capacitor filter types.

The UAF42 is available in 14-pin plastic DIP and ceramic packages, and SOL-16 surface-mount packages, specified for the –25°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

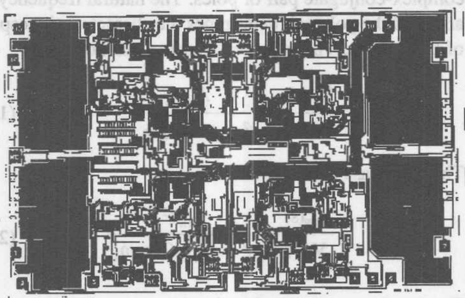
ELECTRICAL

At $T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.

		UAF42AP, AU			UAF42AG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
FILTER PERFORMANCE								
Frequency Range, fn			0 to 100			*		kHz
Frequency Accuracy	f = 1kHz			1			2	%
vs Temperature			0.01			*		%/°C
Maximum Q			400			*		—
Maximun (Q • Frequency) Product			500			*		kHz
Q vs Temperature	$(f_O \cdot Q) < 10^4$		0.01			*		%/°C
	$(f_O \cdot Q) < 10^5$		0.025			*		%/°C
Q Repeatability	$(f_O \cdot Q) < 10^5$		2			*		%
Offset Voltage, Low-Pass Output				±5			*	mV
Resistor Accuracy			0.5	1%		*	*	%
OFFSET VOLTAGE(1)								
Input Offset Voltage			±0.5	±5		*	*	mV
vs Temperature			±3			*		µV/°C
vs Power Supply	$V_S = \pm6$ to $\pm18V$	80	96		*	*		dB
INPUT BIAS CURRENT(1)								
Input Bias Current	$V_{CM} = 0V$		10	50		*	*	pA
Input Offset Current	$V_{CM} = 0V$		5			*		pA
NOISE								
Input Voltage Noise								
Noise Density: f = 10Hz			25			*		$nV/\sqrt{Hz}$
f = 10kHz			10			*		$nV/\sqrt{Hz}$
Voltage Noise: BW = 0.1 to 10Hz			2			*		µVp-p
Input Bias Current Noise								
Noise Density: f = 10kHz			2			*		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE(1)								
Common-Mode Input Range			±11.5			*		V
Common-Mode Rejection	$V_{CM} = \pm10V$	80	96		*	*		dB
INPUT IMPEDANCE(1)								
Differential			$10^{13} \parallel 2$			*		Ω || pF
Common-Mode			$10^{13} \parallel 6$			*		Ω || pF
OPEN-LOOP GAIN(1)								
Open-Loop Voltage Gain	$V_O = \pm10V$, $R_L = 2k\Omega$	90	126		*	*		dB
FREQUENCY RESPONSE(1)								
Slew Rate			10			*		V/µs
Gain-Bandwidth Product	G = +1		4			*		MHz
Total Harmonic Distortion	G = +1, f = 1kHz		0.0004			*		%
OUTPUT(1)								
Voltage Output	$R_L = 2k\Omega$	±11	±11.5		*	*		V
Short Circuit Current			±25			*		mA
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±6		±18	*		*	V
Current			±6	±7		*	*	mA
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	–55		+125	°C
Storage		–40		+125	–65		+150	°C
Thermal Resistance, θ_{JA}			100			*		°C/W

* Same as specification for UAF42AP.

NOTES: (1) Specifications apply to uncommitted op amp, A_4. The three op amps forming the filter are identical to A_4 but are tested as a complete filter.



UAF42 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNC TION
1	Low Pass V_O	7	Bandpass V_O
2	V_{IN3}	8	Frequency Adj_1
3	V_{IN2}	9	V–
4	Aux. Op Amp, +In	10	V+
		11	Ground
5	Aux. Op Amp, –In	12	V_{IN1}
		13	High-Pass V_O
6	Aux. Op Amp, V_O	14	Frequency Adj_2

NC: No Connection.
Substrate Bias: Electrically connected to V– supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	205 x 130 ±5	5.21 x 3.30 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

PIN CONFIGURATION

Top View

Plastic DIP, P
Ceramic DIP, G

Function	Pin	Pin	Function
Low-Pass V_O	1	14	Frequency Adj_2
V_{IN3}	2	13	High-Pass V_O
V_{IN2}	3	12	V_{IN1}
Auxiliary Op Amp, +In	4	11	Ground
Auxiliary Op Amp, –In	5	10	V+
Auxiliary Op Amp, V_O	6	9	V–
Bandpass V_O	7	8	Frequency Adj_1

U Package
SOL-16, 16-Pin SOIC

Function	Pin	Pin	Function
Low-Pass V_O	1	16	Frequency Adj_2
NC	2	15	NC
V_{IN3}	3	14	High-Pass V_O
V_{IN2}	4	13	V_{IN1}
Auxiliary Op Amp, +In	5	12	Ground
Auxiliary Op Amp, –In	6	11	V+
Auxiliary Op Amp, V_O	7	10	V–
Bandpass V_O	8	9	Frequency Adj_1

NOTE: NC: No Connection. For best performance connect all "NC" pins to ground to minimize inter-lead capacitance.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	$\pm V_S$ ±0.7V
Output Short Circuit	Continuous
Operating Temperature:	
Plastic DIP, P; SOIC, U	–40°C to +85°C
Ceramic DIP, G	–55°C to +125°C
Storage Temperature:	
Plastic DIP, P; SOIC, U	–40°C to +125°C
Ceramic DIP, G	–65°C to +150°C
Junction Temperature:	
Plastic DIP, P; SOIC, U	+125°C
Ceramic DIP, G	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
UAF42AP	Plastic 14-pin DIP	–25°C to +85°C
UAF42AG	Ceramic 14-pin DIP	–25°C to +85°C
UAF42AU	SOL-16	–25°C to +85°C

PACKAGING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER (1)
UAF42AP	Plastic 14-pin DIP	010
UAF42AG	Ceramic 14-pin DIP	163
UAF42AU	SOL-16	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

APPLICATIONS INFORMATION

The UAF42 is a monolithic implementation of the proven state-variable analog filter topology. Pin-compatible with the popular UAF41 Analog Filter, it provides several improvements.

Slew Rate of the UAF42 has been increased to 10V/µs versus 1.6V/µs for the UAF41. Frequency • Q product of the UAF42 has been improved, and the useful natural frequency extended by a factor of four to 100kHz. FET-input op amps on the UAF42 provide very low input bias current. The monolithic construction of the UAF42 provides lower cost and improved reliability.

DESIGN PROGRAM

Application Bulletin AB-035 and a computer-aided design program, available from Burr-Brown, make it easy to design and implement many kinds of active filters. The DOS-compatible program guides you through the design process and automatically calculates component values.

Low-pass, high-pass, band-pass and band-reject (notch) filters can be designed. The program supports the three most commonly used all-pole filter types: Butterworth, Chebyshev and Bessel. The less-familiar Inverse Chebyshev is also supported, providing a smooth passband response with ripple in the stop-band.

With each data entry, the program automatically calculates and displays filter performance. This allows a spreadsheet-like "what if" design approach. For example, you can quickly determine, by trial and error, how many poles are required for a desired attenuation in the stopband. Gain/phase plots may be viewed for any response type.

The basic building element of the most commonly used filter types is the second-order section. This section provides a complex-conjugate pair of poles. The natural frequency, ω_n, and Q of the pole pair determines the characteristic response of the section. The low-pass transfer function is

$$\frac{V_O(s)}{V_I(s)} = \frac{A_{LP}\omega_n^2}{s^2 + s\,\omega_n/Q + \omega_n^2} \quad (1)$$

The high-pass transfer function is

$$\frac{V_{HP}(s)}{V_I(s)} = \frac{A_{HP}s^2}{s^2 + s\,\omega_n/Q + \omega_n^2} \quad (2)$$

The band-pass transfer function is

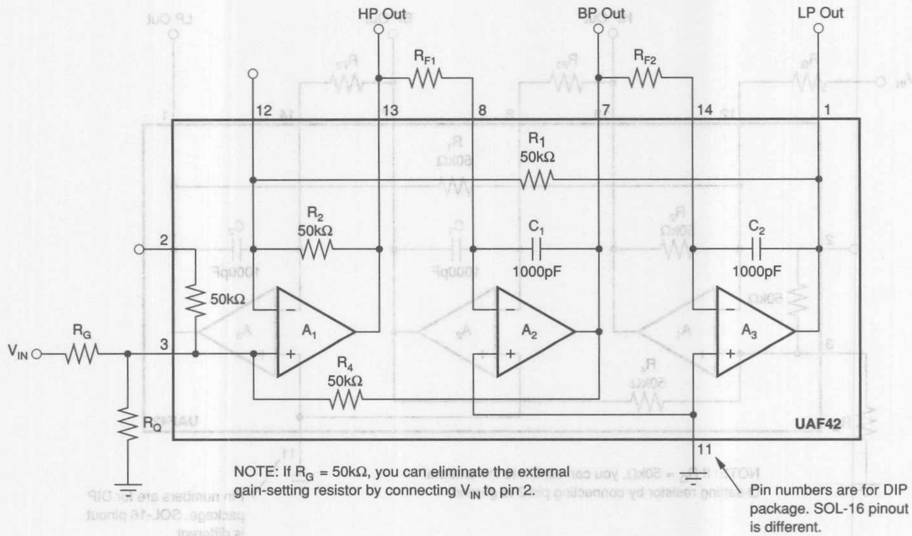
$$\frac{V_{BP}(s)}{V_I(s)} = \frac{A_{BP}(\omega_n/Q)\ s}{s^2 + s\,\omega_n/Q + \omega_n^2} \quad (3)$$

A band-reject response is obtained by summing the low-pass and high-pass outputs, yielding the transfer function

$$\frac{V_{BR}(s)}{V_I(s)} = \frac{A_{BR}(s^2 + \omega_n^2)}{s^2 + s\,\omega_n/Q + \omega_n^2} \quad (4)$$

The most commonly used filter types are formed with one or more cascaded second-order sections. Each section is designed for ω_n and Q according to the filter type (Butterworth, Bessel, Chebyshev, etc.) and cutoff frequency. While tabulated data can be found in virtually any filter design text, the design program eliminates this tedious procedure.

Second-order sections may be non-inverting (Figure 1) or inverting (Figure 2). Design equations for these two basic configurations are shown for reference. The design program solves these equations, providing complete results, including component values.



Design Equations

1. $$\omega_n^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$$

2. $$Q = \frac{1 + \dfrac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \dfrac{R_2}{R_1}} \left(\frac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2}\right)^{1/2}$$

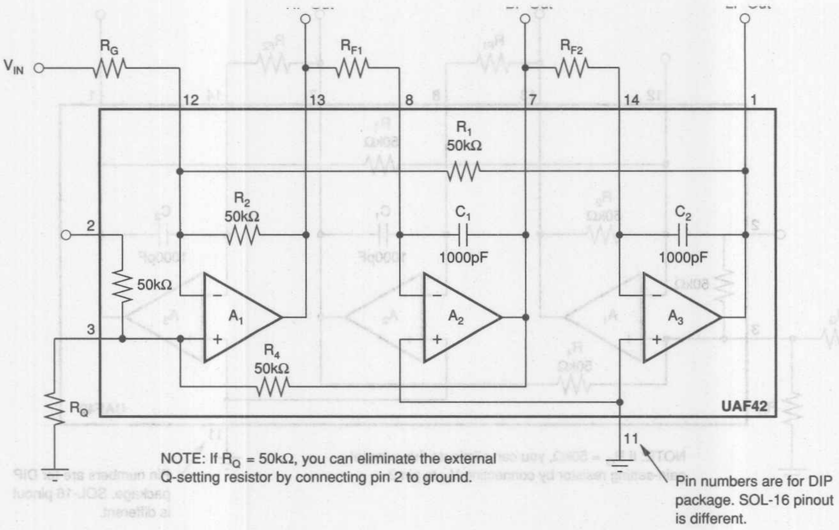
3. $$QA_{LP} = QA_{HP}\left(\frac{R_1}{R_2}\right) = A_{BP}\left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$$

4. $$A_{LP} = \frac{1 + \dfrac{R_1}{R_2}}{R_G\left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4}\right)}$$

5. $$A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{1 + \dfrac{R_2}{R_1}}{R_G\left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4}\right)}$$

6. $$A_{BP} = \frac{R_4}{R_G}$$

FIGURE 1. Non-Inverting Pole-Pair.



Design Equations

1. $$\omega_n^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$$

2. $$Q = \left(1 + \frac{R_4}{R_Q}\right) \frac{1}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)} \left(\frac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$$

3. $$QA_{LP} = QA_{HP}\left(\frac{R_1}{R_2}\right) = A_{BP}\left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$$

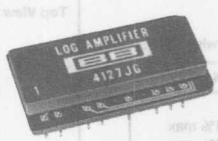
4. $$A_{LP} = \frac{R_1}{R_G}$$

5. $$A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{R_2}{R_G}$$

6. $$A_{BP} = \left(1 + \frac{R_4}{R_Q}\right) \frac{1}{R_G\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)}$$

FIGURE 2. Inverting Pole-Pair.

BURR - BROWN®



4127

ABRIDGED DATA SHEET
For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 10346

LOGARITHMIC AMPLIFIER

FEATURES

- **ACCEPTS INPUT VOLTAGES OR CURRENTS OF EITHER POLARITY**
- **WIDE INPUT DYNAMIC RANGE**
  6 Decades of Current
  4 Decades of Voltage
- **VERSATILE**
  Log, Antilog, and Log Ratio Capability

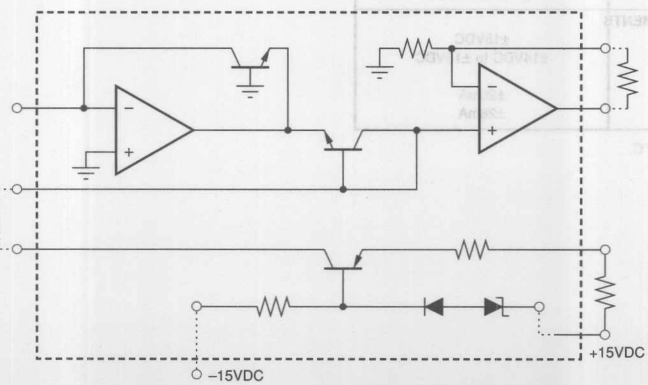
DESCRIPTION

Packaged in a ceramic double wide DIP, the 4127 is the first hybrid logarithmic amplifier that accepts signals of either polarity from current or voltage sources. A special purpose monolithic chip, developed specifically for logarithmic conversions, functions accurately for up to six decades of input current and four decades of input voltage. In addition, a current inverter and a precise internal reference allow pin programming of the 4127 as a logarithmic, log ratio, or antilog amplifier.

To further increase its versatility and reduce your system cost, the 4127 has an uncommitted operational amplifier in its package that can be used as a buffer, inverter, filter, or gain element.

The 4127 is available with initial accuracies (log conformity) of 0.5% and 1.0%, and operates over an ambient temperature range of –10°C to +70°C.

With its versatility and high performance, the 4127 has many applications in signal compression, transducer linearization, and phototube buffering. Manufacturers of medical equipment, analytical instruments, and process control instrumentation will find the 4127 a low cost solution to many signal processing problems.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

Typical Specifications at +25°C with rated supplies, unless otherwise noted.

MODEL	4127KG	4127JG
ACCURACY(1), % of FSR		
Current Source Input: 1nA to 1mA	0.5% max	1% max
Voltage Input: 1mV to 10V	0.5% max	1% max
INPUT		
Current Source Input, Pin 4	+1nA to +1mA	
Current Source Input, Pin 7	–1nA to –1mA	
Reference Current Input, Pin 2	+1µA to +1mA	
Absolute Maximum Inputs	±10mA or ±Supply Volts	
OUTPUT		
Voltage	±10V	
Current	±5mA	
Impedance	10Ω	
FREQUENCY RESPONSE		
–3dB Small Signal at Current Input		
of 100µA	90kHz	
of 10µA	50kHz	
of 1µA	5kHz	
of 100nA	250Hz	
of 10nA	80Hz	
Step Response to within ±1% of Final Value (I_R = 1µA, A = 5)	10ms	
STABILITY		
Scale Factor Drift (ΔA/°C)	±0.0005A/°C	
Reference Current Drift (ΔI_R/°C)	±0.001 I_R/°C for $I_R \geq$ 1µA	
	±0.003 I_R/°C for 400nA < I_R < 1µA	
Input Offset Current Drift (ΔI_S/°C)	10pA at +25°C, Doubles Every 10°C	
Input Offset Voltage Drift	±10µV/°C	
Accuracy vs Supply Variation		
Reference Current	±0.001I_R/V	
Input Offset Voltage	±300µV/V	
Input Noise - Current Input	1pA, rms, 10Hz to 10kHz	
Input Noise - Voltage Input	10µA, rms, 10Hz to 10kHz	
UNCOMMITTED OP AMP CHARACTERISTICS		
Input Offset Voltage	5mV	
Input Bias Current	40nA	
Input Impedance	1MΩ	
Large Signal Voltage Gain	85dB	
Output Current	5mA	
TEMPERATURE RANGE		
Specification	0°C to +60°C	
Operating	–10°C to +70°C	
Storage	–55°C to +125°C	
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltages	±15VDC	
Supply Voltage Range	±14VDC to ±16VDC	
Supply Current Drain		
at Quiescent, max	±20mA	
at Full Load, max	±26mA	

NOTE: (1) Log conformity at 25°C.

PIN CONFIGURATION

Top View

Function	Pin	Pin	Function
I_{REF} Output	1	24	No Pin Present
I_{REF} Input	2	23	I_{REF}Bias
No Pin Present	3	22	Postive Supply
+I Input(1)	4	21	Common
Current Inverter Output(1)	5	20	No Pin Present
No Pin Present	6	19	Gain Adjust
Current Inverter Input	7	18	Log Output
No Pin Present	8	17	No Pin Present
Op Amp + Input	9	16	No Pin Present
Op Amp –Input	10	15	No Pin Present
Op Amp Output	11	14	Negative Supply
No Pin Present	12	13	NC

NOTE: (1) Pins 4 and 5 are internally connected.

PACKAGE INFORMATION

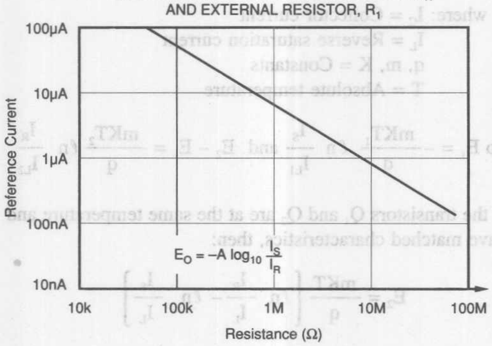
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
4127KG	24-Pin	075
4127JG	24-Pin	075

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

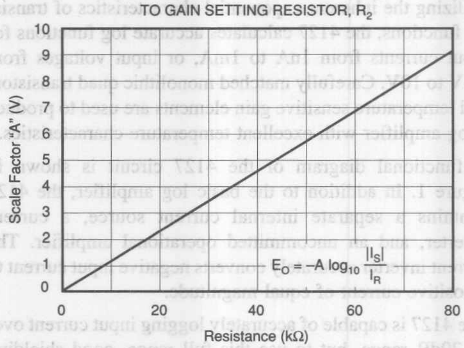
TYPICAL PERFORMANCE CURVES

At +25°C with rated supplies, unless otherwise noted.

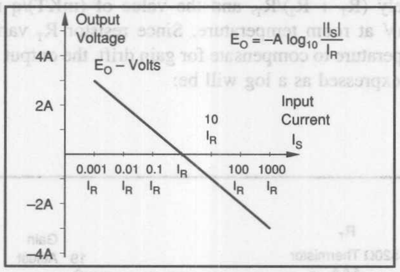
RELATIONSHIP OF REFERENCE CURRENT, I_R AND EXTERNAL RESISTOR, R_1



RELATIONSHIP OF SCALE FACTOR "A" TO GAIN SETTING RESISTOR, R_2

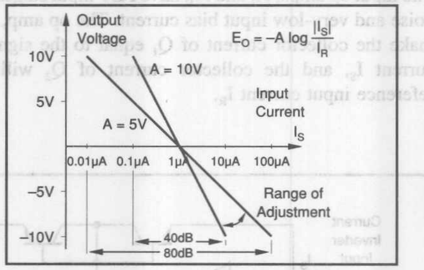


LOG RELATIONSHIP OF $\frac{|I_S|}{I_R}$ AND OUTPUT VOLTAGE IN TERMS OF "A"



RELATIONSHIP OF $\frac{|I_S|}{I_R}$ AND OUTPUT VOLTAGE

For I_R = 1µA and A = 5V and 10V



DISCUSSION OF SPECIFICATIONS

ACCURACY

The deviation from the ideal output voltage defined as a percent of the full scale output voltage.

INPUT/OUTPUT RANGE

The log relationships of $-A \log \frac{I_S}{I_R}$ and $-A \log \frac{E_S}{I_R R}$ are subject to the constraints specified. The 4127 can be operated with inputs lower than those given, but the accuracy will be degraded.

FREQUENCY RESPONSE

The small-signal frequency response varies considerably with signal level and scaling, so the frequency response is specified under several different operating conditions.

STABILITY

The use of a monolithic transistor quad and low-drift amps minimizes drift, but some drift remains in the scale-factor, reference current, and input offset. Input offset consists of a bias current plus the op amp input voltage offset divided by the signal source resistance. Also, there is some slight drift in conformity to the log function and in output amplifier offset, but this is generally negligible.

THEORY OF OPERATION

The 4127 is a complete logarithmic amplifier that can be pin-programmed to accept input currents or voltages of either polarity. By making use of the internal current inverter, reference current generator, log ratio element, and uncommitted op amp, you can generate a variety of logarith-

The unique FET-input current-inverting element removes the polarity limitations present in most conventional log amplifiers.

Utilizing the inherent exponential characteristics of transistor functions, the 4127 calculates accurate log functions for input currents from 1nA to 1mA, or input voltages from 1mV to 10V. Carefully matched monolithic quad transistors and temperature sensitive gain elements are used to produce a log amplifier with excellent temperature characteristics.

A functional diagram of the 4127 circuit is shown in Figure 1. In addition to the basic log amplifier, the 4127 contains a separate internal current source, a current inverter, and an uncommitted operational amplifier. The current inverter accurately converts negative input current to a positive current of equal magnitude.

The 4127 is capable of accurately logging input current over a 120dB range, but to use this full range, good shielding practice must be followed. A current source input is, by definition, a high impedance source and is therefore subject to electrostatic pickup.

The input op amps, A_1 and A_3, have FET input stages for low noise and very-low input bias current. The op amp, A_1, will make the collector current of Q_1 equal to the signal input current I_S, and the collector current of Q_2 will be the reference input current I_R.

$$V_{BE} \approx \frac{mKT}{q} \; \ell n \; \frac{I_C}{I_L},$$

where: I_C = Collector current
I_L = Reverse saturation current
q, m, K = Constants
T = Absolute temperature

$$\text{So } E_1 = -\frac{mKT_1}{q} \; \ell n \; \frac{I_S}{I_{L1}} \text{ and } E_2 - E_1 = \frac{mKT_2}{q} \; \ell n \; \frac{I_R}{I_{L2}}$$

If the transistors Q_1 and Q_2 are at the same temperature and have matched characteristics, then:

$$E_2 = \frac{mKT}{q} \left(\ell n \; \frac{I_R}{I_L} - \ell n \; \frac{I_S}{I_L} \right)$$

$$E_2 = \frac{-mKT}{q} \; \ell n \; \frac{I_S}{I_R}$$

The output op amp, A_2, provides a voltage gain of approximately $(R_T + R_2)/R_T$, and the value of $(mKT)/q$ is about 26mV at room temperature. Since resistor R_T varies with temperature to compensate for gain drift, the output voltage, E_O, expressed as a log will be:

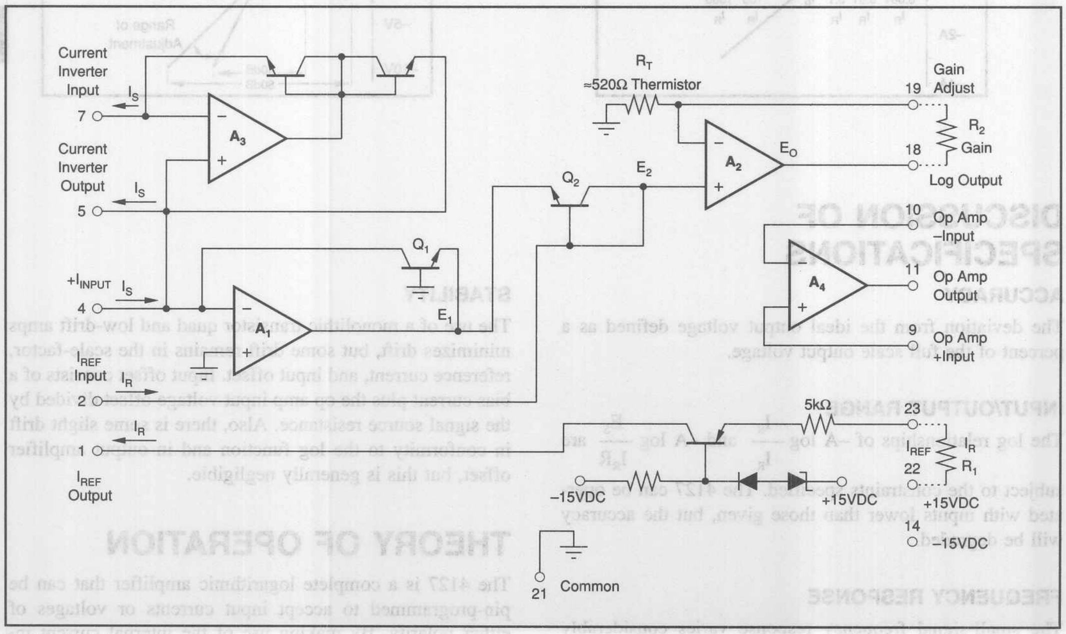


FIGURE 1. Functional Diagram.

8 References and Regulators

Voltage and current references are used for bridge circuits, calibration standards, D/A and A/D converter reference, sensor excitation and other applications requiring a stable voltage or current reference.

Regulators are used for battery management, distributed power, SCSI-2 termination and any other applications requiring regulated power.

Choose from our complete line of references and regulators which include:

REF1004-1.2—1.235V ±4mV bandgap reference that will operate from as little as 10µA in an 8-lead SOIC package.

REF1004-2.5—2.500V ±20mV bandgap reference that will operate from as little as 20µA in an 8-lead SOIC package.

REF02—5.0V ±5mV buried zener reference that will operate over an input range of 8VDC to 40VDC in an 8-lead SOIC, PDIP and TO-99 packages.

REF102—10.0V ±2.5mV buried zener precision reference that will operate over an input range of 11.4VDC to 36VDC in an 8-lead SOIC, PDIP and TO-99 packages.

REF200—100µA ±0.5µA dual current reference with a compliance voltage range of 2.5VDC to 40VDC in an 8-lead SOIC, PDIP AND TO-99 packages.

REG1117—Positive 2.85V, 3.0V, 3.3V, and 5.0V regulators that will operate down to 1V input to output and up to 800mA output in an SOT-223 package.

REG5601—Electrically equivalent to industry-standard "5601" terminators, this 18-line SCSI bus terminator comes in a 28-lead fine pitch SSOP package that requires only half the circuit board area.

REG5608—A low capacitance (2pF) 18-line active terminator for SCSI parallel bus systems. Meets requirements for high data rate systems (20MHz, Fast-20).

REFERENCES AND REGULATORS

VOLTAGE REFERENCE
(Drift Accuracy, max)

OUTPUT VOLTAGE = 10V

- REF101 (1ppm/°C)
- REF10 (1ppm/°C)
- REF102 (2.5ppm/°C)
- REF01 (8.5ppm/°C)

OUTPUT VOLTAGE = 5V

- REF02 (8.5ppm/°C)
- REF05 (8.5ppm/°C)

OUTPUT VOLTAGE = 2.5V

- REF1004 (20ppm/°C)

OUTPUT VOLTAGE = 1.25V

- REF1004 (20ppm/°C)

CURRENT REFERENCE
(Drift Accuracy, typ)

- REF200 (25ppm/°C)

LOW DROPOUT VOLTAGE REGULATORS
(Output Voltage, typ
Output Current, max)

- REG1117 (Adj., 800mA)
- REG1117-2.85 (2.85V, 800mA)
- REG1117-3 (3V, 800mA)
- REG1117-3.3 (3.3V, 800mA)
- REG1117-5 (5V, 800mA)

INTEGRATED SCSI TERMINATORS
18-Line Terminator
(Output Capacitance, typ)

- **REG5608 (2.5pF)**
- REG5601 (10pF)

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

VOLTAGE REFERENCE

Product	Output (V)	Output Current min (mA)	Output Voltage Drift max (±ppm/°C)	Power Supply min, max (V)	Power Supply max (mA)	Temp Range(1)	Cerdip Pkg	Description
REF01M, G	+10.00 ±0.025	10	8.5	+11.4/40	1.4	Mil, Ind, Ceramic	TO-99, CDIP	Guaranteed Long-Term Stability
REF01P, U	+10.00 ±0.020	10	15	+11.4/40	1.4	Ind, Com	PDIP, SO	Guaranteed Long-Term Stability
REF02M, G	+5.00 ±0.01	10	8.5	+7/40	1.4	Mil, Ind, Ceramic	TO-99, CDIP	Guaranteed Long-Term Stability—±25ppm/1k hrs
REF02P, U	+5.00 ±0.015	10	10	+7/40	1.4	Com, Ind	PDIP, SO	Guaranteed Long-Term Stability—±25ppm/1k hrs
REF05M	+5.00 ±0.01	10	8.5	+7/40	1.4	Mil	TO-99, CDIP	Guaranteed Long-Term Stability—±25ppm/1k hrs
REF10M	+10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	Guaranteed Long-Term Stability
REF101	+10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	Guaranteed Long-Term Stability
REF102	+10.00 ±0.0025	10	2.5	+11.4/36	1.4	Ind, Mil	TO-99, DIP, SOIC	Guaranteed Long-Term Stability
REF1004C	+1.235 ±0.006	NS	20	NS	10µA(2)	Com	SOIC	Precision Micropower Voltage Reference
REF1004I	+1.235 ±0.01	NS	20	NS	10µA(2)	XInd	SOIC	Precision Micropower Voltage Reference
REF1004C	+2.50 ±0.013	NS	20	NS	20µA(2)	Com	SOIC	Precision Micropower Voltage Reference
REF1004I	+2.50 ±0.02	NS	20	NS	20µA(2)	XInd	SOIC	Precision Micropower Voltage Reference

NOTE: (1) Com = 0°C to +70°C. Ind = –25°C to +85°C, Mil = –55°C to +125°C. XInd = –40°C to +85°C. (2) Minimum Operating Current.

CURRENT REFERENCE

Product	Output Current (µA)	Voltage Compliance	Drift (max) (ppm/°C)	Pkg	Temp Range(1)	Description
REF200	Dual 100 ±0.5	2.5 V to 40V	25	DIP, SO-8	Ind	Includes 0.5% accurate current mirror

NOTE: (1) Ind = –25°C to +85°C.

LOW DROPOUT VOLTAGE REGULATORS

Product	Output Voltage (V) typ	Dropout Voltage at 800mA (V) max	Line Regulation (mV)	Load Regulation (mV) max	Quiescent Current (mA)	Temp Range	Pkg	Description
REG1117	ADJ.	1.2	0.4%	0.4%	10	Com	SOT-223	
REG1117-2.85	+2.85	1.2	7	7	10	Com	SOT-223	+2.85V Voltage Regulator For SCSI-2 Active Termination
REG1117-3, 3.3	+3, +3.3	1.2	7	7	10	Com	SOT-223	+3V/+3.3V Voltage Regulator
REG1117-5	+5	1.2	10	10	10	Com	SOT-223	+5.0V Voltage Regulator

INTEGRATED SCSI TERMINATORS

Product	Output Line Capacitance, typ	Termination Impedance (typ)	Output Current mA (typ)	Operating Temperature	Pkg	Description
REG5601	10pF	110Ω	21.7	T_A = 0°C to 70°C	SOIC	18 Line Terminator
REG5608	**2pF**	**110Ω**	**22.4**	**T_A = 0°C to 70°C**	**SOIC, SSOP**	**18 Line Terminator**

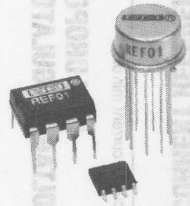
* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR - BROWN®

REF01



+10V Precision VOLTAGE REFERENCE

FEATURES

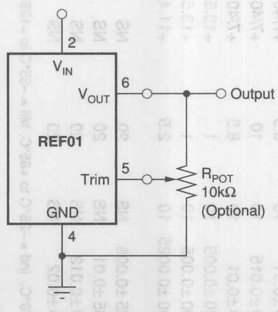
- OUTPUT VOLTAGE: +10V ±0.2% max
- EXCELLENT TEMPERATURE STABILITY: 8.5ppm/°C max (–40°C to +85°C)
- LOW NOISE: 5μVp-p typ (0.1Hz to 10Hz)
- EXCELLENT LINE REGULATION: 0.001%/V max
- EXCELLENT LOAD REGULATION: 0.002%/mA max
- SOURCES 10mA, SINKS 5mA min
- LOW SUPPLY CURRENT: 1.4mA max
- SHORT-CIRCUIT PROTECTED
- WIDE SUPPLY RANGE: 11.4VDC to 40VDC
- PACKAGE OPTIONS: Plastic DIP, SOIC
- EXTENDED INDUSTRIAL TEMPERATURE RANGE: –40°C to +85°C

APPLICATIONS

- PRECISION REGULATORS
- CONSTANT CURRENT SOURCE/SINK
- DIGITAL VOLTMETERS
- A/D AND D/A CONVERTERS
- PRECISION CALIBRATION STANDARD
- TEST EQUIPMENT

DESCRIPTION

The REF01 is a high performance, low price, precision pin compatible second source voltage reference. Output accuracy of ±0.2% is a 30% improvement over industry standard REF01s. Output noise is 5μVp-p, which is a 75% decrease in noise over all other REF01s. Line regulation is 0.001%/V max and load regulation is 0.002%/mA max, which far exceeds the performance of our competitors. Quiescent current is a low 1.4mA. REF01 provides extended supply range when compared to industry standard devices. Burr-Brown's REF01 is the best choice for applications which requires improved accuracy, low noise, low power consumption, low drift, and the lowest price. Popular package options are available: Plastic DIP, and SOIC. For guaranteed long-term drift see Burr-Brown's model REF10.



+10V Reference with Trimmed Output

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

T_A = +25°C and V_S = +15V power supply unless otherwise noted.

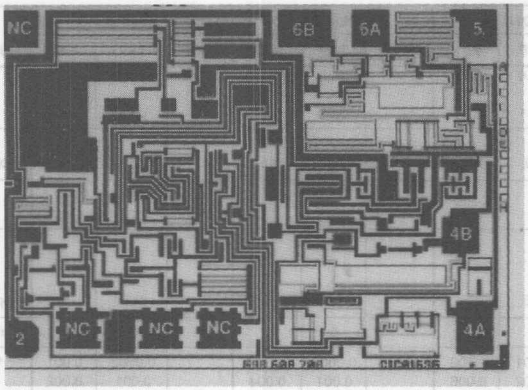
PARAMETER	CONDITIONS	REF01A			REF01B			REF01C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE (ΔV_{OT})	I_L = 0mA	9.970	10.0	10.030	9.975	10.0	10.025	9.980	10.0	10.020	V
Change with Temperature(1, 2) –40°C to +85°C			0.11	0.18		0.06	0.11		0.04	0.07	%
OUTPUT VOLTAGE DRIFT(3) –40°C to +85°C (TCV_O)			10	25		8	15		3	8.5	±ppm/°C
OUTPUT ADJUSTMENT RANGE	R_{POT} = 10kΩ(6)	±3			±3			±3			%
CHANGE IN V_O TEMP COEFFICIENT WITH OUTPUT ADJUSTMENT (–55°C to +125°C)	R_{POT} = 10kΩ		0.5			0.5			0.5		ppm/%
OUTPUT VOLTAGE NOISE	0.1Hz to 10Hz(5)		5			5			5		µVp-p
LINE REGULATION(4)	V_{IN} = 11.4V to 36V		0.001	0.003		0.0007	0.002		0.0003	0.001	%/V
–40°C to +85°C			0.002	0.006		0.001	0.004		0.001	0.002	
LOAD REGULATION(4)	I_L = 0mA to +10mA		0.001	0.004		0.001	0.003		0.001	0.002	%/mA
	I_L = 0mA to –5mA		0.003	0.008		0.002	0.006		0.001	0.004	
–40°C to +85°C	I_L = 0mA to +10mA		0.005	0.016		0.004	0.012		0.003	0.008	
TURN-ON SETTLING TIME	To ±0.1% of Final Value		5			5			5		µs
QUIESCENT CURRENT	No Load		1.2	1.4		1.2	1.4		1.2	1.4	mA
LOAD CURRENT		10	21		10	21		10	21		mA
SINK CURRENT		–5	–10		*	*		*	*		mA
SHORT-CIRCUIT CURRENT	V_O = 0		30			30			30		mA
POWER DISSIPATION			18			18			18		mW
TEMPERATURE RANGE Specification REF01A, B, C		–40		+85	*		*	*		*	°C

NOTES: (1) ΔV_{OT} is defined as the absolute difference between the maximum output and the minimum output voltage over the specified temperature range expressed as a percentage of 10V: $\Delta V_O = \frac{|V_{MAX} - V_{MIN}|}{10V} \times 100\%$ (2) ΔV_{OT} specification applies trimmed to +10.000V or untrimmed. (3) TCV_O is defined as ΔV_{OT} divided by the temperature range. (4) Line and load regulation specifications include the effect of self heating. (5) Sample tested. (6) 10kΩ potentiometer connected between V_O and ground with wiper connected to trim pin. See Figure 3.

ORDERING INFORMATION

MODEL	V_{OUT} AT 25°C	MAX DRIFT (ppm/°C)	TEMPERATURE	PACKAGE
REF01AU	10V±30mV	±25	–40°C to +85°C	8-Pin SOIC
REF01BU	10V±25mV	±15	–40°C to +85°C	8-Pin SOIC
REF01AP	10V±30mV	±25	–40°C to +85°C	8-Pin Plastic DIP
REF01BG	10V±25mV	±15	–40°C to+85°C	8-Pin Ceramic DIP
REF01BP	10V±25mV	±15	–40°C to +85°C	8-Pin Plastic DIP

DICE INFORMATION



REF01 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
2	V_{IN}	4B	GND
3A	NC	5	Trim
3B	NC	6A	V_{OUT}
3C	NC	6B	V_{OUT} (Sense)
4A	GND		

Substrate Bias: Common, pad 4B.
NOTE: Both common pads must be connected and both V_{OUT} pads must be tied together.

MECHANICAL INFORMATION

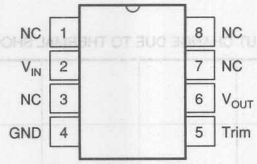
	MILS (0.001")	MILLIMETERS
Die Size	55 x 75	1.40 x 1.91 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	5 x 5	0.10 x 0.10
Backing		Gold

ABSOLUTE MAXIMUM RATINGS

Input Voltage	+40V
Operating Temperature	
P, U	–40°C to +85°C
Storage Temperature Range	
P, U	–65°C to +125°
Output Short Circuit Duration (to Ground or V_{IN})	Indefinite
Junction Temperature	–65°C to +150°
θ_{JA} P	120°C/W
U	80°C/W
Lead Temperature (soldering, 60s)	+300°C

PIN CONFIGURATIONS

Top View | DIP/SOIC



PACKAGE INFORMATION

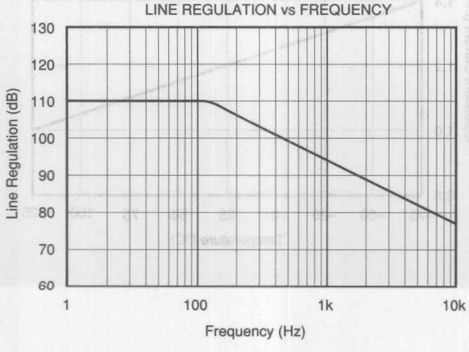
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
REF01AU	8-Pin SOIC	182
REF01BU	8-Pin SOIC	182
REF01AP	8-Pin Plastic DIP	006
REF01BP	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

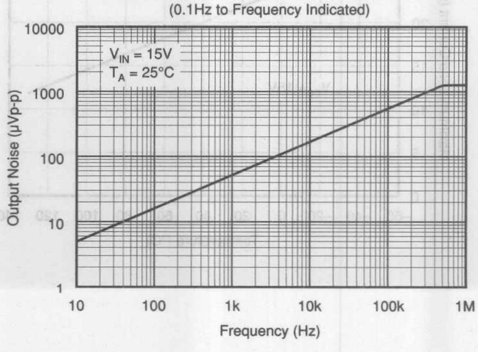
TYPICAL PERFORMANCE CURVES

T_A = +25°C and V_S = +15V power supply unless otherwise noted.

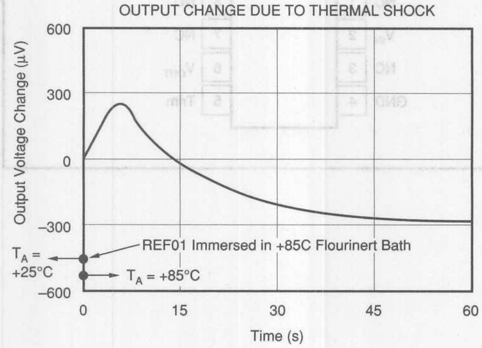
LINE REGULATION vs FREQUENCY

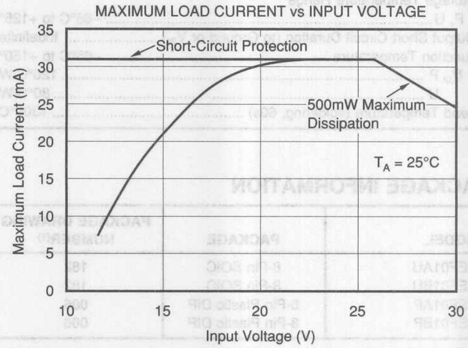


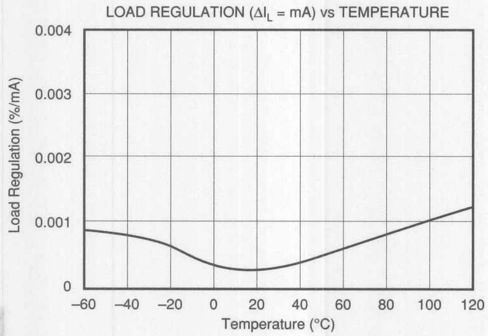
OUTPUT WIDEBAND NOISE vs BANDWIDTH
(0.1Hz to Frequency Indicated)

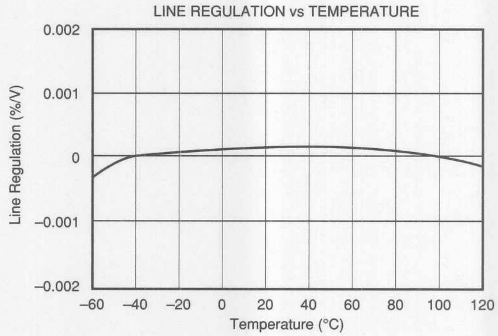


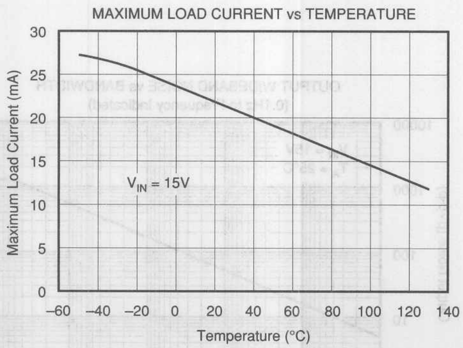
T_A = +25°C and V_S = +15V power supply unless otherwise noted.

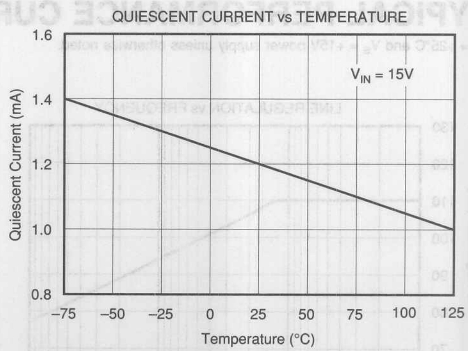












OUTPUT ADJUSTMENT

The REF01 trim terminal can be used to adjust the voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V, including 10.240V for binary applications (see circuit on the first page).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.5ppm/°C for 100mV of output adjustment.

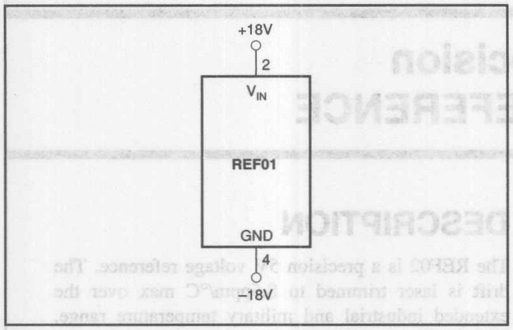


FIGURE 1. Burn-In Circuit.

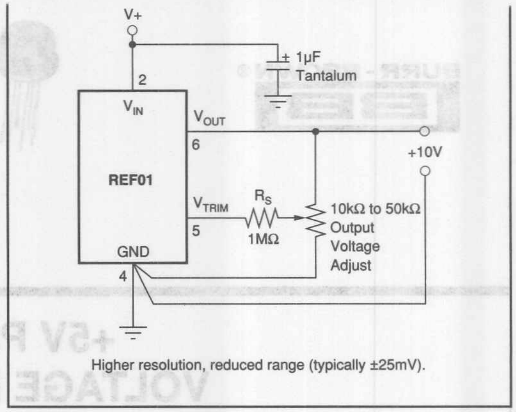
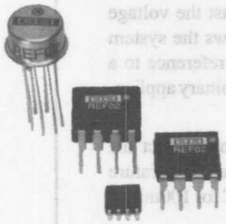


FIGURE 2. High Resolution Output Adjustment.

BURR - BROWN®

REF02



+5V Precision VOLTAGE REFERENCE

FEATURES

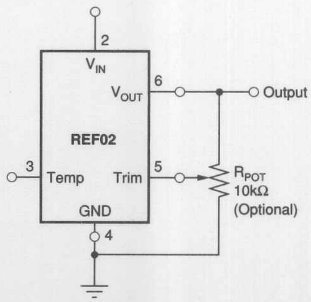
- OUTPUT VOLTAGE: +5V ±0.1% max
- EXCELLENT TEMPERATURE STABILITY: 8.5ppm/°C max (–40°C to +85°C)
- LOW NOISE: 10μVp-p max (0.1Hz to 10Hz)
- EXCELLENT LINE REGULATION: 0.008%/V max
- EXCELLENT LOAD REGULATION: 0.005%/mA max
- LOW SUPPLY CURRENT: 1.4mA max
- SHORT-CIRCUIT PROTECTED
- WIDE SUPPLY RANGE: 8V to 40V
- EXTENDED INDUSTRIAL TEMPERATURE RANGE: –40°C to +85°C
- PACKAGE OPTIONS: Plastic DIP, SOIC

DESCRIPTION

The REF02 is a precision 5V voltage reference. The drift is laser trimmed to 8.5ppm/°C max over the extended industrial and military temperature range. The REF02 provides a stable 5V output that can be externally adjusted over a ±6% range with minimal effect on temperature stability. REF02 operates from a single supply with an input range of 8V to 40V with a very low current drain of 1mA, and excellent temperature stability due to an improved design. Excellent line and load regulation, low noise, low power, and low cost make the REF02 the best choice whenever a 5V voltage reference is required. All popular package options are available: plastic DIP, and SOIC. The REF02 is an ideal choice for portable instrumentation, temperature transducers, A/D and D/A converters, and digital voltmeter.

APPLICATIONS

- PRECISION REGULATORS
- CONSTANT CURRENT SOURCE/SINK
- DIGITAL VOLTMETERS
- V/F CONVERTERS
- A/D AND D/A CONVERTERS
- PRECISION CALIBRATION STANDARD
- TEST EQUIPMENT



+5V Reference with Trimmed Output

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

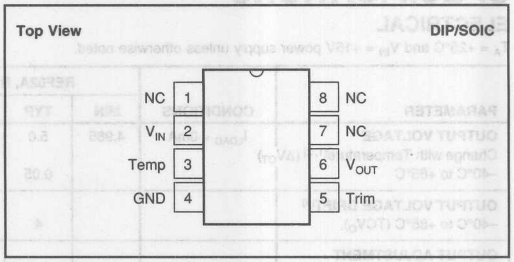
ELECTRICAL

T_A = +25°C and V_{IN} = +15V power supply unless otherwise noted.

		REF02A, R			REF02B, S			REF02C			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE	I_{LOAD} = 0mA	4.985	5.0	5.015	4.990	*	5.010	4.995	*	5.005	V
Change with Temperature(1, 2) (ΔV_{OT}) –40°C to +85°C			0.05	0.19		0.05	0.13		0.05	0.11	%
OUTPUT VOLTAGE DRIFT(3) –40°C to +85°C (TCV_O)			4	15		4	10		4	8.5	±ppm/°C
OUTPUT ADJUSTMENT RANGE	R_{POT} = 10kΩ(6)	±3	±6		*	*		*	*		%
CHANGE IN V_O TEMP COEFFICIENT WITH OUTPUT ADJUSTMENT (–55°C to +125°C)	R_{POT} = 10kΩ		0.7			*			*		ppm/%
OUTPUT VOLTAGE NOISE	0.1Hz to 10Hz(5)		4	10		*	*		*	*	µVp-p
LINE REGULATION(4) –40°C to +85°C	V_{IN} = 8V to 33V V_{IN} = 8.5V to 33V		0.006 0.008	0.010 0.012		* *	* *		0.004 0.005	0.008 0.010	%/V
LOAD REGULATION(4) –40°C to +85°C	I_L = 0mA to +10mA I_L = 0mA to +10mA		0.005 0.007	0.010 0.012		* *	0.008 0.010		0.003 0.004	0.005 0.005	%/mA
TURN-ON SETTLING TIME	To ±0.1% of Final Value		5			*			*		µs
QUIESCENT CURRENT	No Load		1.0	1.4		*	*		*	*	mA
LOAD CURRENT (SOURCE)		10	21		*	*		*	*		mA
LOAD CURRENT (SINK)		–0.3	–0.5		*	*		*	*		mA
SHORT-CIRCUIT CURRENT	V_{OUT} = 0		30			*			*		mA
POWER DISSIPATION	No Load		15	21		*	*		*	*	mW
TEMPERATURE VOLTAGE OUTPUT(7)			630			*			*		mV
TEMPERATURE COEFFICIENT of Temperature Pin Voltage –55°C to +125°C			2.1								mV/°C
TEMPERATURE RANGE Specification REF02A, B, C		–40		+85	*		*	*		*	°C

NOTES: (1) ΔV_{OT} is defined as the absolute difference between the maximum output and the minimum output voltage over the specified temperature range expressed as a percentage of 5V: $\Delta V_O = \left|\frac{V_{MAX} - V_{MIN}}{5V}\right| \times 100$ (2) ΔV_{OT} specification applies trimmed to +5.000V or untrimmed. (3) TCV_O is defined as ΔV_{OT} divided by the temperature range. (4) Line and load regulation specifications include the effect of self heating. (5) Sample tested. (6) 10kΩ potentiometer connected between V_{OUT} and ground with wiper connected to Trim pin. See Figure on page 1. (7) Pin 3 is insensitive to capacitive loading. The temperature voltage will be modified by 7mV for each µA of loading.

Input Voltage .... +40V
Operating Temperature
G, P, U .... –40°C to +85°C
Storage Temperature Range
G, P, U .... –65°C to +125°
M .... –65°C to +150°
Output Short Circuit Duration (to Ground or V_{IN}) .... Indefinite
Junction Temperature .... –65°C to +150°
θ_{JA} P .... 120°C/W
U .... 80°C/W
Lead Temperature (soldering, 60s) .... +300°C



PACKAGE INFORMATION

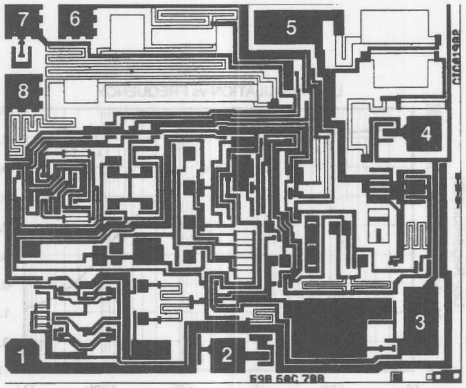
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
REF02AU	SOIC	182
REF02BU	SOIC	182
REF02AP	Plastic DIP	006
REF02BP	Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	V_{OUT} AT 25°C	MAX DRIFT (ppm/°C)	TEMPERATURE	PACKAGE
REF02AU	5V±15mV	±15	–40°C to +85°C	SOIC
REF02BU	5V±10mV	±10	–40°C to +85°C	SOIC
REF02AP	5V±15mV	±15	–40°C to +85°C	Plastic DIP
REF02BP	5V±10mV	±10	–40°C to +85°C	Plastic DIP

DICE INFORMATION



REF02 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	V_{IN}	5	V_{OUT}
2	Temp	6	NC
3	GND	7	NC
4	Trim	8	NC

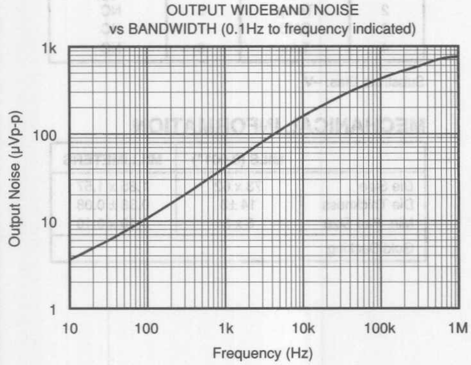
Substrate Bias: –V

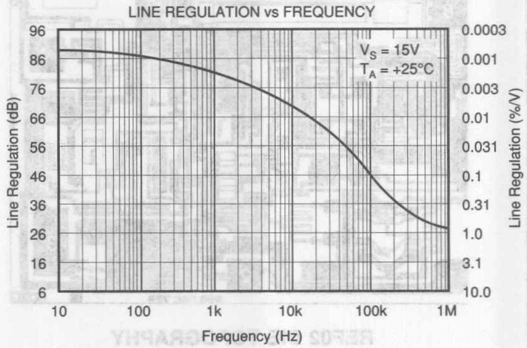
MECHANICAL INFORMATION

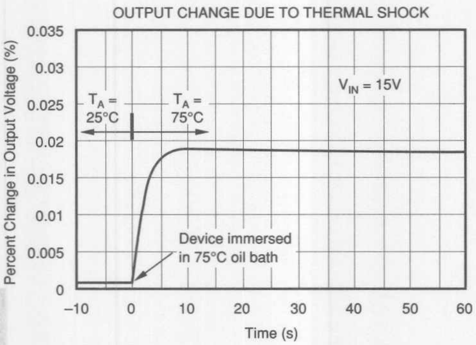
	MILS (0.001")	MILLIMETERS
Die Size	73 x 62	1.85 x 1.57
Die Thickness	14 ±3	0.36 ± 0.08
Min. Pad Size	5 x 5	0.10 x 0.10
Gold Backing		

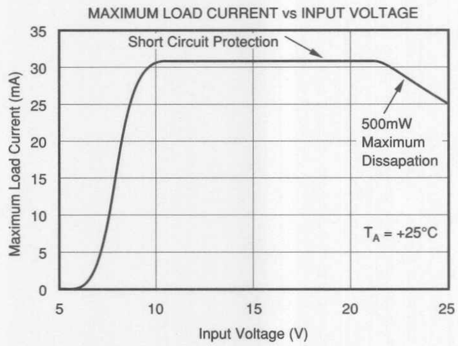
TYPICAL PERFORMANCE CURVES

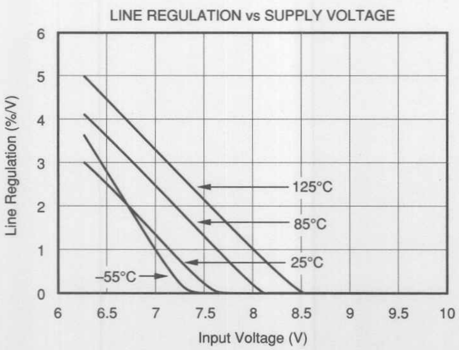
T_A = +25°C unless otherwise noted.

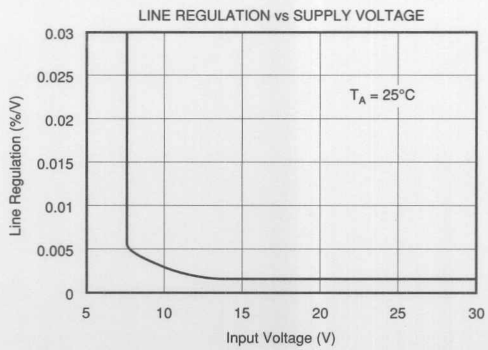








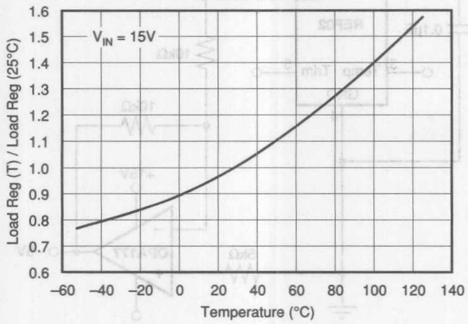




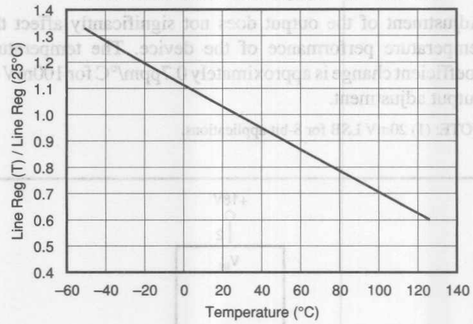
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

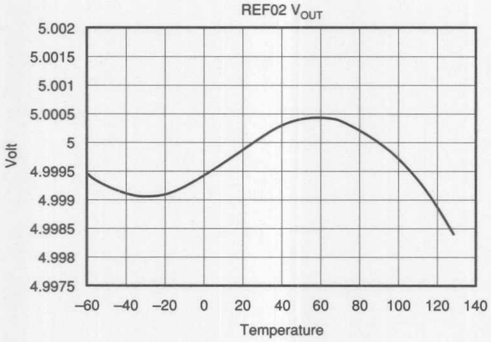
NORMALIZED LOAD REGULATION (ΔIL = 10mA) vs TEMPERATURE



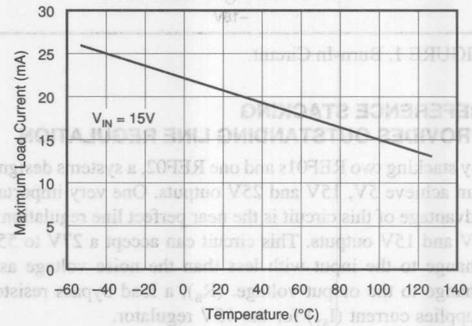
NORMALIZED LINE REGULATION vs TEMPERATURE



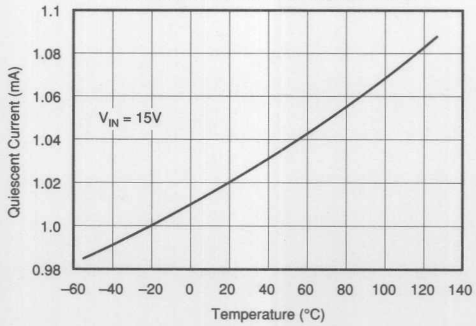
REF02 V_{OUT}



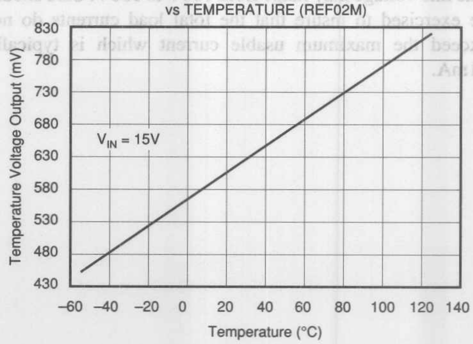
MAXIMUM LOAD CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF02M)



The REF02 trim terminal can be used to adjust the voltage over a 5V ±150mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V, including 5.12V[(1)] for binary applications (see circuit on page one).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7ppm/°C for 100mV of output adjustment.

NOTE: (1) 20mV LSB for 8-bit applications.

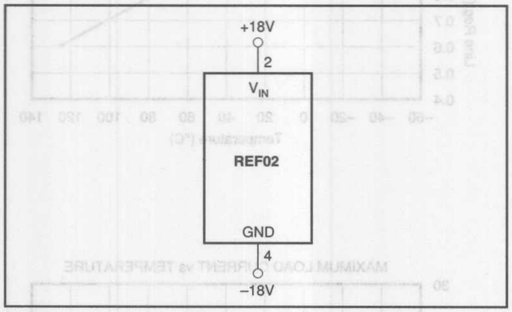


FIGURE 1. Burn-In Circuit.

REFERENCE STACKING PROVIDES OUTSTANDING LINE REGULATION

By stacking two REF01s and one REF02, a systems designer can achieve 5V, 15V and 25V outputs. One very important advantage of this circuit is the near perfect line regulation at 5V and 15V outputs. This circuit can accept a 27V to 55V change to the input with less than the noise voltage as a change to the output voltage. (R_B), a load bypass resistor, supplies current (I_{SY}) for the 15V regulator.

Any number of REF01s and REF02s can be stacked in this configuration. If ten devices can be stacked in this configuration, for example, ten 5V or five 10V outputs are achieved. The line voltage may range from 100V to 130V. Care should be exercised to insure that the total load currents do not exceed the maximum usable current which is typically 21mA.

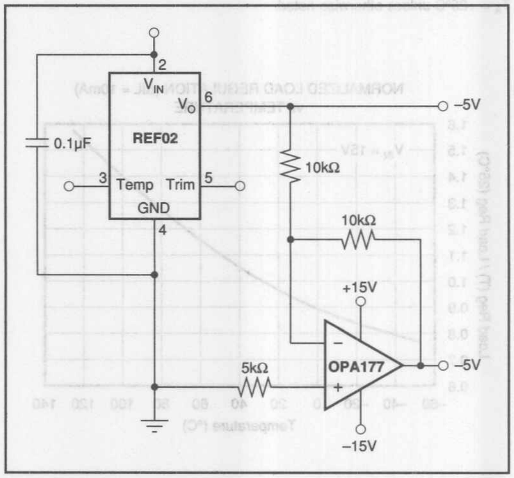
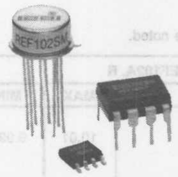


FIGURE 2. ±5V Precision Reference.

BURR - BROWN®



REF102

Precision VOLTAGE REFERENCE

FEATURES

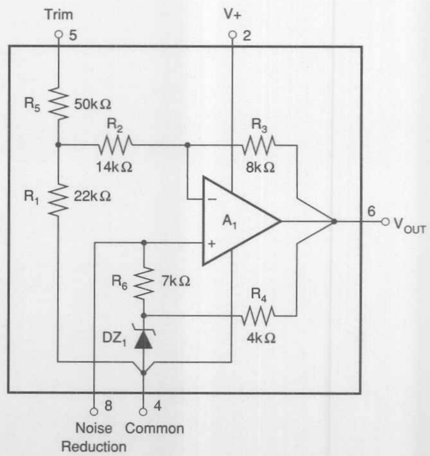
- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5µVp-p typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: HERMETIC TO-99, PLASTIC DIP, SOIC

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max (CM grade) over the industrial temperature range and 5ppm/°C max (SM grade) over the military temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = +15V power supply unless otherwise noted.

PARAMETER	CONDITIONS	REF102A, R MIN	REF102A, R TYP	REF102A, R MAX	REF102B, S MIN	REF102B, S TYP	REF102B, S MAX	REF102C, M MIN	REF102C, M TYP	REF102C, M MAX	UNITS
OUTPUT VOLTAGE											
Initial	T_A = 25°C	9.99		10.01	9.995		10.005	9.9975		10.0025	V
vs Temperature (1)				10			5			2.5	ppm/°C
vs Supply (Line Regulation)	V_S = 11.4V to 36V			2			1			1	ppm/V
vs Output Current (Load Regulation)	I_L = 0mA to +10mA			20			10			10	ppm/mA
	I_L = 0mA to –5mA			40			20			20	ppm/mA
vs Time	T_A = 25°										
M Package			5			*			*		ppm/1000hr
P, U Packages (2)			20			*					ppm/1000hr
Trim Range (3)		±3			*			*			%
Capacitive Load, max			1000			*			*		pF
NOISE	(0.1Hz to 10Hz)		5			*			*		µVp-p
OUTPUT CURRENT		+10, –5			*			*			mA
INPUT VOLTAGE RANGE		+11.4		+36	*		*	*		*	V
QUIESCENT CURRENT	(I_{OUT} = 0)			+1.4			*			*	mA
WARM-UP TIME (4)	(To 0.1%)		15			*			*		µs
TEMPERATURE RANGE											
Specification											
REF102A, B, C		–25		+85	*		*	*		*	°C
REF102R, S		–55		+125	*		*				°C

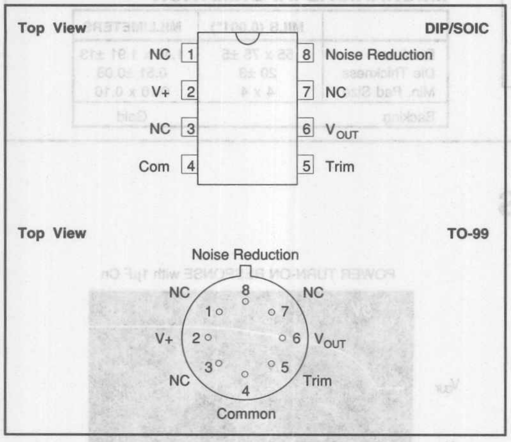
*Specifications same as REF102A/R.

NOTES: (1) The "box" method is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (2) Typically 5ppm/1000hrs after 168hr powered stabilization. (3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details. (4) With noise reduction pin floating. See Typical Performance Curves for details.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	MAX INITIAL ERROR (mV)	MAX DRIFT (ppm/°C)
REF102AU	8-Pin SOIC	–25°C to +85°C	±10	±10
REF102AP	8-Pin Plastic DIP	–25°C to +85°C	±10	±10
REF102BP	8-Pin Plastic DIP	–25°C to +85°C	±5	±5
REF102AM	Metal TO-99	–25°C to +85°C	±10	±10
REF102BM	Metal TO-99	–25°C to +85°C	±5	±5
REF102CM	Metal TO-99	–25°C to +85°C	±2.5	±2.5
REF102RM	Metal TO-99	–55°C to +125°C	±10	±10
REF102SM	Metal TO-99	–55°C to +125°C	±5	±5

PIN CONFIGURATIONS



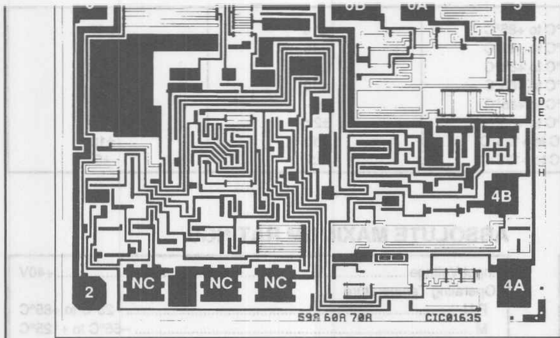
ABSOLUTE MAXIMUM RATINGS

Input Voltage .... +40V
Operating Temperature
  P,U .... –25°C to +85°C
  M .... –55°C to +125°C
Storage Temperature Range
  P,U .... –40°C to +85°C
  M .... –65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
  (SOIC, 3s) .... +260°C
Short-Circuit Protection to Common or V+ .... Continuous

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
REF102AU	8-Pin SOIC	182
REF102AP	8-Pin Plastic DIP	006
REF102BP	8-Pin Plastic DIP	006
REF102AM	Metal-TO-99	001
REF102BM	Metal-TO-99	001
REF102CM	Metal-TO-99	001
REF102RM	Metal-TO-99	001
REF102SM	Metal-TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



REF102 DIE TOPOGRAPHY

2	V_{CC}
3A	NC
3B	NC
3C	NC
4A	Common (Sense)
4B	Common (Force)
5	Trim
6A	V_{OUT}
6B	V_{OUT} (Feedback)
8	Noise Reduction

Substrate Bias: $-V_{CC}$.

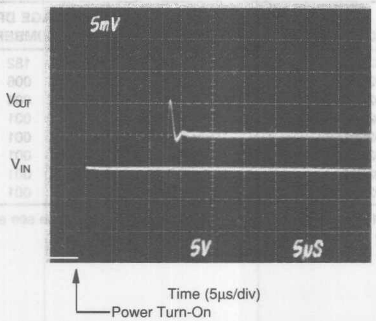
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	55 x 75 ±5	1.40 x 1.91 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

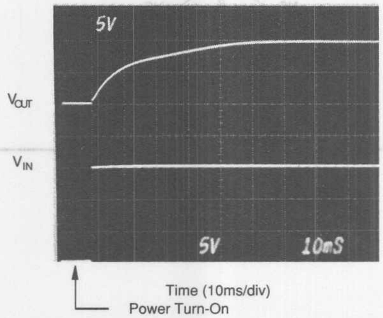
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = +15V$ unless otherwise noted.

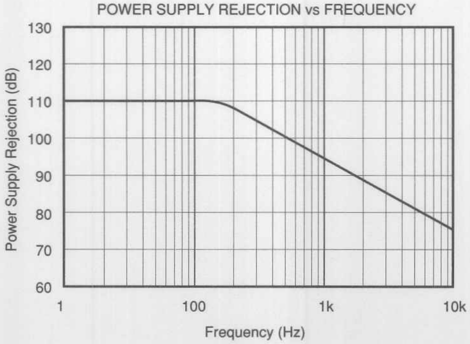
POWER TURN-ON RESPONSE



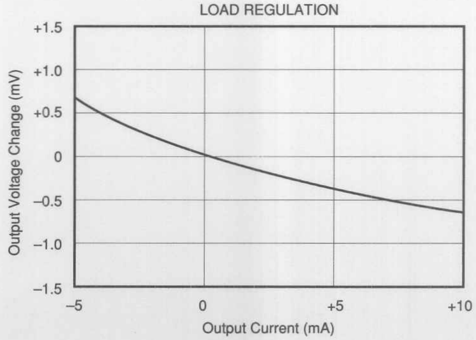
POWER TURN-ON RESPONSE with 1μF Cn



POWER SUPPLY REJECTION vs FREQUENCY



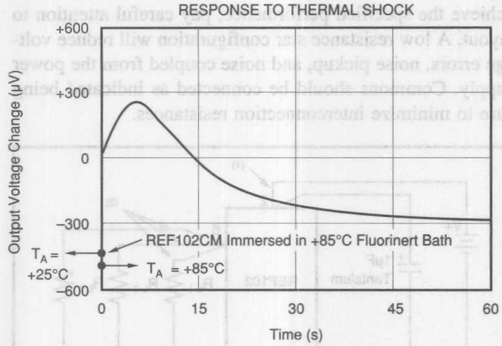
LOAD REGULATION



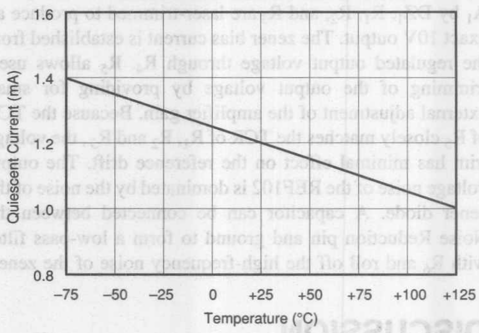
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = +15V$ unless otherwise noted.

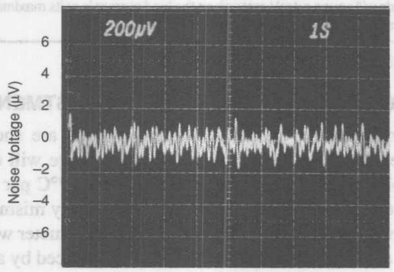
RESPONSE TO THERMAL SHOCK



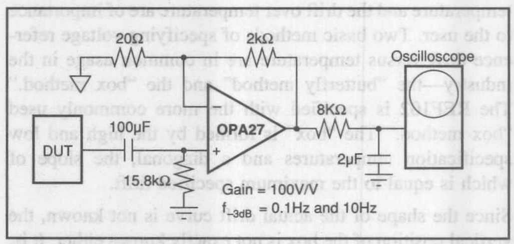
QUIESCENT CURRENT vs TEMPERATURE



TYPICAL REF102 REFERENCE NOISE



Low Frequency Noise (1s /div)
(See Noise Test Circuit)



Noise Test Circuit.

THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ_1, op amp A_1, and resistor network R_1–R_6.

Approximately 8.2V is applied to the non-inverting input of A_1 by DZ_1. R_1, R_2, and R_3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R_4. R_5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the TCR of R_5 closely matches the TCR of R_1, R_2 and R_3, the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R_6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the "butterfly method" and the "box method." The REF102 is specified with the more commonly used "box method." The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1). Figure 1 uses the REF102CM as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of –25°C to +85°C. The "box" height, V_1 to V_2, is 2.75mV.

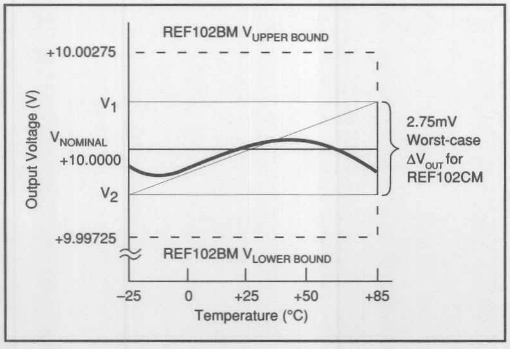
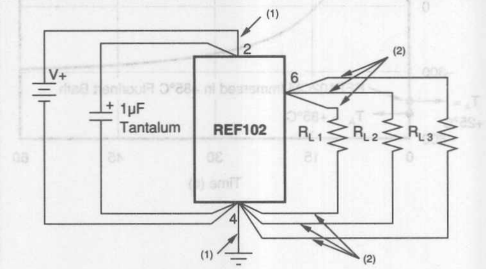


FIGURE 1. REF102CM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.



NOTES: (1) Lead resistances here of up to a few ohms have negligible effect on performance. (2) A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF102 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

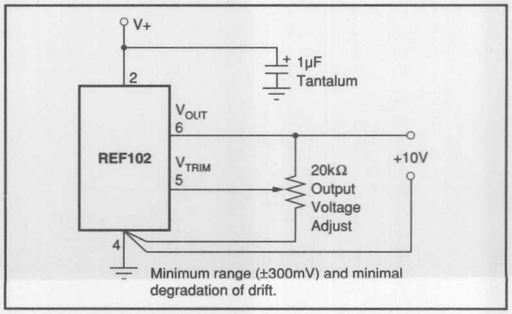


FIGURE 3. REF102 Optional Output Voltage Adjust.

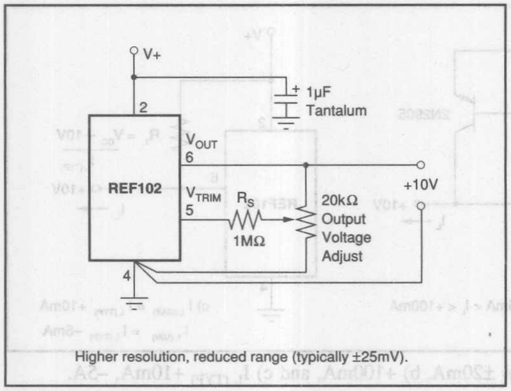


FIGURE 4. REF102 Optional Output Voltage Fine Adjust.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low pass filter with R_6 (refer to the figure on the first page of the data sheet) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1µF noise reduction capacitor on the high frequency noise of the REF102. R_6 is typically 7kΩ so the filter has a –3dB frequency of about 22Hz. The result is a reduction in noise from about 800µVp-p to under 200µ Vp-p. If further noise reduction is required, use the circuit in Figure 14.

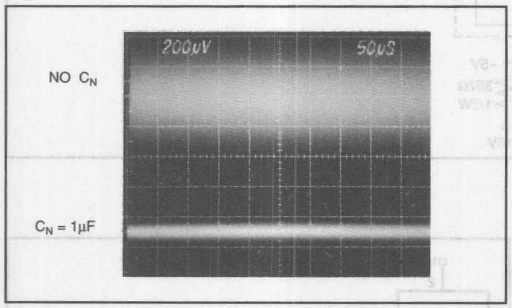


FIGURE 5. Effect of 1µF Noise Reduction Capacitor on Broadband Noise (f_{-3dB} = 1MHz).

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

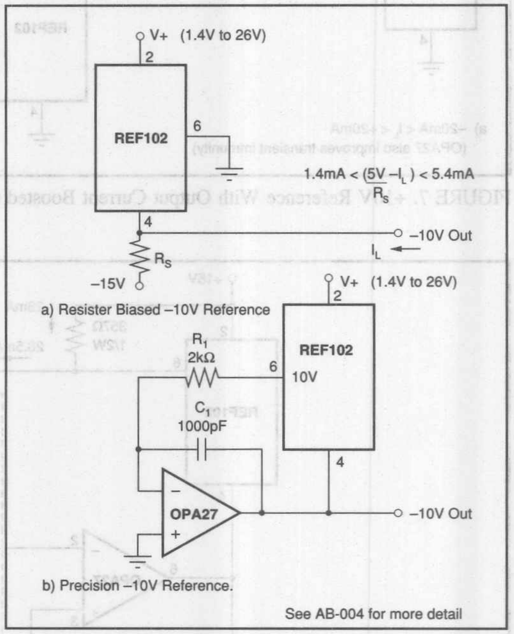


FIGURE 6. –10V Reference Using a) Resistor or b) OPA27.

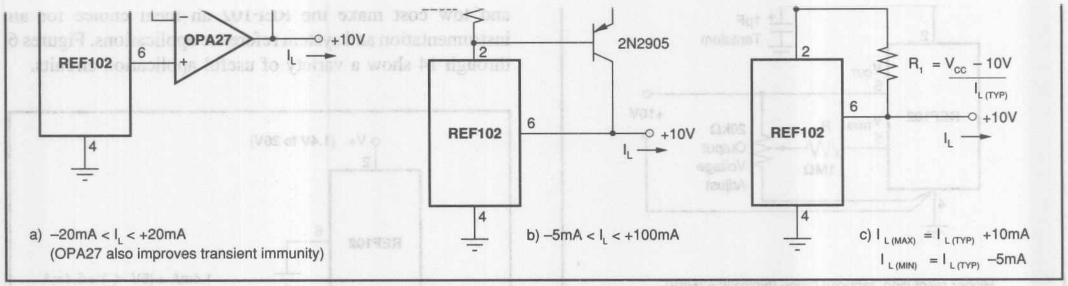


FIGURE 7. +10V Reference With Output Current Boosted to: a) ±20mA, b) +100mA, and c) $I_{L\,(TYP)}$ +10mA, −5A.

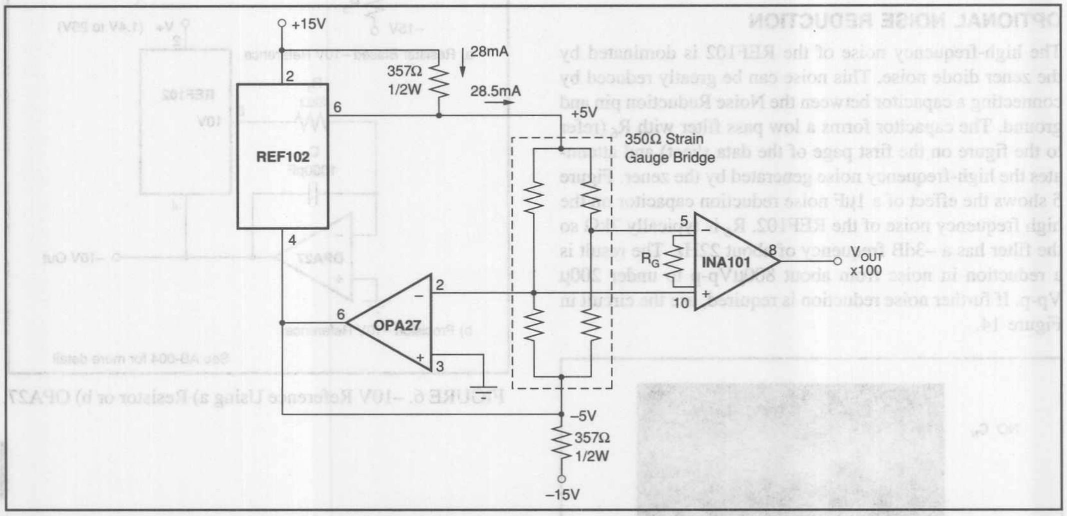


FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

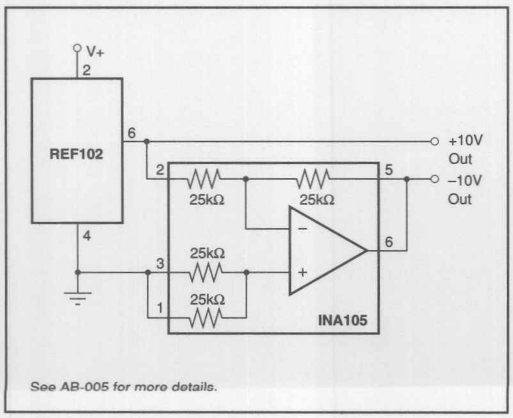


FIGURE 9. ±10V Reference.

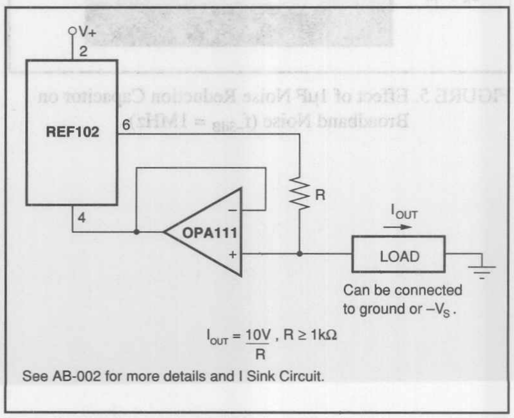
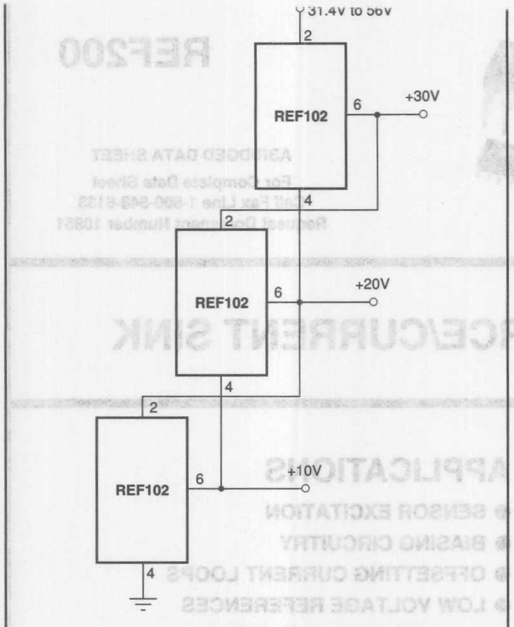


FIGURE 10. Positive Precision Current Source.



NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26 where n is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, –5mA. This includes the current delivered to the lower REF102.

FIGURE 11. Stacked References.

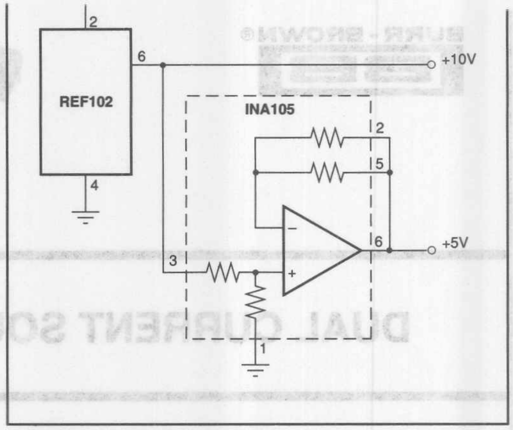


FIGURE 13. +5V and +10V Reference.

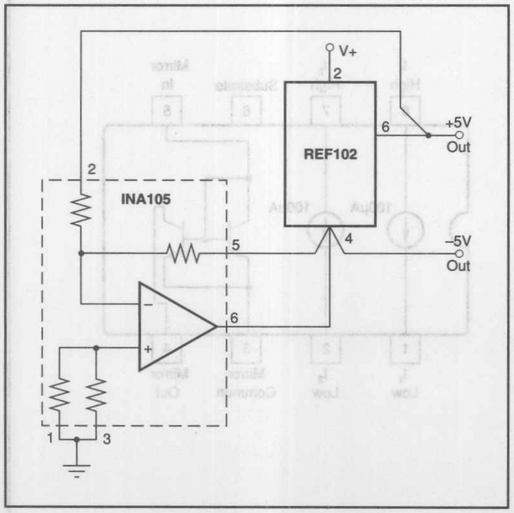


FIGURE 12. ±5V Reference.

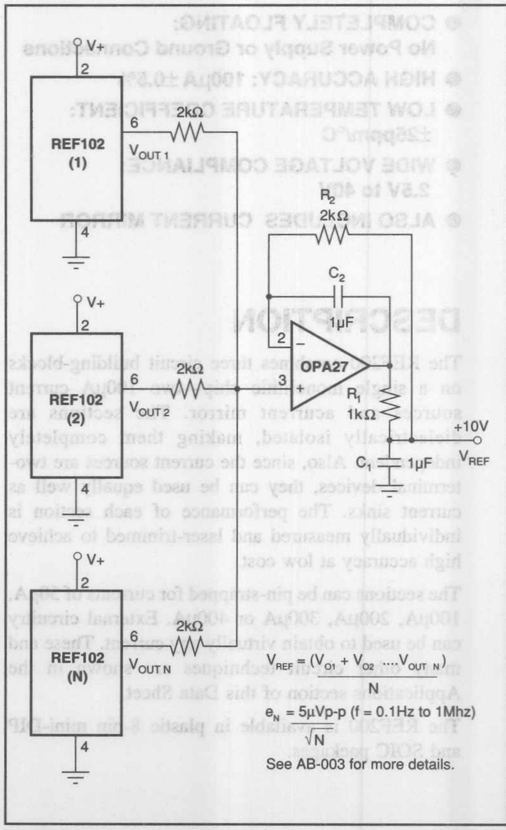
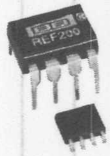


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

BURR - BROWN®

REF200



ABRIDGED DATA SHEET
For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 10851

DUAL CURRENT SOURCE/CURRENT SINK

FEATURES

- COMPLETELY FLOATING: No Power Supply or Ground Connections
- HIGH ACCURACY: 100µA ±0.5%
- LOW TEMPERATURE COEFFICIENT: ±25ppm/°C
- WIDE VOLTAGE COMPLIANCE: 2.5V to 40V
- ALSO INCLUDES CURRENT MIRROR

APPLICATIONS

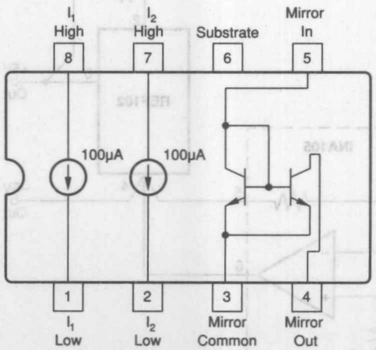
- SENSOR EXCITATION
- BIASING CIRCUITRY
- OFFSETTING CURRENT LOOPS
- LOW VOLTAGE REFERENCES
- CHARGE-PUMP CIRCUITRY
- HYBRID MICROCIRCUITS

DESCRIPTION

The REF200 combines three circuit building-blocks on a single monolithic chip—two 100µA current sources and acurrent mirror. The sections are dielectrically isolated, making them completely independent. Also, since the current sources are two-terminal devices, they can be used equally well as current sinks. The performance of each section is individually measured and laser-trimmed to achieve high accuracy at low cost.

The sections can be pin-strapped for currents of 50µA, 100µA, 200µA, 300µA or 400µA. External circuitry can be used to obtain virtually any current. These and many other circuit techniques are shown in the Applications section of this Data Sheet.

The REF200 is available in plastic 8-pin mini-DIP and SOIC packages.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-851C

SPECIFICATIONS

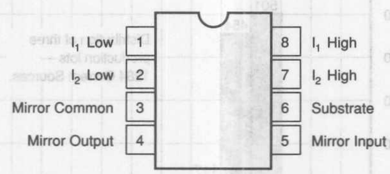
ELECTRICAL

T_A = +25°C, V_S = 15V unless otherwise noted.

PARAMETER	CONDITION	REF200AP, AU MIN	TYP	MAX	UNITS
CURRENT SOURCES					
Current Accuracy			±0.25	±1	%
Current Match			±0.25	±1	%
Temperature Drift	Specified Temp Range		25		ppm/°C
Output Impedance	2.5V to 40V	20	100		MΩ
	3.5V to 30V	200	500		MΩ
Noise	BW = 0.1Hz to 10Hz		1		nAp-p
	f = 10kHz		20		pA/√Hz
Voltage Compliance (1%)	T_{MIN} to T_{MAX}		See Curves		
Capacitance			10		pF
CURRENT MIRROR	I = 100µA Unless Otherwise Noted				
Gain		0.995	1	1.005	
Temperature Drift			25		ppm/°C
Impedance (output)	2V to 40V	40	100		MΩ
Nonlinearity	I = 0µA to 250µA		0.05		%
Input Voltage			1.4		V
Output Compliance Voltage			See Curves		
Frequency Response (–3dB)	Transfer		5		MHz
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–40		+85	°C
Storage		–40		+125	°C

PIN CONFIGURATION

Top View DIP/SOIC



ABSOLUTE MAXIMUM RATINGS

Applied Voltage	–6V to +40V
Reverse Current	–350µA
Voltage Between Any Two Sections	±80V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(SOIC 3s)	+260°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
REF200AP	8-Pin Plastic DIP	006
REF200AU	8-Pin SOIC	182

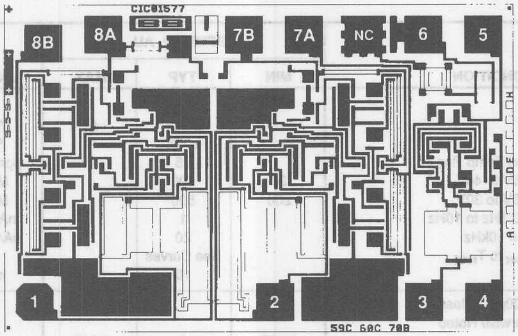
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL (1)	PACKAGE	TEMPERATURE RANGE
REF200AP	8-Pin Plastic DIP	–25°C to +85°C
REF200AU	8-Pin Plastic SOIC	–25°C to +85°C

NOTE: (1) Grade designation "A" may not be marked. Absence of grade designation indicates A grade.

DICE INFORMATION



REF200 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	I_1 Low	6	Substrate
2	I_2 Low	7A	I_2 High
3	Mirror Common	7B	I_2 High
4	Mirror Output	8A	I_1 High
5	Mirror Input	8B	I_1 High

Substrate Bias: $-V_{CC}$.

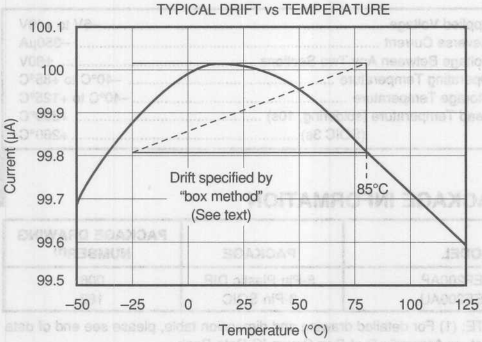
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	48 x 72 ±5	1.22 x 1.83 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None

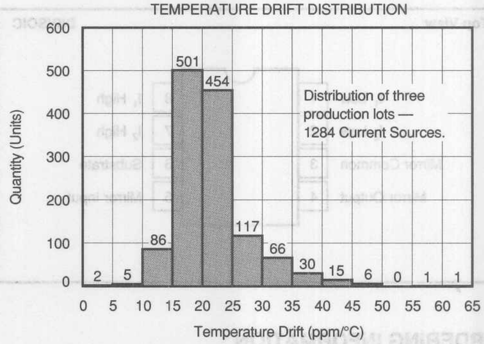
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = +15V$ unless otherwise noted.

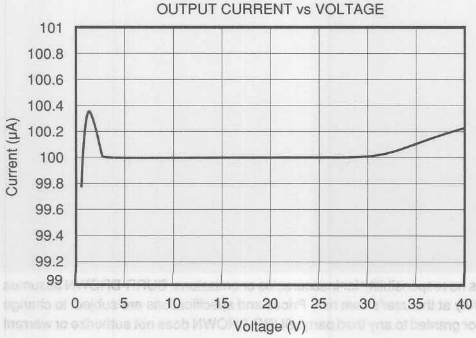
CURRENT SOURCE
TYPICAL DRIFT vs TEMPERATURE



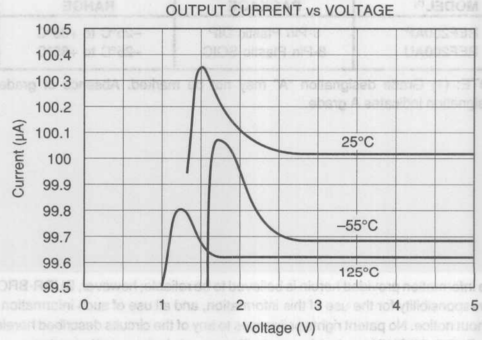
CURRENT SOURCE
TEMPERATURE DRIFT DISTRIBUTION



CURRENT SOURCE
OUTPUT CURRENT vs VOLTAGE

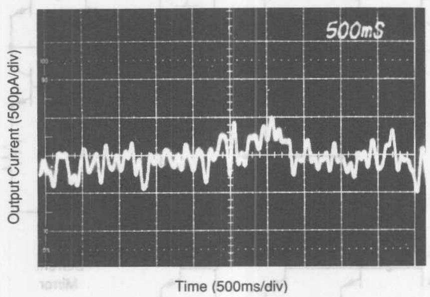


CURRENT SOURCE
OUTPUT CURRENT vs VOLTAGE

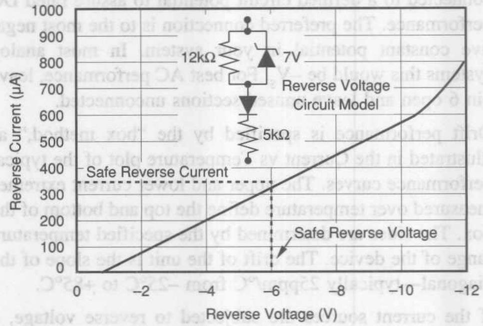


$T_A = +25°C$, $V_S = +15V$ unless otherwise noted.

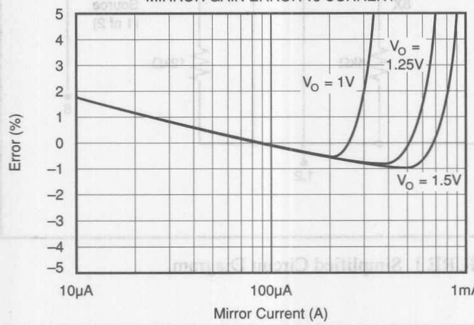
CURRENT SOURCE
CURRENT NOISE (0.1Hz to 10Hz)



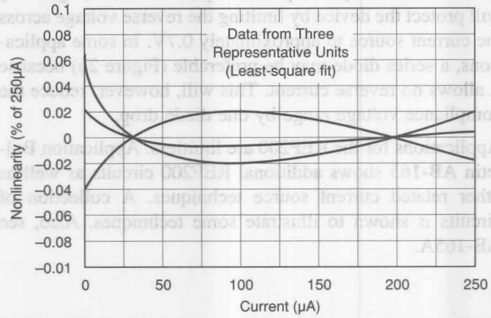
CURRENT SOURCE
REVERSE CURRENT vs REVERSE VOLTAGE



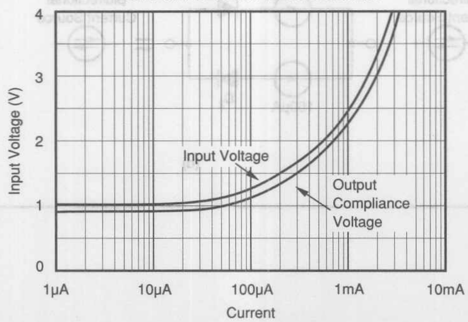
MIRROR GAIN ERROR vs CURRENT



MIRROR TRANSFER NONLINEARITY



MIRROR INPUT VOTAGE/OUTPUT
COMPLIANCE VOLTAGE vs CURRENT



APPLICATIONS INFORMATION

The three circuit sections of the REF200 are electrically isolated from one another using a dielectrically isolated fabrication process. A substrate connection is provided (pin 6), which is isolated from all circuitry. This pin should be connected to a defined circuit potential to assure rated DC performance. The preferred connection is to the most negative constant potential in your system. In most analog systems this would be $-V_S$. For best AC performance, leave pin 6 open and leave unused sections unconnected.

Drift performance is specified by the "box method," as illustrated in the Current vs Temperature plot of the typical performance curves. The upper and lower current extremes measured over temperature define the top and bottom of the box. The sides are determined by the specified temperature range of the device. The drift of the unit is the slope of the diagonal—typically 25ppm/°C from –25°C to +85°C.

If the current sources are subjected to reverse voltage, a protection diode may be required. A reverse voltage circuit model of the REF200 is shown in the Reverse Current vs Reverse Voltage curve. If reverse voltage is limited to less than 6V *or* reverse current is limited to less than 350µA, no protection circuitry is required. A parallel diode (Figure 2a) will protect the device by limiting the reverse voltage across the current source to approximately 0.7V. In some applications, a series diode may be preferable (Figure 2b) because it allows no reverse current. This will, however, reduce the compliance voltage range by one diode drop.

Applications for the REF200 are limitless. Application Bulletin AB-165 shows additional REF200 circuits as well as other related current source techniques. A collection of circuits is shown to illustrate some techniques. Also, see AB-165A.

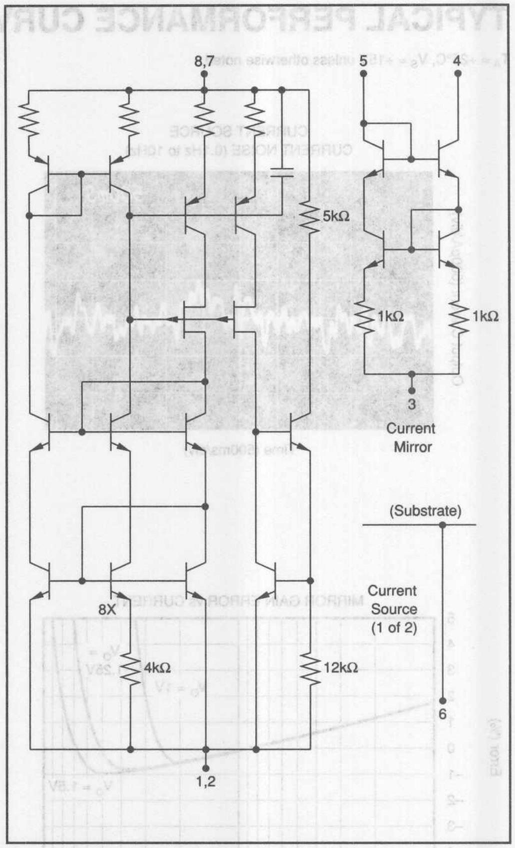


FIGURE 1. Simplified Circuit Diagram.

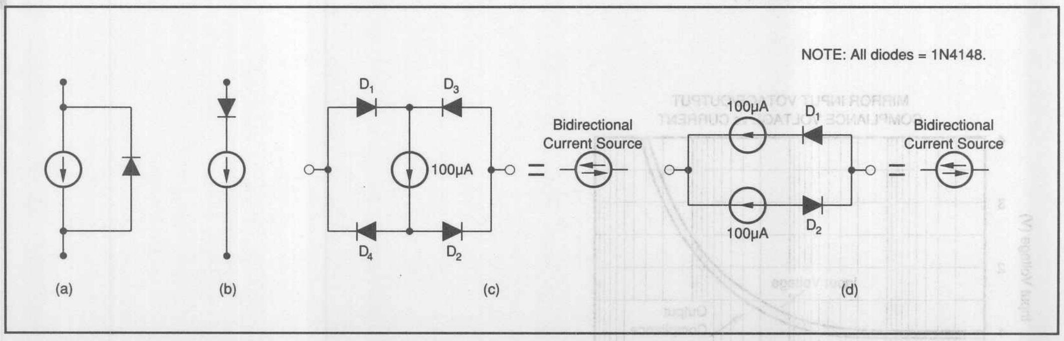


FIGURE 2. Reverse Voltage Protection.

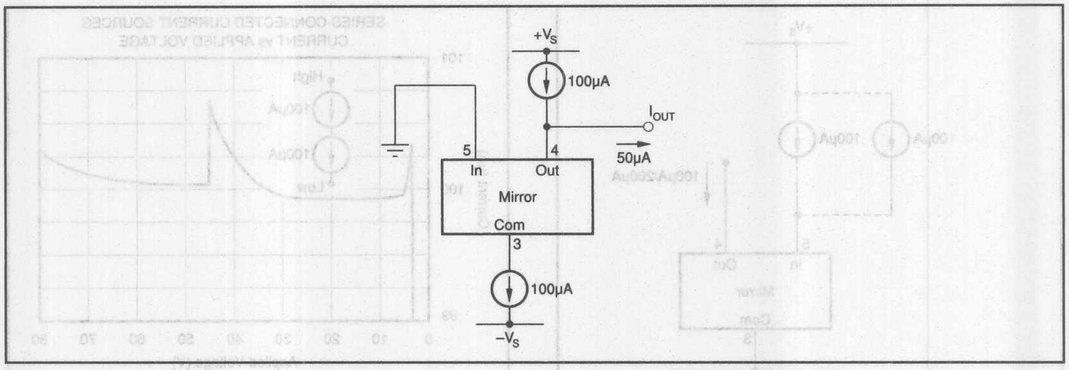


FIGURE 3. 50μA Current Source.

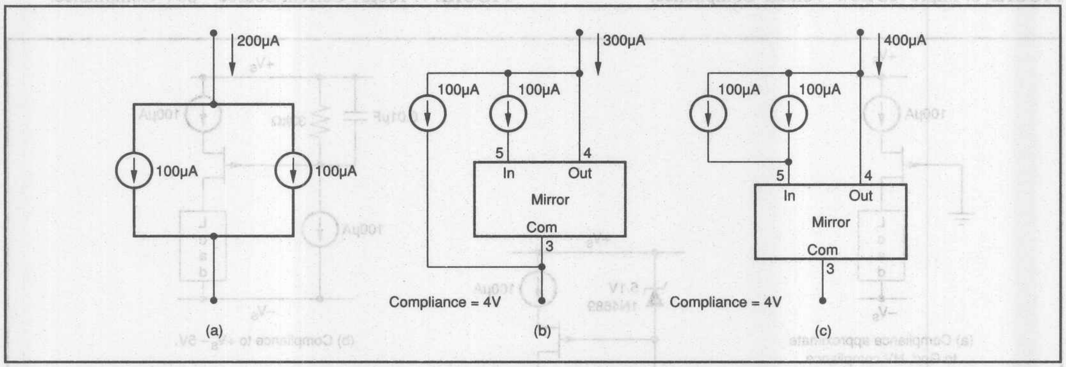


FIGURE 4. 200μA, 300μA, and 400μA Floating Current Sources.

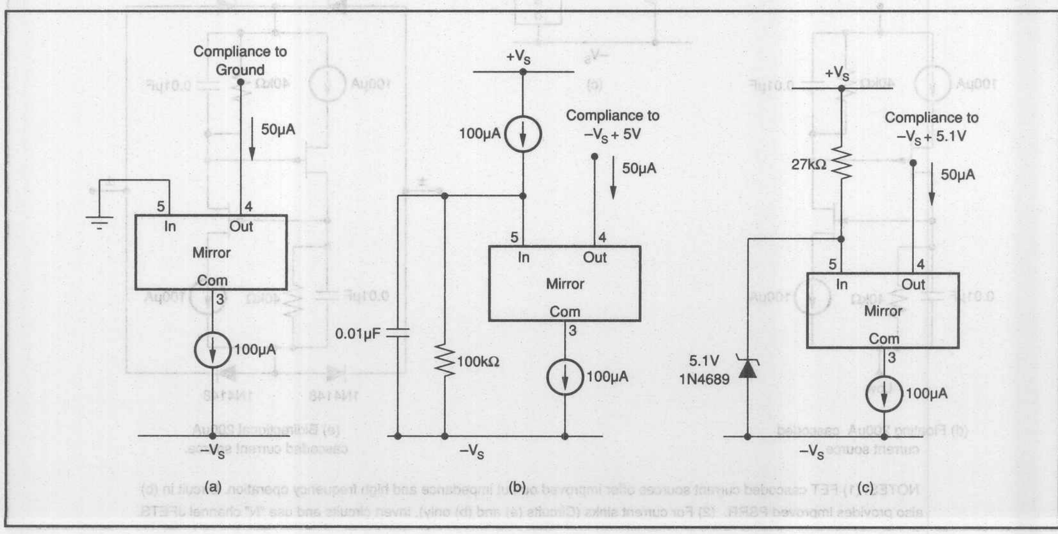


FIGURE 5. 50μA Current Sinks.

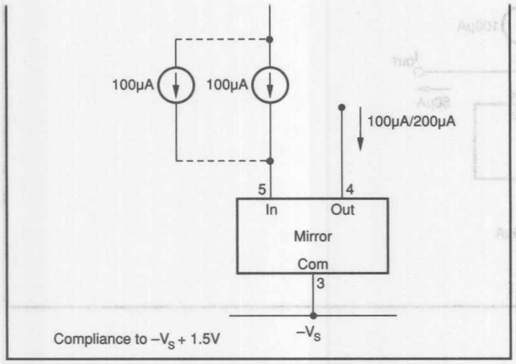


FIGURE 6. Improved Low-Voltage Compliance.

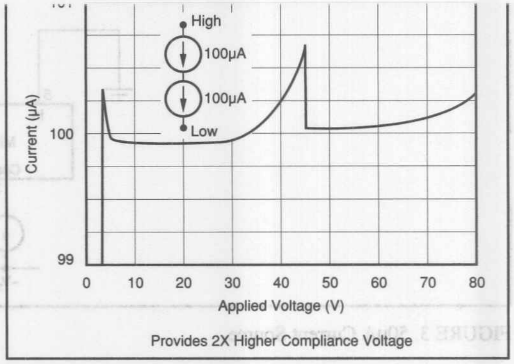
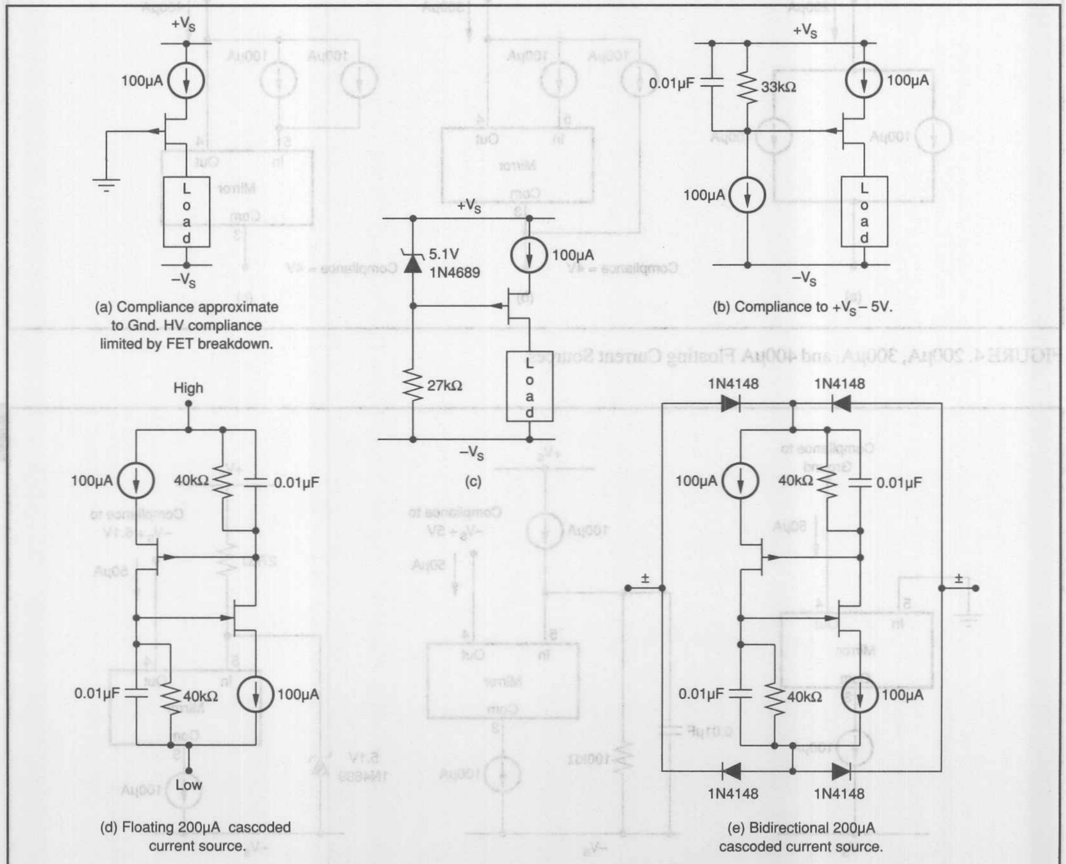
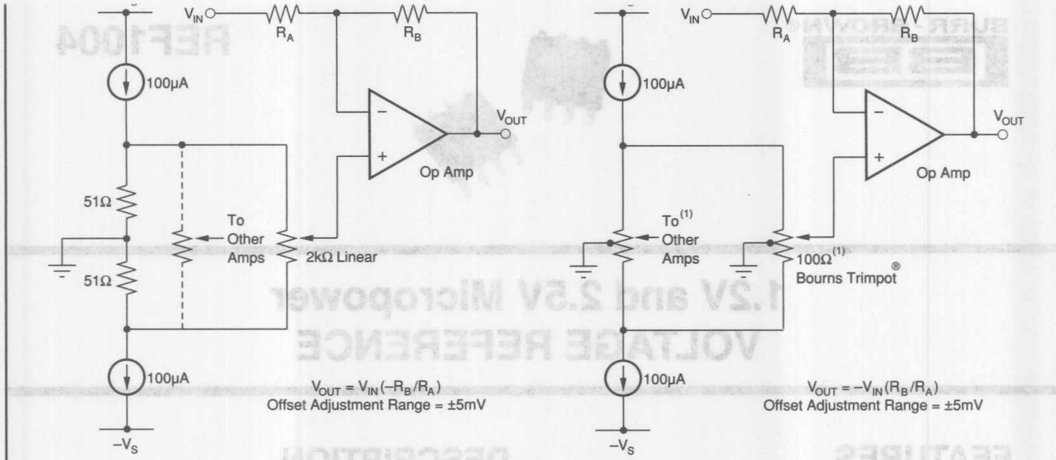


FIGURE 7. 100µA Current Source—80V Compliance.



NOTES: (1) FET cascoded current sources offer improved output impedance and high frequency operation. Circuit in (b) also provides improved PSRR. (2) For current sinks (Circuits (a) and (b) only), invert circuits and use "N" channel JFETS.

FIGURE 8. FET Cascode Circuits.

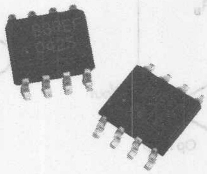


NOTE: (1) For N Op Amps, use Potentiometer Resistance = N • 100Ω.

FIGURE 9. Op Amp Offset Adjustment Circuits.

BURR - BROWN®

REF1004



1.2V and 2.5V Micropower VOLTAGE REFERENCE

FEATURES

- **INITIAL ACCURACY:**
  REF1004-1.2 ±4mV
  REF1004-2.5 ±20mV
- **MINIMUM OPERATING CURRENT:**
  REF1004-1.2 10µA
  REF1004-2.5 20µA
- **EXCELLENT LONG TERM TEMPERATURE STABILITY**
- **VERY LOW DYNAMIC IMPEDANCE**
- **OPERATES UP TO 20mA**
- **PACKAGE: 8-Lead SOIC**

APPLICATIONS

- **BATTERY POWERED TEST EQUIPMENT**
- **PORTABLE MEDICAL INSTRUMENTATION**
- **PORTABLE COMMUNICATIONS DEVICES**
- **A/D AND D/A CONVERTERS**
- **NOTEBOOK AND PALMTOP COMPUTERS**

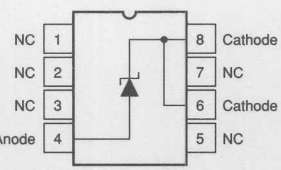
DESCRIPTION

The REF1004-1.2 and REF1004-2.5 are two terminal bandgap reference diodes designed for high accuracy with outstanding temperature characteristics at low operating currents. Prior to the introduction of the REF1004 Micropower Voltage References, accuracy and stability specifications could only be attained by expensive screening of standard devices. The REF1004 is a cost effective solution when reference voltage accuracy, low power, and long term temperature stability are required.

REF1004 is a drop-in replacement for the LT1004 as well as an upgraded replacement of the LM185/385 series references. The REF1004C is characterized for operation from 0°C to 70°C and the REF1004I is characterized for operation from –40°C to +85°C.

The REF1004 is offered in an 8-lead Plastic SOIC package and shipped in anti-static rails or tape and reel.

Typical Operating Circuit



(Top View)

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C unless otherwise noted.

		REF1004-1.2			REF1004-2.5			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
REFERENCE VOLTAGE	I_R = 100µA	1.231	1.235	1.239	2.490	2.500	2.511	V
REF1004C(1)		1.229	1.235	1.239	2.487	2.500	2.511	
REF1004I(2)		1.225	1.235	1.239	2.480	2.500	2.511	
AVERAGE TEMPERATURE COEFFICIENT	$I_{MIN} \le I_R \le$ 20mA		20			20		ppm/°C
MINIMUM OPERATION CURRENT(3)			8	10		12	20	µA
REVERSE BREAKDOWN VOLTAGE CHANGE WITH CURRENT	$I_{MIN} \le I_R \le$ 1mA			1 1.5(3)			1 1.5(3)	mV
	1mA $\le I_R \le$ 20mA			10 20(3)			10 20(3)	
REVERSE DYNAMIC IMPEDANCE(3)	I_R = 100µA		0.2	0.6		0.2	0.6	Ω
WIDE BAND NOISE (RMS) 10Hz $\le I_R \le$ 10kHz	I_R = 100µA		60			120		µV
LONG TERM STABILITY T_A = 25°C ± 0.1°C	I_R = 100µA		20			20		ppm/KHr

NOTES: (1) This specification applies over the full operating temperature range of 0°C $\le T_A \le$ 70°C. (2) This specification applies over the full operating temperature range of 40°C $\le T_A \le$ +85°C. (3) Denotes the specifications which apply over the full operating temperature range.

ORDERING INFORMATION

MODEL	T_A	V_Z	PACKAGE
REF1004C-1.2	0°C to +70°C	1.2V	8-Lead SOIC
REF1004C-2.5	0°C to +70°C	2.5V	8-Lead SOIC
REF1004I-1.2	–40°C to +85°C	1.2V	8-Lead SOIC
REF1004I-2.5	–40°C to +85°C	2.5V	8-Lead SOIC

NOTE: Available in Tape and Reel, Add –TR to Model Number.

ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current	30mA
Forward Current	10mA
Operating Temperature Range	
REF1004C	0°C to +70°C
REF1004I	–40°C to +85°C
Storage Temperature	
REF1004C	–65°C to +150°C
REF1004I	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

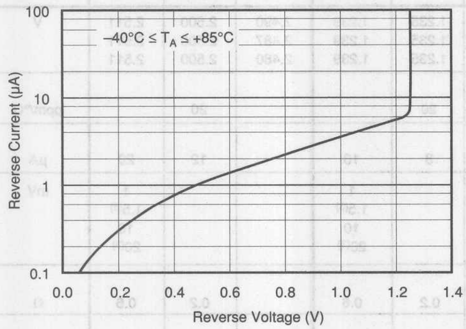
MODEL	PART MARKING
REF1004C-1.2	BBREF0412
REF1004C-2.5	BBREF0425
REF1004I-1.2	BBREF0412
REF1004I-2.5	BBREF0425

PACKAGE INFORMATION

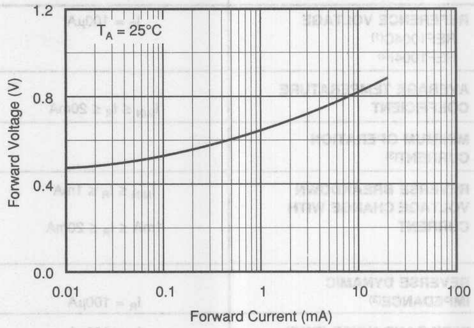
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
REF1004C-1.2	8-Pin SOIC	182
REF1004C-2.5	8-Pin SOIC	182
REF1004I-1.2	8-Pin SOIC	182
REF1004I-2.5	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

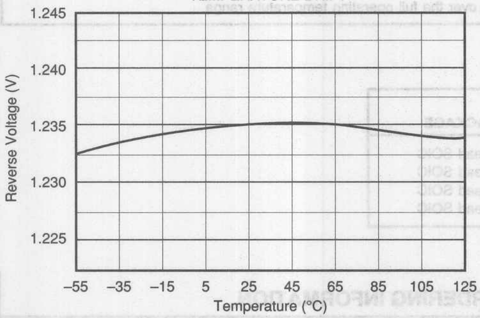
REVERSE CHARACTERISTICS



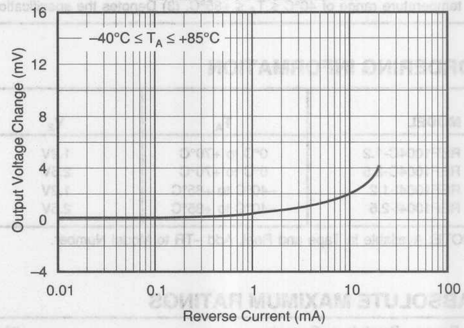
FORWARD CHARACTERISTICS



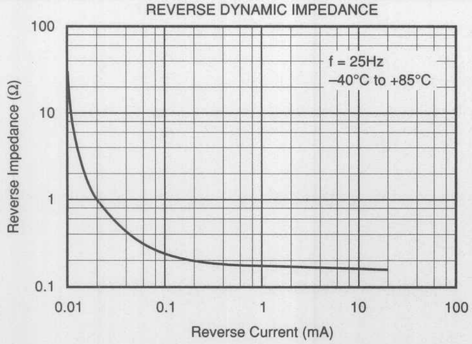
TEMPERATURE DRIFT



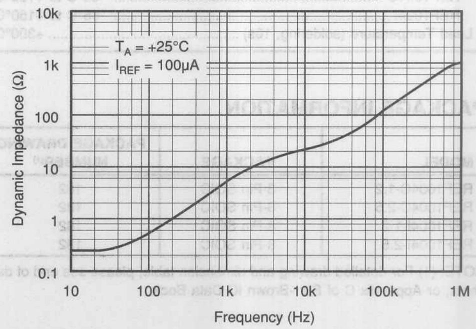
REVERSE VOLTAGE CHANGE



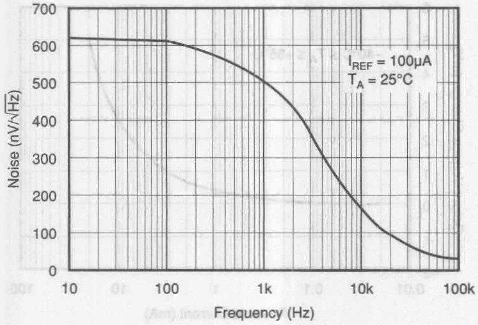
REVERSE DYNAMIC IMPEDANCE



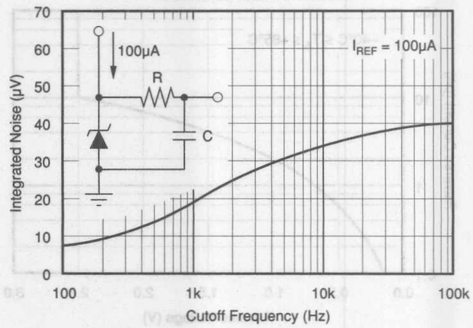
REVERSE DYNAMIC IMPEDANCE



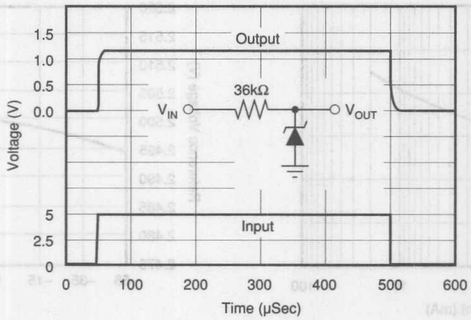
NOISE VOLTAGE



FILTERED OUTPUT NOISE

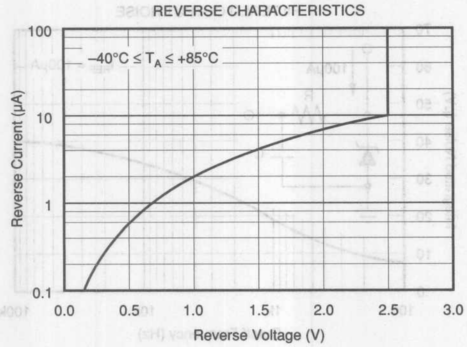


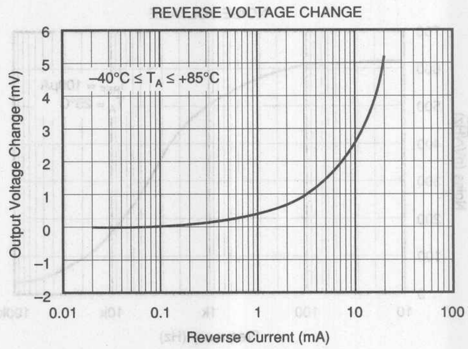
RESPONSE TIME

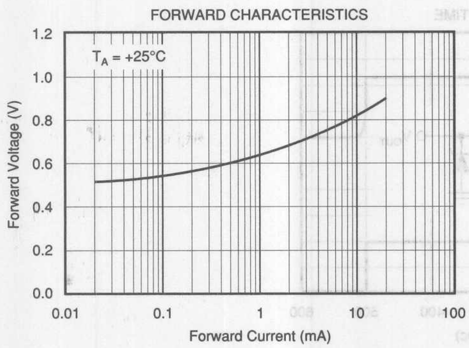


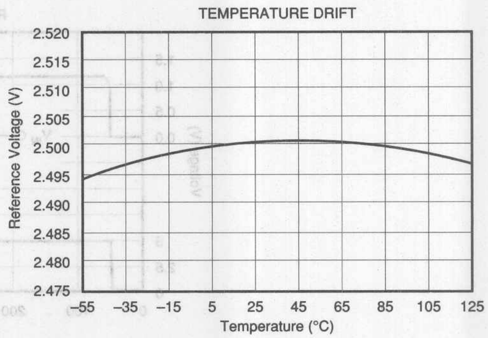
TYPICAL PERFORMANCE CURVES 2.5V

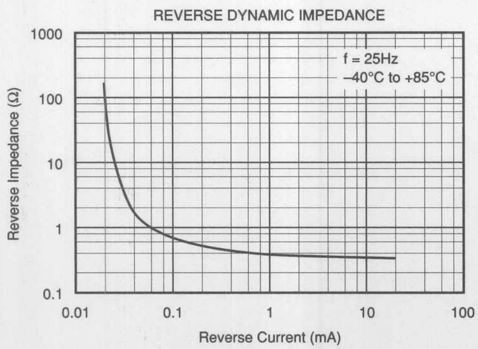
T_A = +25°C unless otherwise noted.

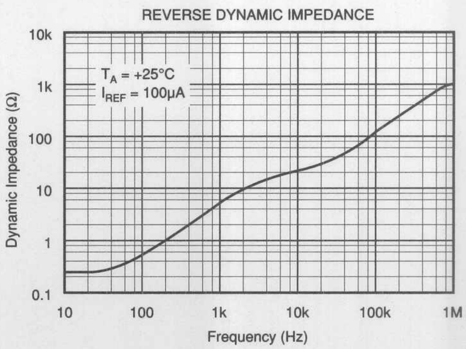








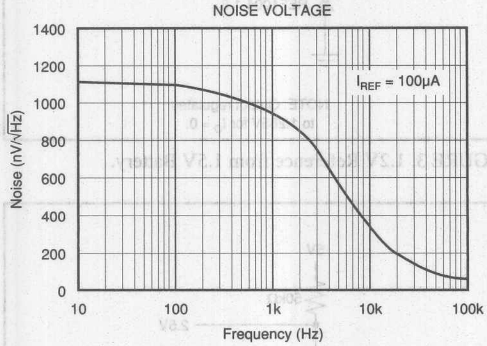




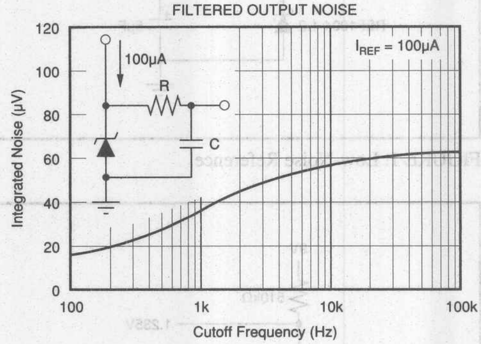
TYPICAL PERFORMANCE CURVES 2.5V (CONT)

T_A = +25°C unless otherwise noted.

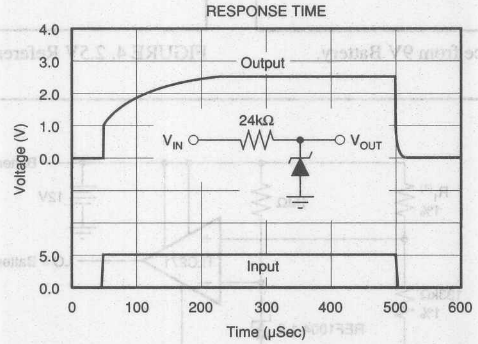
NOISE VOLTAGE



FILTERED OUTPUT NOISE



RESPONSE TIME



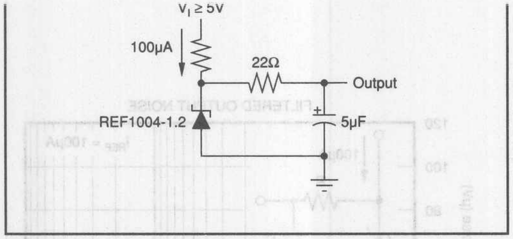


FIGURE 1. Low-Noise Reference.

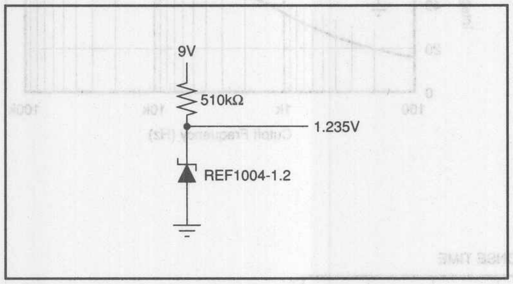


FIGURE 2. Micropower Reference from 9V Battery.

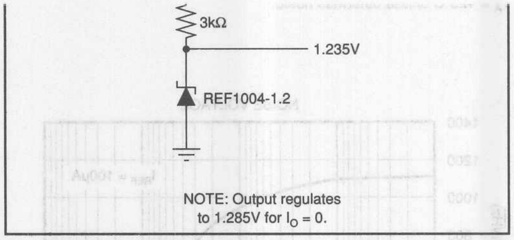


FIGURE 3. 1.2V Reference from 1.5V Battery.

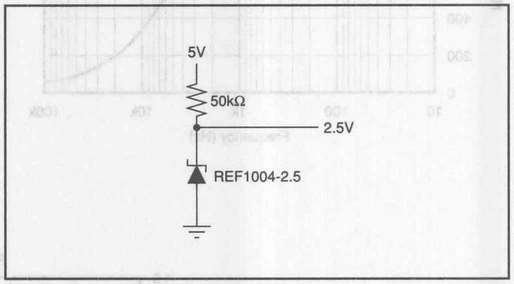


FIGURE 4. 2.5V Reference.

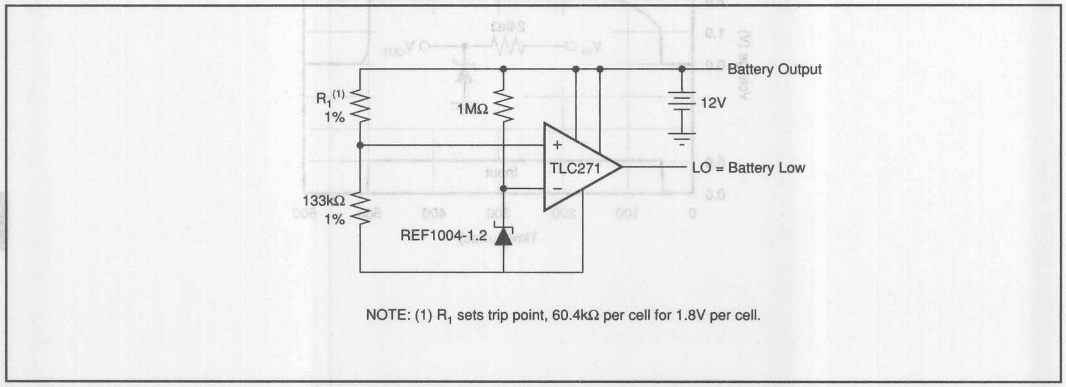


FIGURE 5. Lead-Acid Low-Battery-Voltage Detector.

REG1117

800mA Low Dropout Positive Regulator
2.85V, 3V, 3.3V, 5V, and Adjustable

FEATURES

- 2.85V, 3V, 3.3V, 5V, and ADJUSTABLE VERSIONS
- 2.85V MODEL FOR SCSI-2 ACTIVE TERMINATION
- OUTPUT CURRENT: 800mA max
- OUTPUT TOLERANCE: ±1% max
- TOTAL OUTPUT VARIATION: ±2%
- 1.2V max DROPOUT VOLTAGE AT I_O = 800mA
- INTERNAL CURRENT LIMIT
- THERMAL OVERLOAD PROTECTION
- SOT-223 SURFACE MOUNT PACKAGE

APPLICATIONS

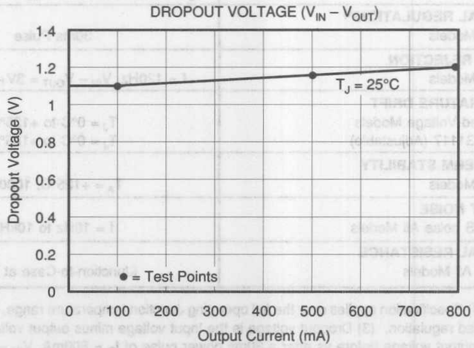
- SCSI-2 ACTIVE TERMINATION
- HAND-HELD DATA COLLECTION DEVICES
- HIGH EFFICIENCY LINEAR REGULATORS
- 5V LINEAR REGULATORS
- BATTERY POWERED INSTRUMENTATION
- BATTERY MANAGEMENT CIRCUITS FOR NOTEBOOK AND PALMTOP PCs

DESCRIPTION

The REG1117 is a family of three-terminal voltage regulators capable of up to 800mA output. Fixed output models include 2.85V, 3V, 3.3V and 5V versions. Output voltage of the adjustable version is set with two external resistors. The REG1117's low dropout voltage allows its use with as little as 1V input-output voltage differential.

Laser trimming assures excellent output voltage accuracy without adjustment. An NPN output stage allows output stage drive to contribute to the load current for maximum efficiency.

REG1117 is packaged in an SOT-223 surface-mount package, suitable for reflow soldering techniques.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

T_J = +25°C unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE						
REG1117-2.85		I_O = 10mA, V_{IN} = 4.85V	2.82	2.85	2.88	V
	Note 1	I_O = 0 to 800mA, V_{IN} = 4.05 to 10V	2.79	2.85	2.91	V
REG1117-3		I_O = 10mA, V_{IN} = 5V	2.97	3.00	3.03	V
	Note 1	I_O = 0 to 800mA, V_{IN} = 4.5 to 10V	2.94	3.00	3.06	V
REG1117-3.3		I_O = 10mA, V_{IN} = 5.3V	3.27	3.30	3.33	V
	Note 1	I_O = 0 to 800mA, V_{IN} = 4.8 to 10V	3.24	3.30	3.36	V
REG1117-5		I_O = 10mA, V_{IN} = 7V	4.95	5.00	5.05	V
	Note 1	I_O = 0 to 800mA, V_{IN} = 6.5 to 10V	4.90	5.00	5.10	V
REFERENCE VOLTAGE						
REG1117 (Adjustable)		I_O = 10mA, V_{IN} = 3.25V	1.238	1.250	1.262	V
	Note 1	I_O = 10 to 800mA, $V_{IN} - V_O$ = 1.4 to 10V	1.225	1.250	1.280	V
LINE REGULATION						
REG1117-2.85	Note 1	I_O = 0, V_{IN} = 4.25 to 10V		1	7	mV
REG1117-3	Note 1	I_O = 0, V_{IN} = 4.5 to 10V		2	7	mV
REG1117-3.3	Note 1	I_O = 0, V_{IN} = 4.8 to 10V		2	7	mV
REG1117-5	Note 1	I_O = 0, V_{IN} = 6.5 to 15V		3	10	mV
REG1117 (Adjustable)	Note 1	I_O = 10mA, $V_{IN} - V_O$ = 1.5 to 13.75V		0.1	0.4	%
LOAD REGULATION						
REG1117-2.85	Note 1	I_O = 0 to 800mA, V_{IN} = 4.25V		2	10	mV
REG1117-3	Note 1	I_O = 0 to 800mA, V_{IN} = 4.5V		2	12	mV
REG1117-3.3	Note 1	I_O = 0 to 800mA, V_{IN} = 4.8V		3	12	mV
REG1117-5	Note 1	I_O = 0 to 800mA, V_{IN} = 6.5V		3	15	mV
REG1117(2) (Adjustable)	Note 1	I_O = 10 to 800mA, $V_{IN} - V_O$ = 3V		0.1	0.4	%
DROPOUT VOLTAGE(3)						
All Models	Note 1	I_O = 100mA		1.00	1.10	V
	Note 1	I_O = 500mA		1.05	1.15	V
	Note 1	I_O = 800mA		1.10	1.20	V
CURRENT LIMIT						
All Models		$V_{IN} - V_O$ = 5V	800	950	1200	mA
MINIMUM LOAD CURRENT						
REG1117 (Adjustable)	Note 1	$V_{IN} - V_O$ = 13.75V		1.7	5	mA
QUIESCENT CURRENT						
Fixed-Voltage Models	Note 1	$V_{IN} - V_O$ = 5V		4	10	mA
REG1117 Adjust Pin Current(2)	Note 1			50	120	µA
vs Load Current	Note 1	I_O = 10mA to 800mA, $V_{IN} - V_O$ = 1.4 to 10V		0.5	5	µA
THERMAL REGULATION(4)						
All Models		30ms Pulse		0.01	0.1	%/W
RIPPLE REJECTION						
All Models		f = 120Hz, $V_{IN} - V_{OUT}$ = 3V+1V_{PP} Ripple		62		dB
TEMPERATURE DRIFT						
Fixed-Voltage Models		T_J = 0°C to +125°C		0.5		%
REG1117 (Adjustable)		T_J = 0°C to +125°C		2		%
LONG-TERM STABILITY						
All Models		T_A = +125°C, 1000Hr		0.3		%
OUTPUT NOISE						
RMS noise All Models		f = 10Hz to 10kHz		0.003		%
THERMAL RESISTANCE						
θ_{JC} All Models		(Junction-to-Case at Tab)		15		°C/W

NOTES: (1) Specification applies over the full operating Junction temperature range, 0°C to 125°C. (2) REG1117 adjustable version requires a minimum load current for ±2% load regulation. (3) Dropout voltage is the Input voltage minus output voltage that produces a 1% decrease in output voltage. (4) Percentage change in unloaded output voltage before vs after a 30ms power pulse of I_O = 800mA, $V_{IN} - V_O$ = 1.4V.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	Internally Limited
Input Voltage	15V
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	–40°C to +150°C
Lead Temperature (soldering, 10s)(1)	+300°C

NOTE: (1) See "Soldering Methods."

ORDERING INFORMATION

MODEL(1)	PART MARKING	PACKAGE
REG1117-2.85	BB11172	Plastic SOT-223
REG1117-3	BB11173	Plastic SOT-223
REG1117-3.3	BB11174	Plastic SOT-223
REG1117-5	BB11175	Plastic SOT-223
REG1117	BB1117	Plastic SOT-223

NOTE: (1) Available in Tape and Reel, add –TR to Model Number.

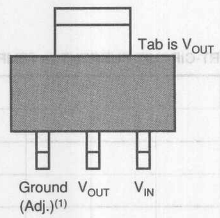
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
REG1117-2.85	Plastic SOT-223	311
REG1117-3	Plastic SOT-223	311
REG1117-3.3	Plastic SOT-223	311
REG1117-5	Plastic SOT-223	311
REG1117	Plastic SOT-223	311

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

CONNECTION DIAGRAM

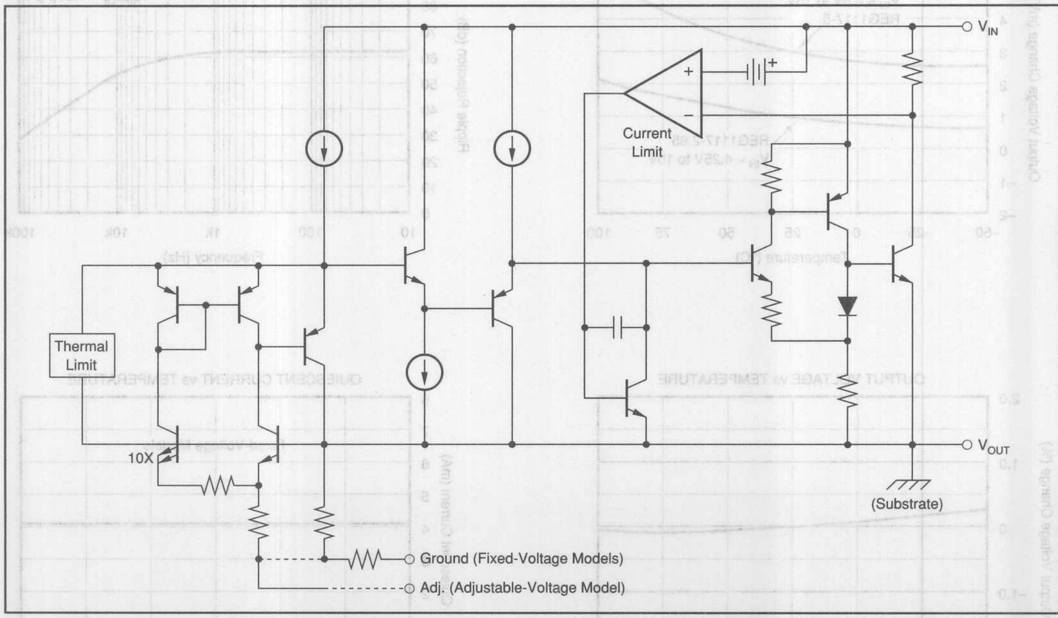
Front View **SOT-223**



Plastic SOT-223

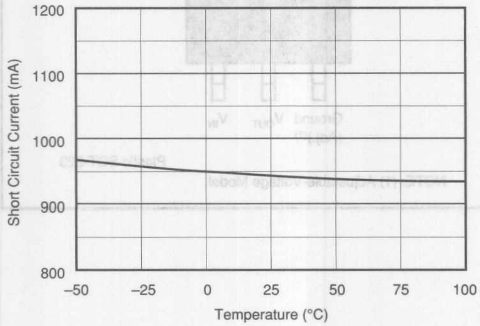
NOTE: (1) Adjustable-Voltage Model.

SIMPLIFIED SCHEMATIC



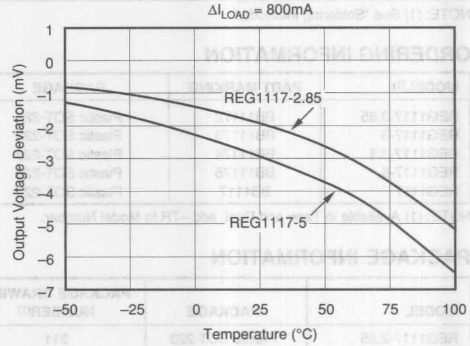
T_J = +25°C, unless otherwise specified.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

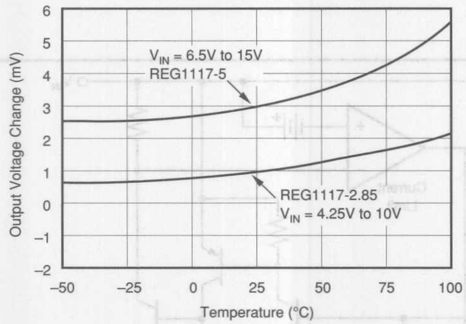


LOAD REGULATION

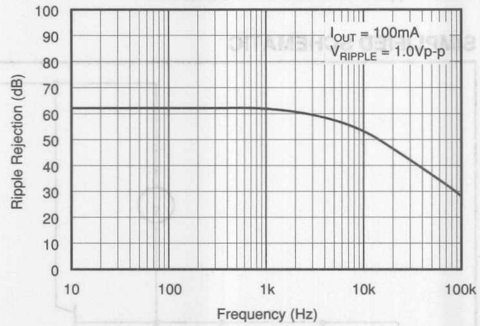
ΔI_{LOAD} = 800mA



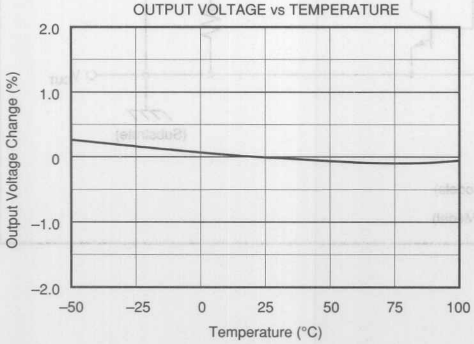
LINE REGULATION vs TEMPERATURE



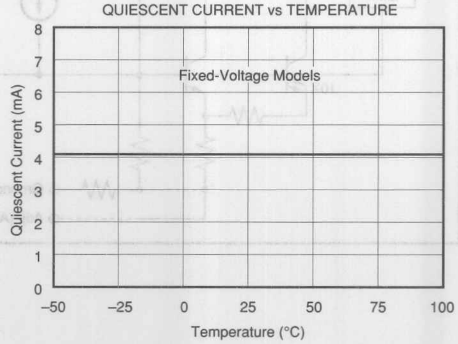
RIPPLE REJECTION vs FREQUENCY



OUTPUT VOLTAGE vs TEMPERATURE

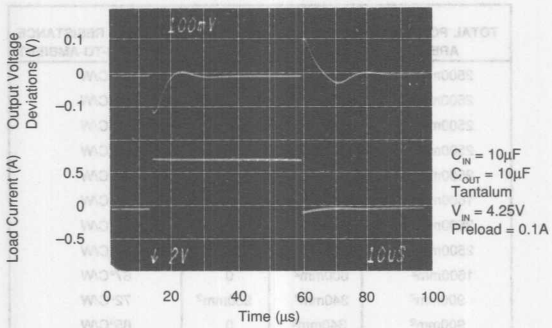


QUIESCENT CURRENT vs TEMPERATURE

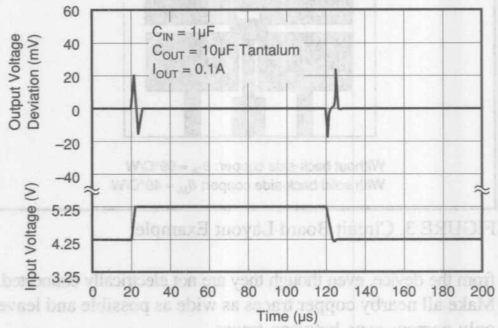


T_J = +25°C, unless otherwise specified.

LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



APPLICATIONS INFORMATION

Figure 1 shows the basic hookup diagram for fixed-voltage models. All models require an output capacitor for proper operation and to improve high frequency load regulation. A 10µF tantalum capacitor is recommended. Aluminum electrolytic types of 50µF or greater can also be used. A high quality capacitor should be used to assure that the ESR (effective series resistance) is less than 0.5Ω.

Figure 2 shows a the hookup diagram for the adjustable voltage model. Resistor values are shown for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2. For best load regulation, connect R_1 close to the output pin and R_2 close to the ground side of the load as shown.

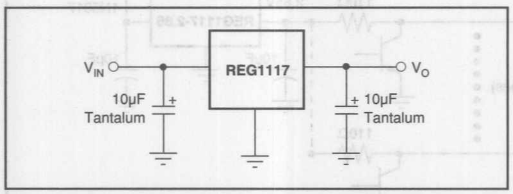


FIGURE 1. Fixed-Voltage Model—Basic Connections.

THERMAL CONSIDERATIONS

The REG1117 has current limit and thermal shutdown circuits that protect it from overload. The thermal shutdown activates at approximately T_J = 165°C. For continuous operation, however, the junction temperature should not be allowed to exceed 125°C. Any tendency to activate the thermal shutdown in normal use is an indication of an inadequate heat sink or excessive power dissipation. The power dissipation is equal to:

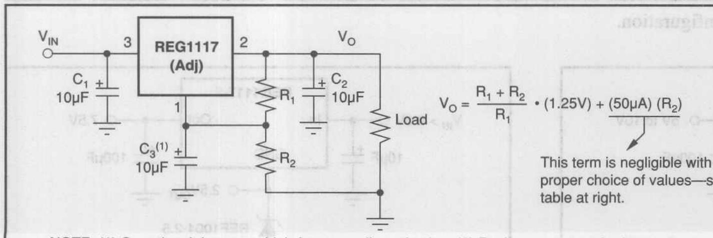
$$P_D = (V_{IN} – V_{OUT})\, I_{OUT}$$

The junction temperature can be calculated by:

$$T_J = T_A + P_D\,(\theta_{JA})$$

where T_A is the ambient temperature, and
θ_{JA} is the junction-to-ambient thermal resistance

The REG1117 derives heat sinking from conduction through its copper leads, especially the large mounting tab. These must be soldered to a circuit board with a substantial amount of copper remaining (see Figure 3). Circuit board traces connecting to the tab and the leads should be made as large as practical. Other nearby circuit traces, including those on the back side of the circuit board, help conduct heat away



$$V_O = \frac{R_1 + R_2}{R_1} \cdot (1.25V) + (50µA)\,(R_2)$$

V_{OUT} (V)	R_1 (Ω)(2)	R_2 (Ω)(2)
1.25	Open	Short
1.5	750	147
2.1	158	107
2.85	169	215
3	137	191
3.3	115	187
5	113	340
10	113	787

NOTE: (1) C_3 optional. Improves high-frequency line rejection. (2) Resistors are standard 1% values.

FIGURE 2. Adjustable-Voltage Model—Basic Connections.

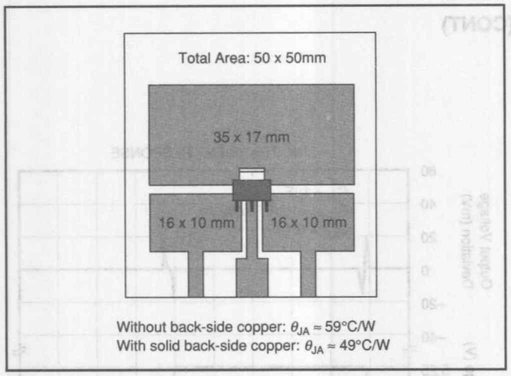


FIGURE 3. Circuit Board Layout Example.

from the device, even though they are not electrically connected. Make all nearby copper traces as wide as possible and leave only narrow gaps between traces.

Table I shows approximate values of θ_{JA} for various circuit board and copper areas. Nearby heat dissipating components, circuit board mounting conditions and ventilation can dramatically affect the actual θ_{JA}.

A simple experiment will determine whether the maximum recommended junction temperature is exceeded in an actual circuit board and mounting configuration: Increase the ambient temperature above that expected in normal operation until the device's thermal shutdown is activated. If this occurs at more than 40°C above the maximum expected ambient temperature, then the T_J will be less than 125°C during normal operation.

SOLDERING METHODS

The REG1117 package is suitable for infrared reflow and vapor-phase reflow soldering techniques. The high rate of temperature change that occurs with wave soldering, or hand soldering can damage the REG1117.

TOTAL PC BOARD AREA	TOPSIDE(1) COPPER AREA	BACKSIDE COPPER AREA	THERMAL RESISTANCE JUNCTION-TO-AMBIENT
2500mm²	2500mm²	2500mm²	46°C/W
2500mm²	1250mm²	2500mm²	47°C/W
2500mm²	950mm²	2500mm²	49°C/W
2500mm²	2500mm²	0	51°C/W
2500mm²	1800mm²	0	53°C/W
1600mm²	600mm²	1600mm²	55°C/W
2500mm²	1250mm²	0	58°C/W
2500mm²	915mm²	0	59°C/W
1600mm²	600mm²	0	67°C/W
900mm²	340mm²	900mm²	72°C/W
900mm²	340mm²	0	85°C/W

NOTE: (1) Tab is attached to the topside copper.

TABLE I.

INSPEC Abstract Number: B91007604, C91012627
Kelly, E.G. "Thermal Characteristics of Surface 5WK9Ω Packages." The Proceedings of SMTCON. Surface Mount Technology Conference and Exposition: *Competitive Surface Mount Technology*, April 3-6, 1990, Atlantic City, NJ, USA. *Abstract Publisher*: IC Manage, 1990, Chicago, IL, USA.

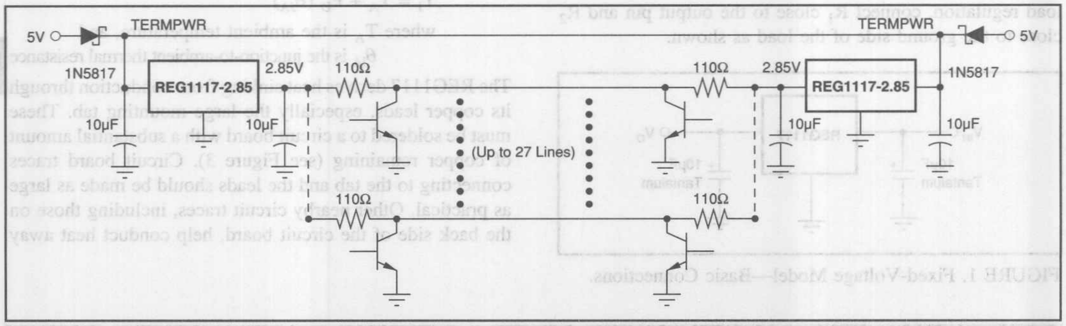


FIGURE 4. SCSI Active Termination Configuration.

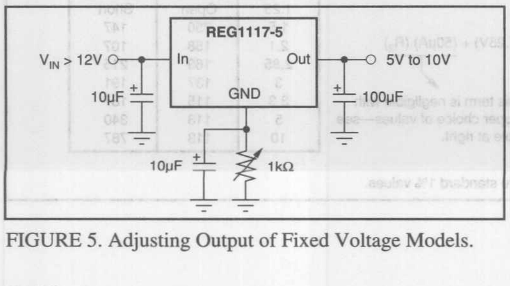


FIGURE 5. Adjusting Output of Fixed Voltage Models.

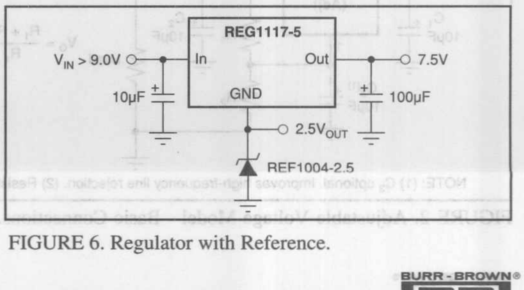


FIGURE 6. Regulator with Reference.

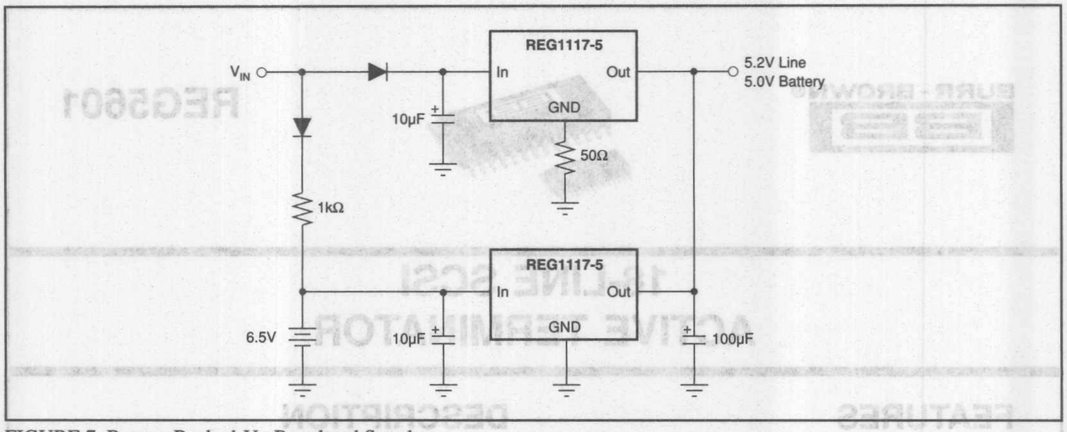


FIGURE 7. Battery Backed-Up Regulated Supply.

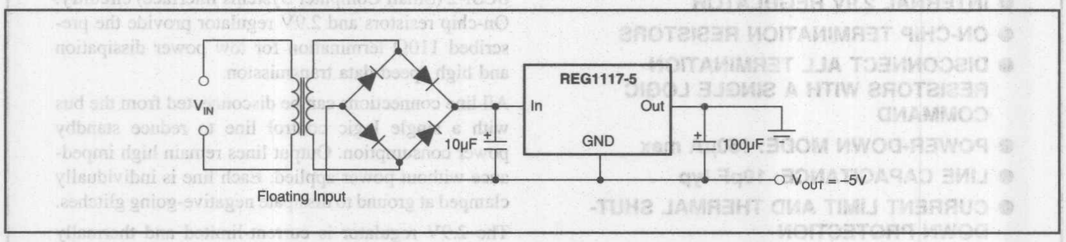


FIGURE 8. Low Dropout Negative Supply.

BURR - BROWN®

REG5601

18-LINE SCSI ACTIVE TERMINATOR

FEATURES

- COMPLIES WITH SCSI-2 SPECIFICATIONS
- INTERNAL 2.9V REGULATOR
- ON-CHIP TERMINATION RESISTORS
- DISCONNECT ALL TERMINATION RESISTORS WITH A SINGLE LOGIC COMMAND
- POWER-DOWN MODE: 150µA max
- LINE CAPACITANCE: 10pF typ
- CURRENT LIMIT AND THERMAL SHUT-DOWN PROTECTION
- 28-Lead SOIC and SSOP PACKAGES

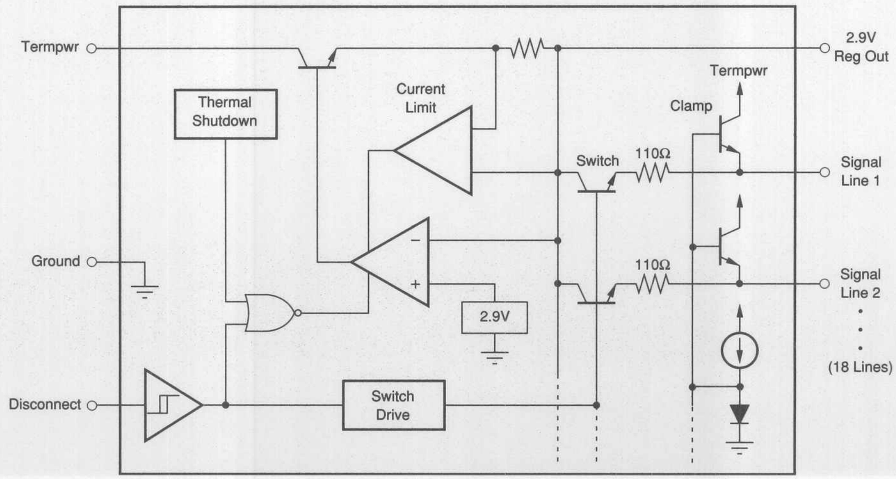
DESCRIPTION

The REG5601 is an 18-line active terminator for SCSI-2 (Small Computer Systems Interface) circuitry. On-chip resistors and 2.9V regulator provide the prescribed 110Ω termination for low power dissipation and high speed data transmission.

All line connections can be disconnected from the bus with a single logic control line to reduce standby power consumption. Output lines remain high impedance without power applied. Each line is individually clamped at ground to dissipate negative-going glitches.

The 2.9V regulator is current-limited and thermally protected. Regulated output is available for external circuitry.

The REG5601 is available in 28-lead SOIC and fine-pitch SSOP packages and is specified for operation over the 0°C to 70°C temperature range.



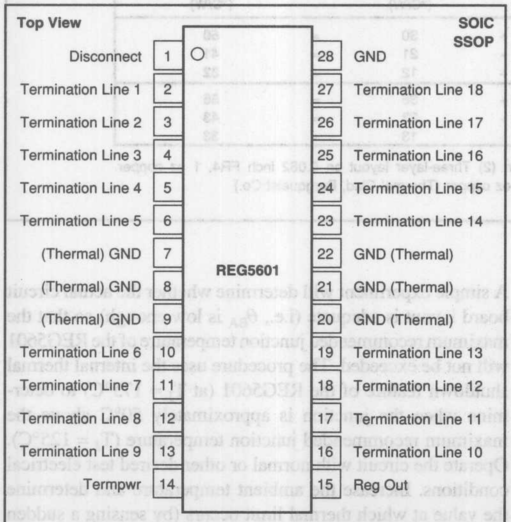
International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

T_A = 0°C to +70°C, Termpwr = 4.75V, and Disconnect = 0V unless otherwise specified.

		REG5601U			REG5601E			
PARAMETERS	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
POWER SUPPLY								
Termpwr Supply Voltage		4.0		5.25	4.0		5.25	V
Termpwr Supply Current	All Termination Lines = Open		14	25		14	25	mA
	All V_{TERM} = 0.5V		385	430		385	430	mA
Power-Down Mode	Disconnect = Open (High)		100	150		100	150	µA
TERMINATION LINES								
Termination Impedance	ΔI_{TERM} = 5mA to 15mA	107	110	115	107	110	115.5	Ω
Output High Voltage	Termpwr = 4V(1)	2.65	2.8		2.65	2.8		V
Maximum Output Current	V_{TERM} = 0.5V	20.5	21.7	22.4	19.8	21.7	22.4	mA
	Termpwr = 4V, V_{TERM} = 0.5V(1)	19.4	21	22.4	19	21	22.4	mA
Output Clamp Level	I_{TERM} = –30mA	–0.2	–0.05	0.1	–0.2	–0.05	0.1	V
Output Leakage	Disconnect = Open (High), Tempwr = 0V to 5.25V		20	400		20	400	nA
Output Capacitance	Disconnect = Open (High)		10			10		pF
REGULATOR								
Regulator Output Voltage		2.8	2.9	3.0	2.8	2.9	3.0	V
Line Regulation	Termpwr = 4V to 6V		6	20		6	20	mV
Load Regulation	I_{REG} = 0 to 400mA		20	50		20	50	mV
Drop-Out Voltage	All V_{TERM} = 0.5V, ΔV_{REG} = 100mV		1.0	1.2		1.0	1.2	V
Short-Circuit Current	V_{REG} = 0V	450	1350	1650	450	1350	1650	mA
Current Sink	V_{REG} = 3.5V	8	11		8	11		mA
Thermal Shutdown			170			170		°C
DISCONNECT LOGIC INPUT								
Disconnect Threshold		0.8	1.6	2.0	0.8	1.6	2.0	V
Threshold Hysterisis			200			200		mV
Input Current (Internal Pull-Up)	Disconnect = 0V		6	15		6	15	µA
TEMPERATURE RANGE								
Operating		0		70	0		70	°C
Storage		–40		150	–40		150	°C
θ_{JL} (junction to lead)			20			20		°C/W

NOTE: (1) Measurement of each termination line while the other 17 lines are held low (0.5V).

CONNECTION DIAGRAM



NOTE: Pin 28 is electrical ground. Connect pins 7, 8, 9, 20, 21, 22 to large circuit trace for proper heat sinking. Connect to ground or leave open-circuit.

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage .... +7V
Signal Line Voltage .... 0V to +7V
Regulator Output Current 1.65A
Power Dissipation 2.5W
Operating Junction Temperature .... –40°C to +150°C
Storage Temperature .... –40°C to +150°C

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
REG5601U	Plastic 28-Lead SOIC	217
REG5601E	Plastic 28-Lead SSOP	324

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

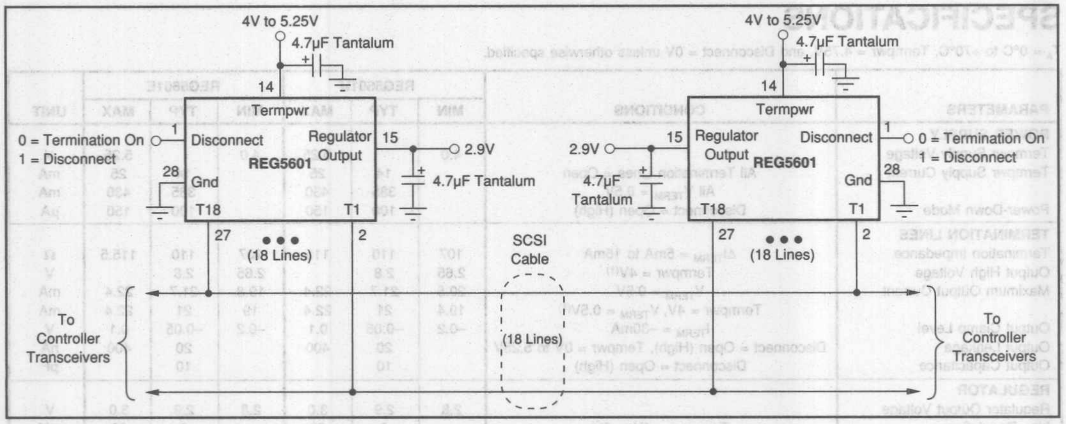
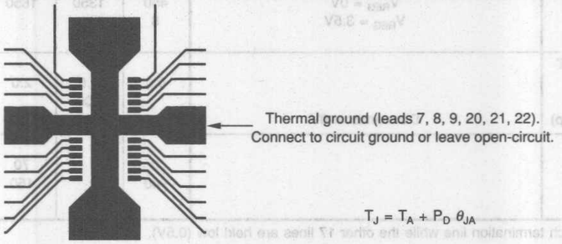


FIGURE 1. Standard SCSI Termination Application.



$$T_J = T_A + P_D\,\theta_{JA}$$

PACKAGE	CIRCUIT BOARD MATERIAL	θ_{JL} JUNCTION TO LEAD (°C/W)	+	θ_{BA} BOARD TO AMBIENT (°C/W)	=	θ_{JA} **JUNCTION TO AMBIENT (°C/W)**
SO-28	1-Layer(1)	20	+	30	=	**50**
	3-Layer(2)	20	+	21	=	**41**
	Aluminum(3)	20	+	12	=	**32**
SSOP-28	1-Layer(1)	20	+	36	=	**56**
	3-Layer(2)	20	+	23	=	**43**
	Aluminum(3)	20	+	13	=	**33**

NOTES: (1) Single-side layout on 0.062 inch FR4, 1 oz copper. (2) Three-layer layout on 0.062 inch FR4, 1 oz copper. (3) Aluminum 0.062 inch substrate, 0.003 insulation, one layer, 1 oz copper (Thermal Clad, Bergqueist Co.)

FIGURE 2. Circuit Board Layout.

The REG5601 has current limit and thermal shutdown that protect it from damage during output short-circuit or overload. The current limit is approximately 1350mA and thermal shutdown activates at a junction temperature of approximately 175°C. For good reliability, the junction temperature should not exceed 125°C. Any tendency to activate the thermal shutdown during normal operation is an indication of inadequate heat sinking and/or excessive power dissipation.

Heat is dissipated primarily by conduction through the leads to circuit board traces. It is important to connect the six thermal ground leads (7, 8, 9, 20, 21, 22) to a large circuit trace—see Figure 2. Measured values of thermal resistance for various circuit board materials are shown. These are approximate values. Variations in circuit board pattern, mounting techniques, air flow, proximity to other circuit boards and heat sources will affect thermal performance.

A simple experiment will determine whether the actual circuit board layout is adequate (i.e., θ_{BA} is low enough) so that the maximum recommended junction temperature of the REG5601 will not be exceeded. The procedure uses the internal thermal shutdown feature of the REG5601 (at $T_J \approx 175°C$) to determine when the junction is approximately 50°C above the maximum recommended junction temperature ($T_J = 125°C$). Operate the circuit with normal or other desired test electrical conditions. Increase the ambient temperature and determine the value at which thermal limit occurs (by sensing a sudden drop in V_{REG} output). At this point T_J is approximately 175°C. If this occurs at an ambient temperature of more than 50°C above the system ambient temperature design goal, the T_J will not exceed 125°C under the same electrical conditions when the ambient temperature is at the system design goal value.

BURR - BROWN®

REG5608

LOW CAPACITANCE 18-Line SCSI ACTIVE TERMINATOR

FEATURES

- ACTIVE 18-Line TERMINATOR
- 2pF CAPACITANCE PER LINE IMPORTANT FOR SCSI FAST-20
- ON-CHIP TERMINATION RESISTORS
- ALL TERMINATIONS DISCONNECT WITH SINGLE LOGIC SIGNAL
- 325mA CURRENT SINKING FOR ACTIVE NEGATION
- 22.4mA PER LINE DURING ASSERTION
- CURRENT LIMIT AND THERMAL LIMIT
- HOT-SOCKET CAPABLE
- 28-Lead SOIC and SSOP PACKAGES

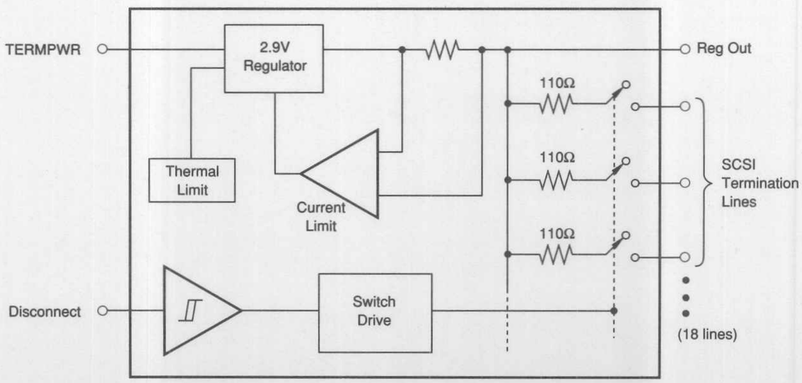
DESCRIPTION

The REG5608 is a low capacitance 18-line active terminator for SCSI (Small Computer Systems Interface) parallel bus systems. On-chip resistors and voltage regulator provide the prescribed SCSI bus termination. Low line capacitance (2pF) meets requirements for high data rate systems.

All terminations can be disconnected from the bus with a single logic control line. In the disconnect mode, output lines remain high impedance with or without power applied. This allows "hot socket" equipment plugging as required for "plug and play" applications.

The internal voltage regulator is temperature-compensated to assure proper termination characteristics over a wide operating range. Output current and thermal limit circuitry protect against damage.

The REG5608 is available in 28-lead SOIC and fine-pitch SSOP packages and is specified for 0°C to 70°C operation.

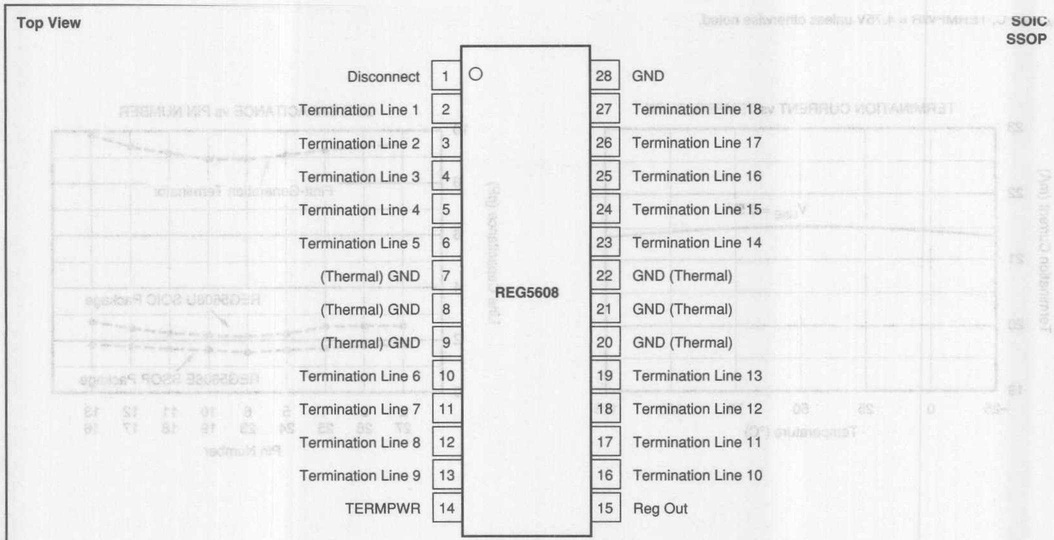


International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

At T_A = 0°C to +70°C, TERMPWR = 4.75V, and Disconnect = Low and $I_{REG\ OUT}$ = 0, unless otherwise specified.

PARAMETERS	CONDITIONS	REG5608U REG5608E MIN	TYP	MAX	UNITS
POWER SUPPLY					
TERMPWR Supply Voltage		4		5.25	V
TERMPWR Supply Current	All Termination Lines Open Circuit		18	25	mA
	All V_{LINE} = 0.5V		390	430	mA
	Disconnect = High		5		mA
TERMINATION LINES					
Termination Impedance	ΔI_{LINE} = 5 to 15mA	104.5	110	115.5	Ω
Output Termination High Voltage(1)	TERMPWR = 4.0V	2.65	2.9	3.0	V
Maximum Line Current	V_{LINE} = 0.5V				
	T_A = 0°C to 70°C	19.8	21.5	22.4	mA
	T_A = 25°C	20.3	21.5	22.4	mA
	TERMPWR = 4.0V, T_A=0°C to 70°C(1)	19.0	21.5	22.4	mA
	TERMPWR = 4.0V, T_A = 25°C(1)	19.5	21.5	22.4	mA
Line Leakage Current	Disconnect = High				
	TERMPWR = 5.25V, V_{LINE} = 0V		10	400	nA
	TERMPWR = 5.25V, V_{LINE} = 5.25V		10	400	nA
	TERMPWR = 0V, V_{LINE} = 5.25V		10	400	nA
Line Capacitance	Disconnect = High				
REG5608U SO-28 Package			2.5		pF
REG5608E SSOP-28			1.8		pF
REGULATOR					
Output Voltage		2.8	2.9	3.0	V
Line Regulation	TERMPWR = 4.0 to 6.0V		2	20	mV
Drop-Out Voltage	All V_{LINE} = 0.5V, ΔReg Out = 100mV		0.9	1.2	V
Source Current Limit	Reg Out = 0V	400	550	950	mA
Sink Current Limit	Reg Out = 3.5V	100	325	500	mA
Thermal Shutdown, T_J			145		°C
DISCONNECT LOGIC INPUT					
Input High Voltage	(Logic High = Switches Open)	2		TERMPWR	V
Input Low Voltage	(Logic Low = Switches Closed)	0		0.8	V
Input Low Current			10	20	µA
Threshold Hysteresis			50		mV
TEMPERATURE RANGE					
Specification		0	25	70	°C
Storage		-40		150	°C
θ_{JL} (Junction to Lead)			20		°C/W

NOTE: (1) Measurement of each termination line while the other 17 lines are held low (V_{LINE} = 0.5V).



NOTE: Pin 28 is electrical ground. Connect pins 7, 8, 9, 20, 21, 22 to large circuit trace for proper heat sinking. Connect to ground or leave open-circuit.

ABSOLUTE MAXIMUM RATINGS

TERMPWR Voltage	+7V
Signal Line Voltage	0V to +7V
Junction Temperature	+150°C
Storage Temperature	–40°C to +150°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

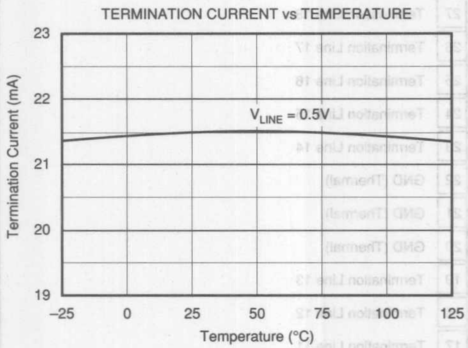
PACKAGE/ORDERING INFORMATION

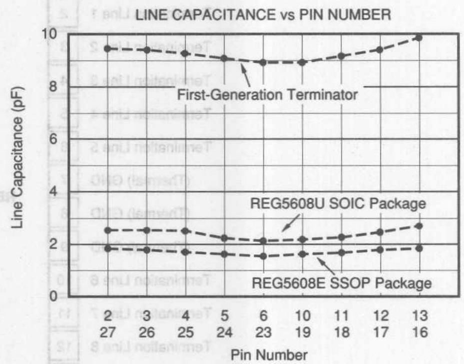
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
REG5608U	Plastic 28-Lead SOIC	217
REG5608E	Plastic 28-Lead SSOP	324

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

$T_A = 25°C$, TERMPWR = 4.75V unless otherwise noted.





APPLICATION INFORMATION

Figure 1 shows a typical SCSI parallel bus termination circuit. Bypass capacitors should be connected to TERMPWR and Reg Out pins as shown.

Line capacitance of the REG5608 has been reduced to less than one-fourth that of the first-generation integrated terminator ICs. Capacitance difference between package types and variation by pin number is shown in the typical performance curve, "Line Capacitance vs Pin Number." It shows that the SSOP package provides the lowest capacitance with typical values under 2pF. This variation is produced primarily by the differences in the interconnection length to the IC. Of course, actual line capacitance on a circuit board is generally determined by circuit board layout. To achieve lowest line capacitance, minimize the total circuit board interconnection length from the interface cable to the SCSI transceiver IC and to the REG5608 terminator.

THERMAL CONSIDERATIONS

The REG5608 has internal current limit and thermal shutdown that protect it from damage in case of output short-circuit or overload. The current limit is approximately 550mA and thermal shutdown activates at a junction temperature of approximately 145°C. For good long-term reliability, the junction temperature should not exceed 125°C. Any tendency to activate the thermal shutdown during normal operation is an indication of inadequate heat sinking and/or excessive power dissipation.

The terminator's internal power is dissipated primarily by conduction through the package leads to circuit board traces. It is important to connect the six thermal ground leads (7, 8, 9, 20, 21, 22) to a large circuit trace—see Figure 2. Typical measured values of thermal resistance for various circuit board materials are shown. These are approximate values. Variations in circuit board pattern, mounting techniques, air flow, proximity to other circuit boards and heat sources will affect thermal performance.

A simple experiment will determine whether the actual circuit board layout is adequate (i.e., θ_{BA} is low enough) so that the maximum recommended junction temperature of the REG5608 will not be exceeded. The procedure uses the internal thermal shutdown feature of the REG5608 (at $T_J \approx 145°C$) to determine when the junction is approximately 20°C above the maximum recommended junction temperature ($T_J = 125°C$). Operate the circuit with normal or other desired test electrical conditions. Increase the ambient temperature and determine the value at which thermal limit occurs (by sensing a sudden drop in V_{REG} output). At this point T_J is approximately 145°C. If this occurs at an ambient temperature of more than 20°C above the system ambient temperature design goal, the T_J will not exceed 125°C under the same electrical conditions when the ambient temperature is at the system design goal value.

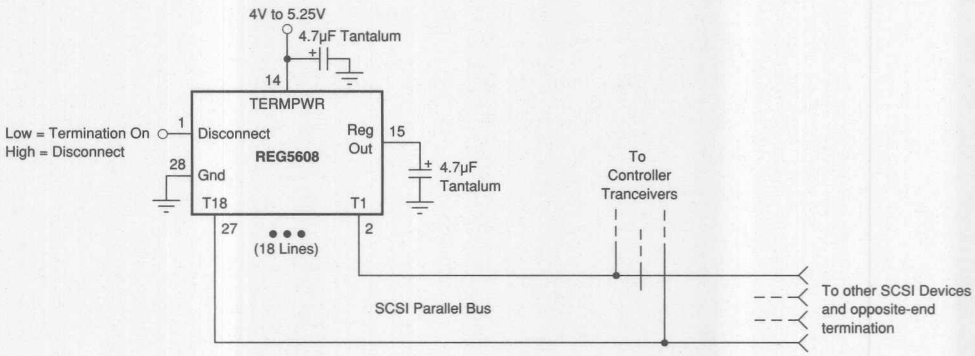
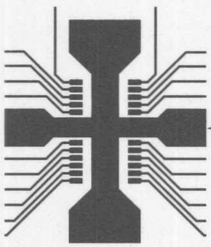


FIGURE 1. SCSI Parallel Bus Termination.



$$T_J = T_A + P_D\ \theta_{JA}$$

PACKAGE	CIRCUIT BOARD MATERIAL	θ_{JL} JUNCTION TO LEAD (°C/W)	+	θ_{BA} BOARD TO AMBIENT (°C/W)	=	θ_{JA} JUNCTION TO AMBIENT (°C/W)
SO-28	1-Layer(1)	20	+	30	=	**50**
	3-Layer(2)	20	+	21	=	**41**
	Aluminum(3)	20	+	12	=	**32**
SSOP-28	1-Layer(1)	20	+	36	=	**56**
	3-Layer(2)	20	+	23	=	**43**
	Aluminum(3)	20	+	13	=	**33**

NOTES: (1) Single-side layout on 0.062 inch FR4, 1 oz copper. (2) Three-layer layout on 0.062 inch FR4, 1 oz copper. (3) Aluminum 0.062 inch substrate, 0.003 insulation, one layer, 1 oz copper (Thermal Clad, Bergqueist Co.)

FIGURE 2. Circuit Board Layout.

Appendix A

Demonstration Boards

Burr-Brown offers a wide variety of demonstration boards for both its Linear and Mixed Signal Products. New boards for new products are continually being added to the selection—contact the factory your local salesperson for availability.

NOTE: All evaluation fixtures whose model number ends with a 'C' include the product or products mentioned. All others do not include the product, except where specifically noted.

MODEL	PRODUCT	DESCRIPTION
DEM-ACF2101BP-C	ACF2101BP	Evaluation Fixture with Programmable Timing Generator
DEM-ADS1210P-C	ADS1210P	Evaluation Fixture—24-bit single channel A/D converter; includes FFT Software and IBM PC Interface.
DEM-ADS1211P-C	ADS1211P	Evaluation Fixture—24-bit four channel A/D converter; includes FFT Software and IBM PC Interface.
DEM-ADS7804/05C	ADS7804/05	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7806/07C	ADS7806/07	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7808/09C	ADS7808/09	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7810/19C	ADS7810/19	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7833	ADS7833	Evaluation Fixture—12-bit data acquisition system; board includes LCD display, microcontroller and reconstruction DAC.
DEM-ADS800U	ADS800U	Evaluation Fixture—12-bit, 40MHz ADC, AC-and DC-coupled inputs, on-board clock, bus driver, SMA connectors.
DEM-ADS801U	ADS801U	Evaluation Fixture—12-bit, 25MHz ADC, AC- and DC-coupled inputs, on-board clock, bus driver, SMA connectors.
DEM-ADS802U	ADS802U	Evaluation Fixture—12-bit, 10MHz ADC, AC- and DC-coupled inputs, on-board clock, bus driver, SMA connectors.
DEM-ADS820U	ADS820U	Evaluation Fixture—10-bit, 20MHz ADC, AC- and DC-coupled inputs, on-board clock, bus driver, SMA connectors.
DEM-ADS821U	ADS821U	Evaluation Fixture—10-bit, 40MHz ADC, AC- and DC-coupled inputs, on-board clock, bus driver, SMA connectors.
DEM-BUF600-1GC	BUF600AP	Evaluation Fixture—900MHz Buffer Amplifier
DEM-BUF601-1GC	BUF601AP	Evaluation Fixture—650MHz Buffer Amplifier
DEM-DAC650J-E	DAC650JL	Evaluation Fixture—Digital Input and Analog Output (all SMA connectors). The part is included and soldered to the board.
DEM-DDC101P-C	DDC101P	Evaluation Fixture,— includes the DDC101 board, interface board to connect to parallel PC-port and software. Supports all DDC101 options plus FFT.
DEM-MPC100-1GC	MPC100AU	Evaluation Fixture—4 to 1 High Speed Multiplexer and Output Buffer BUF601AU.

MODEL	PRODUCT	DESCRIPTION
DEM-MPC102-1GC	MPC102AU	Evaluation Fixture—Dual 2 to 1 High Speed Multiplexer and optional output buffer, BUF601AU.
DEM-OPA465xP	OPA465xP	Evaluation Fixture—Unpopulated board for quad High Speed op amp OPA465x in DIP package.
DEM-OPA465xU	OPA465xU	Evaluation Fixture—Unpopulated board for quad High Speed op amp OPA465x in SOIC package.
DEM-OPA622-1GC	OPA622AP	Evaluation Fixture—For voltage and current feedback configuration.
DEM-OPA623-1GC	OPA623AP	Evaluation Fixture—High Speed current feedback Op Amp.
DEM-OPA628AP-C	OPA628AP	Evaluation Fixture—User selectable configuration for the DIP package.
DEM-OPA628AU-C	OPA628AU	Evaluation Fixture-User selectable configuration for the SOIC package.
DEM-OPA64XP-Y	OPA64XP	Evaluation Fixture—Three boards are offered for the DIP package of the OPA64X series of operational amplifiers. DEM-OPA64XP-F: follower configuration; DEM-OPA64XP-N: noninverting configuration; DEM-OPA64XP-I: inverting configuration. (Note: each board will operate with any OPA64XP series op amp. No component is included—it must be ordered separately.)
DEM-OPA64XU-Y	OPA64XU	Evaluation Fixture—Three boards are offered for the SOIC package of the OPA64X series of operational amplifiers. DEM-OPA64XU-F: follower configuration; DEM-OPA64XU-N: noninverting configuration; DEM-OPA64XU-N: noninverting configuration; DEM-OPA64XU-I: inverting configuration. (Note: each board will operate with any OPA64XU series op amp. No component is included—it must be ordered separately.)
DEM-OPA65XP	OPA65XP	Evaluation Fixture—One board for OPA65X single op amps for the DIP package.
DEM-OPA65XU	OPA65XU	Evaluation Fixture—One board for OPA65X single op amps for the SOIC package.
DEM-OPA265XP	OPA265XP	Evaluation Fixture—One board for OPA265X dual op amps for the DIP package.
DEM-OPA265XU	OPA265XU	Evaluation Fixture—One board for OPA265X dual op amps for the SOIC package.
DEM-OPA660-XXX	OPA660	Evaluation Fixture—Five boards are offered for five different configurations. DEM-OPA660-1GC: Diamond transistor and buffer; DEM-OPA660-2GC: Current-feedback operational amplifier; DEM-OPA660-3GC: Direct-feedback amplifier; DEM-OPA660-4G: Layouts for all applications using SOIC (unassembled); DEM-OPA660-5G: Layouts for all applications using DIP packages (unassembled)
DEM-OPA2662-1GC	OPA2662	Evaluation Fixture—High speed voltage controlled current source.

MODEL	PRODUCT	DESCRIPTION
DEM-PCM1700P-C	PCM1700	Evaluation Fixture—Serial/SPDIF Inputs (formerly DEM-1143). Includes product.
DEM-PCM1702	PCM1702	Evaluation Fixture—Serial digital input, 8X digital interpolator (NPC5842), and analog output. A PCM1702P is included. The board will interface directly to the DEM-1760. The fixture does not accept SPDIF input.
DEM-PCM1710	PCM1710U	Evaluation Fixture—Serial Digital Audio In. Left and Right channel analog out.
DEM-DAI1710	PCM1710U	Evaluation Fixture—Includes Digital Audio Interface (DAI) receiver chip and dual 2nd-order lowpass output filters.
DEM-PCM1712	PCM1712U	Evaluation Fixture—Low cost version of PCM1710.
DEM-PCM1715	PCM1715U	Evaluation Fixture—Serial digital audio in. Left and right channel analog out,
DEM-PCM1717	PCM1717	Evaluation Fixture—For the 16-/18-bit PCM1717
DEM-PCM1717-1	PCM1717	Evaluation Fixture—For the 16-/18-bit PMC1717; includes PC interface and control software.
DEM-DAI1717	PCM1717	Evaluation Fixture—For the 16-/18-bit PCM1717; includes Digital Audio Interface, PC interface and control software.
DEM-PCM1750P-C	PCM1750	Evaluation Fixture—Serial/Parallel Output, SPDF Out (Formerly DEM 1133). Includes product.
DEM-PCM1760	PCM1760/DF1760	Evaluation Fixture—Analog input and serial digital output. A PCM1760P and DF1760P are included. The board will interface directly to the DEM-1702. The fixture does not provide SPDIF output.
DEM-PCM63P-C	PCM63P	Evaluation Fixture—Includes Dual PCM63s, SPDIF Input
DEM-PCM67P-C	PCM67P	Evaluation Fixture—Includes Dual PCM67s (single/dual supply operation), SPDIF Input.
DEMPCM78P-C	PCM78P	Evaluation Fixture—Analog Input, Parallel Data Output. Includes SHC5320 sample hold and PCM56 as a reconstruction ADC (formerly DEM-1122).
DEM-SHC605AU	SHC605AU	Evaluation Fixture—Analog input, digital control input, and sample/hold output (all SMA connectors). A SHC605AU is included and is soldered to the board.
DEM-VCA610AP-C	VCA610AP	Evaluation Fixture—Voltage Controlled Amplifier.

Tape and Reel Information

The listed surface mount packages are available spooled on embossed carrier tape and reel, meeting EIA481-A requirements. Package numbers can be found in individual product data sheet. Package drawings can be found in Appendix C.

PACKAGE NUMBER[1]	DESCRIPTION	TAPE WIDTH, W (mm)	PITCH, P (mm)	DEVICES PER REEL	REEL DIAMETER (mm)
178		24	16	1000	360
182	SO-8	12	8	2500	360
211	SOL-16	16	12	1000	360
217	SO-28	24	12	1000	360
219	SOL-18	24	16	1000	360
221		24	12	1000	360
235	SO-14	16	8	2500	360
239	SO-24	24	12	1000	360
248		24	12	1000	360
311	SOT-23	12	8	2500	360
322	SSOP-16	12	8	2500	360
				250	178
324		24	12	1000	360
325		24	16	1000	360
328		24	16	1000	360
331	SOT23-5	8	4	10,000 3000 250	360 178 178
332	SOT23-6	8	4	3000 250	178 178
333			32	16	1000 360
334			32	16	1000 360
337	MSOP-8	12	8	2500 250	360 178

NOTE: (1) Package numbers can be found in individual product data sheet in the "Package Information" table. Package drawings are in Appendix C.

TABLE I.

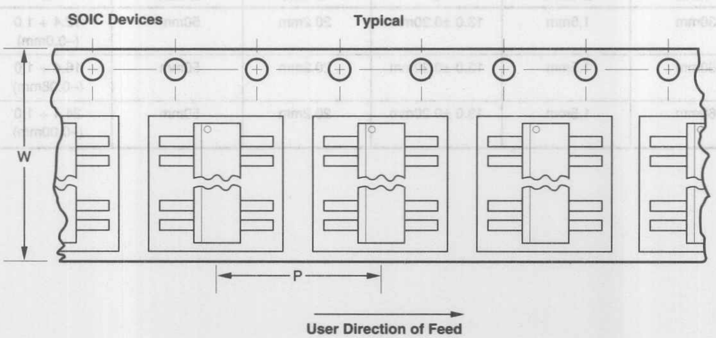


FIGURE 1.

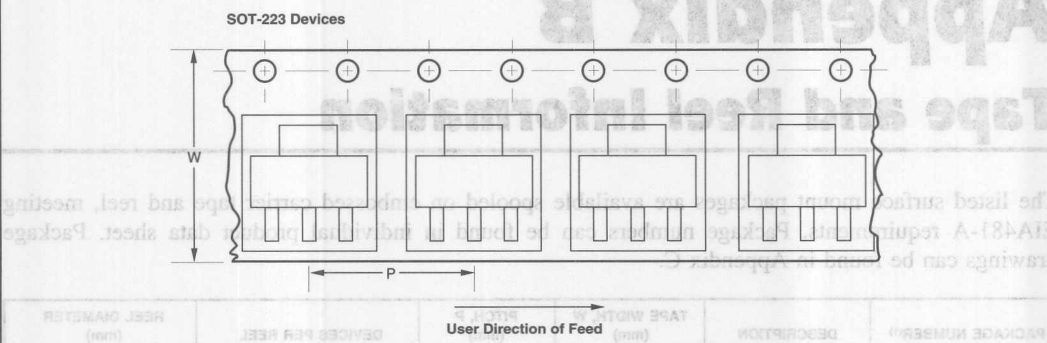
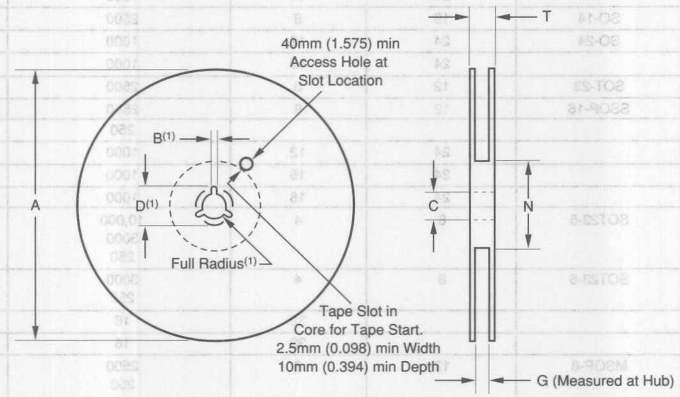


FIGURE 2.



NOTE: (1) Drive spokes optional. Noted dimensions apply if used.

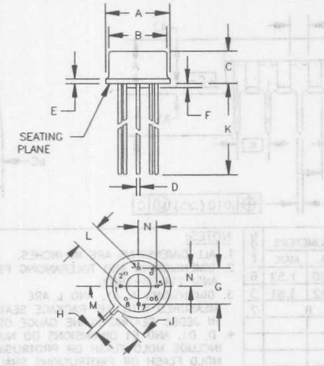
FIGURE 3.

TAPE SIZE	A MAX	B MAX	C	D MIN	N MIN	G	T MAX
12mm	330mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	12.4 + 1.0 (–0.0mm)	18.4mm
16mm	360mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	16.4 + 1.0 (–0.08mm)	22.4mm
24mm	360mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	24.4 + 1.0 (–0.00mm)	30.4mm

TABLE II.

Appendix C
Package Drawings (Mechanicals)

Package Number 001 - Metal TO-99



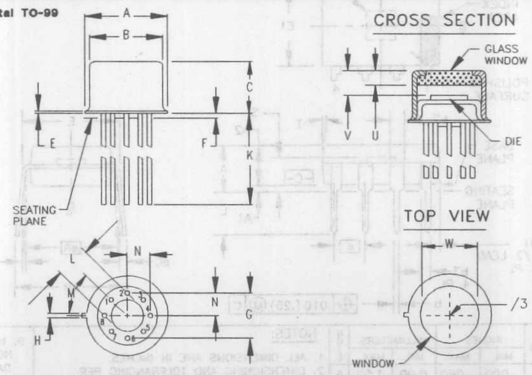
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.335	.380	8.51	9.65							
B	.305	.335	7.75	8.51							
C	.165	.185	4.19	4.70							
D	.016	.021	0.41	0.53							
E	.010	.040	0.25	1.02							
F	.010	.040	0.25	1.02							
G	.200 BASIC		5.08 BASIC								
H	.028	.034	0.71	0.86							
J	.029	.045	0.74	1.14							
K	.500	--	12.7	--							
L	.110	.160	2.79	4.06							
M	45° BASIC		45° BASIC								
N	.095	.105	2.41	2.67							

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER:	ZZ001	REV.:	B
JEDEC NUMBER:	UNKNOWN		

Package Number 001-1 - Metal TO-99

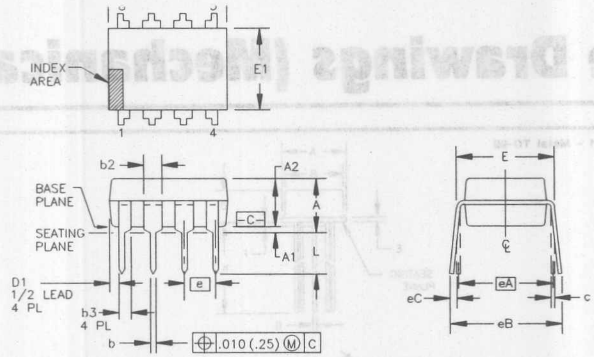


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.335	.370	8.51	9.40		V	.058	.077	1.47	1.96	
B	.305	.335	7.75	8.51		W	.246	.254	6.25	6.45	
C	.149	.165	3.79	4.19							
D	.016	.021	0.41	0.53							
E	.010	.040	0.25	1.02							
F	.010	.040	0.25	1.02							
G	.200 BASIC		5.08 BASIC								
H	.028	.034	0.71	0.86							
J	.029	.045	0.74	1.14							
K	.500	--	12.70	--							
L	.110	.160	2.79	4.06							
M	45° BASIC		45° BASIC								
N	.095	.105	2.41	2.67							
U	.040	.050	1.02	1.27							

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. DIE MAY BE ROTATED WITH RESPECT TO INDICATED AXIS.

PACKAGE NUMBER:	ZZ001-1	REV.:	C
JEDEC NUMBER:	UNKNOWN		



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6

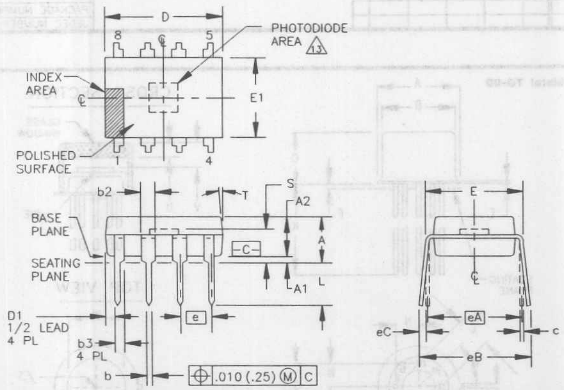
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	8		8		7

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER:	ZZ006	REV.:	E
JEDEC NUMBER:	MS-001-BA		

Package Number 006-1 - 8-Pin Transparent Plastic Single-Wide DIP



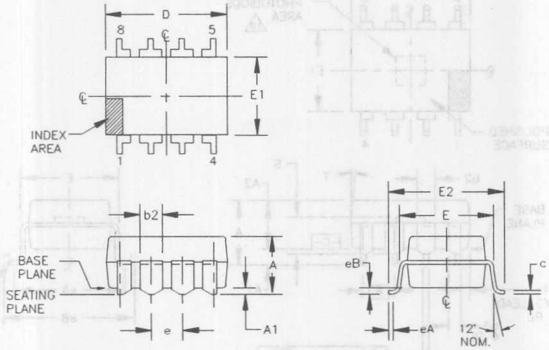
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.165	--	4.19	3
A1	.015	--	0.38	--	3
A2	.120	.135	3.05	3.43	
b	.014	.022	0.36	0.56	
b2	.040	.050	1.02	1.27	9
b3	.030	.045	0.762	1.143	9
c	.008	.015	0.20	0.38	
D	.360	.390	9.14	9.91	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.238	.275	6.05	6.99	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6

DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
eC	.000	.060	0.00	1.52	6
L	.115	.160	2.92	4.06	3
N	8		8		7
S	.100	.120	2.54	3.05	
T	5.5°	8.5°	5.5°	8.5°	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
13. CENTER OF PHOTODIODE MUST BE WITHIN .010 (0.25mm) OF CENTER OF PHOTODIODE AREA.

PACKAGE NUMBER:	ZZ006-1	REV.:	D
JEDEC NUMBER:	NONE		



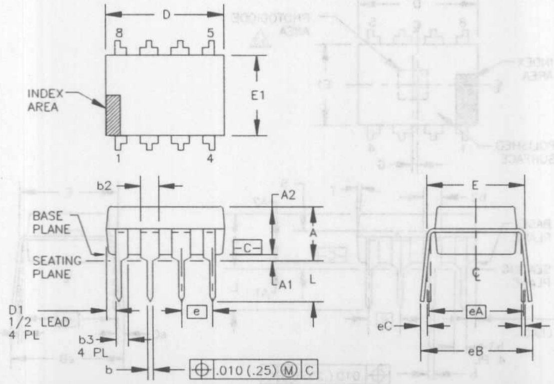
DIM	INCHES		MILLIMETERS		NOTE	DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	--	.185	--	4.70							
A1	.020	--	0.51	--							
b2	--	.070	--	1.78							
c	.007	.013	0.18	0.33							
D	.370	.390	9.40	9.91	3						
E	.290	.310	7.37	7.87							
E1	.240	.260	6.10	6.60	3						
E2	.370	.390	9.40	9.91							
e	.090	.110	2.29	2.79							
eA	.015	.035	0.38	0.89							
eB	.015	.025	0.38	0.64							
N	8		8		4						

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
4. N IS THE MAXIMUM OF TERMINAL POSITIONS.
5. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
7. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006-2 REV.: C
JEDEC NUMBER: NONE

Package Number 006-3 - 8-Pin Plastic, Single-Wide DIP



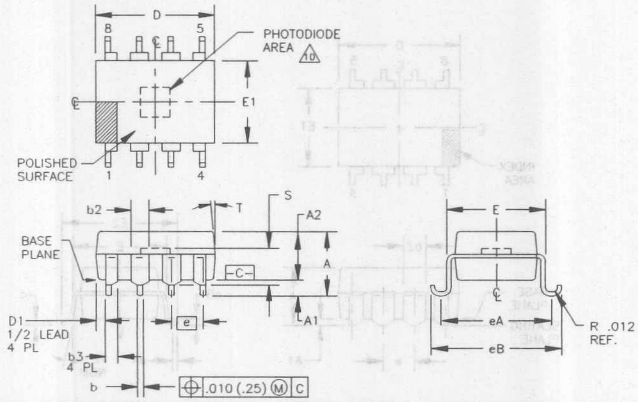
DIM	INCHES		MILLIMETERS		NOTE	DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3	eC	.000	.060	0.00	1.52	6
A1	.015	--	0.38	--	3	L	.115	.150	2.92	3.81	3
A2	.115	.195	2.92	4.95		N	8		8		7
b	.014	.025	0.36	.635							
b2	.045	.070	1.14	1.78	9						
b3	.030	.045	0.76	1.14	9						
c	.008	.014	0.20	0.36							
D	.355	.400	9.02	10.16	4						
D1	.005	--	0.13	--	4						
E	.300	.325	7.62	8.26	5						
E1	.240	.280	6.10	7.11	4						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.63 BASIC		5						
eB	--	.430	--	10.92	6						

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006-3 REV.: C
JEDEC NUMBER: MS-001-BA WITH THE EXCEPTION OF DIM. b

Package Number 006-4 - Transparent J-Formed 8-Lead Surface-Mount DIP



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.255	--	6.48	
A1	.040	.060	1.02	1.52	
A2	.120	.135	3.05	3.43	
b	.014	.022	0.36	0.56	
b2	.040	.050	1.02	1.27	6
b3	.030	.045	0.76	1.14	6
D	.360	.390	9.14	9.91	3
D1	.005	--	0.13	--	3
E	.300	.325	7.62	8.26	4
E1	.238	.275	6.05	6.99	3
e	.100 BASIC		2.54 BASIC		
eA	.350	.370	8.89	9.40	4
eB	--	.415	--	10.54	
N	8		8		5

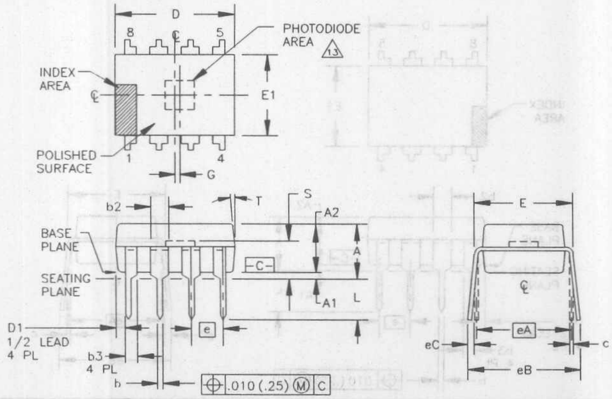
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
S	.100	.120	2.54	3.05	
T	5.5°	8.5°	5.5°	8.5°	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
5. N IS THE MAXIMUM OF TERMINAL POSITIONS.
6. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
7. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
10. CENTER OF PHOTODIODE MUST BE WITHIN .010 (0.25mm) OF CENTER OF PHOTODIODE AREA.

PACKAGE NUMBER:	ZZ006-4	REV.:	C
JEDEC NUMBER:	NONE		

Package Number 006-5 - 8-Pin Transparent Plastic Single-Wide DIP



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.165	--	4.19	3
A1	.015	--	0.38	--	3
A2	.120	.135	3.05	3.43	
b	.014	.022	0.36	0.56	
b2	.040	.050	1.02	1.27	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.360	.390	9.14	9.91	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.238	.275	6.05	6.99	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6

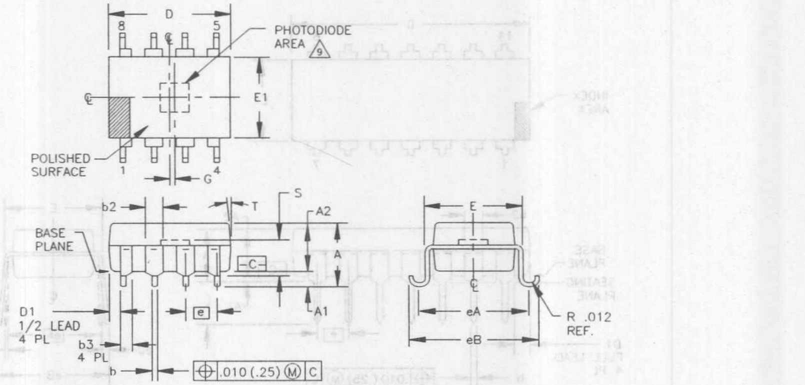
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
eC	.000	.060	0.00	1.52	6
G	.011	.021	0.28	0.53	
L	.115	.150	2.92	3.81	3
N	8		8		7
S	.100	.120	2.54	3.05	
T	5.5°	8.5°	5.5°	8.5°	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
13. CENTER OF PHOTODIODE MUST BE WITHIN .010 (0.25mm) OF CENTER OF PHOTODIODE AREA.

PACKAGE NUMBER:	ZZ006-5	REV.:	B
JEDEC NUMBER:	NONE		

Package Number 006-6 - Transparent J-Formed 8-Lead Surface-Mount DIP



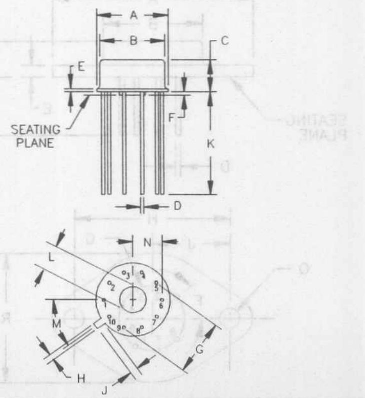
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.255	--	6.48		N	8		8		4
A1	.040	.060	1.02	1.52		S	.100	.120	2.54	3.05	
A2	.120	.135	3.05	3.43		T	5.5°	8.5°	5.5°	8.5°	
b	.014	.022	0.36	0.56							
b2	.040	.050	1.02	1.27	5						
b3	.030	.045	0.76	1.14	5						
D	.360	.390	9.14	9.91	3						
D1	.005	--	0.13	--	3						
E	.300	.325	7.62	8.26							
E1	.238	.275	6.05	6.99	3						
e	.100 BASIC		2.54 BASIC								
eA	.350	.370	8.89	9.40							
eB	--	.415	--	10.54							
G	.011	.021	0.28	0.53							

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
3. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
4. N IS THE MAXIMUM OF TERMINAL POSITIONS.
5. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
6. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
7. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. CENTER OF PHOTODIODE MUST BE WITHIN .010 (0.25mm) OF CENTER OF PHOTODIODE AREA.

PACKAGE NUMBER: ZZ006-6 REV.: B
JEDEC NUMBER: NONE

Package Number 007 - TO-100 Package

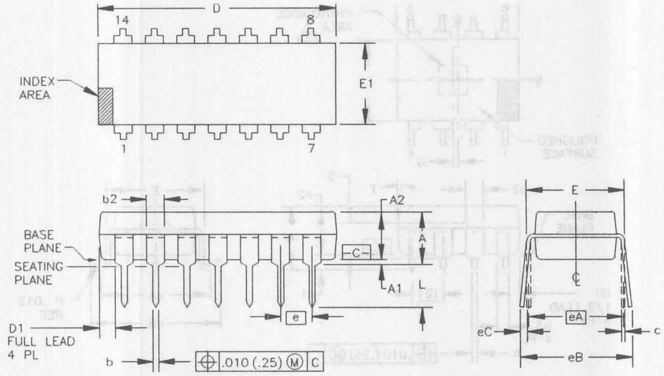


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.335	.370	8.51	9.40							
B	.305	.335	7.75	8.51							
C	.165	.185	4.19	4.70							
D	.016	.021	0.41	0.53							
E	.010	.040	0.25	1.02							
F	.010	.040	0.25	1.02							
G	.230 BASIC		5.84 BASIC								
H	.028	.034	0.71	0.86							
J	.029	.045	0.74	1.14							
K	.500	--	12.70	--							
L	.120	.160	3.05	4.06							
M	36° BASIC		36° BASIC								
N	.110	.120	2.79	3.05							

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ007 REV.: A
JEDEC NUMBER: UNKNOWN



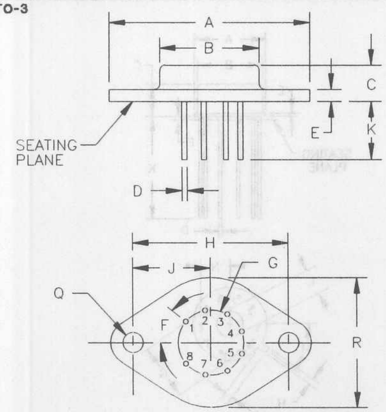
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3	L	.115	.150	2.92	3.81	3
A1	.015	--	0.38	--	3	N	14		14		7
A2	.115	.195	2.92	4.95							
b	.014	.022	0.36	0.56							
b2	.045	.070	1.14	1.78	9						
c	.008	.014	0.20	0.36							
D	.735	.775	18.67	19.69	4						
D1	.005	--	0.13	--	4						
E	.300	.325	7.62	8.26	5						
E1	.240	.280	6.10	7.11	4						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.63 BASIC		5						
eB	--	.430	--	10.92	6						
eC	.000	.060	0.00	1.52	6						

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER:	ZZ010	REV.:	G
JEDEC NUMBER:	MS-001-AA		

Package Number 030 - 8-Pin Metal TO-3



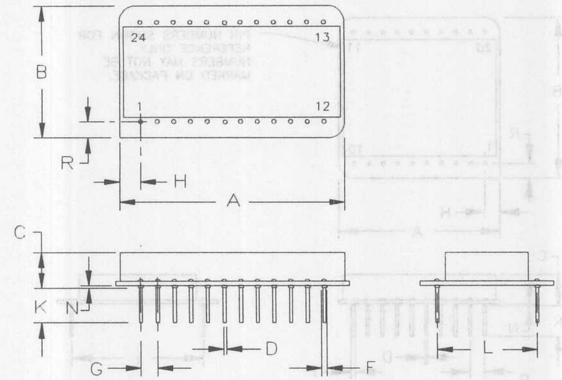
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	1.510	1.550	38.35	39.37							
B	.745	.770	18.92	19.56							
C	.260	.300	6.60	7.62							
D	.038	.042	0.97	1.07							
E	.080	.105	2.03	2.67							
F	40° BASIC		40° BASIC								
G	.500 BASIC		12.70 BASIC								
H	1.182	1.192	30.02	30.28							
J	.591	.596	15.01	15.14							
K	.400	.500	10.16	12.70							
Q	.151	.161	3.84	4.09							
R	.980	1.020	24.89	25.91							

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER:	ZZ030	REV.:	C
JEDEC NUMBER:	UNKNOWN		

Package Number 075 - 24-Pin



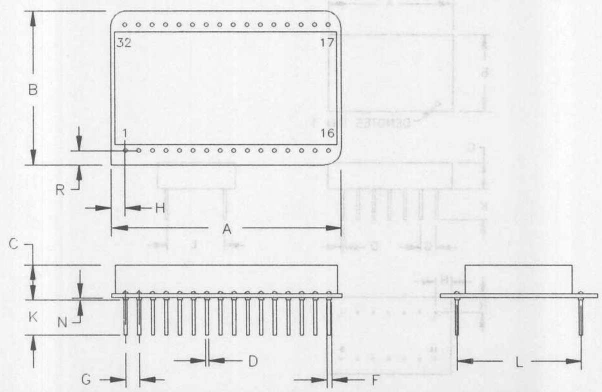
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	1.310	1.360	33.27	34.54	
B	.770	.810	19.56	20.57	
C	.150	.210	3.81	5.33	
D	.018	.021	0.46	0.53	
F	.035	.050	0.89	1.27	
G	.100	BASIC	2.54	BASIC	
H	.110	.130	2.79	3.30	
K	.150	.250	3.81	6.35	
L	.600	BASIC	15.24	BASIC	
N	.002	.010	0.05	0.25	
R	.085	.105	2.16	2.67	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER:	ZZ075	REV.:	A
JEDEC NUMBER:	NONE		

Package Number 077 - 32-Pin Omnipak



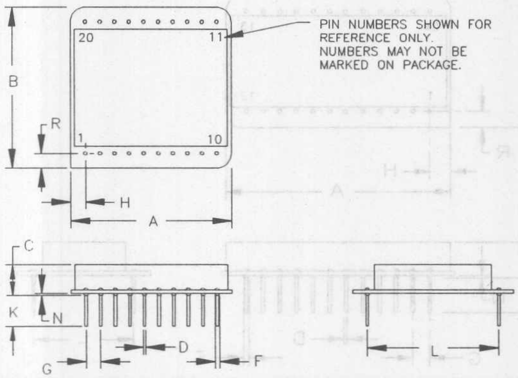
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	1.700	1.760	43.18	44.70	
B	1.120	1.160	28.45	29.46	
C	170	.230	4.32	5.84	
D	.018	.021	0.46	0.53	
F	.035	.050	0.89	1.27	
G	.100	BASIC	2.54	BASIC	
H	.110	.130	2.79	3.30	
K	.160	.180	4.06	4.57	
L	.900	BASIC	22.86	BASIC	
N	.002	.010	0.05	0.25	
R	.110	130	2.79	3.30	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER:	ZZ077	REV.:	B
JEDEC NUMBER:	NONE		

Package Number 102 - 20-Lead ISO Omni



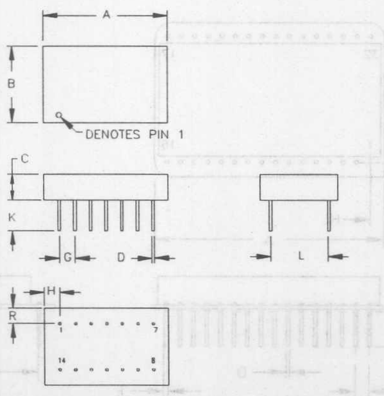
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	1.080	1.120	27.43	28.45							
B	1.080	1.120	27.43	28.45							
C	.235	.285	5.97	7.24							
D	.018	.021	0.46	0.53							
F	.035	.050	0.89	1.27							
G	.100	BASIC	2.54	BASIC							
H	.100	BASIC	2.54	BASIC							
K	.150	.350	3.81	8.89							
L	.900	BASIC	22.86	BASIC							
N	.002	.010	0.05	0.25							
R	.100	BASIC	2.54	BASIC							

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.

PACKAGE NUMBER:	ZZ102	REV.:	A
JEDEC NUMBER:	NONE		

Package Number 105 - 14-Pin DIP



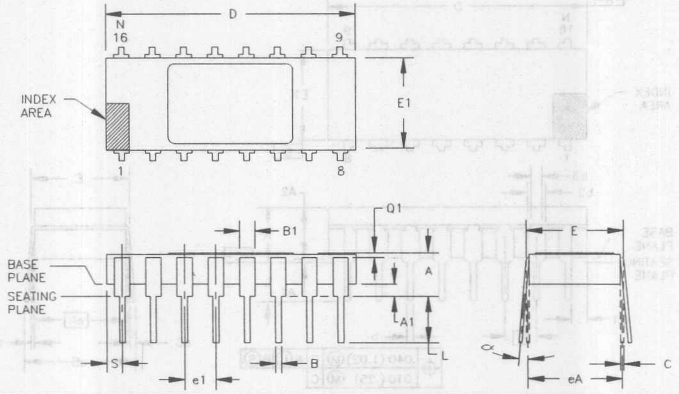
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.790	.810	20.07	20.57							
B	.490	.510	12.45	12.95							
C	.190	.260	4.83	6.60							
D	.018	.021	0.46	0.53							
G	.100	BASIC	2.54	BASIC							
H	.080	.115	2.03	2.92							
K	.130	.300	3.30	7.62							
L	.300	BASIC	7.62	BASIC							
R	.080	.115	2.03	2.92							

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS ARE NOT MARKED ON PACKAGE.

PACKAGE NUMBER:	ZZ105	REV.:	A
JEDEC NUMBER:	NONE		

Package Number 109 - 16-Lead, Ceramic Side Braze DIP, .300 Wide



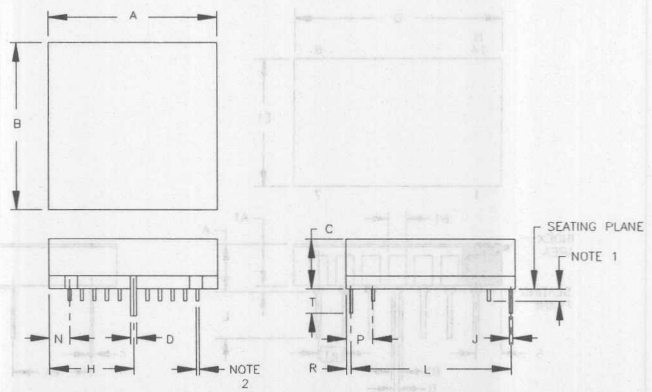
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.105	.175	2.67	4.45		α	0°	15°	0°	15°	3
A1	.025	.055	0.64	1.40							
B	.015	.021	0.38	0.53	5						
B1	.038	.060	0.97	1.52	5						
C	.008	.012	0.20	0.30							
D	.770	.830	19.56	21.08							
E	.290	.325	7.37	8.26							
E1	.280	.310	7.11	7.87	6						
e1	.100 TYP.		2.54 TYP.		2						
eA	.300 TYP.		7.62 TYP.		2						
L	.125	.175	3.18	4.45							
N	16		16		4						
Q1	.010	--	0.25	--							
S	.020	.065	0.51	1.65							

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ109 REV.: D
JEDEC NUMBER: MO-36-AD

Package Number 124 - EMI Shield



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	1.320	1.380	33.53	35.05	
B	1.320	1.380	33.53	35.05	
C	.350	.450	8.89	11.43	
D	.040	.060	1.02	1.52	
H	.600	.700	15.24	17.78	
J	.015	.025	0.38	0.64	
L	1.180	1.280	29.97	32.51	
N	.150	.250	3.81	6.35	
P	.150	.250	3.81	6.35	
R	.015	.055	0.38	1.40	
T	.130	.230	3.30	5.84	

NOTES:

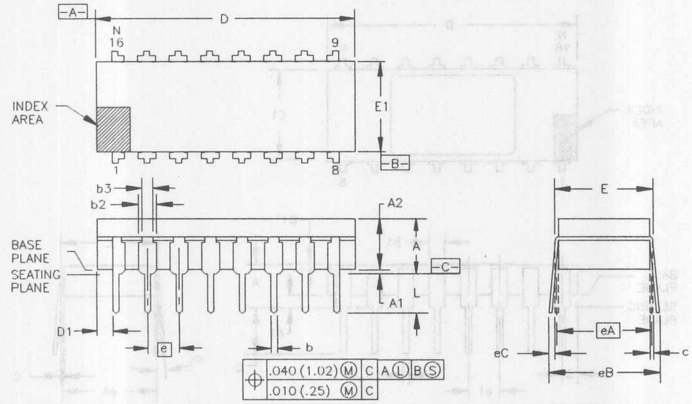
1. ENCLOSED MODULE LEAD LENGTH MINUS .050" TO .100" (1.27mm TO 2.54mm).
2. PIN DIAMETER DETERMINED BY ENCLOSED MODULE.

PACKAGE NUMBER: ZZ124 REV.: A
JEDEC NUMBER: NONE

PACKAGE DRAWINGS (Mechanicals)

C

Package Number 129 - 16-Lead CERDIP, .300 Wide



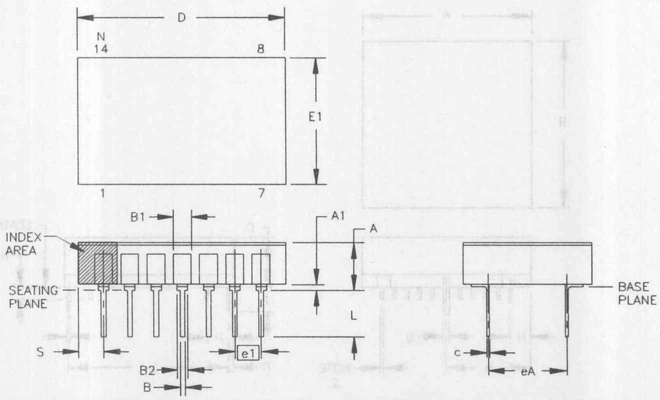
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.230	--	5.84		eC	.000	--	0.00	--	5
A1	.015	--	0.38	--		L	.100	--	2.54	--	
A2	.140	.180	3.56	4.57		N	16		16		6
b	.015	.023	0.38	0.58	9						
b2	.045	.070	1.14	1.78							
b3	.035 TYP		0.89 TYP								
c	.008	.015	0.20	0.38	9						
D	.753	.885	19.13	22.48	3						
D1	.005	--	0.13	--							
E	.300	.325	7.62	8.25	4						
E1	.280	.295	7.11	7.50	3						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.62 BASIC		4						
eB	--	.450	--	11.43	5						

NOTES:

1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE C.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
10. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER:	ZZ129	REV.:	D
JEDEC NUMBER:	NONE		

Package Number 148 - 14-Lead Bottom Braze DIP, .300 Wide



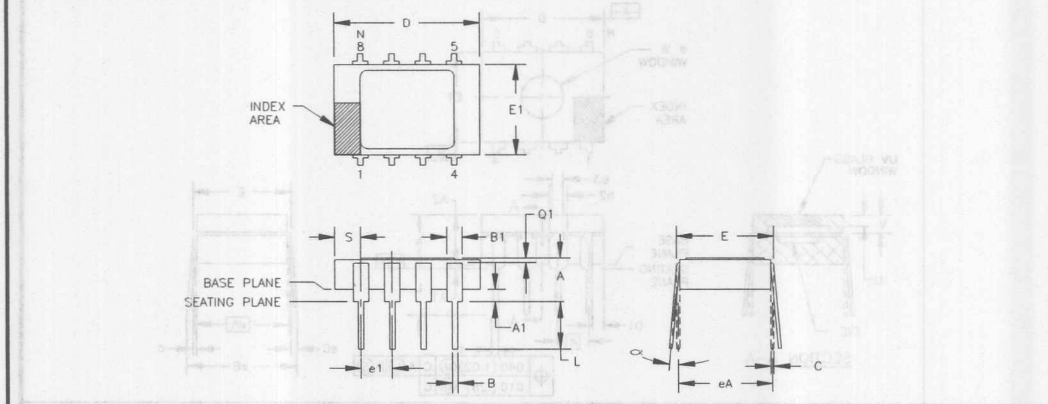
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.155	.215	3.94	5.46							
A1	.015	.035	0.38	0.89							
B	.016	.020	0.41	0.51							
B1	.045	.055	1.14	1.40							
B2	.035	.045	0.89	1.14							
c	.009	.012	0.23	0.30							
D	.770	.810	19.56	20.57							
E1	.480	.500	12.19	12.70							
e1	.100 BASIC		2.54 BASIC								
eA	.290	.310	7.37	7.87							
L	.150	.210	3.81	5.33							
N	14		14								
S	.080	.110	2.03	2.79							

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER:	ZZ148	REV.:	A
JEDEC NUMBER:	NONE		

Package Number 157 - 8-Lead, Ceramic Side Braze DIP, .300 Wide



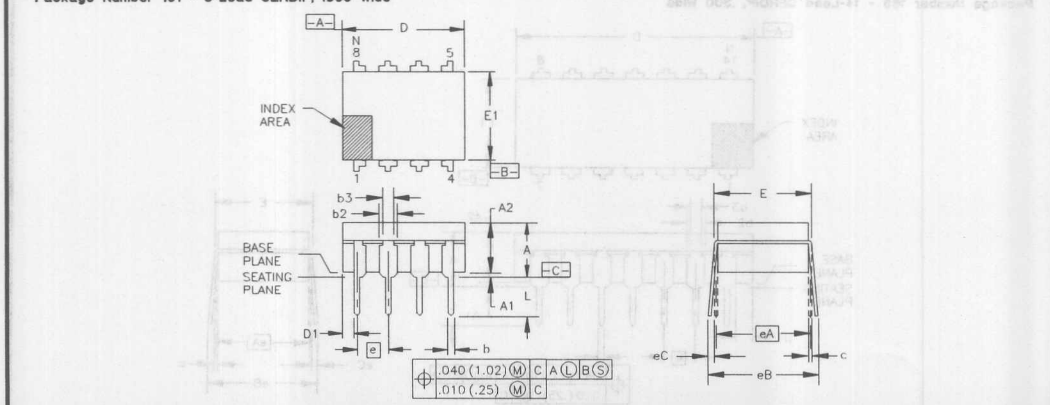
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.105	.175	2.67	4.45		∝	0°	15°	0°	15°	3
A1	.025	.055	0.64	1.40							
B	.015	.021	0.38	0.53	5						
B1	.038	.060	0.97	1.52	5						
C	.008	.012	0.20	0.30							
D	.380	.550	9.65	13.97							
E	.290	.325	7.37	8.26							
E1	.280	.310	7.11	7.87	6						
e1	.100 TYP.		2.54 TYP.		2						
eA	.300 TYP.		7.62 TYP.		2						
L	.125	.175	3.18	4.45							
N	8		8		4						
Q1	.010	--	2.54	--							
S	.030	.120	0.76	3.05							

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ157	REV.: C
JEDEC NUMBER: MO-36-AA	

Package Number 161 - 8-Lead CERDIP, .300 Wide



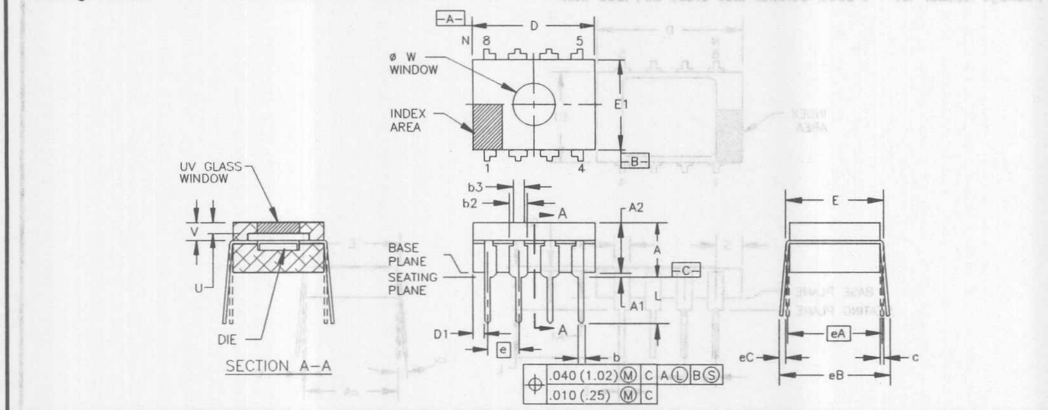
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.230	--	5.84		eC	.000	--	0.00	--	5
A1	.015	--	0.38	--		L	.100	--	2.54	--	
A2	.140	.180	3.56	4.57		N	8		8		6
b	.015	.023	0.38	0.58	9						
b2	.045	.070	1.14	1.78							
b3	.035 TYP		0.89 TYP								
c	.008	.015	0.20	0.38	9						
D	.375	.405	9.53	10.28	3						
D1	.005	--	0.13	--							
E	.300	.325	7.62	8.25	4						
E1	.280	.295	7.11	7.50	3						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.62 BASIC		4						
eB	--	.450	--	11.43	5						

NOTES:

1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE C.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
10. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ161	REV.: C
JEDEC NUMBER: NONE	

Package Number 161-1 - 8-Lead CERDIP With Window, .300 Wide



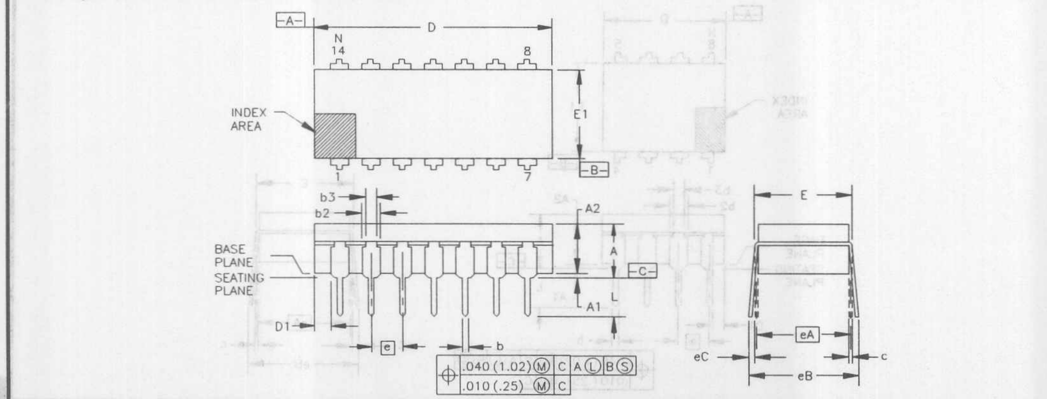
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.230	--	5.84		eC	.000	--	0.00	--	5
A1	.015	--	0.38	--		L	.100	--	2.54	--	
A2	.140	.180	3.56	4.57		N	8		8		6
b	.015	.023	0.38	0.58	9	U	.032	.038	0.81	0.97	
b2	.045	.070	1.14	1.78		V	.058	.064	1.47	1.63	
b3	.035 TYP		0.89 TYP			W	.131	.139	3.33	3.53	
c	.008	.015	0.20	0.38	9						
D	.395	.425	10.03	10.80	3						
D1	.005	--	0.13	--							
E	.300	.325	7.62	8.25	4						
E1	.280	.295	7.11	7.50	3						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.62 BASIC		4						
eB	--	.450	--	11.43	5						

NOTES:

1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE C.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
10. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ161-1	REV.: C
JEDEC NUMBER: NONE	

Package Number 163 - 14-Lead CERDIP, .300 Wide



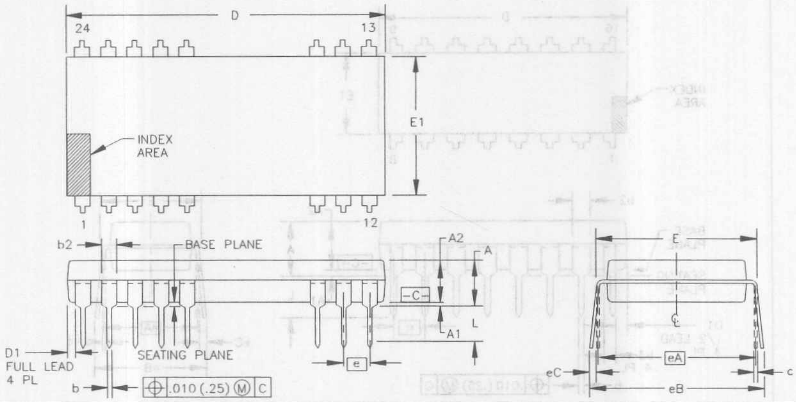
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.230	--	5.84		eC	.000	--	0.00	--	5
A1	.015	--	0.38	--		L	.100	--	2.54	--	
A2	.140	.180	3.56	4.57		N	14		14		6
b	.015	.023	0.38	0.58	9						
b2	.045	.070	1.14	1.78							
b3	.035 TYP		0.89 TYP								
c	.008	.015	0.20	0.38	9						
D	.753	.767	19.13	19.48	3						
D1	.005	--	0.13	--							
E	.300	.325	7.62	8.26	4						
E1	.280	.295	7.11	7.50	3						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.62 BASIC		4						
eB	--	.450	--	11.43	5						

NOTES:

1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE C.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
10. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ163	REV.: C
JEDEC NUMBER: NONE	

Package Number 167-1 - 24-Pin Plastic Double-Wide DIP



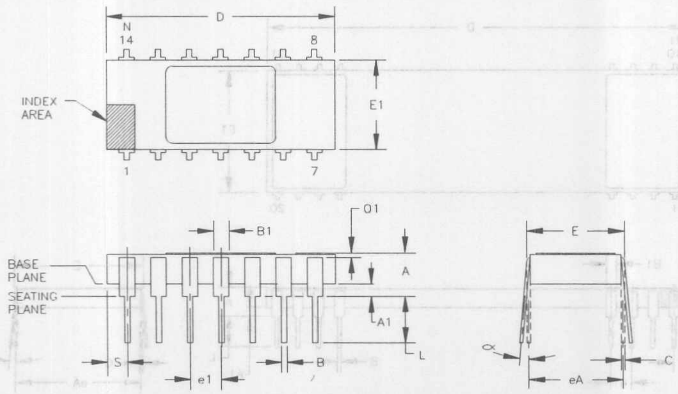
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.250	--	6.35	3	L	.115	.200	2.92	5.08	3
A1	.015	--	0.38	--	3	N	16		16		7
A2	.125	.195	3.18	4.95							
b	.014	.022	0.36	0.56							
b2	.030	.070	0.76	1.78	9						
c	.008	.015	0.20	0.38							
D	1.150	1.290	29.21	32.77	4						
D1	.005	--	0.13	--	4						
E	.600	.625	15.24	15.88	5						
E1	.485	.580	12.32	14.73	4						
e	.100 BASIC		2.54 BASIC								
eA	.600 BASIC		15.26 BASIC		5						
eB	--	.700	--	17.78	6						
eC	.000	.060	0.00	1.52	6						

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ167-1 REV.: B
JEDEC NUMBER: MS-011-AA WITH THE EXCEPTION OF "N".

Package Number 169 - 14-Lead, Ceramic Side Braze DIP, .300 Wide



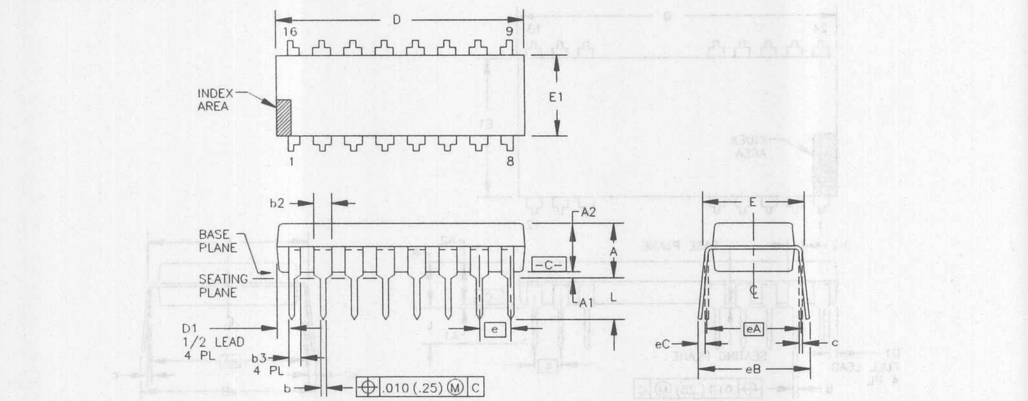
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.105	.175	2.67	4.45		α	0°	15°	0°	15°	3
A1	.025	.055	0.64	1.40							
B	.015	.021	0.38	0.53	5						
B1	.038	.060	0.97	1.52	5						
C	.008	.012	0.20	0.30							
D	.690	.770	17.53	19.56							
E	.290	.325	7.37	8.26							
E1	.280	.310	7.11	7.87	6						
e1	.100 TYP.		2.54 TYP.		2						
eA	.300 TYP.		7.62 TYP.		2						
L	.125	.175	3.18	4.45							
N	14		14		4						
Q1	.010	--	0.25	--							
S	.030	.095	0.76	2.41							

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ169 REV.: F
JEDEC NUMBER: MO-36-AB

Package Number 180 - 16-Pin Plastic, Single-Wide DIP



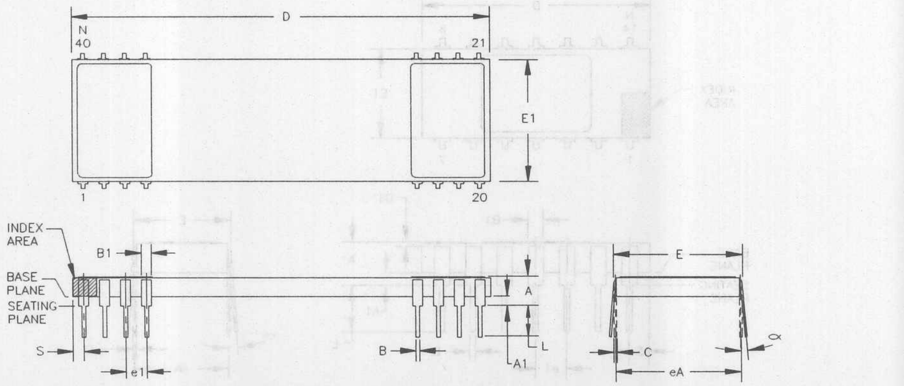
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3	eC	.000	.060	0.00	1.52	6
A1	.015	--	0.38	--	3	L	.115	.150	2.92	3.81	3
A2	.115	.195	2.92	4.95		N	16		16		7
b	.014	.022	0.36	0.56							
b2	.045	.070	1.14	1.78	9						
b3	.030	.045	0.76	1.14	9						
c	.008	.014	0.20	0.36							
D	.735	.775	18.67	21.34	4						
D1	.005	--	0.13	--	4						
E	.300	.325	7.62	8.26	5						
E1	.240	.280	6.10	7.11	4						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.63 BASIC		5						
eB	--	.430	--	10.92	6						

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ180	REV.: F
JEDEC NUMBER: MS-001-BB	

Package Number 206 - 40-Lead Side Braze DIP, .600 Wide, ISO Package



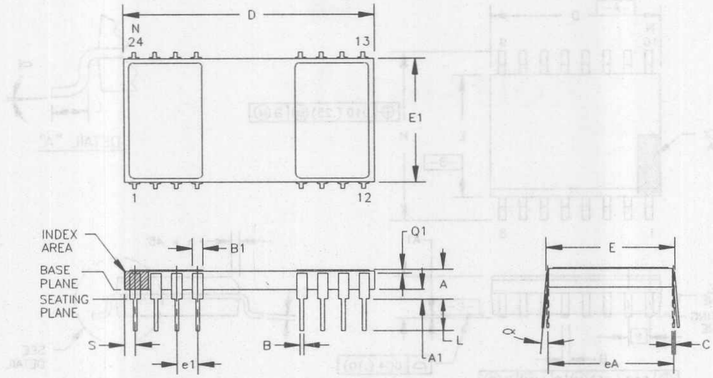
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.085	.190	2.16	4.83							
A1	.020	.070	0.51	1.78							
B	.015	.023	0.38	0.58	5						
B1	.038	.060	0.97	1.52	5						
C	.008	.012	0.20	0.30							
D	1.980	2.030	50.29	51.56							
E	.595	.625	15.11	15.88							
E1	.580	.610	14.73	15.49	6						
e1	.100 TYP.		2.54 TYP.		2						
eA	.600 TYP.		15.24 TYP.		2						
L	.125	.175	3.18	4.45							
N	16		16		4						
S	.030	.065	0.76	1.65							
∝	0°	15°	0°	15°	3						

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ206	REV.: C
JEDEC NUMBER: MO-038-AC WITH THE EXCEPTION OF "N"	

Package Number 208 - 24-Lead Side Braze DIP, .600 Wide, ISO Package



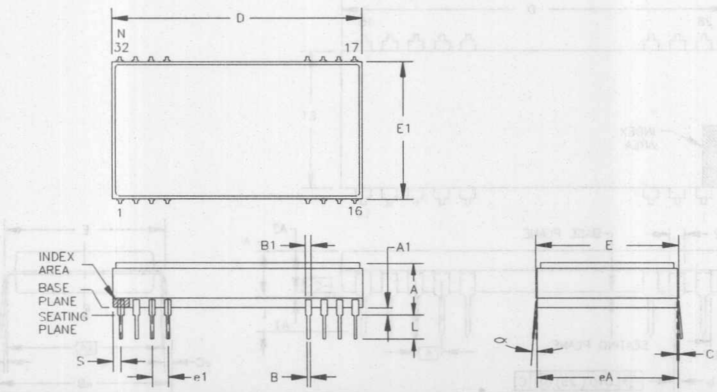
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.085	.190	2.16	4.83		∝	0°	15°	0°	15°	3
A1	.020	.070	0.51	1.78							
B	.015	.023	0.38	0.58	5						
B1	.038	.060	0.97	1.52	5						
C	.008	.012	0.20	0.30							
D	1.180	1.220	29.97	30.99							
E	.595	.625	15.11	15.88							
E1	.580	.610	14.73	15.49	6						
e1	.100 TYP.		2.54 TYP.		2						
eA	.600 TYP.		15.24 TYP.		2						
L	.125	.175	3.18	4.45							
N	16		16		4						
Q1	.010	--	0.25	--							
S	.030	.065	0.76	1.65							

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ208	REV.:	C
JEDEC NUMBER: MO-038-AA WITH THE EXCEPTION OF "N"		

Package Number 210 - 32-Lead Side Braze DIP, .900 Wide, ISO Package



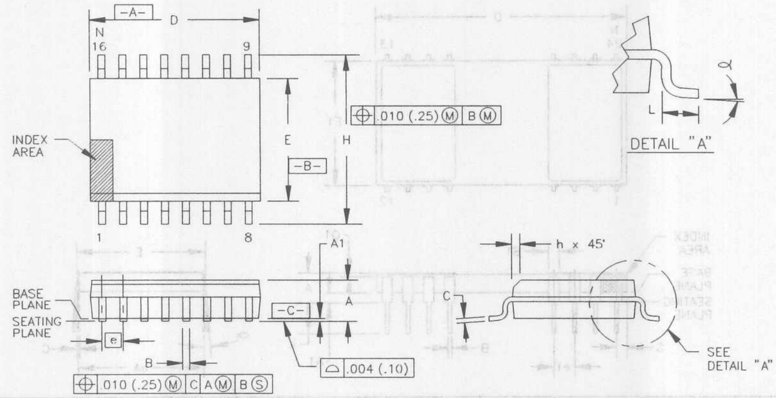
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.310	.370	7.87	9.40							
A1	.040	.060	1.02	1.52							
B	.016	.020	0.41	0.51	5						
B1	.040 TYP.		1.02 TYP.		5						
C	.009	.012	0.23	0.30							
D	1.590	1.630	40.39	41.40							
E	.895	.925	22.73	23.49							
E1	.875	.905	22.23	22.99	6						
e1	.100 TYP.		2.54 TYP.		2						
eA	.900 TYP.		22.86 TYP.		2						
L	.125	.180	3.18	4.57							
N	16		16		4						
S	.044	.056	1.12	1.42							
∝	0°	15°	0°	15°	3						

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER. ZZ210	REV.:	E
JEDEC NUMBER: NONE		

Package Number 211 - 16-Lead SOIC, .300 Wide



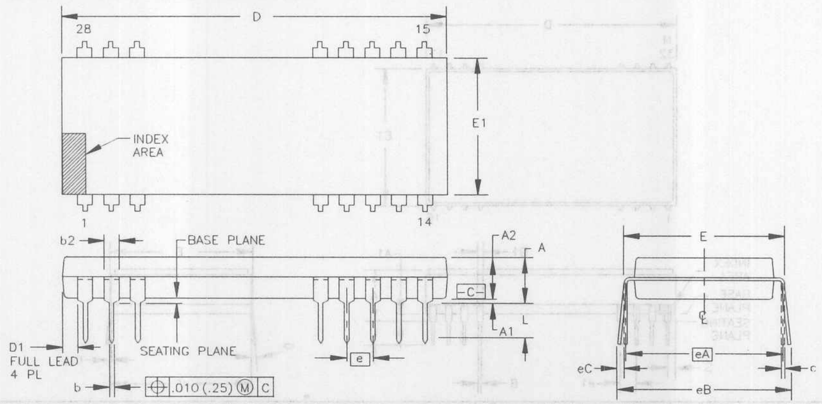
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0926	.1043	2.35	2.65							
A1	.004	.0118	0.10	0.30							
B	.013	.020	0.33	0.51	7						
C	.0091	.0125	0.23	0.32							
D	.3977	.4133	10.10	10.50	2						
E	.2914	.2992	7.40	7.60	3						
e	.050 BASIC		1.27 BASIC								
H	.394	.419	10.00	10.65							
h	.010	.029	0.25	0.75	4						
L	.016	.050	0.40	1.27	5						
N	16		16		6						
α	0°	8°	0°	8°							

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER:	ZZ211	REV.:	F
JEDEC NUMBER:	MS-013-AA		

Package Number 215-1 - 28-Pin Plastic, Double-Wide DIP



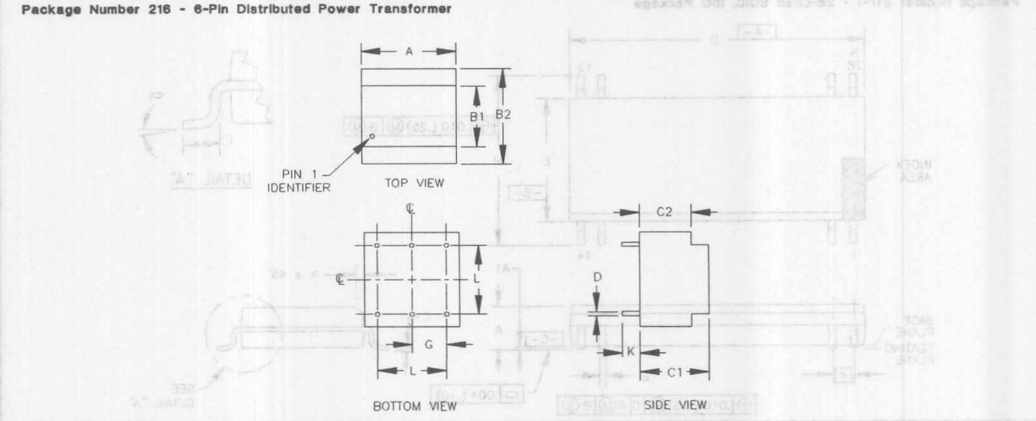
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.250	--	6.35	3	L	.115	.200	2.92	5.08	3
A1	.015	--	0.38	--	3	N	16		16		7
A2	.125	.195	3.18	4.95							
b	.014	.022	0.36	0.56							
b2	.030	.070	0.76	1.78	9						
c	.008	.015	0.20	0.38							
D	1.380	1.565	35.05	39.75	4						
D1	.005	--	0.13	--	4						
E	.600	.625	15.24	15.88	5						
E1	.485	.580	12.32	14.73	4						
e	.100 BASIC		2.54 BASIC								
eA	.600 BASIC		15.26 BASIC		5						
eB	--	.700	--	17.78	6						
eC	.000	.060	0.00	1.52	6						

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM $\boxed{-C-}$
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER:	ZZ215-1	REV.:	B
JEDEC NUMBER:	MS-011-AB WITH THE EXCEPTION OF "N"		

Package Number 216 - 6-Pin Distributed Power Transformer

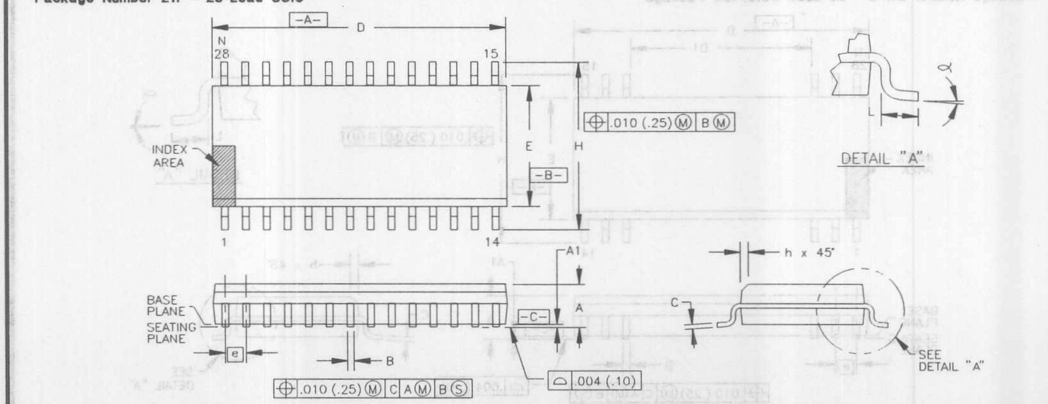


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	0.54	0.64	13.72	16.26							
B1	0.39	0.49	9.91	12.45							
B2	0.54	0.64	13.72	16.26							
C1	0.39	0.52	9.91	13.21							
C2	0.29	0.44	7.37	11.18							
D	.020	.030	0.50	0.76							
G	.177	.217	4.50	5.12							
K	0.11	0.21	2.79	5.33							
L	.375	.425	9.53	10.80							

NOTES:

PACKAGE NUMBER: ZZ216 REV.: E
JEDEC NUMBER: NONE

Package Number 217 - 28-Lead SOIC



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0926	.1043	2.35	2.65							
A1	.004	.0118	0.10	0.30							
B	.013	.020	0.33	0.51	7						
C	.0091	.0125	0.23	0.32							
D	.6969	.7125	17.70	18.10	2						
E	.2914	.2992	7.40	7.60	3						
e	.050 BASIC		1.27 BASIC								
H	.398	.419	10.11	10.65							
h	.010	.0295	0.25	0.75	4						
L	.020	.040	.508	1.02	5						
N	28		28		6						
α	0°	8°	0°	8°							

NOTES:

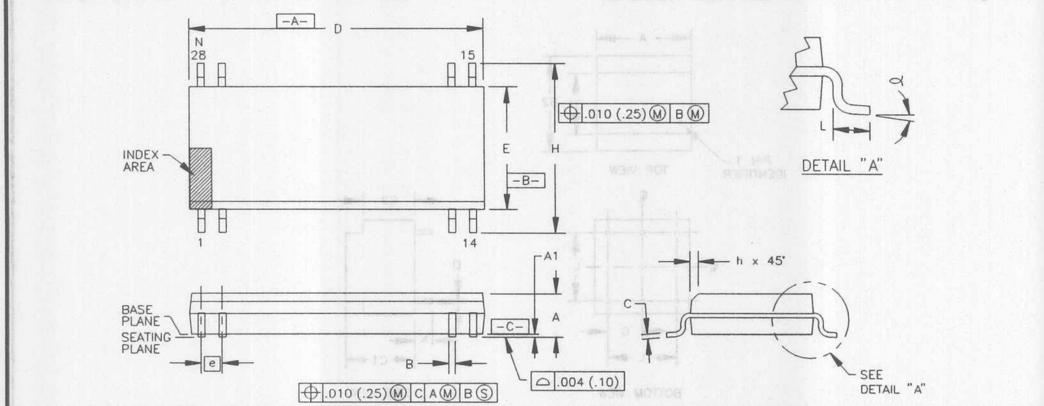
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSSHATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ217 REV.: G
JEDEC NUMBER: MS–013–AE WITH THE EXCEPTION OF DIM. H, L.

PACKAGE DRAWINGS (Mechanicals)

C

Package Number 217-1 - 28-Lead SOIC, ISO Package



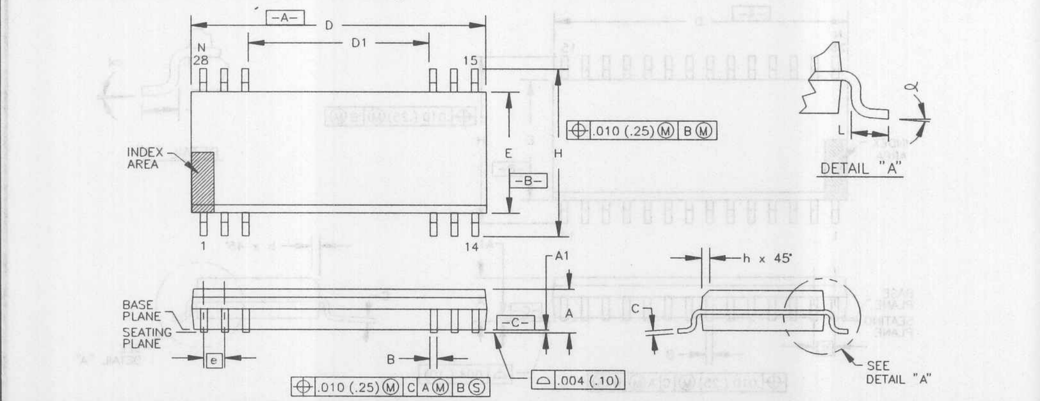
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.6969	.7125	17.70	18.10	2
E	.2914	.2992	7.40	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.01	10.65	
h	.010	.0295	0.25	0.75	4
L	.016	.050	0.40	1.27	5
N	8		8		6
∝	0°	8°	0°	8°	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER:	ZZ217-1	REV.:	G
JEDEC NUMBER:	MS-013-AE WITH THE EXCEPTION OF "N"		

Package Number 217-2 - 28-Lead SOIC, ISO Package



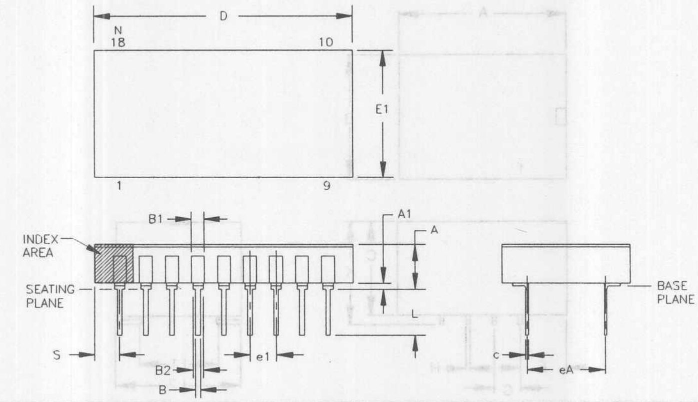
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.6969	.7125	17.70	18.10	2
D1	.426	.441	10.82	11.20	
E	.2914	.2992	7.42	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.01	10.65	
h	.010	.0295	0.25	0.75	4
L	.016	.050	0.41	1.27	5
N	12		12		6
∝	0°	8°	0°	8°	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER:	ZZ217-2	REV.:	D
JEDEC NUMBER:	MS-013-AE WITH THE EXCEPTION OF "N"		

Package Number 220 - 18-Lead Bottom Braze DIP, .300 Wide



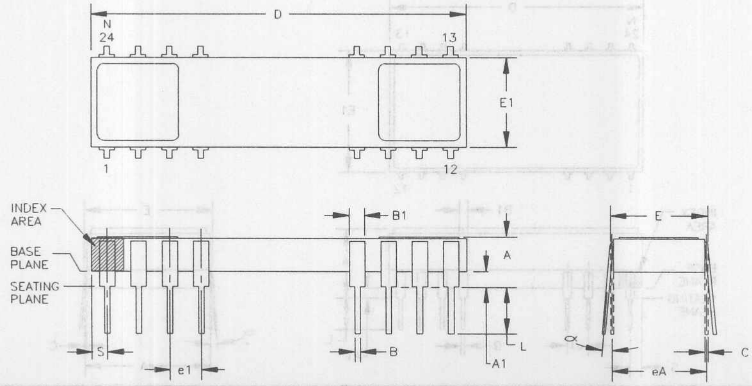
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.148	.197	3.76	5.00							
A1	.015	.035	0.38	0.89							
B	.016	.020	0.41	0.51							
B1	.050 TYP.		1.27 TYP.								
B2	.040 TYP.		1.02 TYP.								
c	.009	.012	0.23	0.30							
D	.982	1.002	24.94	25.45							
E1	.480	.500	12.19	12.70							
e1	.095	.105	2.41	2.67							
eA	.290	.310	7.37	7.87							
L	.150	.200	3.81	5.08							
N	18		18								
S	.038	.103	0.97	2.62							

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.
3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER:	ZZ220	REV.:	C
JEDEC NUMBER:	NONE		

Package Number 225 - 24-Lead Side Braze DIP, .300 Wide, ISO Package



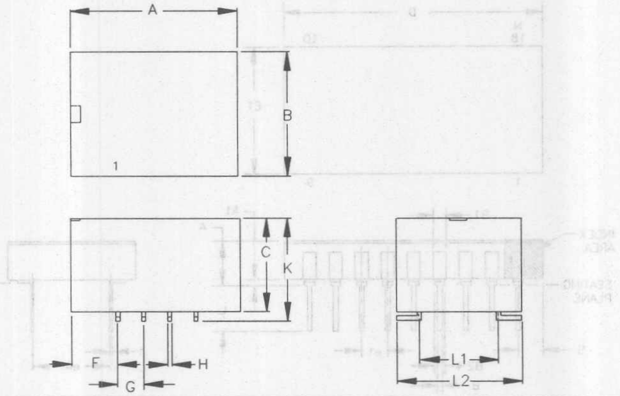
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.140	.185	3.56	4.70							
A1	.040	.060	1.02	1.52							
B	.016	.020	0.41	0.51	5						
B1	.045	.055	1.14	1.40	5						
C	.009	.012	0.23	0.30							
D	1.188	1.212	30.18	30.78							
E	.300	.320	7.62	8.13							
E1	.280	.300	7.11	7.62	6						
e1	.100 TYP.		2.54 TYP.		2						
eA	.300 TYP.		7.62 TYP.		2						
L	.125	.180	3.18	4.57							
N	16		16		4						
S	.035	.065	0.89	1.65							
α	0°	15°	0°	15°	3						

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER:	ZZ225	REV.:	E
JEDEC NUMBER:	NONE		

Package Number 226 - 8-Pin Plastic DIP

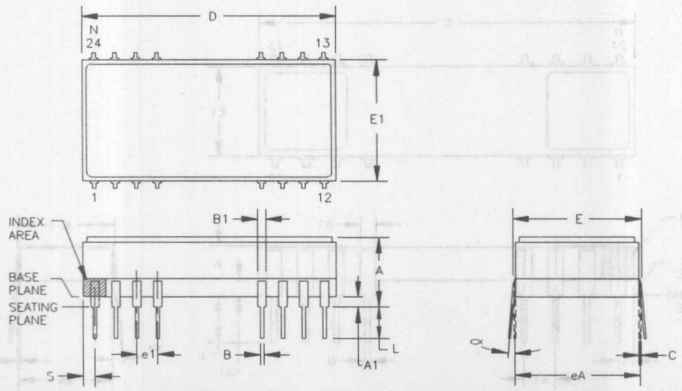


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.620	.640	15.78	16.26	
B	.465	.485	11.81	12.32	
C	.350	.370	8.89	9.40	
F	.165	.185	4.19	4.70	
G	.100 BASIC		2.54 BASIC		
H	.025 SQ.		.635 SQ.		
K	.370	.390	9.40	9.91	
L1	.280	.300	7.11	7.62	
L2	.465	.485	11.81	12.32	

NOTES:

PACKAGE NUMBER:	ZZ226	REV.:	A
JEDEC NUMBER:	NONE		

Package Number 231 - 24-Lead Side Braze DIP, .600 Wide, ISO Package



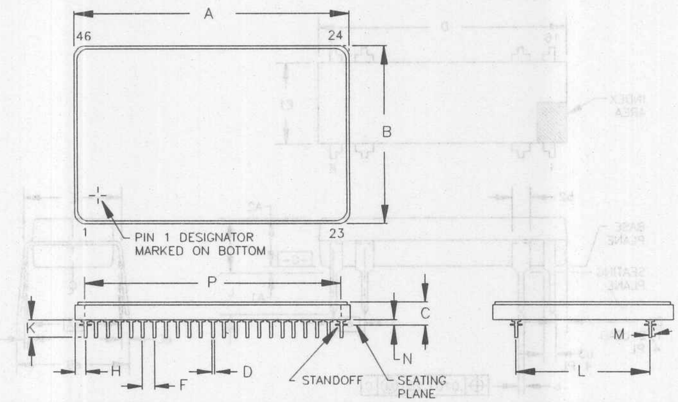
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.310	.375	7.87	9.52	
A1	.040	.060	1.02	1.52	
B	.016	.020	0.41	0.51	5
B1	.040 TYP.		1.02 TYP.		5
C	.009	.012	0.23	0.30	
D	1.180	1.265	29.97	32.13	
E	.600	.620	15.24	15.75	
E1	.570	.610	14.48	15.49	6
e1	.100 TYP.		2.54 TYP.		2
eA	.580	.620	14.73	15.75	2
L	.125	.180	3.18	4.57	
N	16		16		4
S	.044	.056	1.12	1.42	
∝	0°	15°	0°	15°	3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0). TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER:	ZZ231	REV.:	E
JEDEC NUMBER:	NONE		

Package Number 234 - 46-Lead

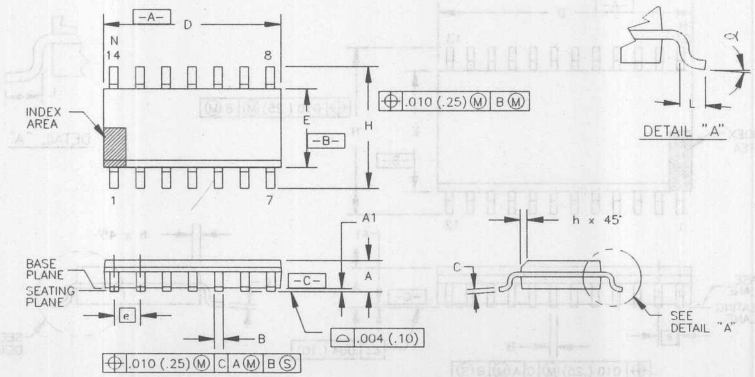


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	2.370	2.420	60.20	61.47							
B	1.560	1.610	39.62	40.89							
C	.205	.251	5.21	6.38							
D	.015	.021	0.38	0.53							
F	.095	.105	2.41	2.67							
H	.085	.105	2.16	2.67							
K	.155	.185	3.94	4.70							
L	1.290	1.310	32.77	33.27							
M	--	10°	--	10°							
N	.045	.055	1.14	1.40							
P	2.190	2.210	55.63	56.13							

NOTES:
1. LEADS IN TRUE POSITION WITHIN 0.01" (0.25mm) R AT MMC AT SEATING PLANE.

PACKAGE NUMBER: ZZ234	REV.: B
JEDEC NUMBER: NONE	

Package Number 235 - 14-Lead SOIC



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0532	.0688	1.35	1.75							
A1	.004	.0098	0.10	0.25							
B	.013	.020	0.33	0.51	7						
C	.0075	.0098	0.19	0.25							
D	.3367	.3444	8.55	8.75	2						
E	.1497	.1574	3.80	4.00	3						
e	.050 BASIC		1.27 BASIC								
H	.2284	.244	5.80	6.20							
h	.0099	.0196	0.25	0.50	4						
L	.016	.050	0.40	1.27	5						
N	14		14		6						
α	0°	8°	0°	8°							

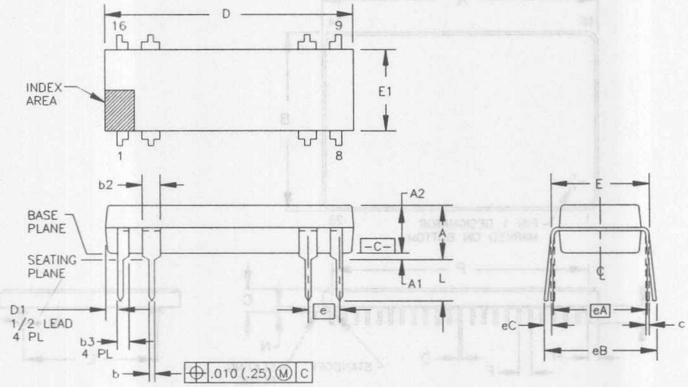
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ235	REV.: E
JEDEC NUMBER: MS-012-AB	

PACKAGE DRAWINGS (Mechanicals)

C

Package Number 238 - 16-Pin Plastic, Single-Wide ISO Package



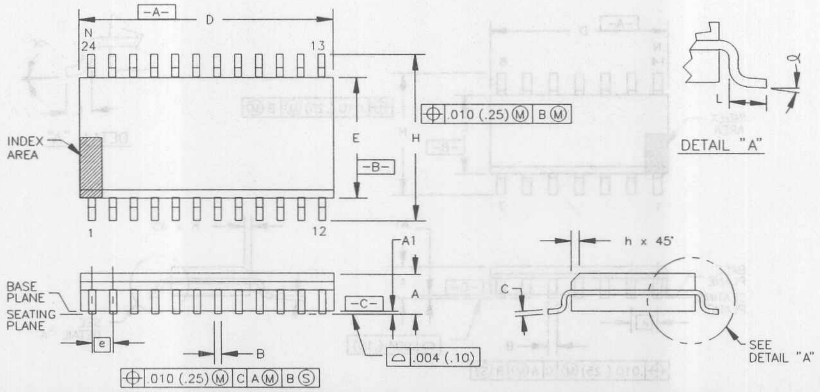
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.735	.775	18.67	21.34	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	8		8		7

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER:	ZZ238	REV.: D
JEDEC NUMBER:	MS–001–BB WITH THE EXCEPTION OF "N"	

Package Number 239 - 24-Lead SOIC

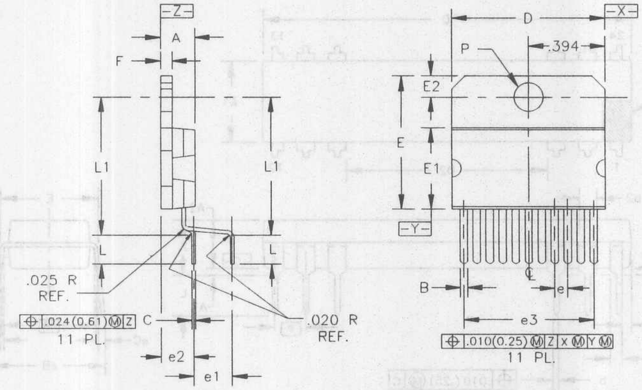


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.5985	.6141	15.20	15.60	2
E	.2914	.2992	7.40	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.00	10.65	
h	.010	.0295	0.25	0.75	4
L	.016	.050	0.40	1.27	5
N	24		24		6
α	0°	8°	0°	8°	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM THE SEATING PLANE.

PACKAGE NUMBER:	ZZ239	REV.: E
JEDEC NUMBER:	MS–013–AD	



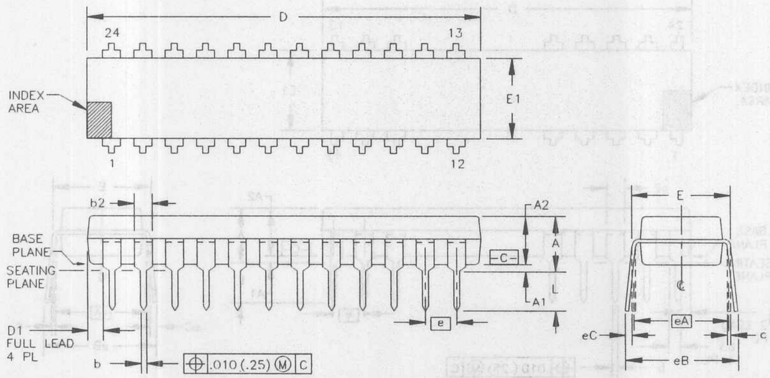
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.172	.182	4.37	4.62		N	11		11		3
B	.035	.041	0.89	1.04		P	.148	.152	3.76	3.86	
C	.014	.024	0.36	0.61		R1	.065	.080	1.65	2.03	
D	.778	.798	19.76	20.27							
E	.684	.694	17.37	17.63							
E1	.416	.426	10.57	10.82							
E2	.110 BASIC		.279 BASIC								
e	.067 BASIC		1.70 BASIC								
e1	.200 BASIC		5.08 BASIC								
e2	.169 BASIC		4.29 BASIC								
e3	.670 BASIC		17.02 BASIC								
F	.057	.063	1.45	1.60							
L	.150	.176	3.81	4.47							
L1	.690	.710	17.53	18.03							

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1982.
2. CONTROLLING DIMENSION: INCH.
3. N IS THE MAXIMUM QUANTITY OF LEAD POSITIONS.

PACKAGE NUMBER:	ZZ242	REV.:	C
JEDEC NUMBER:	MO–48 (AA)		

Package Number 243 - 24-Pin Plastic, Single-Wide DIP



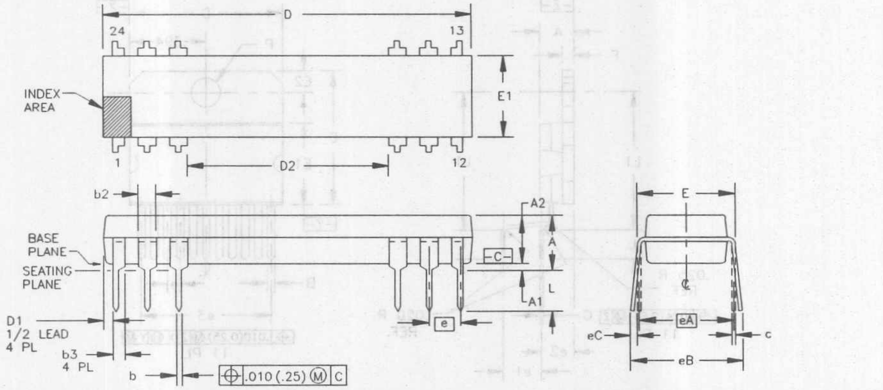
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3	L	.115	.150	2.92	3.81	3
A1	.015	--	0.38	--	3	N	24		24		7
A2	.115	.195	2.92	4.95							
b	.014	.022	0.36	0.56							
b2	.045	.070	1.14	1.78	9						
c	.008	.014	0.20	0.36							
D	1.230	1.280	31.24	32.51	4						
D1	.005	--	0.13	--	4						
E	.300	.325	7.62	8.26	5						
E1	.240	.280	6.10	7.11	4						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.62 BASIC		5						
eB	--	.430	--	10.92	6						
eC	.000	.060	0.00	1.52	6						

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM –C– .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER:	ZZ243	REV.:	D
JEDEC NUMBER:	MS–001–AF		

Package Number 243-1 - 24-Pin Plastic, Single-Wide DIP, ISO Package



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3	eB	--	.430	--	10.92	6
A1	.015	--	0.38	--	3	eC	.000	.060	0.00	1.52	6
A2	.115	.195	2.92	4.95		L	.115	.150	2.92	3.81	3
b	.014	.022	0.36	0.56		N	12		12		7
b2	.045	.070	1.14	1.78	9						
b3	.030	.045	0.76	1.14	9						
c	.008	.014	0.20	0.36							
D	1.160	1.195	29.46	30.35	4						
D1	.005	--	0.13	--	4						
D2	.630	.655	16.00	16.64							
E	.300	.325	7.62	8.26	5						
E1	.240	.280	6.10	7.11	4						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.62 BASIC		5						

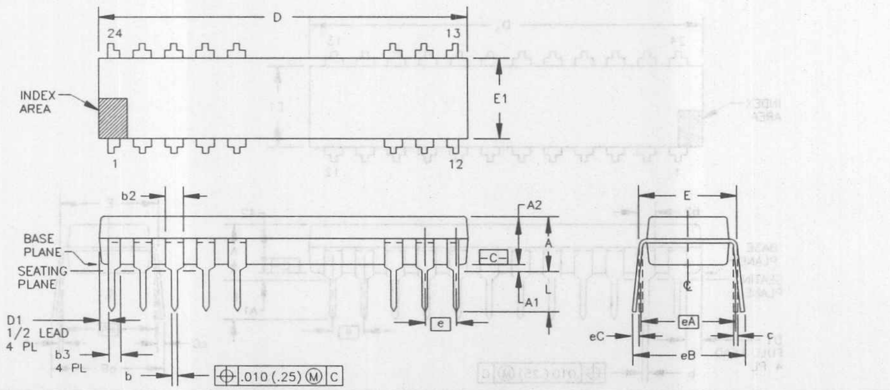
NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ243-1 REV.: J

JEDEC NUMBER: MS-001-BE WITH THE EXCEPTION OF "N"

Package Number 243-2 - 24-Pin Plastic, Single-Wide DIP



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3	eC	.000	.060	0.00	1.52	6
A1	.015	--	0.38	--	3	L	.115	.150	2.92	3.81	3
A2	.115	.195	2.92	4.95		N	16		16		7
b	.014	.022	0.36	0.56							
b2	.045	.070	1.14	1.78	9						
b3	.030	.045	0.76	1.14	9						
c	.008	.014	0.20	0.36							
D	1.160	1.195	29.46	30.35	4						
D1	.005	--	0.13	--	4						
E	.300	.325	7.62	8.26	5						
E1	.240	.280	6.10	7.11	4						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.62 BASIC		5						
eB	--	.430	--	10.92	6						

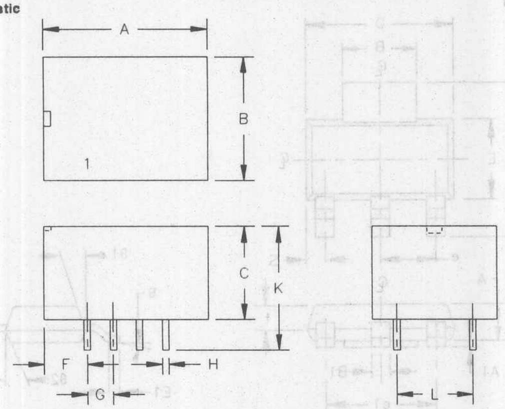
NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ243-2 REV.: C

JEDEC NUMBER: MS-001-BE WITH THE EXCEPTION OF "N"

Package Number 250 - 8-Pin Plastic

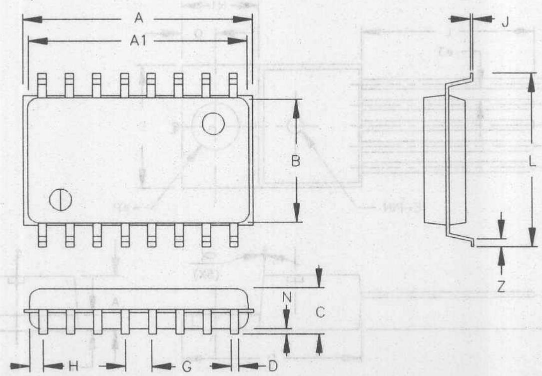


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.620	.640	15.78	16.26							
B	.465	.485	11.81	12.32							
C	.350	.370	8.89	9.40							
F	.165	.185	4.19	4.70							
G	.100 BASIC		2.54 BASIC								
H	.025 SQ.		.635 SQ.								
K	.465	.490	11.81	12.45							
L	.280	.300	7.11	7.62							

NOTES:

PACKAGE NUMBER: ZZ250 REV.: B
JEDEC NUMBER: NONE

Package Number 258 - 16-Lead SOIC

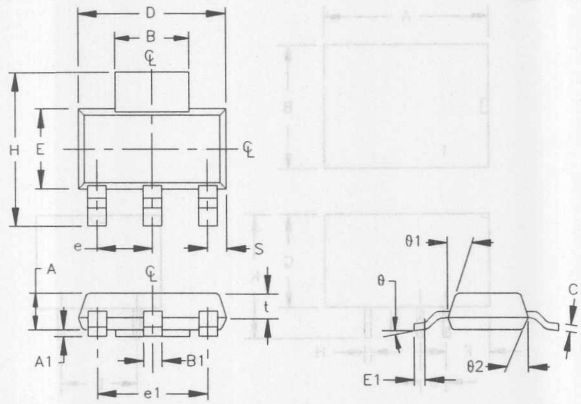


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.400	.415	10.16	10.54							
A1	.395	.400	10.03	10.16							
B	.205	.214	5.21	5.44							
C	— —	.090	— —	2.29							
D	.012	.020	0.30	0.51							
G	.044	.055	1.12	1.40							
H	.020	.031	0.51	0.79							
J	.005	.008	0.13	0.20							
L	.300	.324	7.62	8.23							
N	.004	.008	0.10	0.20							
Z	.012	.036	0.30	0.91							

NOTES:

PACKAGE NUMBER: ZZ258 REV.: B
JEDEC NUMBER: NONE

Package Number 311 - 4-Lead SOT



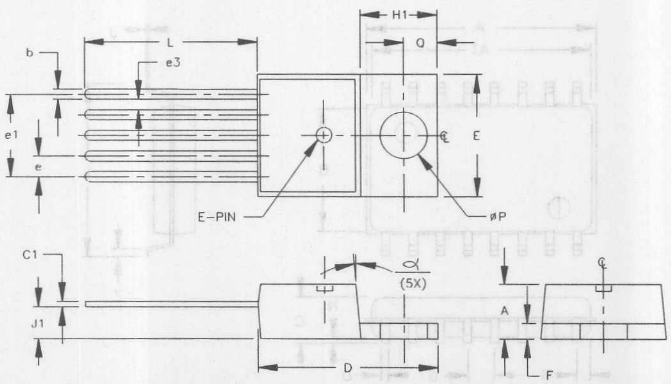
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.060	.067	1.50	1.70	
A1	.0008	.004	0.02	0.10	
B	.116	.124	2.95	3.15	
B1	.026	.033	0.66	0.73	
C	.010	.014	0.25	0.35	
D	.248	.264	6.30	6.70	
E	.130	.146	3.30	3.70	
E1	.012 MIN.		0.30 MIN.		
e	.0905 NOM.		2.30 NOM.		
e1	.181 NOM.		4.60 NOM.		
H	.264	.287	6.70	7.30	
S	.033	.041	0.85	1.05	
t	.043	.051	1.10	1.30	
θ	10° MAX.		10° MAX.		

DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
θ1	10°	16°	10°	16°	
θ2	10°	16°	10°	16°	

NOTES:

PACKAGE NUMBER:	ZZ311	REV.:	A
JEDEC NUMBER:	NONE		

Package Number 315 - TO-220, 5-Lead



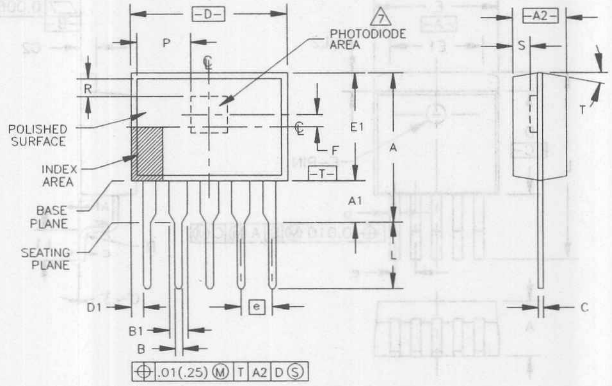
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.160	.190	4.06	4.83	
b	.025	.040	0.63	1.02	
C1	.014	.022	0.36	0.56	
D	.560	.590	14.22	14.99	
E	.385	.415	9.78	10.54	
e	.062	.072	1.57	1.83	
e1	.263	.273	6.68	6.93	
e3	.030	.040	0.76	1.02	
F	.045	.055	1.14	1.40	
H1	.234	.258	5.94	6.55	
J1	.090	.115	2.29	2.92	
øP	.146	.156	3.71	3.96	
Q	.103	.113	2.62	2.87	
L	.540	.560	13.72	14.22	

DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
α	3°	7°	3°	7°	

NOTES:

PACKAGE NUMBER:	ZZ315	REV.:	B
JEDEC NUMBER:	NONE		

Package Number 321 - 5-Pin Transparent Plastic SIP



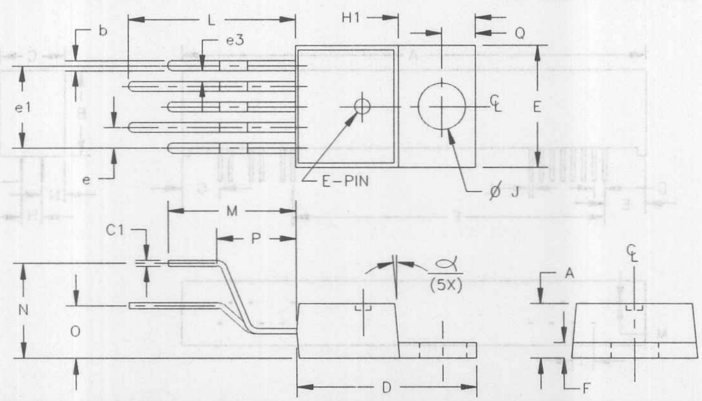
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.360	--	9.14	3	R	.036	.056	0.89	1.42	
A1	.070	--	1.78	--	3	S	.036	.043	0.91	1.09	
A2	.120	.135	3.05	3.43		T	5.5°	8.5°	5.5°	8.5°	
B	.014	.022	0.35	0.56							
B1	.040	.050	1.02	1.27							
C	.008	.012	0.20	0.30							
D	.360	.390	9.14	9.91	4						
D1	.005	--	0.13	--							
E1	.238	.275	6.05	6.99	4						
e	.075 BASIC		1.91 BASIC								
F	.015	.035	0.38	0.89							
L	.140	.180	3.56	4.57	3						
N	5		5		5						
P	.086	.112	2.18	2.84							

NOTES:

1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
6. CENTER OF PHOTODIODE MUST BE WITHIN .01" OF CENTER OF PHOTODIODE AREA.
7. DIMENSIONS REFERENCED CORRELATE TO A PHOTODIODE SIZE .090 X .090 INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.

PACKAGE NUMBER:	ZZ321	REV.:	E
JEDEC NUMBER:	NONE		

Package Number 323 - TO220, 5-Lead ZIP

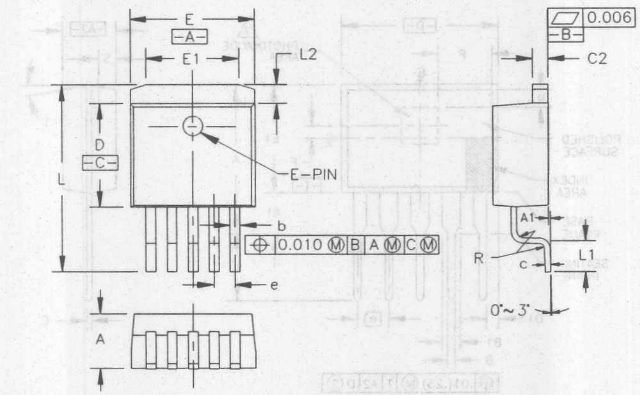


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.160	.190	4.06	4.83		M	.400	.420	10.16	10.67	
b	.025	.040	0.63	1.02		N	.314	.326	7.98	8.28	
C1	.014	.022	0.36	0.56		O	.160	.170	4.06	4.32	
D	.560	.590	14.22	14.99		P	.250	.270	6.35	6.86	
E	.385	4.15	9.78	10.54							
e	.057	.077	1.57	1.83							
e1	.263	.273	6.68	6.93							
e3	.030	.040	0.76	1.02							
F	.045	.055	1.14	1.40							
H1	.234	.258	5.94	6.55							
ØJ	.146	.156	3.71	3.96							
Q	.103	.113	2.62	2.87							
L	.525	.545	13.33	13.84							
α	3°	7°	3°	7°							

NOTES:

PACKAGE NUMBER:	ZZ323	REV.:	C
JEDEC NUMBER:	NONE		

Package Number 325 - 5-Lead DD PAK



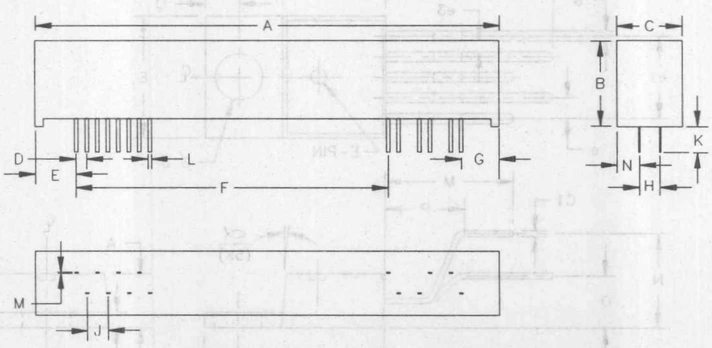
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.170	.183	4.32	4.65							
A1	.000	.004	0.00	0.10							
b	.026	.037	0.66	0.94							
C2	.045	.055	1.14	1.40							
c	.014	.026	0.36	0.66							
D	.310	.350	7.87	8.89							
E	.385	.410	9.78	10.41							
E1	.297	.303	7.54	7.70							
e	.067 REF		1.70 REF								
L	.595	.605	15.11	15.37							
L1	.096	.104	2.44	2.64							
L2	.0585	.0625	1.485	1.587							
N	5		5								
R	.017	.019	0.43	0.48							

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14, 5M-1982.
2. DIMENSION b AND c APPLY TO THE PLATED LEAD.
3. LEADS ARE NOT ALLOWED ABOVE THE DATUM -B-. STAND-OFF HEIGHT IS MEASURED FROM LEAD TIP WITH REFERENCE TO DATUM -B-.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM "b" BY MORE THAN .003".
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.

PACKAGE NUMBER: ZZ325 REV.: C
JEDEC NUMBER: MO-169
WITH THE EXCEPTION OF DIM. D,L,L1,L2

Package Number 326 - 38-Lead Plastic ZIP

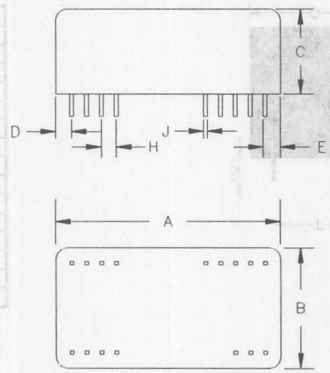


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	2.220	2.246	56.39	57.05							
B	0.418	0.428	10.62	10.87							
C	0.295	0.325	7.49	8.26							
D	0.050 TYPICAL		1.27 TYPICAL								
E	0.190	0.200	4.83	5.08							
F	1.500 TYPICAL		38.10 TYPICAL								
G	0.183	0.193	4.65	4.90							
H	0.100 TYPICAL		2.54 TYPICAL								
J	0.100 TYPICAL		2.54 TYPICAL								
K	0.125 TYPICAL		3.18 TYPICAL								
L	0.016	0.020	0.41	0.51							
M	0.008	0.012	0.20	0.30							
N	0.080	–	2.03	–							

NOTES:

PACKAGE NUMBER: ZZ326 REV.: B
JEDEC NUMBER: NONE

Package Number 335 - Custom Module



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	1.506	1.512	38.24	38.40	
B	0.806	0.812	20.46	20.62	
C	0.568	0.574	14.42	14.58	
D	0.103	0.109	2.62	2.78	
E	0.103	0.109	2.62	2.78	
F	0.132	0.171	3.35	4.35	
G	0.6 BASIC		15.24 BASIC		
H	0.1 BASIC		2.54 BASIC		
J	0.025 TYP.		0.64 TYP.		
K	0.101	0.107	2.57	2.73	

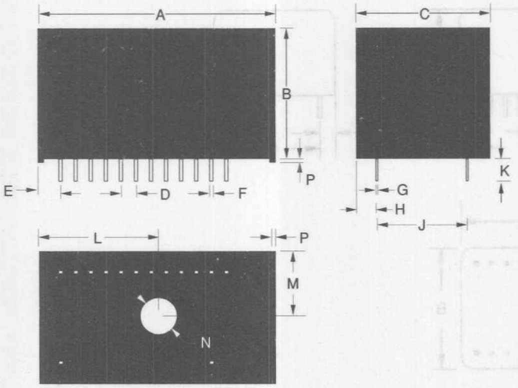
NOTES:

PACKAGE NUMBER: ZZ335 REV.: A
JEDEC NUMBER: NONE

PACKAGE DRAWINGS (Mechanicals)

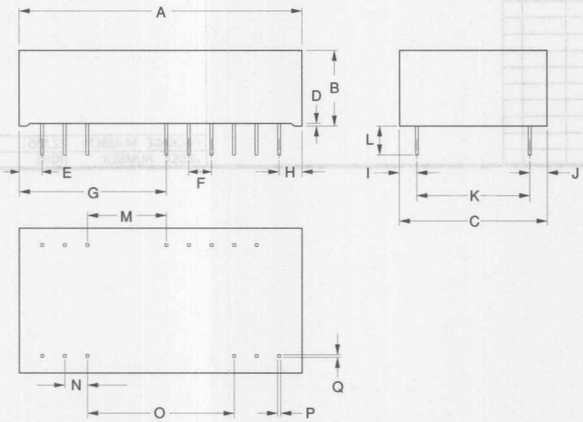
C

Package Number 901



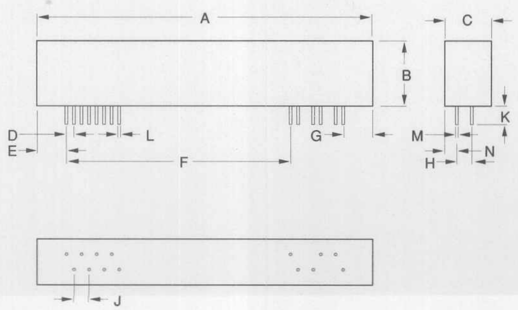
DIM	MILLIMETERS TYP	INCHES TYP
A	40.00	1.58
B	22.00	0.87
C	22.60	0.89
D	2.54	0.10
E	3.49	0.14
F	0.58	.023
G	0.25	.011
H	3.38	0.13
J	15.24	0.60
K	3.81	0.15
L	20.00	0.79
M	11.30	0.44
N	6.00	0.24
P	0.60	0.024

Package Number 902 — 24-Pin Plastic



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.505		63.63	
B	.681		17.30	
C	1.306		33.17	
D	.024		0.60	
E	.202		5.14	
F	.200		5.08	
G	1.302		33.08	
H	.203		5.15	
I	.153		3.885	
J	.153		3.885	
K	1.000		25.40	
L	.256		6.50	
M	.700		17.78	
N	.200		5.08	
O	1.300		33.02	
P	.025		0.64	
Q	.025		0.64	

Package Number 903 — 38-Lead Plastic SIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.220	2.246	56.39	57.05
B	.415	.463	10.54	11.76
C	.295	.325	7.49	8.26
D	.050 TYPICAL		1.27 TYPICAL	
E	.195 TYPICAL		4.95 TYPICAL	
F	1.500 TYPICAL		38.10 TYPICAL	
G	.188 TYPICAL		4.78 TYPICAL	
H	.100 TYPICAL		2.54 TYPICAL	
J	.100 TYPICAL		2.54 TYPICAL	
K	.125 TYPICAL		3.18 TYPICAL	
L	.018 TYPICAL		0.46 TYPICAL	
M	.010 TYPICAL		0.25 TYPICAL	
N	.080	—	2.03	—